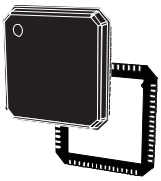
TDA7708

AM/FM/HD-Radio™ submicron technology automotive receiver

Datasheet - production data



VFQFPN64 (9 x 9 x 1.0 mm)

GAPGPS02776

Features

- AEC-Q100 qualified
- AM/FM reception with digital IF processing
- Fully automotive grade CMOS design
- AM/FM Band
- Low-IF, DSP-based architecture
- Very high dynamic range built-in IF-ADC
- Minimum external component count
- Very small footprint package
- Multipath noise mitigation processing
- RDS demodulation with group and block synchronization
- Compatible with HD-Radio™ and DRM
- Digital Audio Output
- Fully RoHS-compliant

Description

The TDA7708 is a single chip fully-CMOS AM/FM tuner aimed at receivers for terrestrial radio broadcasting.

The TDA7708 is a complete integrated and optimized RF tuner for AM/FM reception. It allows the implementation of AM/FM solution (and also HD-Radio™ with external STMicroelectronics's STA680 co-processor) for automotive grade receivers and other applications.

The TDA7708 combines state-of-art performance with minimum external component count, making it therefore ideal for integration into car radios and other radio devices with challenging performance, quality, reliability and, last but not least, cost requirements.

Such a low external component count is made possible by cutting-edge circuit and implementation techniques that overcome the major challenges affecting both very-low and zero IF receivers.

The TDA7708 features multiple front-end low-noise amplifiers (LNAs) to cover AM LW/MW/SW bands, and the entire FM band, with advanced DSP-controlled automatic gain control (AGC) amplifier and mixer stages.

After on-chip IF filtering, the TDA7708 digitizes the signal with a very high dynamic range ADC; it processes the complex phase-quadrature baseband signal allowing applications like multipath noise mitigation, and integrated RDS decoding.

The TDA7708 furthermore integrates the HD-Radio™ channel filtering.

Besides providing optimal AM/FM quality reception, the TDA7708 makes it the ideal solution to realize a complete HD-Radio™ receiver solution (in combination with the external STA680 HD-Radio™ decoder) or a DRM receiver (paired to the STA660DRM), with a low bill of material, high performance and real automotive grade quality and reliability.

The TDA7708CB requires a very small FW code to be downloaded for booting the IC, thus making it especially suited to systems whose microcontroller has limited code storage capability.

Table 1: Device summary

Order code	Package	Packing
TDA7708	VFQFPN64 (9 x 9 x 1 mm)	Tray
TDA7708TR		Tape & Reel
TDA7708CB		Tray
TDA7708CBTR		Tape & Reel

This is information on a product in full production.

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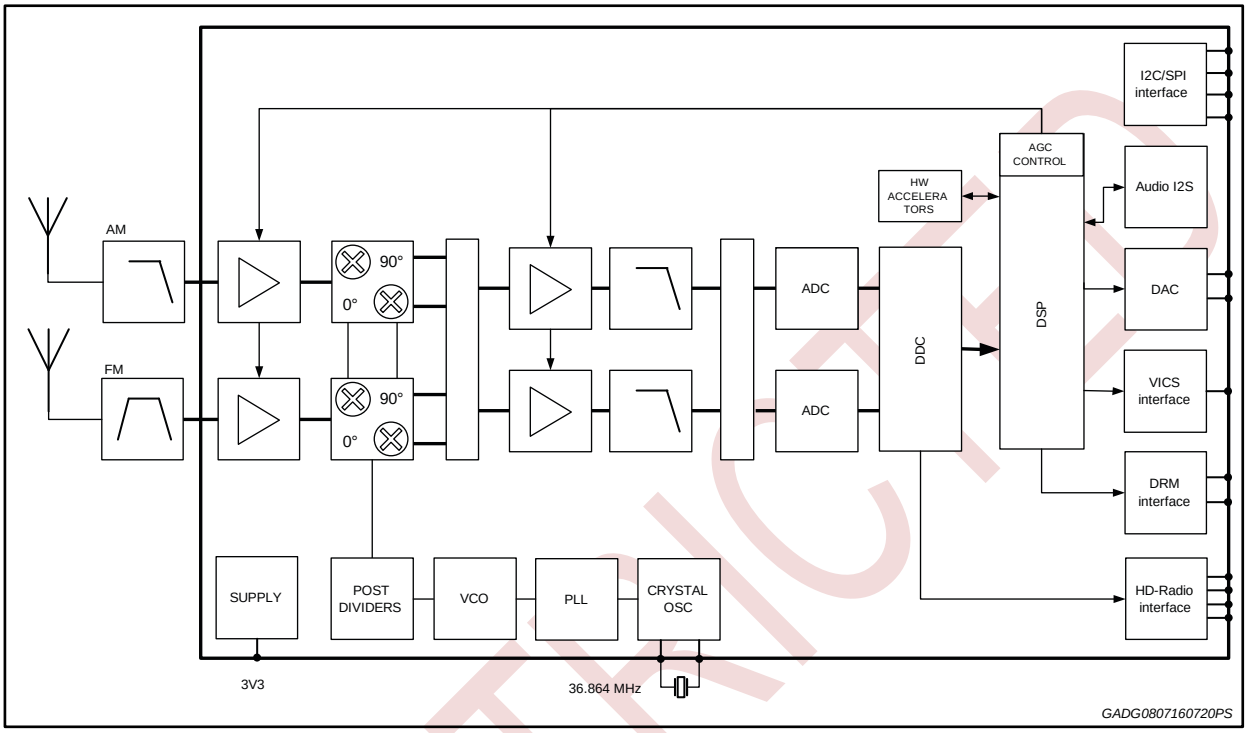
1.1 Block diagram

Figure 1: Functional block diagram



1.2 Pin description

Figure 2: Pin out diagram (top view)

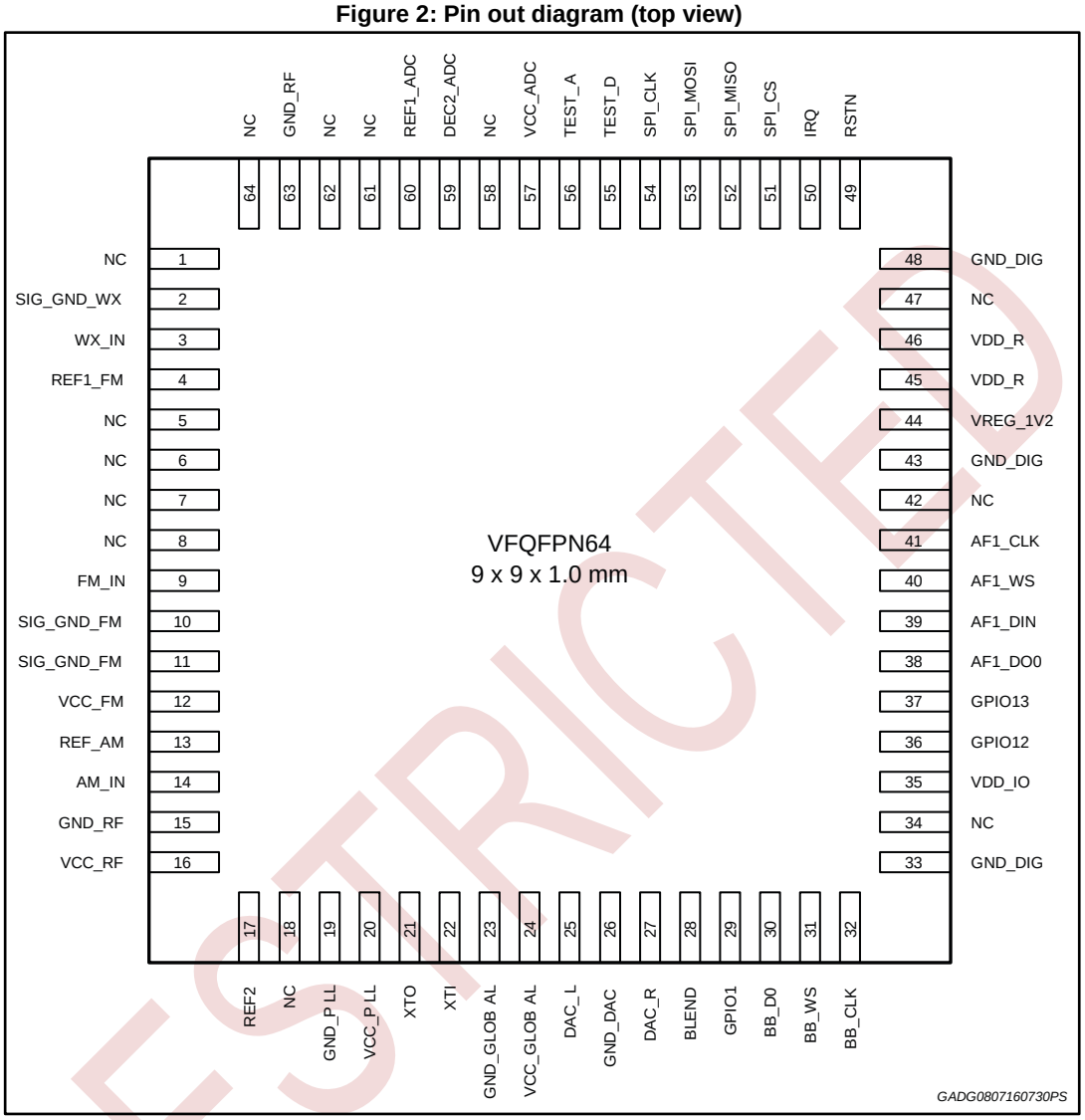
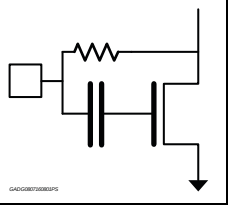
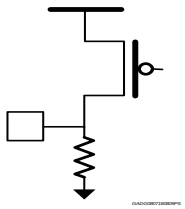
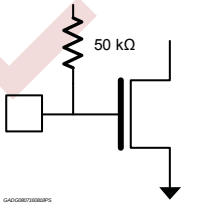
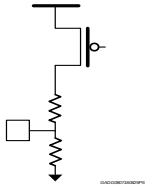
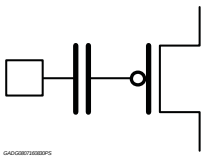
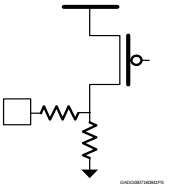
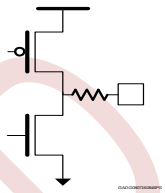
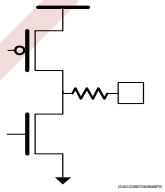
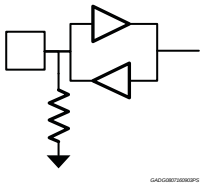
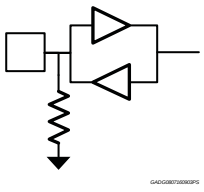
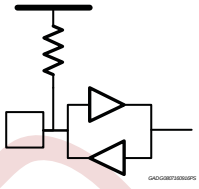
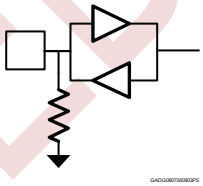
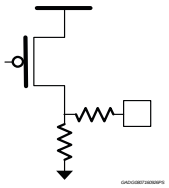


Table 2: Pins description

Pin	Pin name	I/O	Function	Description	Main alternate function	Equivalent circuit
1	NC	-	-	Not connected	-	
2	SIG_GND_WX		Ground	Always connected to ground	-	-
3	WX_IN	I	WX	Weather band LNA input.(1)	-	

Pin	Pin name	I/O	Function	Description	Main alternate function	Equivalent circuit
4	REF1_FM	O	FM	2.5V regulator output	-	
5	NC	-	-	-	-	-
6	NC	-	-	-	-	-
7	NC	-	-	-	-	-
8	NC	-	-	-	-	-
9	FM_IN	I	FM	FM LNA input.(1)	-	
10	SIG_GND_FM	-	Ground	FM signal ground.(2)	-	-
11	SIG_GND_FM	-	Ground	FM signal ground.(2)	-	-
12	VCC_FM	-	Supply	FM power supply.(2)	-	-
13	REF_AM	I/O	AM	AM reference decoupling. In case AM is not used, it can be left unconnected.	-	
14	AM_IN	I	AM	AM LNA input.(1)	-	
15	GND_RF	-	Ground	RF ground	-	-
16	VCC_RF	I	Supply	RF 3.3V power supply	-	-
17	REF2	I/O	-	Reference decoupling 2.5V	-	
18	NC	-	-	Not connected	-	-
19	GND_PLL	-	-	PLL ground	-	-
20	VCC_PLL	I	-	PLL supply 3.3V	-	-

Pin	Pin name	I/O	Function	Description	Main alternate function	Equivalent circuit
21	XTO	O	Oscillator	Crystal output	-	-
22	XTI	I	Oscillator	Crystal input	-	-
23	GND_GLOBAL	-	-	Global Ground	-	-
24	VCC_GLOBAL	I	-	Global 3.3V power supply	-	-
25	DAC_L	O	DAC	DAC output left	TEST_IF_I	
26	GND_DAC	-	Ground	DAC ground	-	-
27	DAC_R	O	DAC	DAC output right	TEST_IF_Q	
28	BLEND	I	-	HD blend input	GPIO5	
29	GPIO1	I/O	-	General purpose I/O 1	CH0_Q	
30	BB_D0	I/O	-	BB I2S data0	CH0_I	
31	BB_WS	I/O	-	BB I2S word select	-	
32	BB_CLK	I/O	-	BB I2S clock	-	
33	GND_DIG	-	-	Digital I/O Ground	-	-
34	NC	-	-	Not connected	-	-
35	VDD_IO	I	-	Digital I/O 3.3V power supply	-	-
36	GPIO12	I/O	-	General purpose I/O 12	-	
37	GPIO13	I/O	-	General purpose I/O 13	-	
38	AIF1_DO0	I/O	-	Audio SAI data 0	General purpose I/O 0	
39	AIF1_DIN	I/O	-	Audio SAI data input	General purpose I/O 6	
40	AIF1_WS	I/O	-	Audio SAI word strobe	General purpose I/O 7	
41	AIF1_CLK	I/O	-	Audio SAI bit clock	General purpose I/O 8	
42	NC		-	Not connected	-	-
43	GND_DIG		-	Digital core Ground	-	-
44	VREG_1V2	O	-	1.2V Regulator output	-	-
45	VDD_R	I	-	Digital power supply	-	-
46	VDD_R	I	-	Digital power supply	-	-

Pin	Pin name	I/O	Function	Description	Main alternate function	Equivalent circuit
47	NC	-	-	Not connected	-	-
48	GND_DIG	-	-	Digital core ground	-	-
49	RSTN	I	-	Reset (Active Low)	-	
50	IRQ	O	Control interface	Interrupt output	-	
51	SPI_CS	I	Control interface	SPI chip select	-	
52	SPI_MISO	O	Control interface	SPI data output	-	
53	SPI_MOSI	I	Control interface	SPI data input	I2C data	
54	SPI_CLK	I	Control interface	SPI clock	I2C clock	
55	TEST_D	I/O	-	Reserved	-	-
56	TEST_A	I/O	-	Reserved	-	-
57	VCC_ADC	I	-	ADC 3.3V power supply	-	-
58	NC	-	-	Not connected	-	-
59	DEC2_ADC	I/O	ADC	ADC reference	-	-
60	REF1_ADC	I/O	ADC	ADC reference decoupling	-	
61	NC	-	-	Not connected	-	-
62	NC	-	-	Not connected	-	-
63	GND_RF	-	Ground	RF ground	-	-
64	NC	-	-	Not connected	-	-
-	EXPOSED PAD	-	-	Global ground	-	-

Notes:

(1)RF input pins, when unused, should be terminated to ground with a 10nF capacitor

(2)Ground and supply pins cannot be left floating.

2 Function description

2.1 FM

The FM signal path is composed by a low-noise-amplifier (LNA) with stepped AGC and an over-tone-rejection mixer. The FM input signal is amplified by the high input impedance LNA with superior linearity and very low noise figure.

The amplifier gain is switchable in 2 dB-steps; the gain is fully controlled by the AGC processing running onto the DSP. The RF signal is then converted into low-IF by a high linearity passive mixer with overtone-rejection structure.

The low-IF signal is then converted into the digital domain by the IF ADC for frequency demodulation and further digital signal processing.

2.2 AM

The AM path is composed by the AM LNA with stepped AGC, an automatically tuned RF filter, the AM over-tone-rejection (OTR) mixer and the IF filter.

The 6 dB-stepped AGC gain is fully controlled by the software running onto the DSP.

OTR is a key issue in low-IF AM receivers because of the large input signal bandwidth; TDA7708 achieves excellent OTR by means of both a high linearity tunable RF filter, and the OTR mixer that rejects up to the 21st harmonic.

The low-IF at the output of the IF-filter is then digitalized by the IF ADC for amplitude demodulation and further signal processing.

2.3 IF A/D converter

The IF digital to analog converter has a 4th order multi-bit topology; it features very high dynamic range and linearity.

The IF-ADC sampling frequency is determined by a control algorithm running on the DSP: this advanced technique changes the sampling frequency depending on the tuning frequency with the goal of avoiding the disturbances generated by the switching discrete-time sections of the IFADC.

2.4 Audio D/A converter

The high-quality audio DAC converts to the analog domain the stereo signal resulting from the digital processing or coming from one of the digital audio interfaces.

The audio DAC is implemented by using an efficient fully integrated 3rd order, single-bit SD architecture with low out-of-band noise thus avoiding being a potential source of disturbances for the AM antenna.

The DAC is capable of generating a full scale signal of 1 V_{rms}.

2.5 VCO

The VCO is fully integrated without any external tuning component. It covers the entire FM band including EU, US, Japan, East-Europe, Weather-Band, all AM-bands including LW, MW and SW.

2.6 PLL

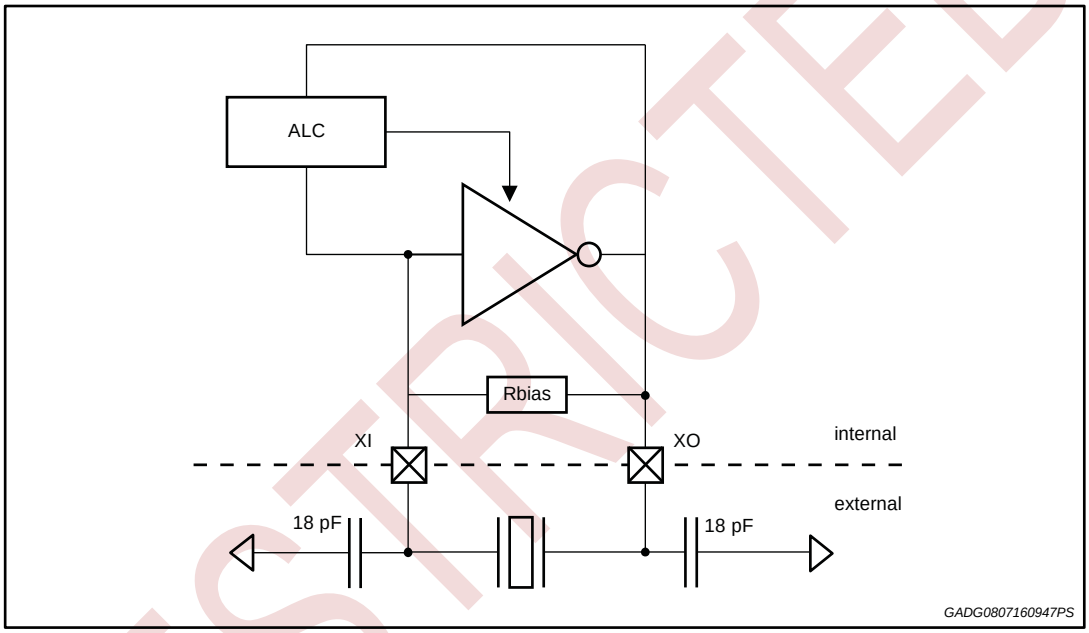
The very high speed fractional PLL has a SD structure; the extremely fast switching PLL settles within 200 µs, as needed by fast RDS applications. The PLL has a fully integrated loop filter, thus not requiring any external component.

2.7 Crystal oscillator

The device works with a 36.864 MHz fundamental tone crystal. The frequency of oscillation has been selected in order to avoid crystal harmonics to fall inside either FM or AM bands.

An automatic level control (ALC) circuit has been designed in order to reduce the harmonic content over the crystal that could potentially be a source of electro-magnetic interference. The crystal oscillator block diagram is shown in *Figure 3: "Crystal oscillator block diagram"*.

Figure 3: Crystal oscillator block diagram



2.8 DSP cluster

TDA7708 embeds a cluster of DSP cores aimed at running advanced signal processing and other key tuner processing functions. The software-defined signal processing allows the flexibility needed by the receivers that need to differentiate from competition.

The DSP cluster provides the needed computational power for:

- Control of digital down-conversion of the IF-signal to zero-IF;
- FM channel selection with variable bandwidth;
- FM/AM noise blanking;
- FM/AM demodulation;
- Weak-signal-processing including soft-mute, high-cut, stereo-blend and quality detection;
- FM stereo decoding with stereo-blend;
- RDS demodulation including error correction and block synchronization with automatic generation of an RDS interrupt for the host microprocessor;
- Autonomous control of RDS-AF tests.

2.9 Digital base-band interface

The TDA7708 transmits the digital base-band I/Q signal to the external processor, such as DCOP for HD-Radio or a SoC.

For maximum flexibility, three different base-band links are available for connecting the tuner to the decoder:

- High speed I²S-like
- JESD204B serial interface
- Coded LVDS bit-stream to DRM DCOP (STA660DRM)

A multi-channel configurable I2S audio interface is available as well.

2.9.1 I²S base-band serial interface

This standard serial interface is needed when pairing TDA7708 to an external I²S-enabled processor.

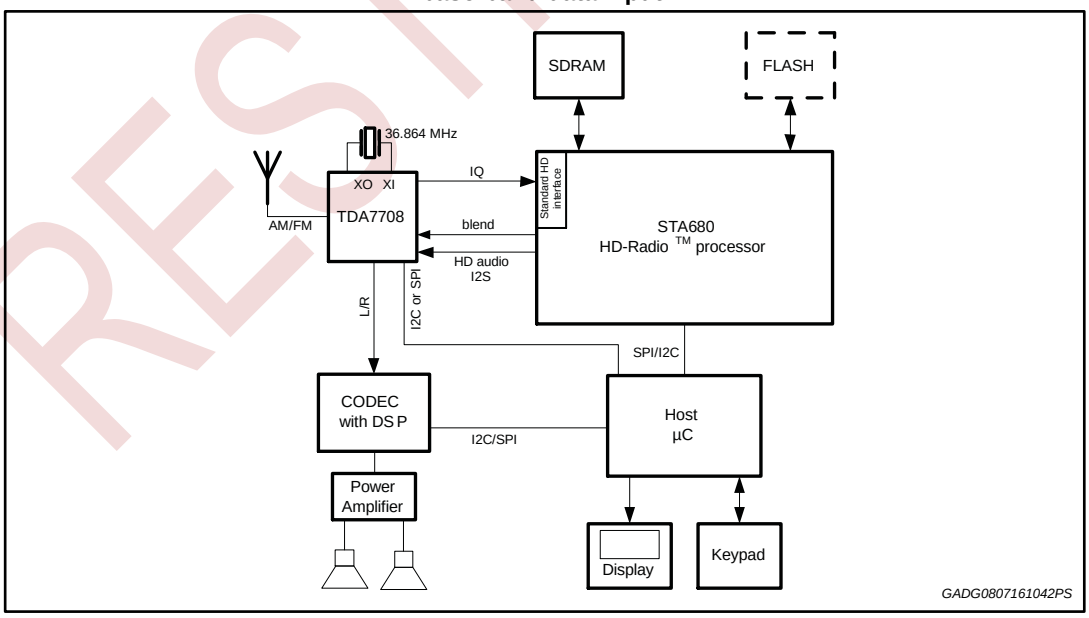
The I²S interface can operate either in 3V3 CMOS single-ended or in LVDS mode.

There are known system drawbacks when employing a 3.3 V single-ended I2S-like format for transmitting data at high rates in a radio tuner device; these ranges from electro-magnetic interference radiation to a large number of signal wires used for the interconnection. On the contrary, LVDS interfaces are recommended for easier application design, highest performance and immunity to disturbances.

The SAI_BB supports the different modes as shown by the signal waveforms in *Figure 5*, *Figure 6* and *Figure 7*, and ; the corresponding timings are specified in *Table 5*, *Table 6* and *Table 7*.

Timing and level specifications for the I2S base-band interface configurations are detailed in *Section 3.4.7: "Digital I/O interface pins"*.

Figure 4: Architecture example for a HD-Radio™ standard receiver based on DCOP with I2S base-band data input



2.9.2 I²S configurations

I²S standard configuration

TDA7708 features a standard I²S interface, operating both with single-ended and differential signals, as shown in *Figure 5: "I2S standard configuration with single-ended signals"* and *Figure 6: "I2S standard configuration with LVDS signals"*.

External LVDS converters are not required in case the SoC processor features LVDS input pads for the I²S link. The half-cycle mode is recommended for standard I²S implementations.

Figure 5: I²S standard configuration with single-ended signals

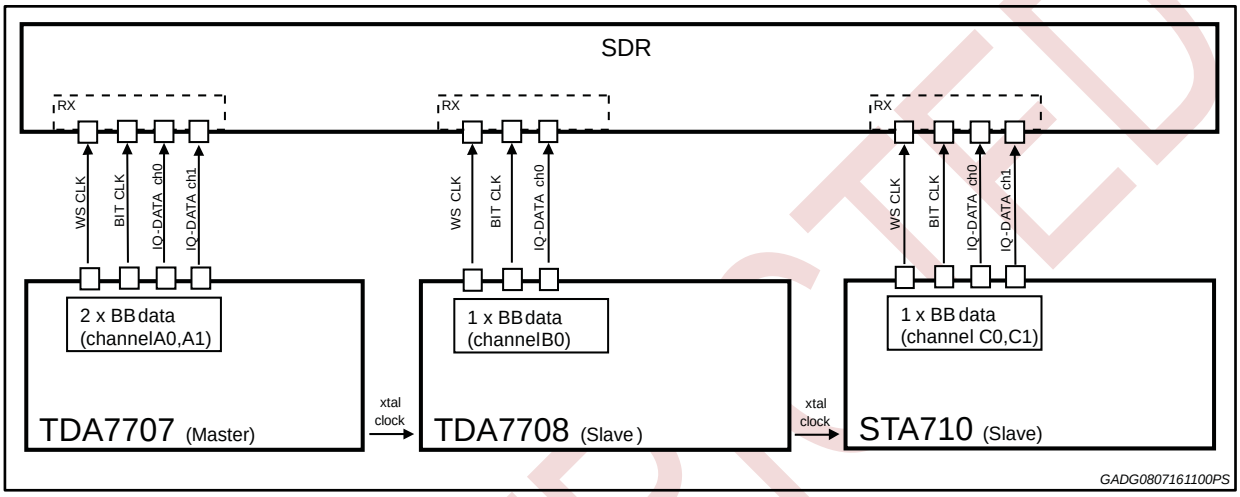
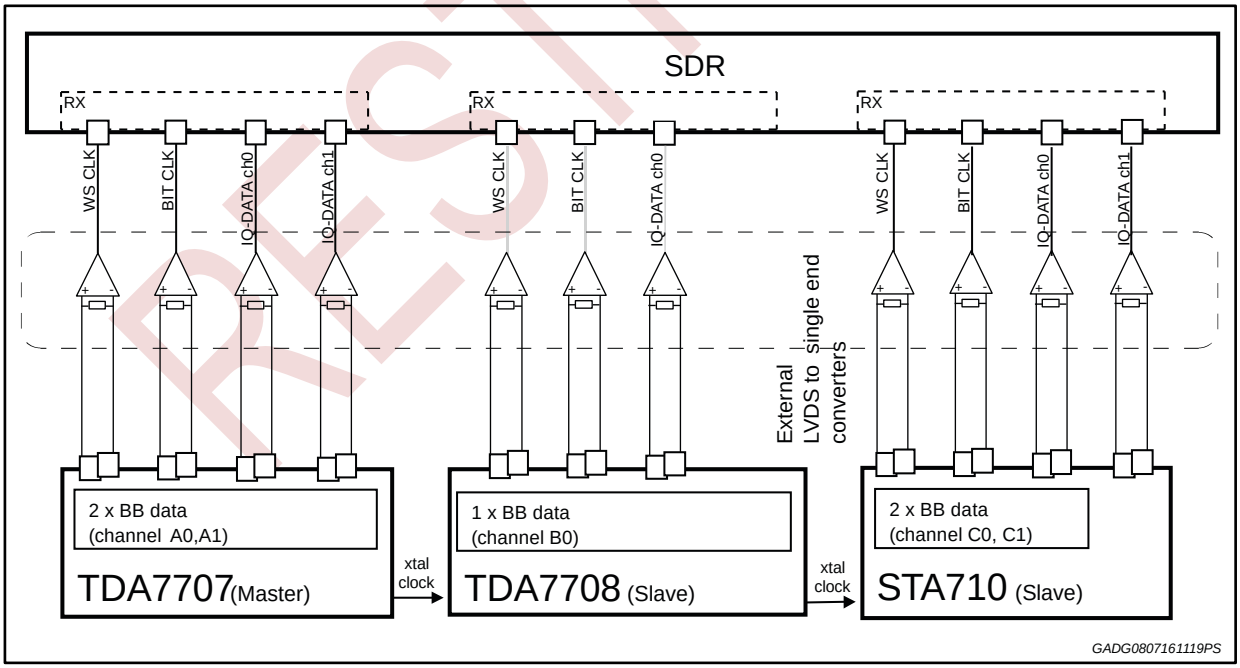


Figure 6: I²S standard configuration with LVDS signals

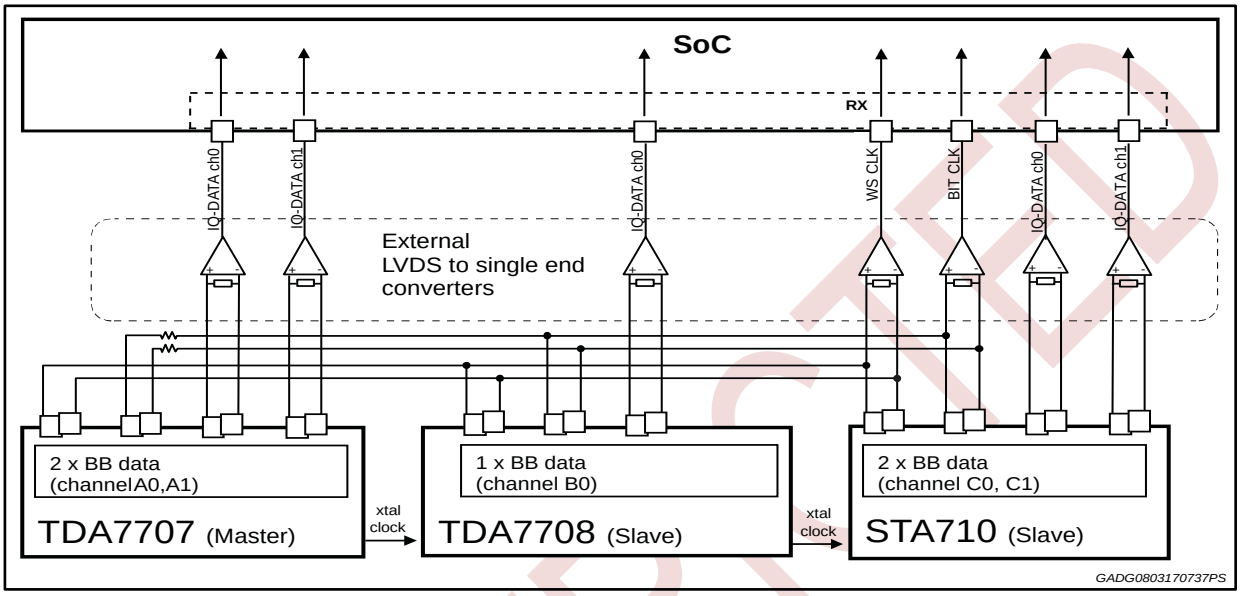


I²S single port configuration

In addition to standard configuration, the TDA7708 allows for a single-port I²S connectivity, i.e. the SoC receives a single clock/word-strobe pair and multiple data lines as shown in *Figure 7: "I2S single-port configuration"*.

The single port configuration requires the signals to be transmitted in LVDS and in full-cycle.

Figure 7: I²S single-port configuration



2.9.3 Status information data on the I²S base-band interface

The implementation of AM/FM processing into a SoC requires the tuner to inform the processor on the status of tuner AGCs. The formatting of the Si and Qi information is shown in *Table 3: "Status information for In-phase data (Si)"* and *Table 4: "Status information for Quadrature-phase data (Qi)"*.

Table 3: Status information for In-phase data (Si)

15	14	13:6	5	4	3	2:0
NU	0 → I	Overall Gain (1dB resolution)	NU	Noise Blanker Event	NU	State Event

Table 4: Status information for Quadrature-phase data (Qi)

15	14	13:9	8:6	5:0
NU	0 → Q	RF Gain (2 dB resolution)	IF Gain (2 dB resolution)	NU

2.9.4 Base-band I²S AM/FM/DRM interface

The complex AM/FM/DRM/HD-Radio™ I/Q baseband signal is sent to the external system on chip by using the serial digital output interface SAI_BB.

Figure 8: SAI_BB waveforms for SoC-based A M/FM/DRM/HD-Radio™. The data are the complex phase/quadrature signals I(16 bit)+ Q(16 bit) and their corresponding status information Si(16 bit)+ Sq(16 bit)

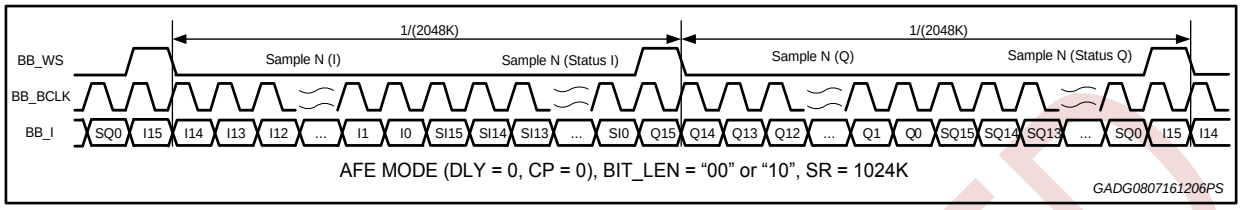


Table 5: SAI_BB timing values (I(16 bit) + Q(16 bit) and Si(16 bit) + Sq(16 bit)) for SoC-based AM/FM/DRM/HD-Radio™; I/Q and status information are multiplexed on a single data line

Symbol	Parameter	Condition	Rate	Unit
-	Data rate	Master mode	1024	kSps
f_{ws}	Word strobe		2048	kHz
f_{bclk}	Bit clock		65.536	MHz

Additionally 512 kSps rate is available with 2 x data replication.

2.9.5 Base-band I²S HD-Radio™ interface

The I/Q base-band signal needed for implementing an HD-Radio™ receiver is sent to the external processor by using the serial digital output interface SAI_BB.

Figure 9: SAI_BB waveforms for data I(16 bit)+SI(16 bit) + Q(16 bit)+SQ(16 bit) transmitted on a single data line; this configuration is used for implementing HDRadio™

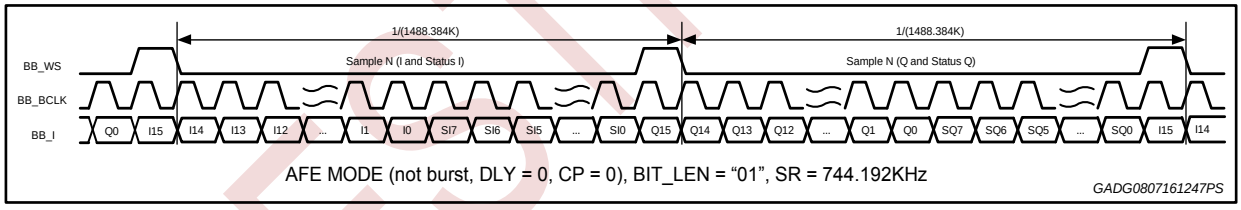


Table 6: SAI_BB timing values (normal mode: I(16 bit)+ SI(16 bit) +Q(16 bit)+SQ(16 bit) on a single data line) for HD-Radio™

Symbol	Parameter	Rate		Unit
-	Data rate	744.192	768	kSps
f_{ws}	Word strobe	1488.384	1536	kHz
f_{bclk}	Bit clock	47.628	49.152	MHz

Figure 10: SAI_BB waveform for data: I(16 bit)+ Q(16 bit) transmitted on a single data line, in DCOP (STA680D)-based HD-Radio™

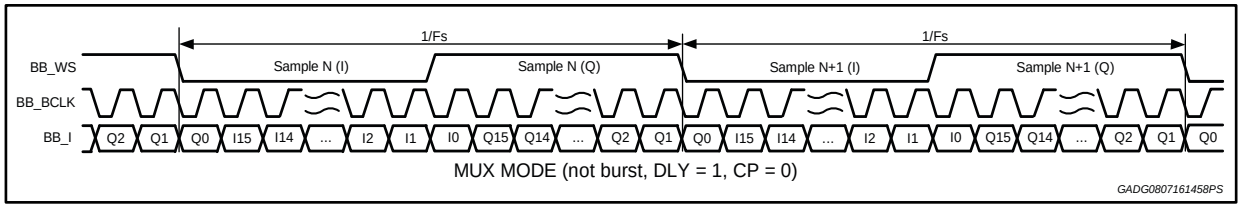


Table 7: SAI_BB timing values (normal mode: I(16 bit)+ Q(16 bit) on a single data line) for DCOP-based HD-Radio™

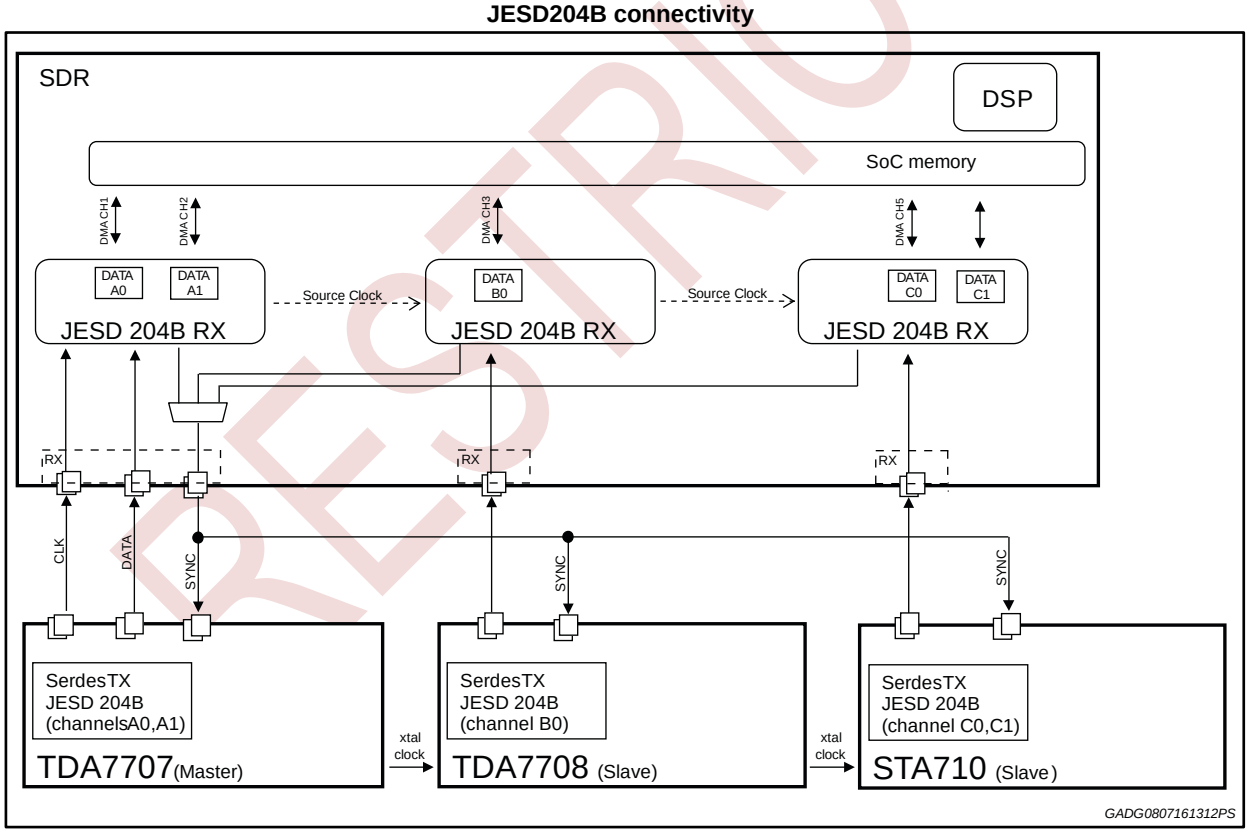
Symbol	Parameter	Rate			Unit
-	Data rate	744.192	912	650	kSps
f_{ws}	Word strobe	744.192	912	650	kHz
f_{bclk}	Bit clock	23.814	29.184	20.800	MHz

2.9.6 JESD204B base-band serial interface

TDA7708 features a standard JESD204B serial interface; this standard was originally created through the JEDEC committee to standardize and reduce the number of data inputs/outputs between high-speed data converters and other devices. Fewer interconnections simplify the PCB layout and allow smaller form factor realization without impacting the overall system performance.

The JESD204B interface offers several advantages over I2S CMOS and LVDS base-band interfaces in terms of speed, pin-count and EMI reduction; in fact, the JESD204B base-band interface is superior in terms of EMI mitigation to the single-ended CMOS I2S, since it uses differential low voltage signals, but it requires fewer pins than a standard LVDS interface.

Figure 11: Example SoC processor receiving the base-band signals from five RF channels based on JESD204B connectivity



The JESD204B physical layer is based on LVDS; a lane rate of 372.096 MHz for HDRadio™ systems is used as shown in *Table 8: "JESD204B transmitter main clocks"*.

The tuner transmission mode is based on the "Multiple Tuner Single Line" architecture, with 16 bits transmitted data (I/Q and status for each tuner stream) and configurable data scrambling and 8b10b coding.

TDA7708 has deterministic latency of Subclass 2 in order to reduce the number of signals required by the JESD204B link. SYNC signal is supported in single ended CMOS format as well.

Table 8: JESD204B transmitter main clocks

Symbol	Parameter	Ratio	DAB mode	HD mode	Unit
-	(Local) Multi Frame Clock LMFC	1	2048/K	744.192/K	kHz
-	Frame clock	K	2048	744.192	kHz
-	Character clock	K*F	32.768	37.2096	MHz
-	Bit clock	K*F*10	327.680	372.096	MHz
-	204B transmitter device clock	K*F*10	327.680	372.096	MHz
-	204B reference clock	D	327.680 (high rate) or 36.864 (low rate)	372.096 (high rate) or 36.864 (low rate)	MHz

Status data transmitted on the JESD204B base-band interface

The implementation of AM/FM processing onto a SoC requires the tuner to inform the SoC on the status of tuner AGCs. The format of the transferred information is shown in the *following tables*.

Table 9: Status information for JESD204b interface Status High (SH) in 32-bit mode

15	14	13:6	5	4	3	2:0
NU	0 → I	Overall Gain (1dB resolution)	NU	Noise Blanker Event	NU	State Event

Table 10: Status information for JESD204b interface Status Low (SL) in 32-bit mode

15	14	13:9	8:6	5:0
NU	0 → Q	RF Gain (2 dB resolution)	IF Gain (2 dB resolution)	NU

Table 11: Status information for JESD204b interface for I&Q data in 16-bit mode

15:9	8:4	3	2:0
Overall gain (1dB resolution)	RF gain + IF gain (2dB resolution)	Noise blanker event	State event

Analog mode

When configured to this mode, the JESD204B interface allows implementing a multi-tuner system aiming at receiving AM/FM/DRM signals.

A 16-bit mode is available for implementing an AM/FM system; the corresponding data formatting is shown in the *next figure*.

Figure 12: JESD204b interface in analog mode (16-bit)

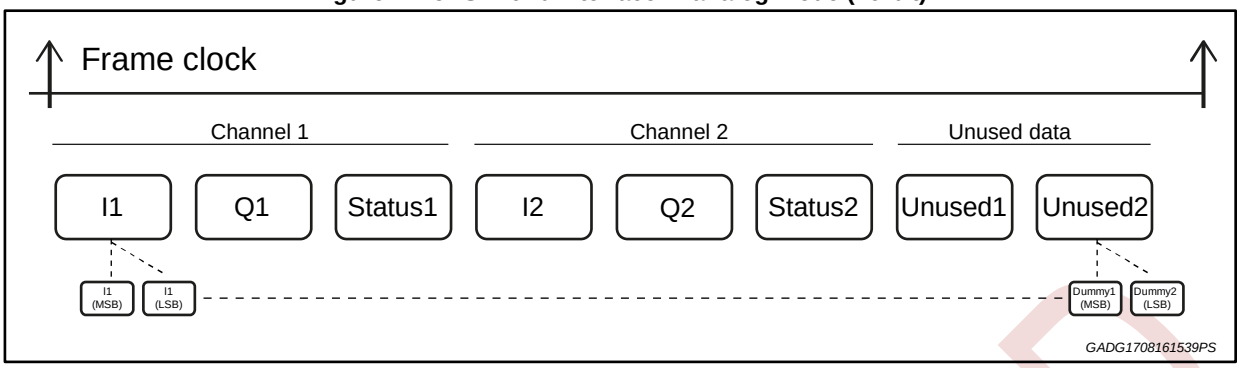


Figure 13: JESD204B interface data padding for FM/AM/DRM @ 1024 kHz in analog mode

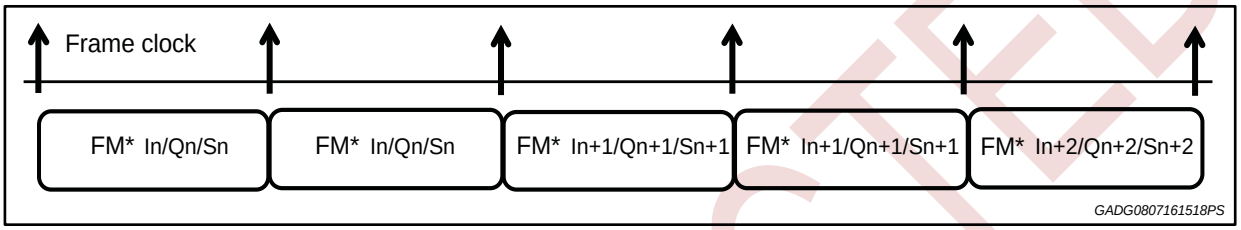


Figure 13: "JESD204B interface data padding for FM/AM/DRM @ 1024 kHz in analog mode" shows a FM/AM/DRM output at 1024 kSps; in this case the output channels are replicated twice in order to fit the transmission rate.

Figure 14: JESD204B interface data padding for FM/AM/DRM @ 512 kHz in Analog mode

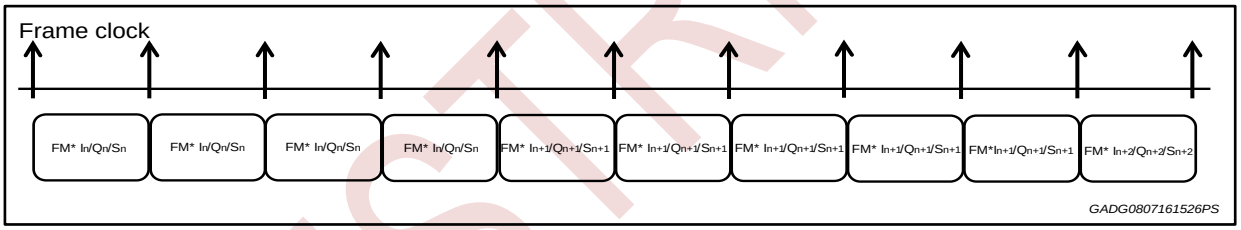
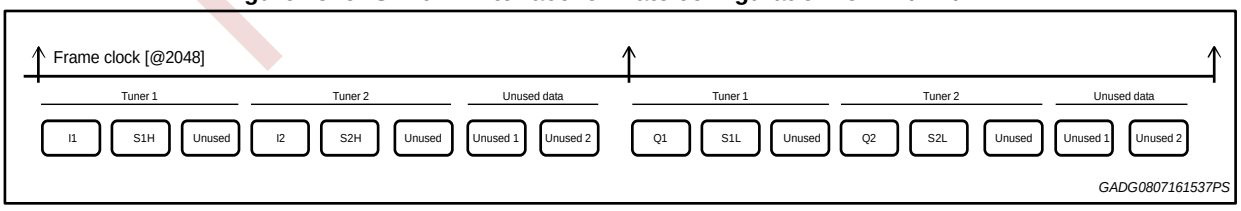


Figure 14: "JESD204B interface data padding for FM/AM/DRM @ 512 kHz in Analog mode" shows a FM/AM/DRM output at 512 kSps; in this case the output channels are replicated four times in order to fit the transmission rate.

A low rate mode is available as well: this configuration is available uniquely for implementing a FM/AM/DRM receiver and no padding is inserted to transmit the (low rate) signal. The data formatting is shown in the *next figure*.

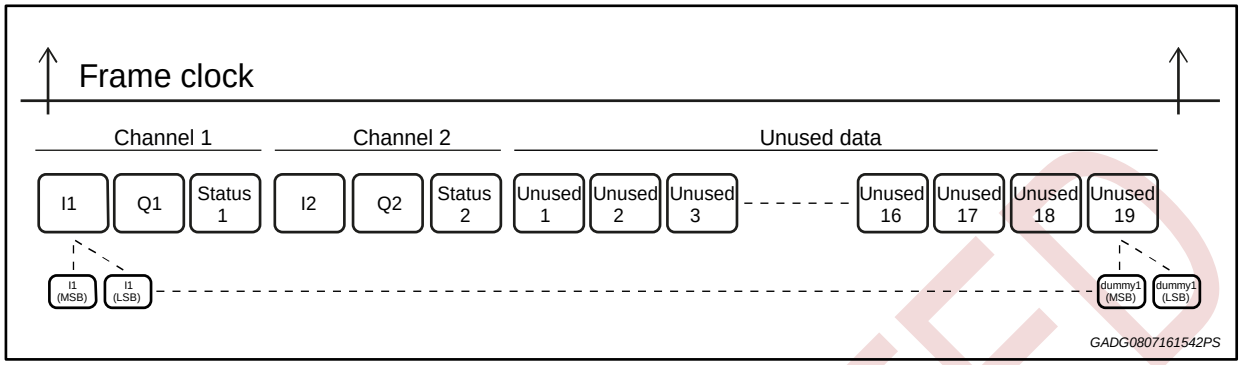
Figure 15: JESD204B interface low-rate configuration for FM/AM/DRM



Analog and HD-Radio™ mode

The structure of the data frame used for implementing an HD-Radio™ is shown in the next figure with a 16-bit implementation; no data padding is used in this case.

Figure 16: JESD204b interface for HD-Radio™ mode (16-bit)



2.9.7 Coded LVDS bit-stream to DCOP (STA660DRM) DRM decoder

This custom interface is needed in order to pair the TDA7708 to the DCOP (STA660) for implementing a complete DRM receiver and decoder.

The complex phase-quadrature base-band signals, after being coded by a custom sigma-delta modulation, are sent to the STA660 base-band processor using a double data rate LVDS digital interface.

Figure 17: Architecture example for a DRM system based on DCOP (STA660DRM) processor

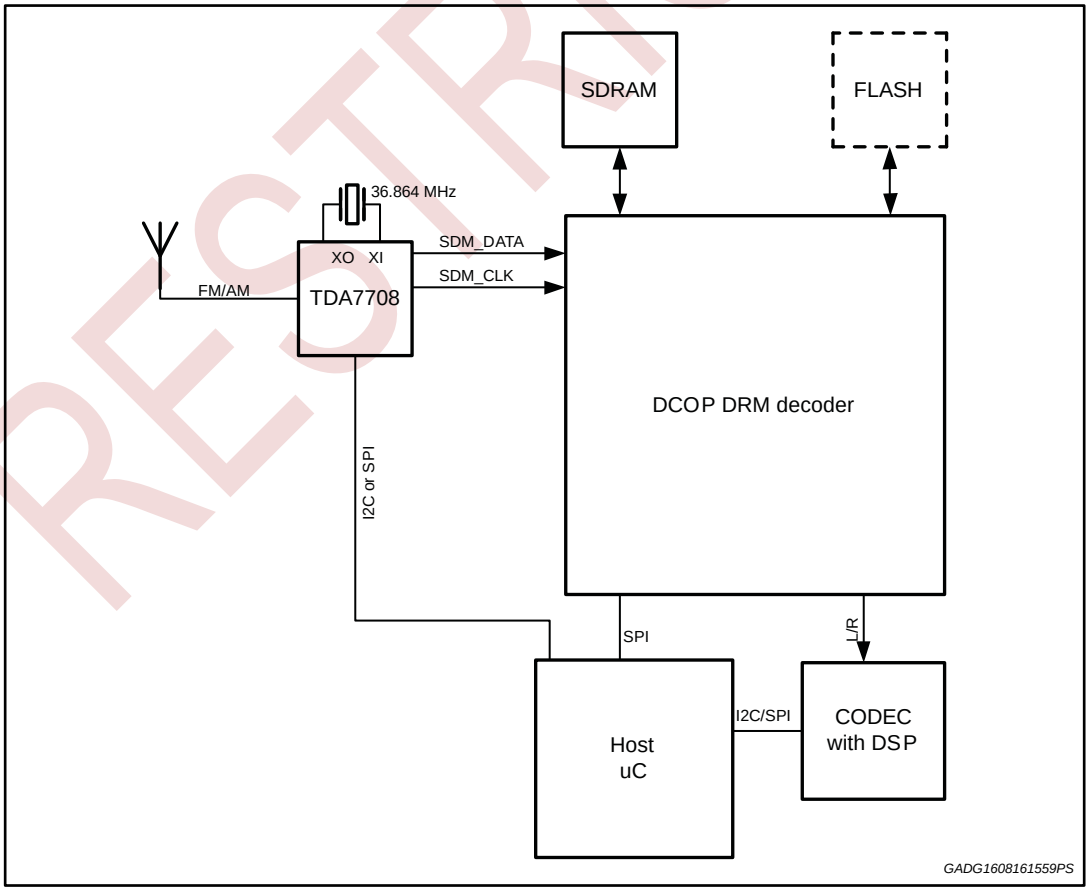
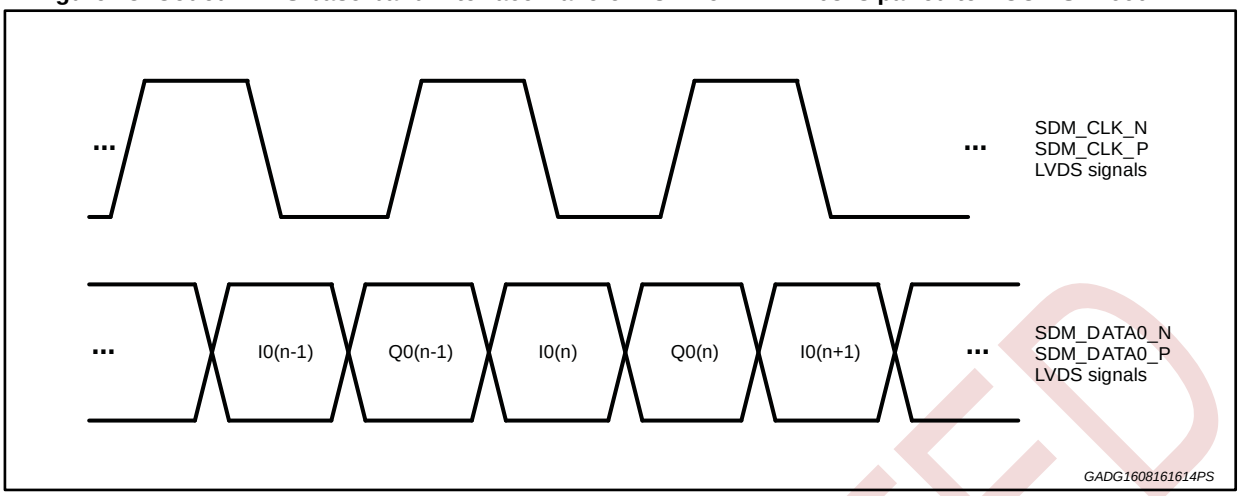


Figure 18: Coded LVDS base-band interface waveforms when TDA7708 is paired to DCOP STA660DRM



2.10 I²S - serial audio interface

The I²S audio interface (a.k.a SAI interface) provides stereo in/output audio-bus interfaces (e.g. to an external audio-processor, external digital-radio decoder) using the I² S protocol. This standard protocol requires a bit clock line, a word select line and data lines.

Two independent SAI interfaces are available in order to operate at different audio data rates. Each interface has dedicated clock lines: AIF1_CLK, AUX_CLK are the bit clock lines, while AIF1_WS, AUX_WS are the word select (frame) clock lines.

AIF1_DIN is the receiver input line, while AIF1_DO0 and AUX_DATA are the transmitter output lines.

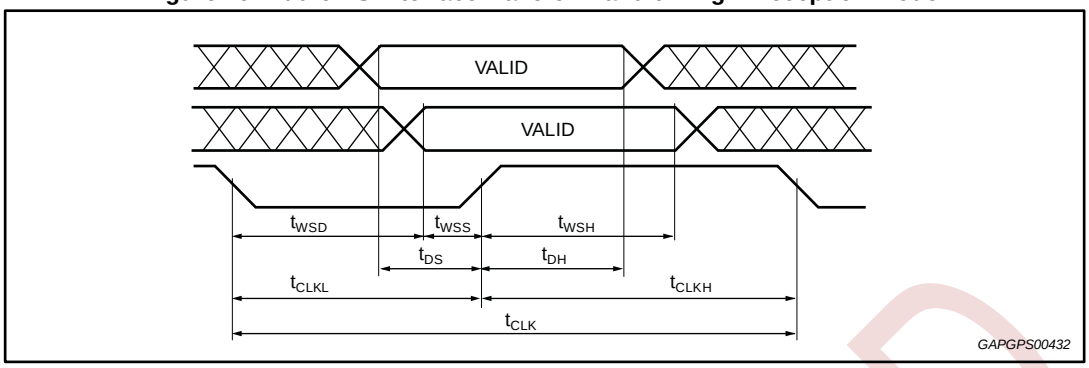
In master mode both the bit and frame clock are configured as outputs, in slave mode these pins are set as inputs.

The bit clock has one pulse for each discrete bit of data on the data lines; the bit clock operates at a frequency which is a multiple of the sample rate.

Table 12: Audio I²S configuration overview

Channels	World length	Bits	Master /Slave mode	Input Rate/kSps	Output Rate /kSps	Max. bit clock frequency
1x2 In	16/24/32	16/24	M/S	32-48	-	3.072 MHz
1x2 Out	16/24/32	16/24	S	-	32-48	3.072 MHz
1x2 Out	16/24/32	16/24	M	-	32, 44.1, 45.6, 48	3.072 MHz

Figure 19: Audio I²S interface waveform and timing in reception mode

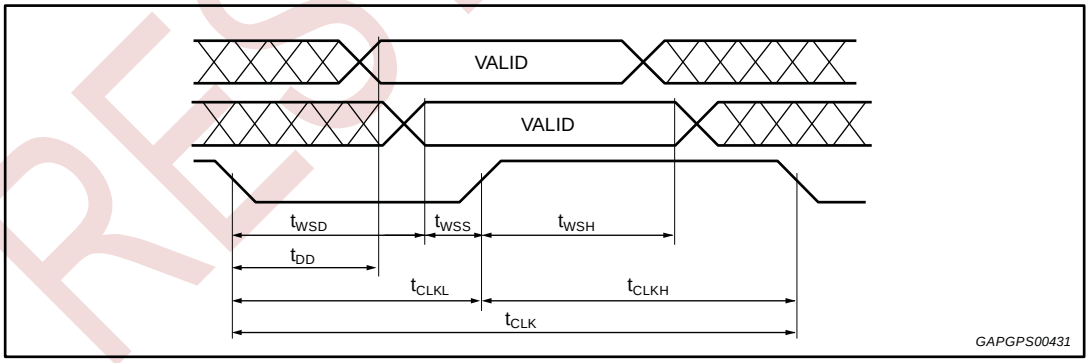


The polarity of the signals and the data bit-shift direction can be selected by configuration bits.

Table 13: Audio I²S interface timing in reception mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{CLK}	Minimum Clock Cycle (CLK)	-	50	-	-	ns
t_{CLKH}	Minimum bit clock high time	-	25	-	-	ns
t_{CLKL}	Minimum bit clock low time	-	25	-	-	ns
t_{WSS}	Word-select setup time	slave mode	5	-	-	ns
t_{WSH}	Word-select hold time	slave mode	3	-	-	ns
t_{WSD}	Word-select delay	master mode	-	-	4	ns
t_{DS}	Data setup time	-	5	-	-	ns
t_{DH}	Data_hold time	-	5	-	-	ns

Figure 20: Audio I²S interface waveform and timing in transmission mode



The polarity of the signals and the data bit-shift direction can be selected by configuration bits.

Table 14: Audio I²S interface timing in transmission mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{CLK}	Minimum Clock Cycle (CLK)	-	50	-	-	ns
t_{CLKH}	Minimum bit clock high time	-	25	-	-	ns
t_{CLKL}	Minimum bit clock low time	-	25	-	-	ns
t_{WSS}	Word-select setup time	slave mode	5	-	-	ns
t_{WSH}	Word-select hold time	slave mode	5	-	-	ns
t_{WSD}	Word-select delay	master mode	5	-	-	ns
t_{DD}	Data delay	-	-	-	5	ns

The SAI can be configured via software for operating either in master or in slave mode. The frame length is selectable as 16/32 bits per word, with either 16/24 valid bits. *Figure 21: "Audio I2S interface 16-bit data"* shows the default setting of SAI for the 16-bit mode. Different settings for clock polarity, word clock polarity, transmission mode (I²S mode) and data direction (either MSB or LSB first transmission) are possible, and can be configured by software.

Figure 22: "Audio I2S interface 32/24/20/16-bit data" shows the supported I²S protocols.

Figure 21: Audio I²S interface 16-bit data

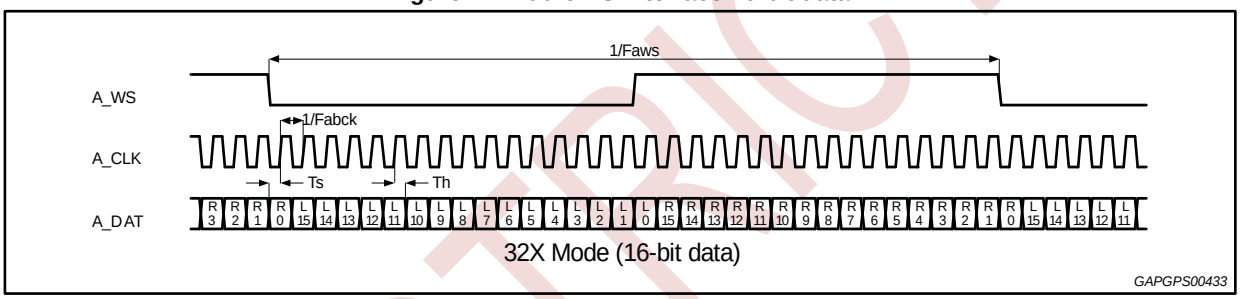
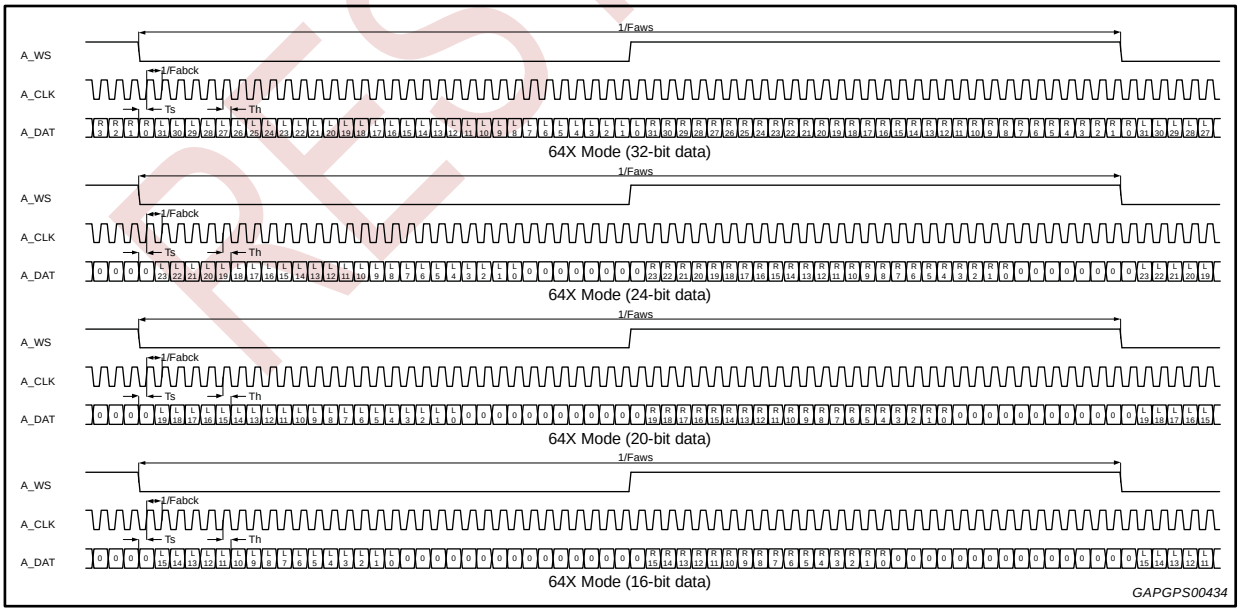


Figure 22: Audio I²S interface 32/24/20/16-bit data

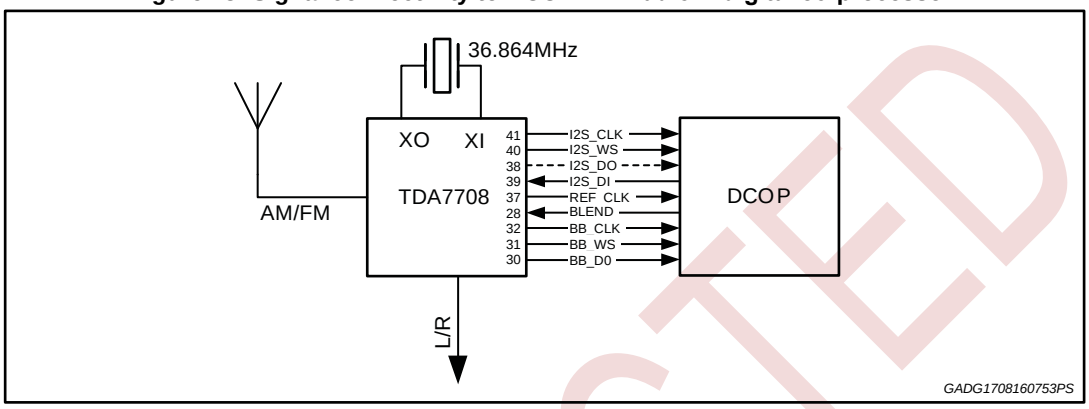


2.10.1 Connectivity to DCOP for HD-Radio™

TDA7708 can generate a 2.9184 MHz clock signal on pin-30 (GPIO13) that can be used by DCOP-HD as reference clock as shown in *Figure 23: "Signal connectivity to DCOP HD-Radio™ digital co-processor"* thus not requiring a dedicated crystal on the digital co-processor.

The electrical characteristic is specified in *Table 29: "Digital I/O interface pins"*.

Figure 23: Signal connectivity to DCOP HD-Radio™ digital co-processor



2.11 Audio sample rate converter

The sample rate converter block consists of three independent sample rate converters (SRC) for stereo input or output. SRC is able to convert input frequencies between 32 kHz and 48 kHz to internal audio processing rate and vice versa.

The integrated LPF channel limits the bandwidth of the input signal to $f_{sout}/2$ in case of down-sampling (i.e. $f_{sin} > f_{sout}$) to get an alias-free output signal.

The sample rates needed for the conversion are automatically computed. Each SRC includes a sample clock jitter rejection function that can be enabled separately. The input-signal word-width is 20-bits for all the three sample rate converters; the output signal word-width can be either 20-bits or 16-bits for each SRC.

2.12 Digital-Down-Converter

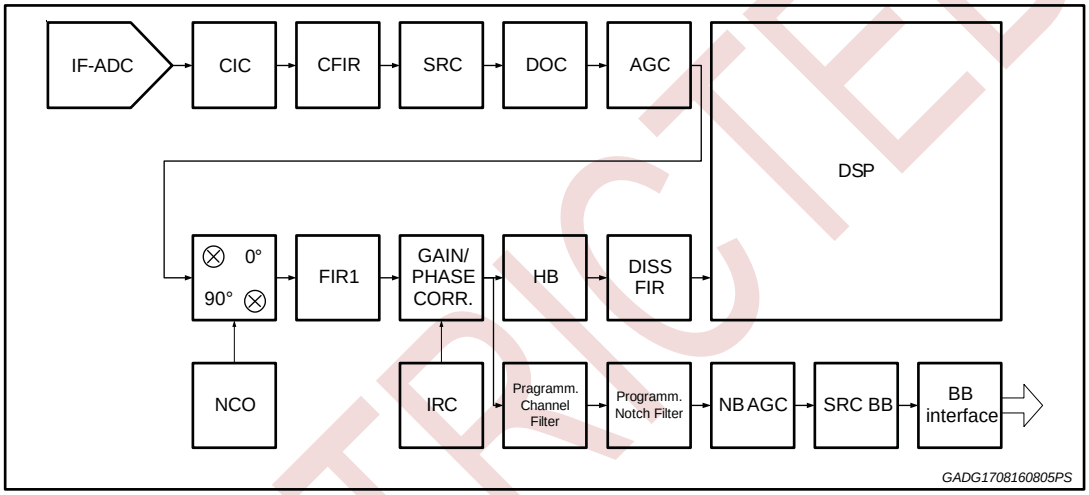
The signal from the IF-ADC is filtered and down-sampled to a lower rate by mean of a digital down converter (DDC).

The DDC is a cascade of a phase-quadrature complex digital mixer, down-sampling filters and image rejection (IR) processing; the block diagram of the DDC is shown in *Figure 24: "Digital-Down-Converter block diagram"*.

The high-precision complex digital mixer in the DDC performs mixing of the low-IF signal to Zero-IF (ZIF).

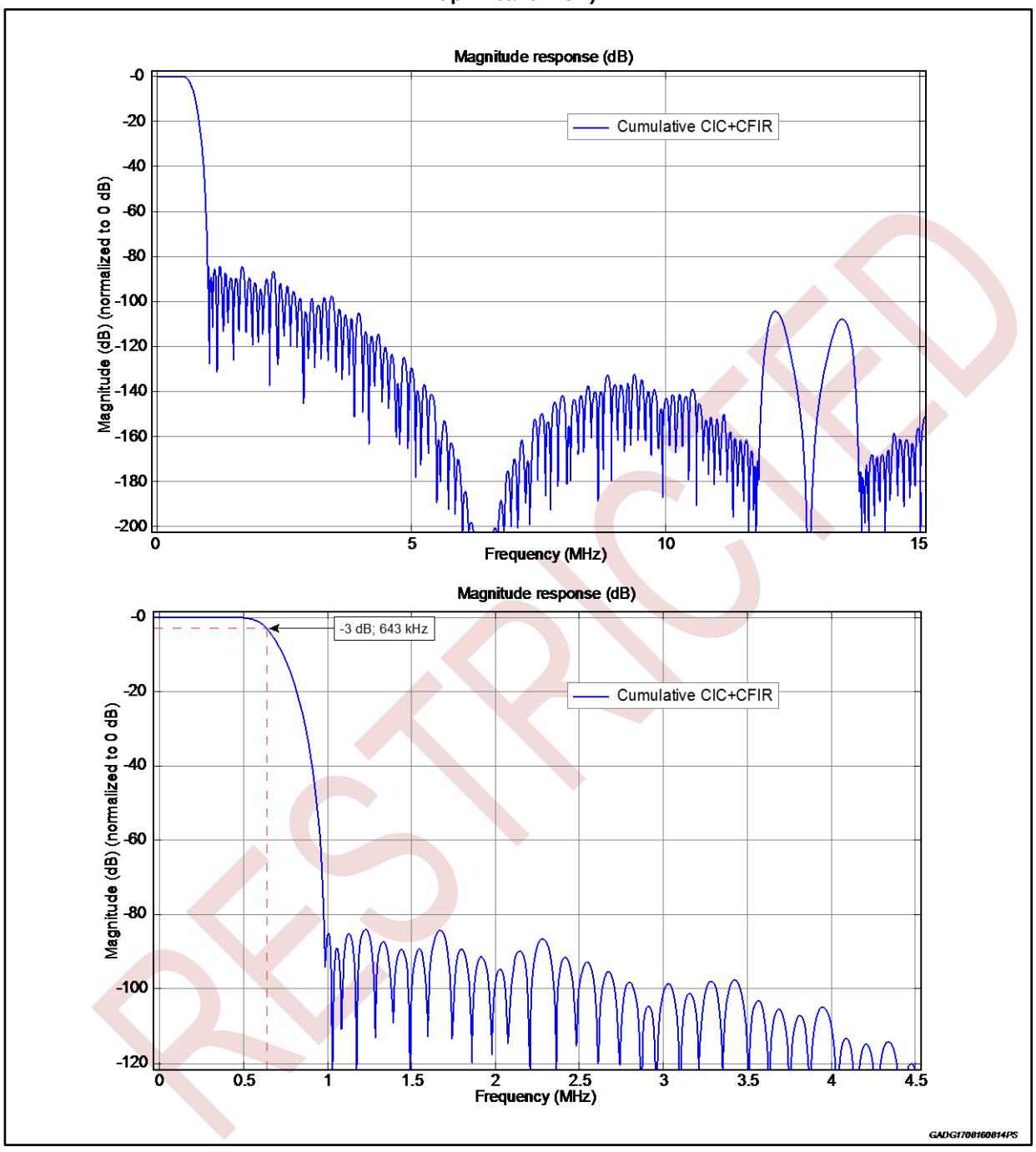
The image rejection processing provides additional suppression of image signals on top of the intrinsic image rejection provided by the RF mixer. The IR processing is designed in order to have very fast convergence for alternative-frequency tests.

Figure 24: Digital-Down-Converter block diagram



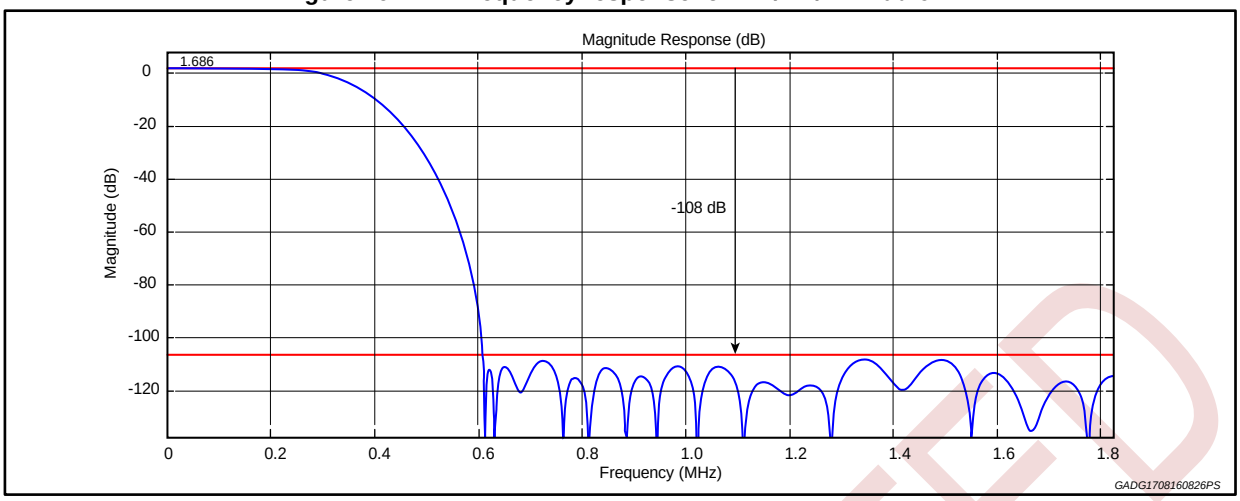
The overall CIC+CFIR frequency response for AM/FM/HD/DRM is reported in the *next figure*.

Figure 25: Cumulative CIC+CFIR Frequency response for AM/FM/HD-Radio™ (top: full band; bottom: close-up in-band view)



The FIR1 frequency response for AM/FM/HD/DRM is reported in *the next figure*.

Figure 26: FIR1 frequency response for AM/FM/HD-Radio™



After the Image Rejection block and the DISS filter, there is a 78th order FIR with programmable coefficients (18-bit quantization), named FIR2, which can be used either as channel filter for HD-FM, FM or as anti-alias filter (in front of the sample rate conversion made by SRC BB).

Albeit FIR2 coefficients are programmable, a set of default parameters for each operative mode has been coded in IC ROM.

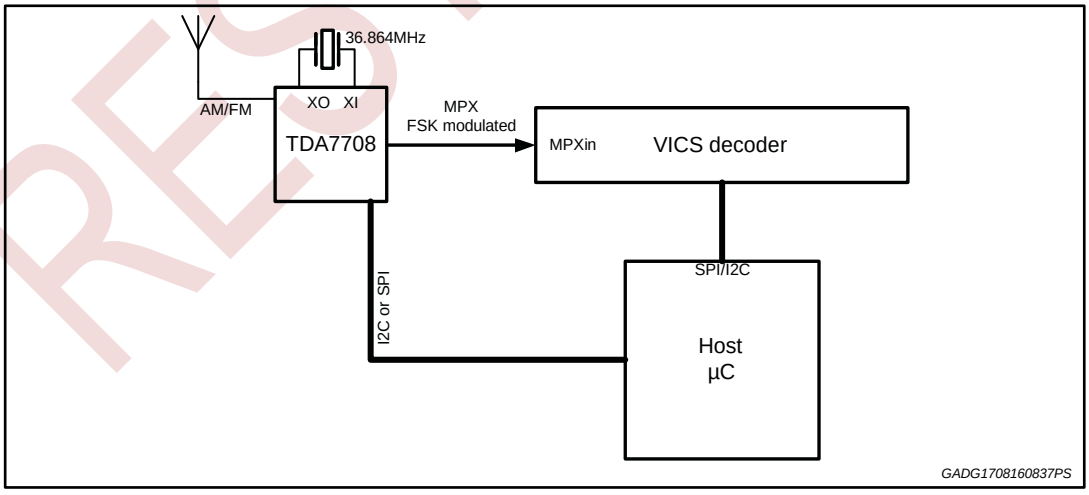
2.13 DARC interface

A single-line VICS interface is available on TDA7708.

The MPX signal is up-sampled at high frequency and modulated in FSK, thus carrying exactly the same information as an analog MPX signal.

The resulting bit-stream can feed the analog-MPX input of an external VICS decoder.

Figure 27: System architecture for VICS reception



2.14 Control interface

Configuration and control data are written to the TDA7708 via the control interface. The control interface supports two standard protocols: I²C and SPI slave.

2.14.1 Control interface selection

The TDA7708 control interface can be configured to be either in I²C, SPI or JTAG mode. Applying either high or low levels at Pin 55, Pin 52 and Pin 50, as indicated in *Table 15: "Control interface configuration pins"*, selects the device operation mode.

The configuration is latched (i.e. made effective) when the RSTN line is released, going from low to high (when RSTN is low, the IC is in reset mode).

The voltage level forced to the boot pins must be released to start the system operation a suitable time after the RSTN line has gone high.

In order to set a high level to the boot configuration pins it is necessary to use an external pull-up resistor smaller than 10 kΩ, to override the internal pull-down resistor (nominal 50 kΩ).

Table 15: Control interface configuration pins

CONF2, Pin 55 (TEST_D)	CONF1,Pin 52 (SPI_MISO)	CONF0,Pin 50 (IRQ)	Boot mode
1	-	-	JTAG
0	0	0	I2C address C2/C3
0	0	1	I2C address C8/C9
0	1	0	I2C address C0/C1
0	1	1	SPI

The function of control interface pins (pin 51 to 54) varies depending on the selected protocol as shown in the *next table*.

Table 16: Mapping of SPI pins to I² C pins

Pin #	I²C	SPI
51	-	SPI_CS
52	-	SPI_MISO
53	I2C_SDA	SPI_MOSI
54	I2C_SCL	SPI_CLK

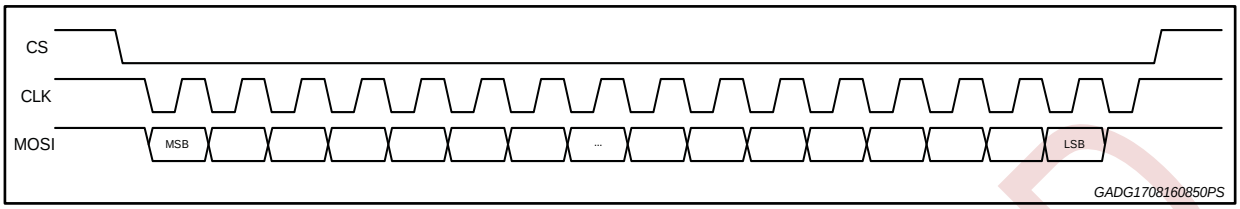
2.14.2 SPI bus protocol description

The SPI requires four signals: clock (CLK), master output/slave input (MOSI - for communication from host controller to TDA7708), master input/slave output (MISO - for communication from the TDA7708 to the host micro-controller) and chip select (CS). CLK is generated by the master device (typically the host micro-controller) and it is used for synchronization. MOSI and MISO are the data lines. The protocol is implemented to support 32 bits of command/address and 32 or 24 bits of data. The master-device pulls down the TDA7708 CS line in order to address it and start the communication. The protocol does not have any transmission acknowledgment.

Among the four possible modes, the data are latched on the clock rising edge, with CPOL = 1 and CPHA = 1. According to the specification of this mode, the polarity of the CLK line is high when no communication is taking place.

A "write" communication example is shown in the *next figure*, for a generic number of bits.

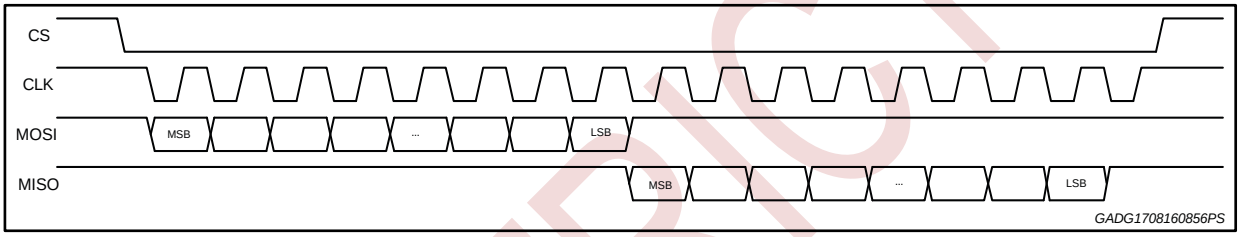
Figure 28: SPI interface write cycle



The cycle is initiated by the high-to-low transition of the SPI_CS line. The CLK pulses clock the instruction and the data into the MOSI line. Data is transmitted MSB first.

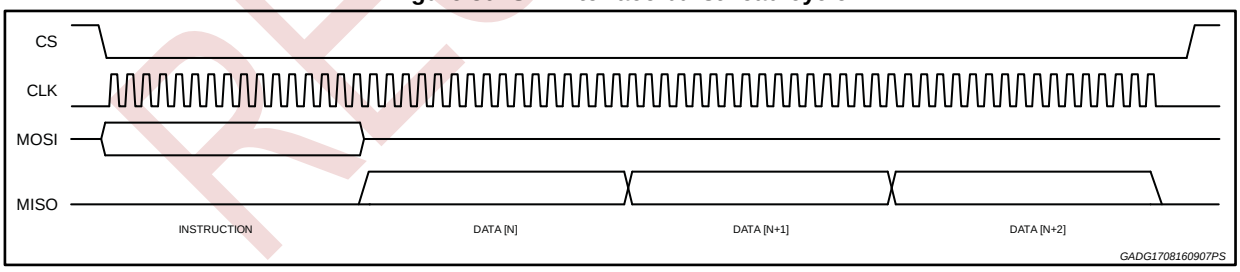
The read cycle is illustrated in *Figure 29: "SPI interface read cycle"*. It is similar to the write cycle, except that instead of the data word being clocked into MOSI during the second half of the cycle, the data word is clocked out of MISO.

Figure 29: SPI interface read cycle



Read and write "burst-mode" transfers are supported. For a block transfer, multiple data words are transmitted following the memory read or write instruction. The data words are read from or written sequentially starting at the address contained in the instruction. The sequential access terminates when the CS line goes high. *Figure 30: "SPI interface burst-read cycle"* shows a register block read cycle. In the illustration, three subsequent register locations are read starting at address N. The block write cycle is similar, except of course when data is clocked into MOSI.

Figure 30: SPI interface burst-read cycle



In all cases, the control interface is reset when CS goes high. If the final CLK is not received before CS goes high, then the cycle will end prematurely. For a read cycle, the transfer of data will terminate; for a write cycle, no data will be written.

2.14.3 I²C bus protocol description

The TDA7708 control interface can be configured to comply with standard I²C protocol.

The TDA7708's I²C address is selected at startup by setting Pin 55, Pin 52 and Pin 50 to either high or low, as shown in *Table 15: "Control interface configuration pins"*.

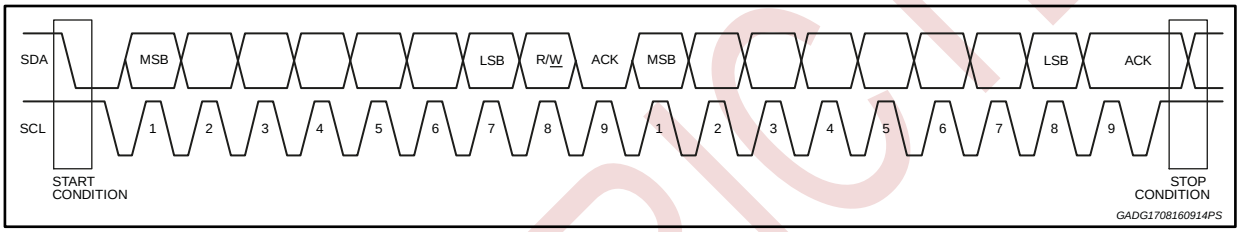
The I²C communication requires two signals: clock (SCL) and data (SDA - bidirectional). The protocol specifies an optional acknowledge signal after any 8-bit transmission.

Each data byte is 8-bits long and must be followed by an acknowledge bit. A start condition is defined as a high to low transition of the SDA signal with SCL high, and a stop condition is defined as a low to high transition of the SDA signal with SCL high. A pulse of the SCL clock signal indicates the transfer of data or an acknowledge bit on the SDA pin. The transmitting device drives SDA data during clock periods 1-8.

The SDA signal is always driven as an open collector output and an external pull-up resistor is required for proper operation.

The receiving device acknowledges by driving SDA low during the 9th clock pulse. Master devices always generate the SCL clock and initiate transactions.

Figure 31: Example of data transfer on the I²C bus



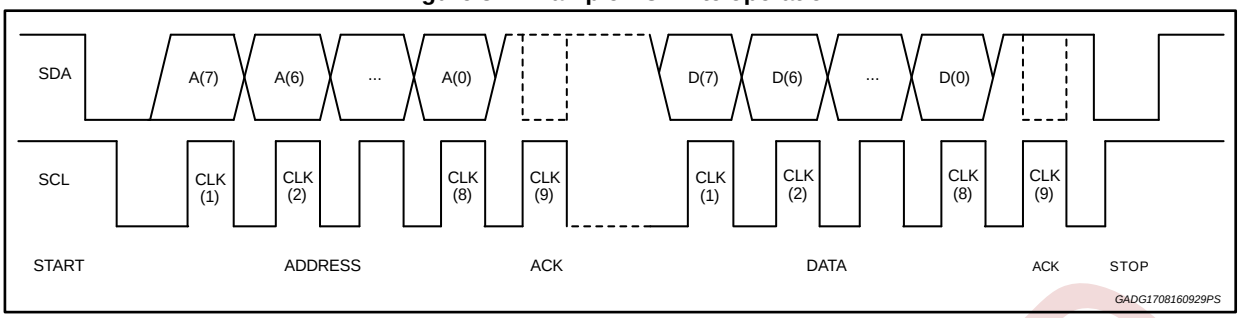
I²C write operation

The write sequence consists of the following phases:

1. START: SDA line transitioning from high to low with SCL fixed to high. This indicates that a new transmission is starting;
2. DATA LATCHING: on the rising SCL edge. The SDA line can vary only when SCL is low (otherwise its transitions are interpreted as either a START or a STOP transition);
3. ACKNOWLEDGE: on the 9th SCL pulse the microprocessor keeps the SDA line high, and the IC pulls it down in case the communication has been successful. Lack of the acknowledge pulse generation from the TDA7708 indicates a communication failure; the chip-address byte must be sent at the beginning of the transmission according to the mode chosen at start-up during boot for "write"; as many data bytes as needed can follow the address before the communication is terminated;
4. STOP: SDA line transitioning from low to high with SCL high. This indicates the end of the transmission.

A "write" communication example is shown in *Figure 32: "Example I2C write operation"*, for an unspecified number of data bytes.

Figure 32: Example I²C write operation



I²C read operation

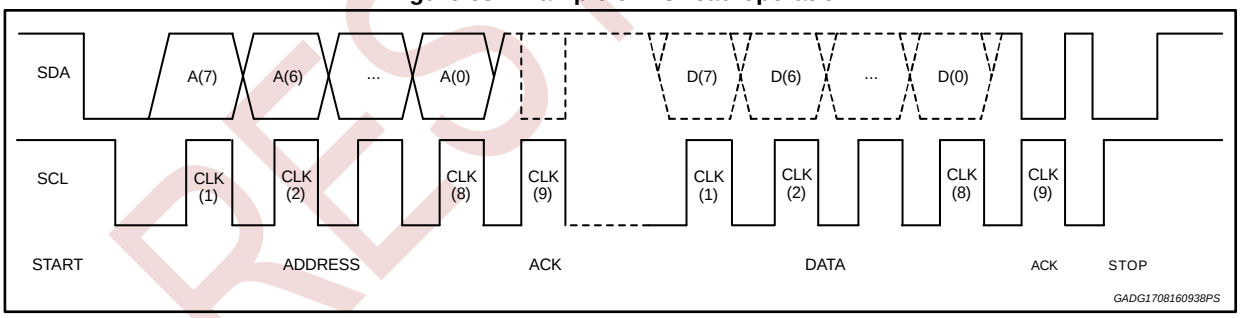
The "read" sequence is similar to the "write" and it has the same constraints for start, stop, data-latching; "read" and "write" operations differ by:

- The chip-address must always be sent by the host to the TDA7708; the address must be C3 (if C2 had been selected at boot), C9 (if C8 had been selected at boot) or C1 (if C0 had been selected at boot);
- The header is transmitted after the chip address (the same happens for "write") before data are transferred from the TDA7708 to the microprocessor;
- When data are transmitted from the TDA7708 to the µP, the latter keeps the SDA line high;
- Acknowledge pulse is generated by the host microprocessor for those data bytes that are sent by the TDA7708 to the micro. Microcontroller's failing to generate an ACK pulse on the 9th clock pulse has the same effect on the TDA7708 as a STOP.

Dashed lines represent transmissions from the to the microprocessor. A "read" communication example is shown in *Figure 33: "Example of I2C read operation"*, for an unspecified number of data bytes.

The maximum clock speed is 400 kbit/s.

Figure 33: Example of I²C read operation



2.15 Start-up sequence

This section describes the sequence required to start TDA7708.

2.15.1 Power-up sequence

TDA7708 requires eight pins to be supplied by an external 3.3 V source as shown in *Table 17: "Power-supply pin description"*. Dedicated supply pins for the most sensitive blocks allow using external filtering and an even distribution of by-passing capacitors; these techniques allow improving the rejection to the power supply noise.

In order to decrease the thermal power to be dissipated by the IC, Pin45 and pin46 need to be supplied by dumping the 3.3 V supply with a series resistance, as shown in the application diagram.

Table 17: Power-supply pin description

Pin #	Pin name	Direction	Description
External power supply			
16	VCC_RF	Input	RF supply
20	VCC_PLL	Input	PLL supply
24	VCC_GLOBAL	Input	Analog supply
35	VDD_IO	Input	Digital I/O supply
45	VDD_R	Input	Digital back-end 1.2 V regulator supply
46	VDD_R	Input	Digital back-end 1.2 V regulator supply
57	VCC_ADC	Input	IF-ADC supply
Internally regulated supply			
4	REF1_FM	Output	Internally regulated 2.5 V output
44	VREG_1V2	Output	Internally regulated 1.2 V output
12	VCC_FM	Input	2.5 V FM supply

It is strictly forbidden to connect any external load to the internally regulated supplies on pin 4 and pin 44.

2.15.2 Start-up sequence

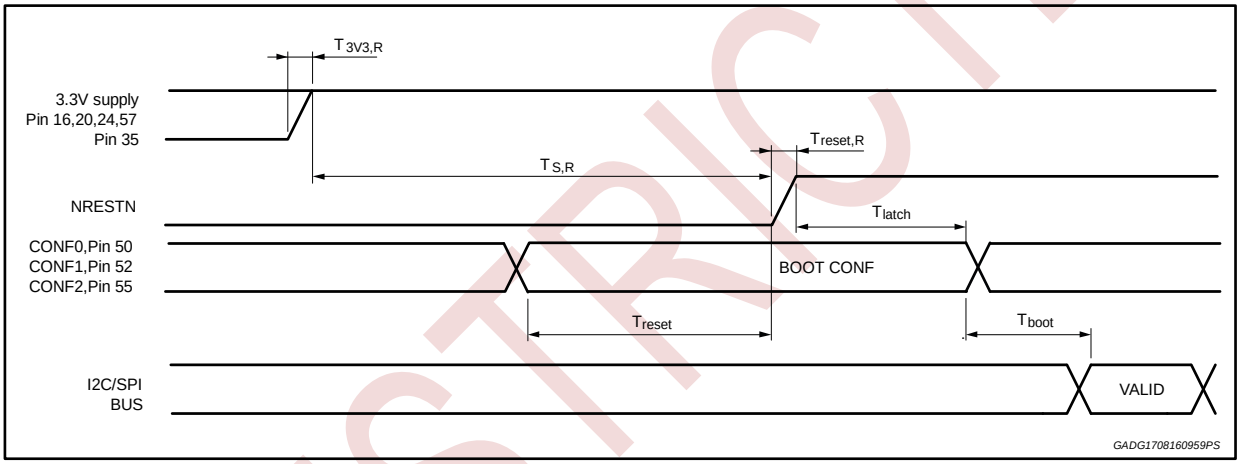
The recommended start-up sequence is shown in *Figure 34: "Start-up sequence"* with values listed in*Table 18: "Start-up sequence timing"*.

The supply to the digital core (pin 46 and 45) needs to be derived from the main 3V3 supply.

Table 18: Start-up sequence timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{3V3,R}$	3.3 V supply rise-time	-	-	-	1	ms
$t_{S,R}$	Power-up time	-	100	-	-	µs
$t_{RESET,R}$	Reset rise-time	-	-	-	1	µs
t_{RESET}	Stable active reset time	-	10	-	-	µs
t_{LATCH}	Configuration latch time	-	10	-	-	µs
t_{BOOT}	Boot time	-	1	-	-	ms

Figure 34: Start-up sequence



2.16 Reset

The reset line drives the global reset of all the digital gates.

Reset timings are shown in *Figure 35: "Reset timing"* and in *Table 19: "Reset timing"*.

Figure 35: Reset timing

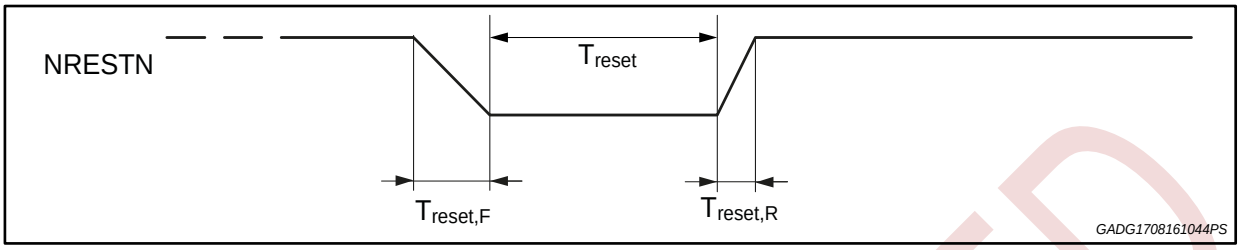


Table 19: Reset timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{RESET,F}$	Reset fall-time	-	-	-	1	µs
$t_{RESET,R}$	Reset rise-time	-	-	-	1	µs
t_{RESET}	Active reset time	-	10	-	-	µs

3 Electrical specification

3.1 Absolute maximum ratings

Table 20: Absolute maximum ratings

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC}	Abs. supply voltage	-	-0.5	-	3.6	V
T_{stg}	Storage temperature	-	-55	-	150	°C
V_{ESD}	ESD absolute minimum withstand voltage	Human Body model	>|±2000|(1)			V
		Charged device model	>|±500|(2)			
		Charged device model, corner pins	>|±750|			
-	Max. input at any pin (latch-up characteristic)	I_{INMAX}	±100			mA

Notes:

(1)|±1000| on pin 14

(2)|±400| on pin 14

3.2 Thermal data

Table 21: Thermal data

Symbol	Parameter	Test condition	Value	Units
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient	Multilayer 2s2p as per JEDEC JESD51-7	27	°C/W

3.3 General key parameters

Table 22: General key parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC}	3.3 V supply voltage	-	3.15	3.3	3.45	V
I_{CC}	Supply current	FM @108 MHz, active interfaces (10 pF load)	-	-	350	mA
T_{amb}	Ambient Temperature Range	-	-40	-	85	°C
T_{j_oper}	Operative Junction Temp	-	-	-	125	°C
V_{DDR}	Digital core unregulated supply voltage	-	1.5	-	-	V
I_{DDR}	Digital core supply current	-	-	-	119	mA
P_{diss}	Dissipated power (1)	R_{ext} = 12 Ohm	-	-	1	W

Notes:

(1)Total power dissipated inside the IC is $V_{cc} * I_{cc} - R_{ext} * I_{DDR}^2$.

3.4 Electrical characteristics

V_{CC} = 3.15 V to 3.45 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

3.4.1 FM - section

Table 23: FM - section

Symbol	Parameter	Test condition	Min	Typ	Max	Units
FM input						
RF Gain	Voltage gain	Including pre-selector Measured at single ended test output @ maximum IF gain	40.5	42	43.5	dB
Z_{in}	LNA input impedance	Resistance @ 100 MHz	-	1	-	kΩ
		Capacitance at max LNA gain @ 100 MHz	-	33	-	pF
NF	Overall Noise Figure	Including pre-selector Measured at single ended test output	-	6	8	dB
IIP3	3rd order intercept point	Max gain (@ Δf = 1MHz)	115	120	-	dBµV
LO harm	LO harmonic suppression	N = 2 – 5 including pre-selection	-	70	-	dB
FM AGC						
FM $AGC_{th,LOW}$	RF AGC threshold Low (programmable by FW)	Far off interferer	75	-	-	dBµV
FM $AGC_{th,HIGH}$	RF AGC threshold High (programmable by FW)	Far off interferer	-	-	82	dBµV
FM $AGC_{deltath}$	RF AGC threshold spread		-2.5	-	2.5	dB
$G_{steps,RF}$	RF AGC gain steps		1	2	3	dB
$AGC_{R,RF}$	RF AGC range		34	36	-	dB
$G_{steps,IF}$	IF AGC gain steps		1.5	2	2.5	dB
$AGC_{R,IF}$	IF AGC range		5	6	7	dB

3.4.2 AM - section

F_{rf} = 999 kHz (1000 kHz for US), unless otherwise specified

Figure 36: AM capacitive antenna dummy

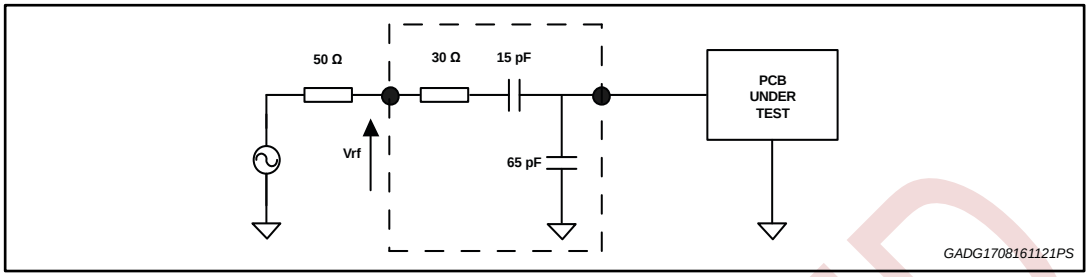


Table 24: AM - section

Symbol	Parameter	Test condition	Min	Typ	Max	Units
AM input						
RF Gain	Voltage gain	AM dummy in to single ended test output	14	15	16	dB
Z_{in}	LNA input impedance	Resistance @ 1 MHz	-	11.3	-	kΩ
		Capacitance @ 1 MHz	-	120	-	pF
Noise	LNA Input noise	At LNA input	-	0.7	0.9	nV/√(Hz)
IIP3	3rd order intercept point	Maximum gain, capacitive dummy antenna (@ Δf = 100 kHz)	130	133	-	dBµV
IIP2	2nd order intercept point	Maximum gain, capacitive dummy antenna	155	165	-	dBµV
LO harm	LO harmonic suppression	N = 2 - 21	-	70	-	dB
AM AGC						
AM $AGC_{th,LOW}$	RF AGC threshold Low (programmable by FW)		88	-	-	dBµV
AM $AGC_{th,HIGH}$	RF AGC threshold High (programmable by FW)		-	-	96	dBµV
AM $AGC_{deltath}$	RF AGC threshold spread		-3	-	3	dB
$G_{steps,RF}$	AGC gain steps	-	5	6	7	dB
$AGC_{R,RF}$	AGC range	-	46	48	-	dB

3.4.3 VCO

Table 25: VCO

Symbol	Parameter	Test condition	Min	Typ	Max	Units
F_{VCO_MIN}	Minimum VCO frequency	-	-	-	4800	MHz
F_{VCO_MAX}	Maximum VCO frequency	-	6080	-	-	MHz

3.4.4 Phase locked loop

Table 26: Phase locked loop

Symbol	Parameter	Test condition	Min	Typ	Max	Units
PN_{PLL}	Phase Noise of PLL	values referred @ 100 MHz @ 1 kHz @ 10 kHz @ 100 kHz @ 1 MHz		 -113 -115 -125 -145		dBc/Hz
f_{step}	Tuning step FM	Programmable by FW	-	1	-	kHz

3.4.5 IF ADC

Table 27: IF ADC

Symbol	Parameter	Test condition	Min	Typ	Max	Units
DR_{FM}	Dynamic range in FM	BW = ±100 kHz	94	97	-	dB
DR_{AM}	Dynamic range in AM	BW = ±3 kHz	110	113	-	dB
$SFDR_{AM}$	Spurious free Dynamic range in AM	BW = ±3 kHz	105	-	-	dB
FS_{IFADC}	Full scale input voltage	Differential	-	1.4	-	V_{rms}

3.4.6 Audio DAC

Table 28: Audio DAC

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{out}	Max. output voltage	Full scale	0.85	0.95	-	Vrms
BW	Bandwidth	3dB attenuation (programmable by FW)	-	19.5	-	kHz
R_{out}	Output resistance	-	150	180	210	Ω
O_{noise}	Output noise	-	-	10	30	µVrms
D	Distortion	-6 dBFS	-	0.03	0.05	%

3.4.7 Digital I/O interface pins

Table 29: Digital I/O interface pins

Symbol	Parameter	Test condition	Min	Typ	Max	Units
-	High level output voltage	I_{out} = 1 mA	2.9	3.2	-	V
-	Low level output voltage	I_{out} = -1 mA	-	0.1	0.3	V
-	Input voltage range	-	0	-	V_{CC} + 0.15	V
-	High level input voltage	-	2.0	-	-	V
-	Low level input voltage	-	-	-	0.8	V
T	Cycle period	-	15.258	-	-	ns
t_R	Rise time	15 pF load (high-speed)	-	-	4.5	ns
t_f	Fall time	15 pF load (high-speed)	-	-	4.5	ns
T_{delay}	Delay time (half cycle)	15 pF load	0	-	3	ns

Figure 37: CMOS base-band timing diagram in half-cycle mode

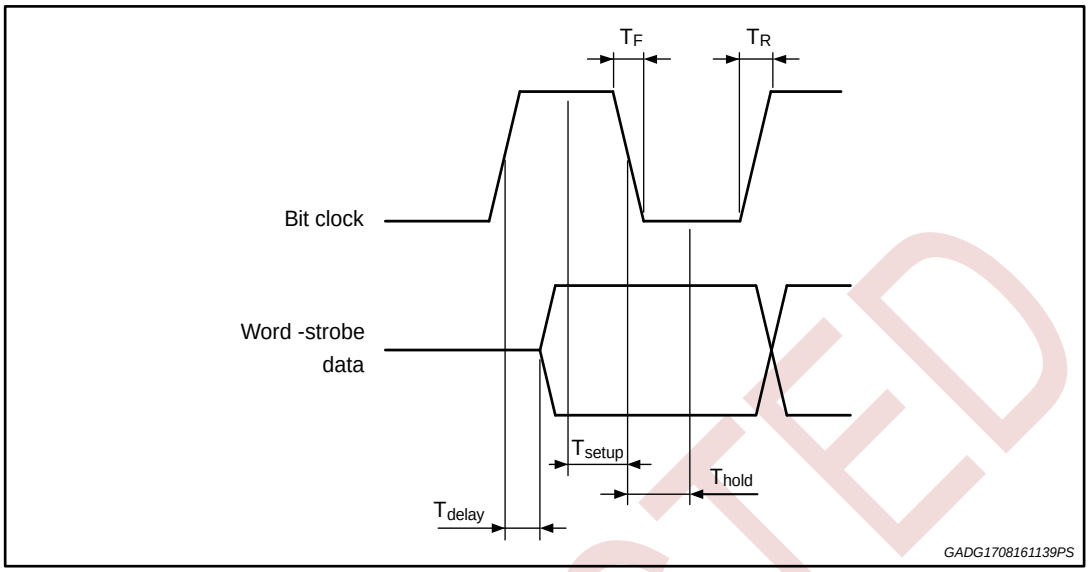


Table 30: LVDS-I²S base-band transmitter characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{OH}	High level output voltage	R_{load} = 100 Ω	-	-	1475	mV
V_{OL}	Low level output voltage	R_{load} = 100 Ω	925	-	-	mV
$\|V_{OD}\|$	Output differential voltage	R_{load} = 100 Ω	250	-	400	mV
V_{OS}	Output offset voltage	R_{load} = 100 Ω	1250	-	1275	mV
$R_{O,diff}$	Output impedance	Differential	75	100	125	Ω
T	Cycle period		15.258	-	-	ns
t_R	Rise time	20% - 80%; supporting up to three LVDS RX load (1)	-	-	2	ns
t_f	Fall time	20% - 80%; supporting up to three LVDS RX load(1)	-	-	2	ns
$T_{delay,HC}$	Delay time (half cycle)	15 pF load	1	-	3.7	ns
$T_{delay,FC}$	Delay time (full cycle)	15 pF load	1	-	10	ns
T_{setup}	Full cycle	No load, for slave tuner interface	3.8	-	-	ns
T_{hold}	Full cycle	No load, for slave tuner interface	0.2	-	-	ns

Notes:

(1)In case of multiple LVDS RX the termination resistor of each LVDS RX is 100 Ω but it depends on the number of parallel LVDS RX.

Figure 38: LVDS-transmitter pin characteristics

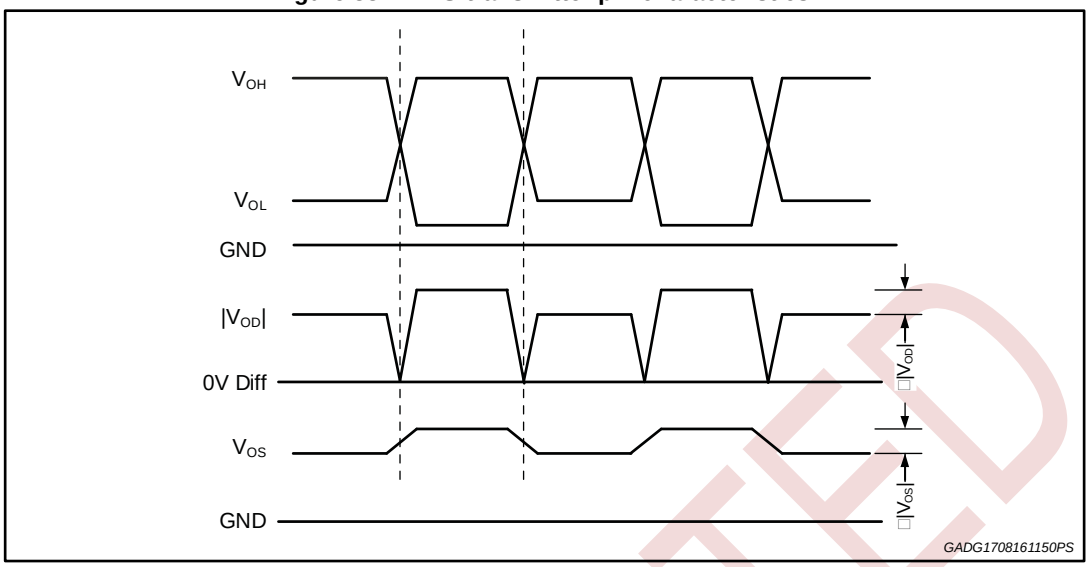


Figure 39: LVDS-I²S base-band pin timing diagram for half-cycle mode

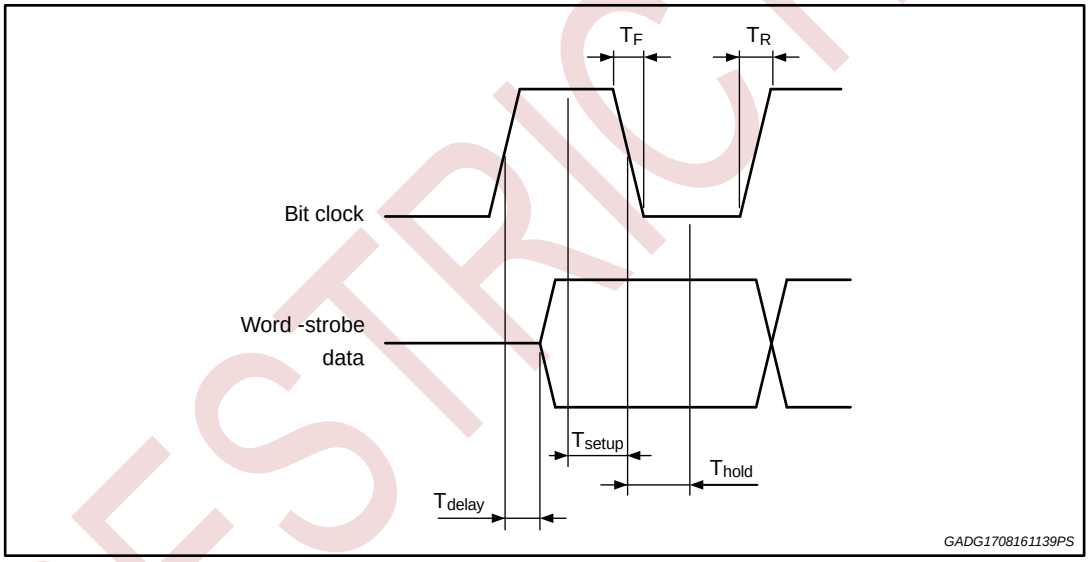


Figure 40: LVDS-I²S base-band pin timing diagram for full-cycle mode

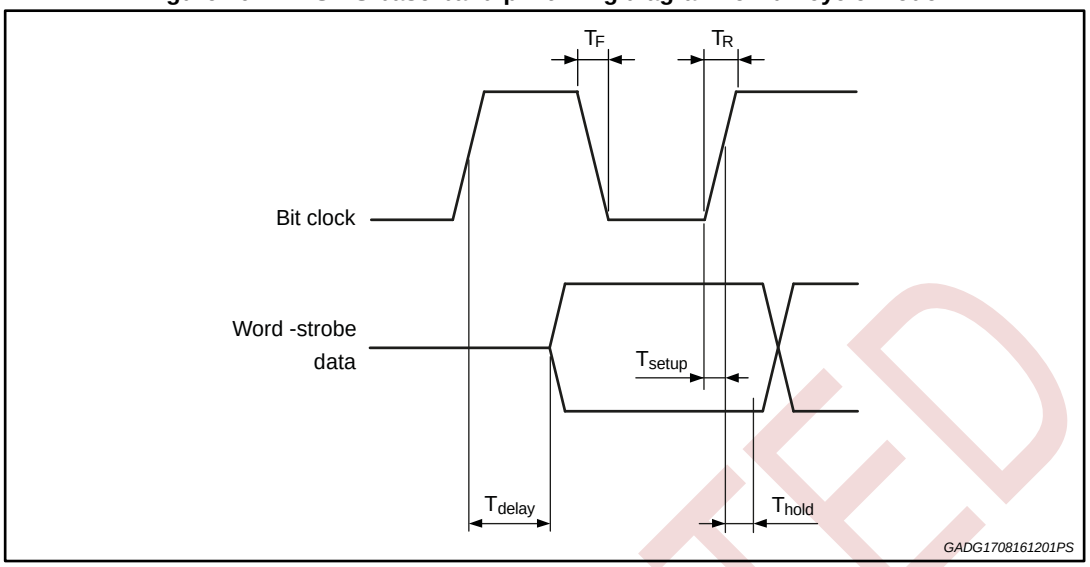


Table 31: LVDS-I²S base-band receiver characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CM}	Common mode input voltage	-	0.4	-	2.4	V
$\|V_{IDTH}\|$	Input differential voltage	-	-100	-	100	mV
$R_{IN,diff}$	Receiver differential input impedance	-	75	-	125	Ω
C_{IN}	Input capacitance	-	-	-	5	pF

Table 32: JESD204B base-band transmitter characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{OH}	High level output voltage	R_{load} = 100 Ω	-	-	1475	mV
V_{OL}	Low level output voltage	R_{load} = 100 Ω	925	-	-	mV
$\|V_{OD}\|$	Output differential voltage	R_{load} = 100 Ω	250	-	400	mV
V_{OS}	Output offset voltage	R_{load} = 100 Ω	1250	-	1275	mV
$R_{O,diff}$	Output impedance	Differential	75	100	125	Ω
-	Maximum operating frequency	-	-	-	400	MHz
DC	Duty cycle	-	40	-	-	%
t_R	Rise time	20% - 80%	-	-	1.5	ns
t_f	Fall time	20% - 80%	-	-	1.5	ns

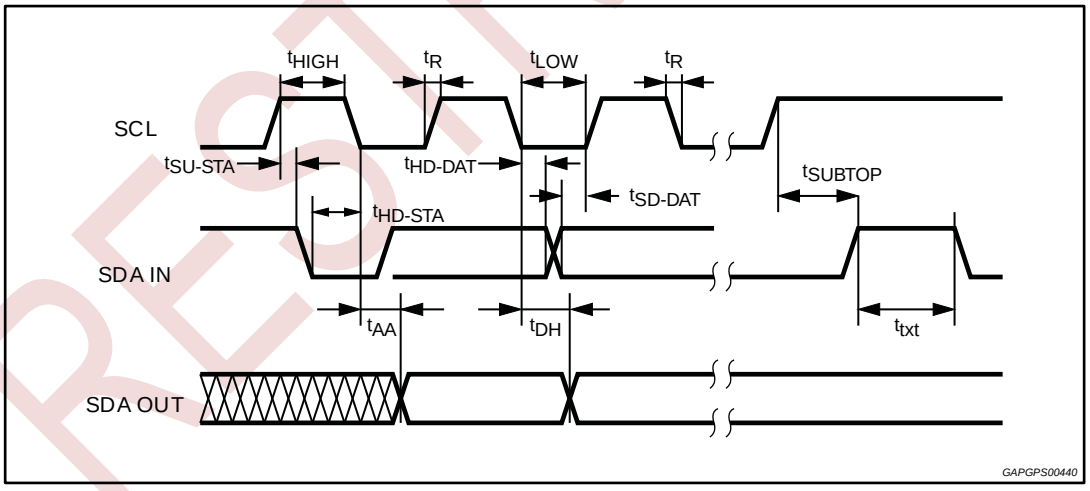
3.4.8 I²C interface

The following parameters apply to the serial bus communication when I²C protocol has been selected at start-up. The parameters of the following table are defined as in *Figure 41: "I2C bus timing diagram"*.

Table 33: I²C interface

Symbol	Parameter	Test condition	Min	Typ	Max	Units
f_{SCL}	SCL Clock frequency	-	-	100	500	kHz
t_{AA}	SCL low to SDA data valid	-	-	300	-	ns
t_{buf}	Time the bus must be kept free before a new transmission	-	-	4.7	-	µs
t_{HD-STA}	START condition hold time	-	4.0	-	-	µs
t_{LOW}	Clock low period	-	4.7	-	-	µs
t_{HIGH}	Clock high period	-	4.0	-	-	µs
t_{SU-SDA}	START condition setup time	-	4.7	-	-	µs
t_{HD-DAT}	Data input hold time	-	0	-	-	µs
t_{SU-DAT}	Data input setup time	-	250	-	-	ns
t_R	SDA & SCL rise time	-	-	-	1000	ns
t_F	SDA & SCL full time	-	-	-	300	ns
$t_{SU-STOP}$	Stop condition setup time	-	4.0	-	-	µs
t_{DH}	Data out time	-	-	300	-	ns

Figure 41: I2C bus timing diagram



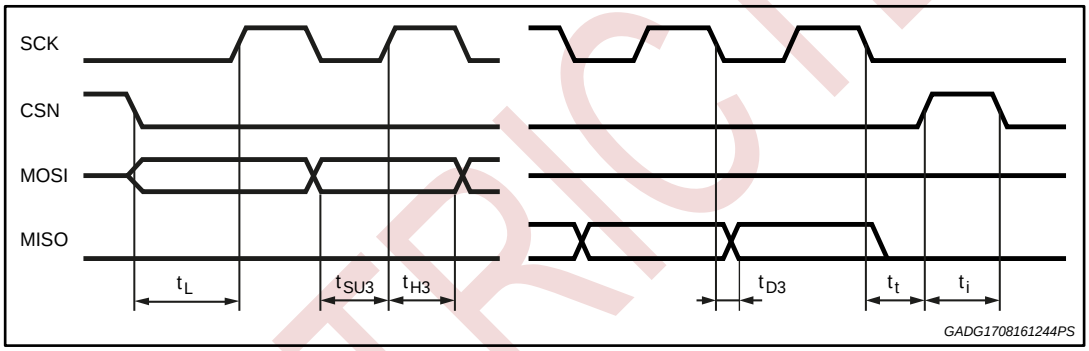
3.4.9 SPI interface

The following parameters apply to the serial bus communication when SPI protocol has been selected at start-up. The parameters of the following table are defined as in *Figure 42: "SPI interface timing"*

Table 34: SPI interface timing

Symbol	Parameter	Test condition	Min	Typ	Max	Units
f_{SCK}	Maximum Clock Frequency	-	-	-	4	MHz
t_L	CSN lead time	Trailing CSN to leading SCK	25	-	-	ns
t_t	CSN trail time	Trailing SCK to leading CSN	25	-	-	ns
t_i	CSN idle time	Leading CSN to trailing CSN	250	-	-	ns
t_{SU3}	MOSI to SCK setup time	-	25	-	-	ns
t_{H3}	MOSI to SCK hold time	-	25	-	-	ns
t_{D3}	SCK to MISO hold time	-	-	-	25	ns

Figure 42: SPI interface timing

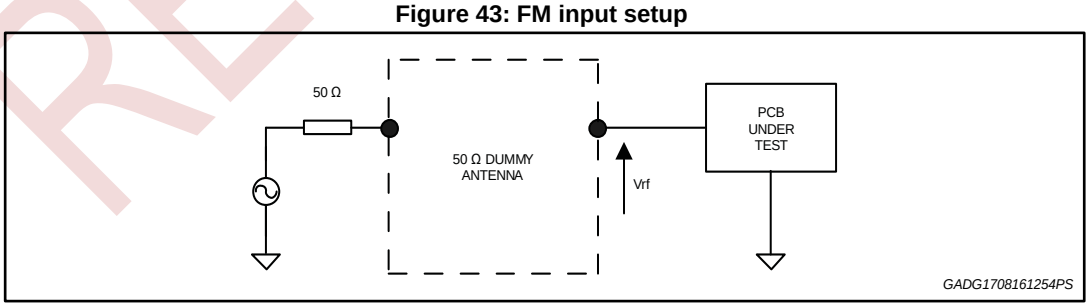


3.5 Overall system performance

3.5.1 FM system performance

Antenna level equivalence: 0 dBµV = 1 µVrms (nominal antenna terminal voltage with 50 Ω dummy load).

Figure 43: FM input setup



Input level referred to 50 Ω antenna dummy output. F_{rf} = 98.1 MHz, V_{rf} = 60 dBµV, mono modulation, f_{dev} = 40 kHz, f_{audio} = 1 kHz audio. De-emphasis = 50 µs, unless otherwise specified.

Table 35: FM system performance

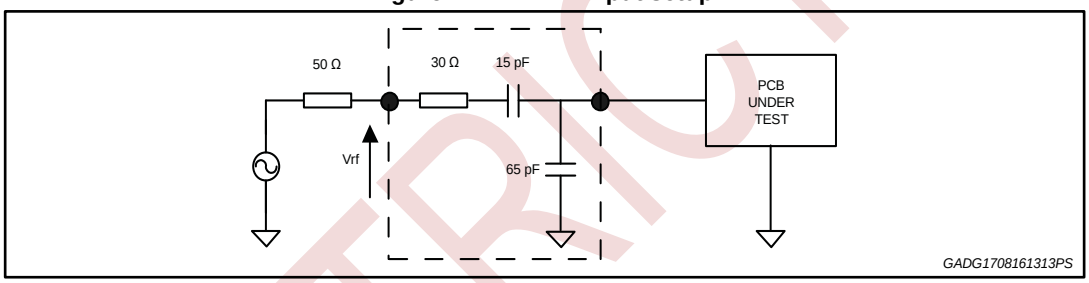
Parameter	Test condition	Min	Typ	Max	Units
Tuning range FM Eu	can be modified by the user	87.5	-	108	MHz
Tuning step FM Eu	can be modified by the user	-	100	-	kHz
Tuning range FM US	can be modified by the user	87.5	-	107.9	MHz
Tuning step FM US	can be modified by the user	-	200	-	kHz
Tuning range FM Jp	can be modified by the user	76	-	90	MHz
Tuning step FM Jp	can be modified by the user	-	100	-	kHz
Tuning range FM Eeu	can be modified by the user	65	-	74	MHz
Tuning step FM Eeu	can be modified by the user	-	100	-	kHz
Sensitivity	S/N = 26 dB	-	-12	-8	dBµV
S/N	V_{rf} = 10 dBµV	63	66	-	dB
Ultimate S/N	V_{rf} = 60 dBµV, mono	84	87	-	dB
	V_{rf} = 60 dBµV, Dev = 75 kHz, mono	90	93	-	dB
	V_{rf} = 60 dBµV, Dev = 68.25 kHz, Pilot = 6.75kHz, Stereo	74	79	-	dB
Distortion	Deviation = 75 kHz	-	0.01	0.05	%
Max deviation	THD = 3%, V_{rf} = 60 dBµV	150	165	-	kHz
Adjacent channel Selectivity |ΔF| = 100 kHz (D/U ratio)	SINAD = 26 dB Desired: V_{rf} = 40 dBµV, Dev = 22.5 kHz, f_{mod} = 400 Hz Undesired: Dev = 22.5 kHz, f_{mod}=1 kHz	58	65	-	dB
Alternate Channel Selectivity |ΔF| = 200 kHz (D/U ratio)	SINAD = 26 dB Desired: V_{rf} = 40 dBµV, dev = 40 kHz, f_{mod} = 400 Hz Undesired: Dev = 40 kHz, f_{mod} = 1 kHz	60	70	-	dB
Two Signal Selectivity |ΔF| =1 MHz (D/U ratio)	SINAD = 26 dB Desired: V_{rf} = 20 dBµV; dev = 40 kHz, f_{mod} = 400 Hz Undesired:: f_{mod} = 1 kHz, Dev = 40 kHz	78	85	-	dB
Two Signal Selectivity |ΔF| =10MHz (D/U ratio)	SINAD = 26 dB Desired: V_{rf} = 20 dBµV, dev = 40 kHz, f_{mod} = 400 Hz Undesired: f_{mod} = 1 kHz, Dev = 40 kHz	81	88	-	dB

Parameter	Test condition	Min	Typ	Max	Units
Three signal performance	SINAD = 26 dB Desired: V_{rf} = 20 dBµV, dev = 40 kHz, f_{mod} = 400 Hz, Undesired1: ±400 kHz, dev = 40 kHz, f_{mod} = 1 kHz Undesired2: ±800 kHz, unmodulated	89	94	-	dBµV
	SINAD = 26 dB Desired: V_{rf} = 20 dBµV, dev = 40 kHz, f_{mod} = 400 Hz, Undesired1: ±4MHz, dev = 40 kHz, f_{mod} = 1 kHz Undesired2: ±8MHz, un-modulated	91	96	-	dBµV

3.5.2 AM MW system performance

Antenna level equivalence: 0 dBµV = 1 μV_{rms}

Figure 44: AM MW input setup



Level referred to SG output before antenna dummy; dummy antenna load as shown above

F_{rf} = 999 kHz (1000 kHz for US), V_{rf} = 74 dBµV, mod = 30%, f_{audio} = 400 Hz, unless otherwise specified.

Table 36: AM MW system performance

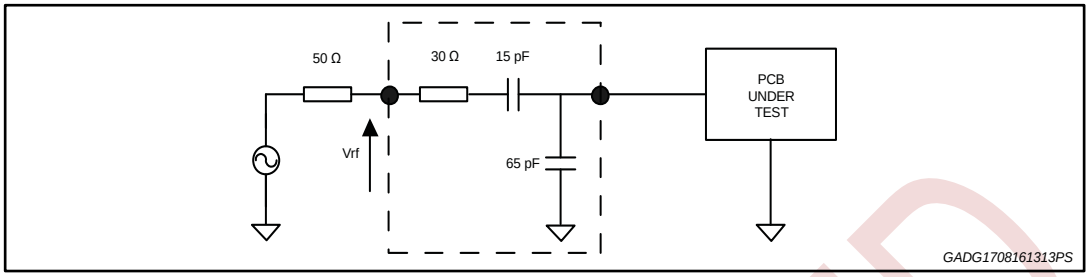
Parameter	Test condition	Min	Typ	Max	Units
Tuning range MW EU/JP	can be modified by the user	531	-	1629	kHz
Tuning step MW EU/JP	can be modified by the user	-	9	-	kHz
Tuning range MW US	can be modified by the user	530	-	1710	kHz
Tuning step MW US	can be modified by the user	-	10	-	kHz
Sensitivity	S/N = 20 dB	-	19	22	dBµV
	S/N = 20 dB (DNR = OFF)	-	25	28	dBµV
Ultimate S/N	V_{rf} = 80 dBµV	76	81	-	dB
Distortion	Mod = 80%	-	0.1	0.3	%
Adjacent channel Selectivity |ΔF| = 9 kHz	SINAD = 26 dB, Desired = 40 dBµV, m = 30%, 400 Hz Undesired: m = 30%, 1 kHz	56	66	-	dB

Parameter	Test condition	Min	Typ	Max	Units
Alternate Channel Selectivity |ΔF| =18kHz	SINAD = 26 dB, Desired = 40 dBµV, m = 30%, 400 Hz Undesired: m = 30%, 1 kHz	56	66	-	dB
Strong signal interferer SNR	|ΔF| = 40 kHz Desired: V_{rf} = 40 dBµV Undesired: V_{rf} = 110 dBµV, m = 30%, f_{mod} = 1 kHz	18	22	-	dB
	|ΔF| = 400 kHz Desired: V_{rf} = 40 dBµV Undesired: V_{rf} = 110 dBµV, m = 30%, f_{mod} = 1 kHz	17	21	-	dB
Strong signal interferer suppression	|ΔF| = 40 kHz Desired: V_{rf} = 40 dBµV Undesired: V_{rf} = 110 dBµV, m = 30%, f_{mod} = 1 kHz	-	0.1	5.0	dB
	|ΔF| = 400kHz Desired: V_{rf} = 40 dBµV Undesired: V_{rf} = 110 dBµV, m = 30%, f_{mod} = 1 kHz	-	0.1	5.0	dB
Strong signal interferer cross-modulation	|ΔF| = 40 kHz Desired: V_{rf} = 80 dBµV Undesired: V_{rf} = 110 dBµV, m=30%, f_{mod} = 1 kHz (noise increase by cross-mod)	-	2	5	dB
	|ΔF| = 400 kHz Desired: V_{rf} = 80 dBµV Undesired: V_{rf} = 110 dBµV, m = 30%, f_{mod} = 1 kHz (noise increase by cross-mod)	-	2	5	dB
Maximum signal handling	50 Ohm direct, THD < 3%	125	-	-	dBµV
Image rejection	-	100	-	-	dB

3.5.3 AM LW system performance

Antenna level equivalence: 0 dBµV = 1µV$_{rms}$

Figure 45: AM LW input setup



Level referred to SG EMF output before antenna dummy; dummy antenna load as shown above f_{rf} = 216 kHz, V_{rf} = 74 dBµV, mod = 30%, f_{audio} = 400 Hz, unless otherwise specified.

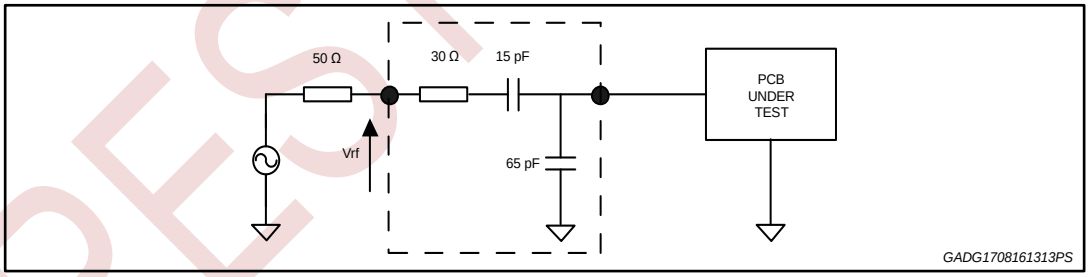
Table 37: AM-LW system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range LW	(can be modified by the user)	144	-	288	kHz
Tuning step LW	(can be modified by the user)	-	1	-	kHz
Sensitivity	S/N = 20dB	-	24	27	dBµV
Ultimate S/N	V_{rf} = 80 dBµV	73	78	-	dB
Distortion	m = 80%	-	0.1	0.3	%
Image rejection	-	-	80	-	dB

3.5.4 AM SW overall system performance

Antenna level equivalence: 0 dBµV = 1 µV$_{rms}$

Figure 46: AM SW input setup



Level referred to SG EMF output before antenna dummy; dummy antenna load as shown above f_{rf} = 6000 kHz, V_{rf} = 74 dBµV, mod = 30%, f_{audio} = 400 Hz, unless otherwise specified.

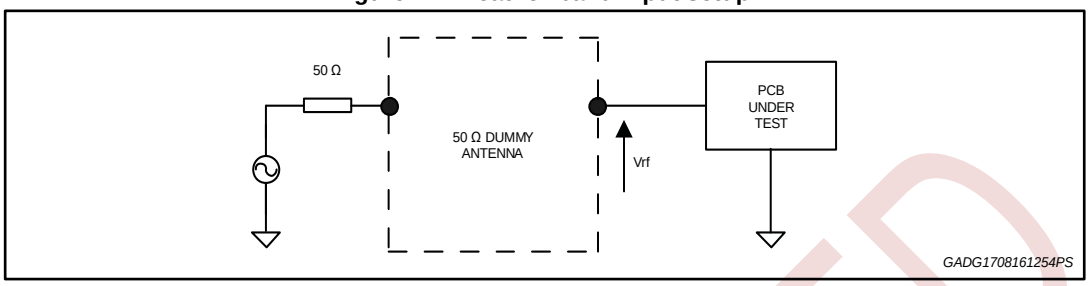
Table 38: AM-SW system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range SW	can be modified by the user	2300	-	30000	kHz
Tuning step SW	can be modified by the user	-	1	-	kHz
Sensitivity	S/N = 20 dB	-	17	20	dBµV
Ultimate S/N	V_{rf} = 80 dBµV	77	82	-	dB
Distortion	m = 80%	-	0.1	0.3	%
Image rejection	-	-	80	-	dB

3.5.5 WX system performance

Antenna level equivalence: 0 dBµV = 1µVrms (Antenna terminal voltage with 50 Ohm dummy load).

Figure 47: Weather-band input setup



Input level referred to 50 Ohm dummy antenna output; antenna dummy as shown above.

F_{rf} = 162.475 MHz, V_{rf} = 60 dBµV, mono modulation, f_{dev} = 2 kHz, f_{audio} = 400 Hz audio.

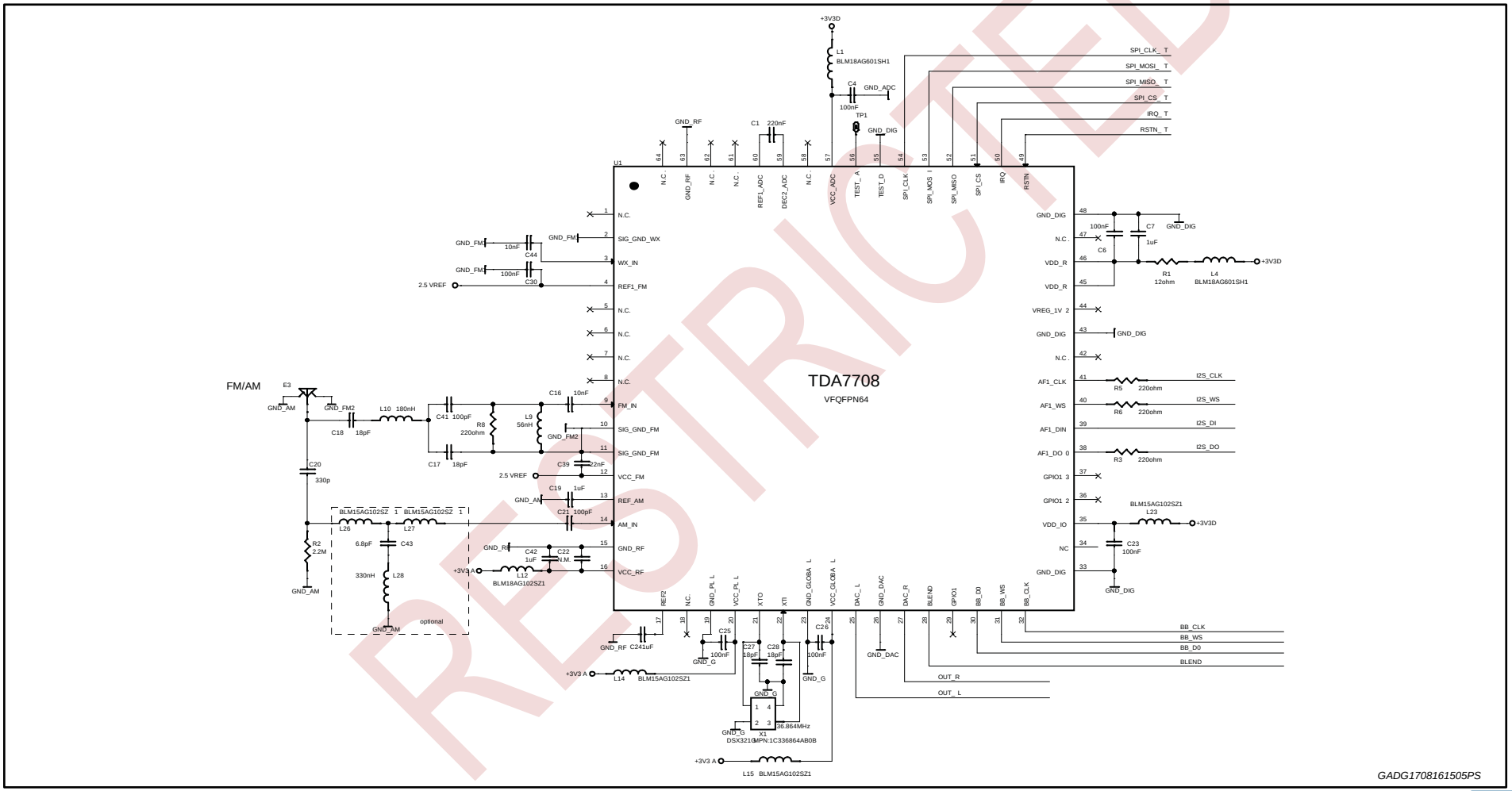
De-emphasis = 75 µs.

Table 39: WX system performance

Parameter	Test condition	Min	Typ	Max	Units
Sensitivity	S/N = 26 dB	-8	-11	-	dBµV
Ultimate S/N	V_{rf} = 60 dBµV	77	82	-	dB
Distortion	Deviation = 4.5 kHz	-	0.1	0.3	%
Max deviation	THD = 3%	5	-	-	kHz
Adjacent channel Selectivity	ΔF = 25 kHz, SINAD = 30 dB Desired: 40 dBµV, dev = 2.0 kHz, 400 Hz Undesired: Dev = 2.0 kHz, 1 kHz	60	-	-	dB
Alternate Channel Selectivity	ΔF = 50kHz, SINAD = 30 dB Desired: 40 dBµV, dev = 2.0 kHz, 400 Hz Undesired: Dev = 2.0 kHz, 1 kHz	60	-	-	dB

4 Application schematic

Figure 48: AM/FM application example



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

5.1 VFQFPN-64 (9x9x1.0mm) package information

Figure 49: VFQFPN-64 (9x9x1.0 mm) package outline

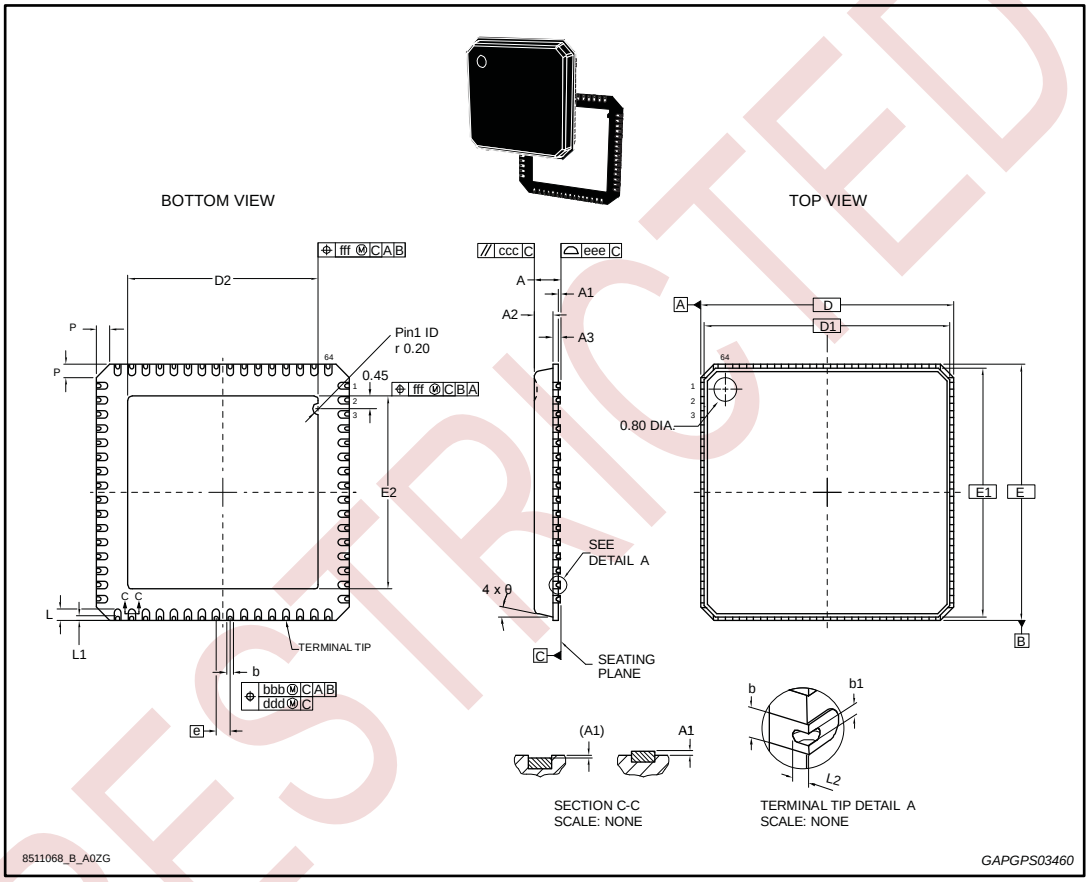


Table 40: VFQFPN-64 (9x9x1.0 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	-	-	14	-	-	0.5511
A	-	-	1.0	-	-	0.0394
A1	0.00	-	0.05	0.0000	-	0.0020
A2	0.55	-	0.80	0.0217	-	0.0314
A3	0.20 REF			0.0079 REF		
b (2)	0.18	0.25	0.30	0.0070	0.0098	0.0118
b1	-	0.15	-	-	0.0059	-

Ref	Dimensions					
	Millimeters			Inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
D		9.00 BSC			0.3543 BSC	
D1 (3)		8.75 BSC			0.3444 BSC	
D2	-	6.70	-	-	0.2638	-
e		0.50 BSC			0.0197 BSC	
E		9.00 BSC			0.3543 BSC	
E1(3)		8.75 BSC			0.3444 BSC	
E2	-	6.70	-	-	0.2638	-
L	0.30	-	0.50	0.0118	-	0.0197
L1		0.15 REF			0.0059 REF	
L2	-	0.10	-	-	0.0039	-
P	-	-	0.60	-	-	0.0236
Tolerance of form and position						
aaa		0.15			0.0059	
bbb		0.10			0.0039	
ccc		0.10			0.0039	
ddd		0.05			0.0019	
eee		0.08			0.0031	
fff		0.10			0.0039	

Notes:

(1)Values in mm are converted into inches and rounded to 4 decimal digits.

(2)Maximum allowable burr is 0.076 mm in all directions.

(3)D1 and E1 are Maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm (0.0098 inch)" per side.

The package is compliant to IPC/JEDEC J-STD-020D June 2007 standard Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices, MSL Level 3.

6 Revision history

Table 41: Document revision history

Date	Revision	Changes
26-Aug-2016	1	Initial release.
22-Sep-2016	2	Removed row Pin 42 in *Table 17: "Power-supply pin description"*. Removed the word Pin 42 in *Figure 34: "Start-up sequence"*.
03-Nov-2016	3	Updated: *Table 2: "Pins description"* *Figure 10: "SAI_BB waveform for data: I(16 bit)+ Q(16 bit) transmitted on a single data line, in DCOP (STA680D)-based HD-Radio™"* *Table 17: "Power-supply pin description"* *Figure 48: "AM/FM application example"*
08-Mar_2017	4	Updated: *Figure 7: "I2S single-port configuration"* Max. value of V_{cc} parameter in *Table 20: "Absolute maximum ratings"*
19-Apr-2017	5	Updated: *Section 2.14.2: "SPI bus protocol description"* Overall Noise Figure in *Table 23: "FM - section"* Input voltage range max value in *Table 29: "Digital I/O interface pins"*;
10-May-2017	6	Added 'RDS demodulation' to *Section "Features"*. Updated: *Section 2.9.4: "Base-band I2S AM/FM/DRM interface"* *Table 7: "SAI_BB timing values (normal mode: I(16 bit)+ Q(16 bit) on a single data line) for DCOP-based HD-Radio™ "*
15-Dec-2017	7	Added TDA7708CB order code and updated description in cover page. Updated: *Table 13: "Audio I2S interface timing in reception mode"* *Table 14: "Audio I2S interface timing in transmission mode"* *Table 20: "Absolute maximum ratings"* *Table 23: "FM - section"* *Table 24: "AM - section"*

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