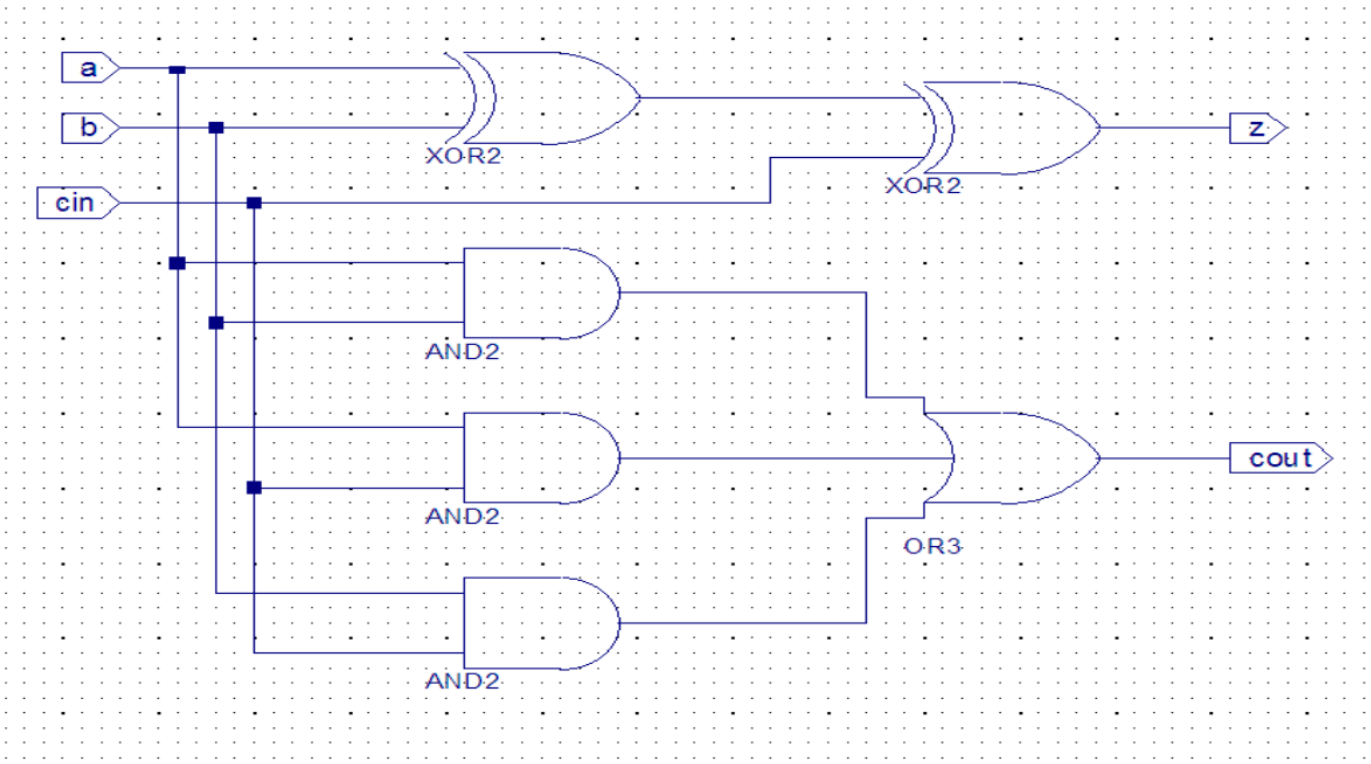

Figure 1: 1-bit full adder

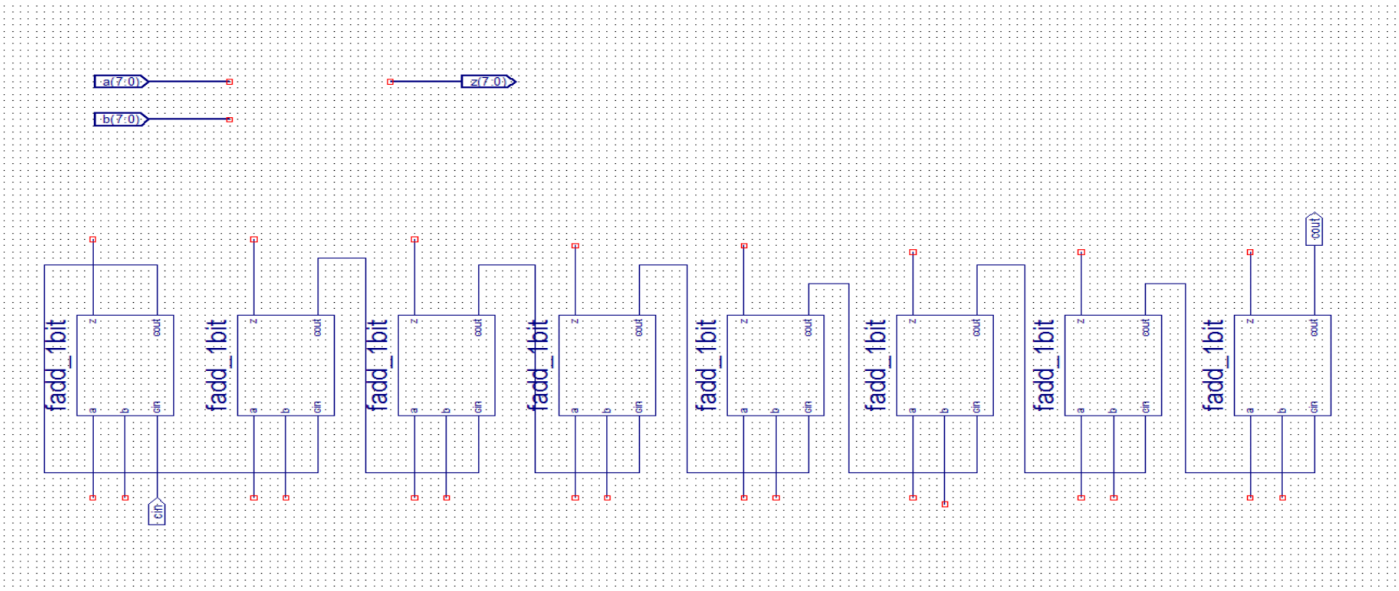

Figure 2: 8-bit full adder

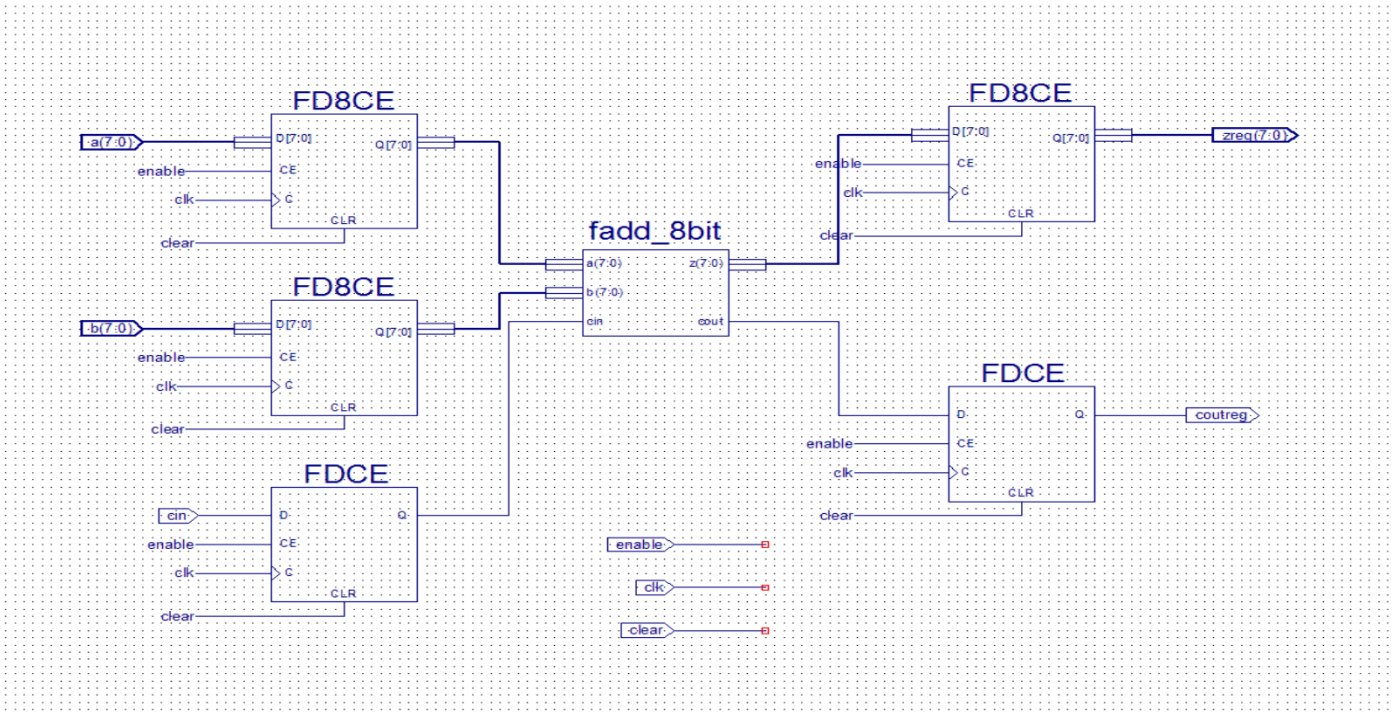

Figure 3: 8-bit full adder with DFFs

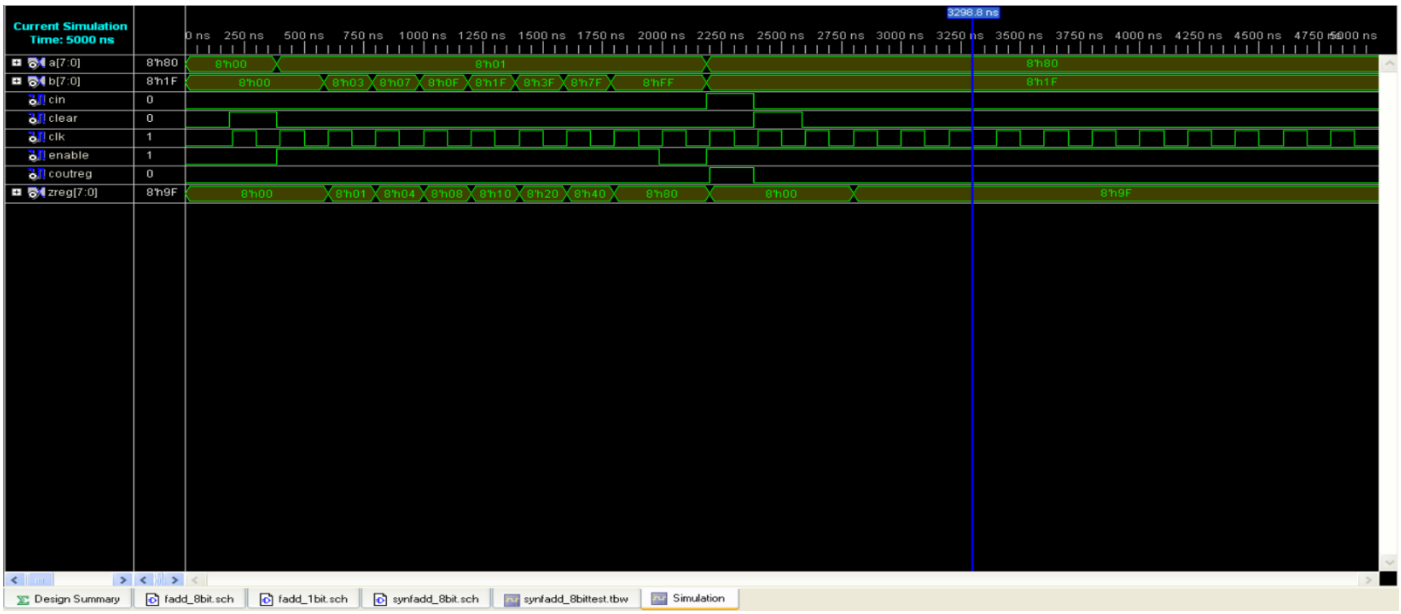

Figure 4: waveform of 8-bit full adder with DFFs

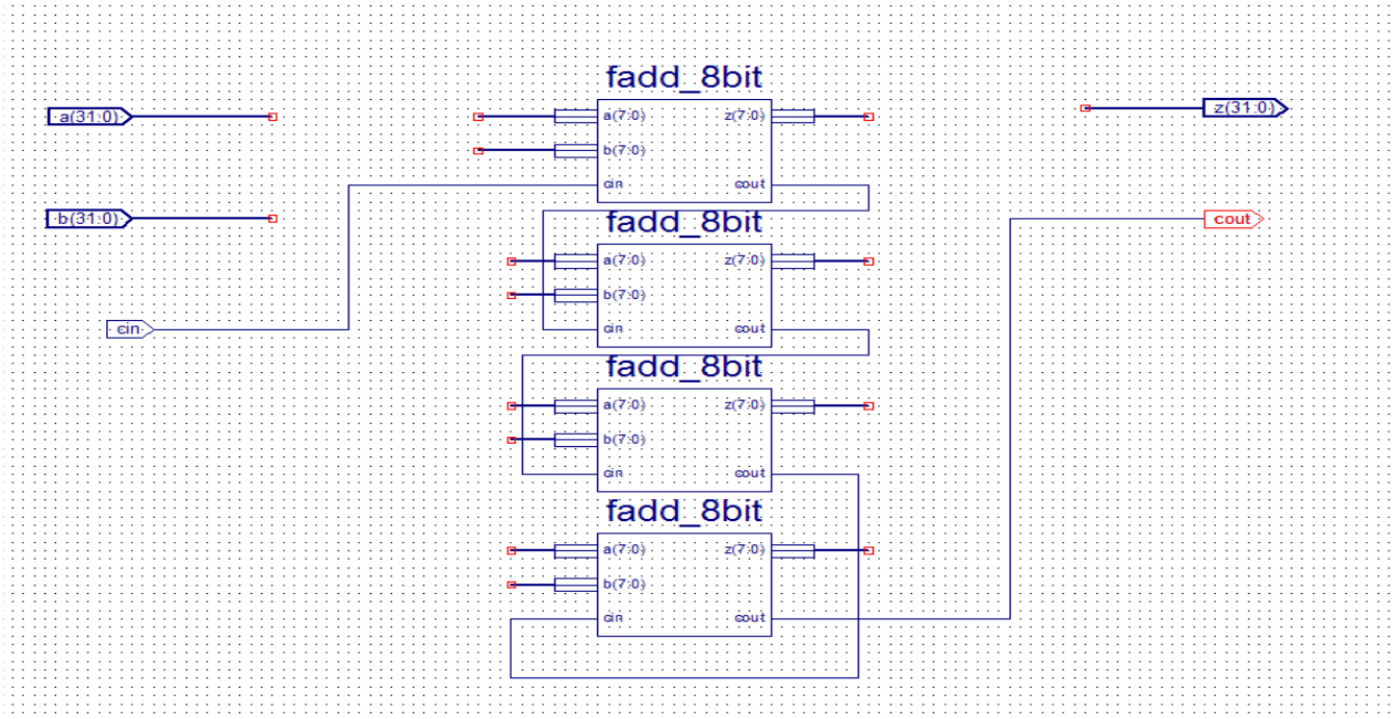

Figure 5: 32-bit full adder

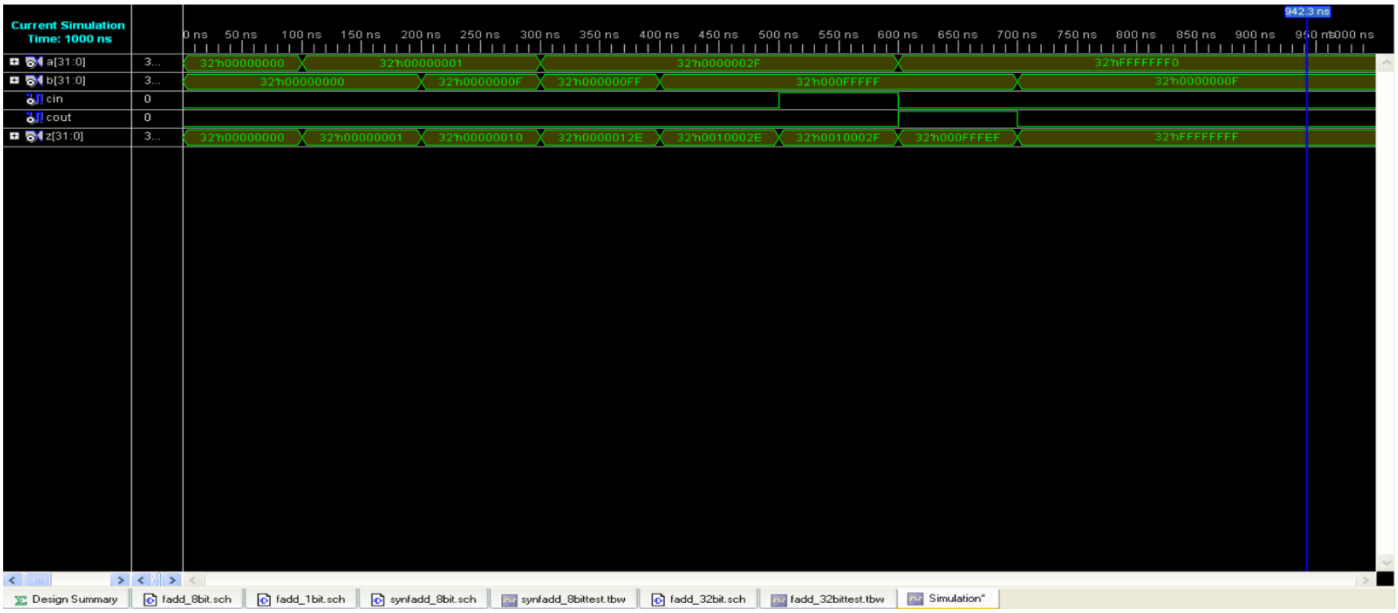

Figure 6: waveform of 32-bit full adder

32-bit ALU (schematic):

Functions:

1. 32-bit adder, when opr(2:0) == 000;
2. 32-bit subtractor, when opr(2:0) == 001;
3. 32-bit logical shifter, shiftdir == 0 is left shift, shiftdir == 1 is right shift, every time shifts 1 bit, opr(2:0) == 010;
4. 32-bit and, opr(2:0) == 011;
5. 32-bit or, when opr(2:0) == 1XX;

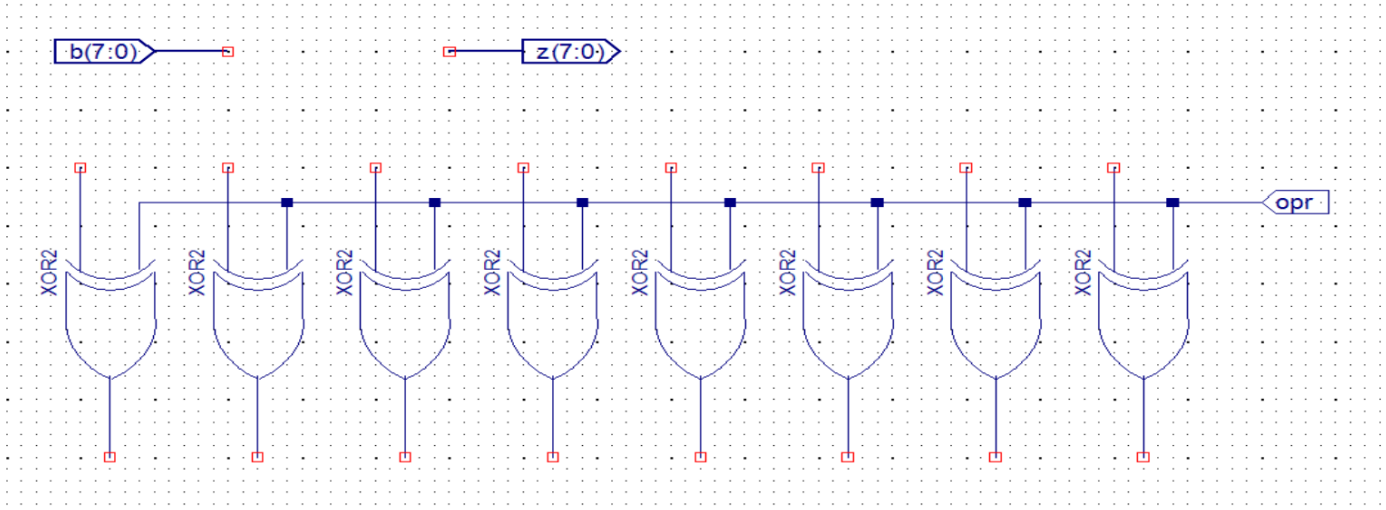

Figure 7: 8-bit xor

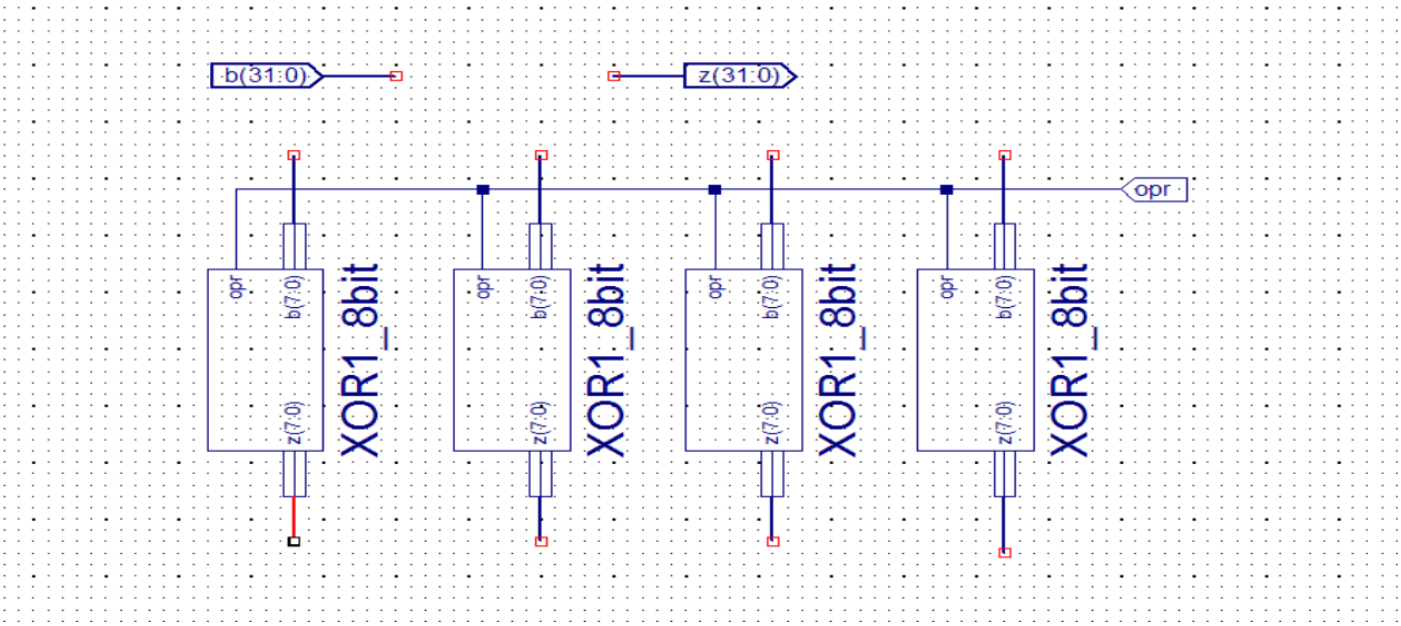

Figure 8: 32-bit xor

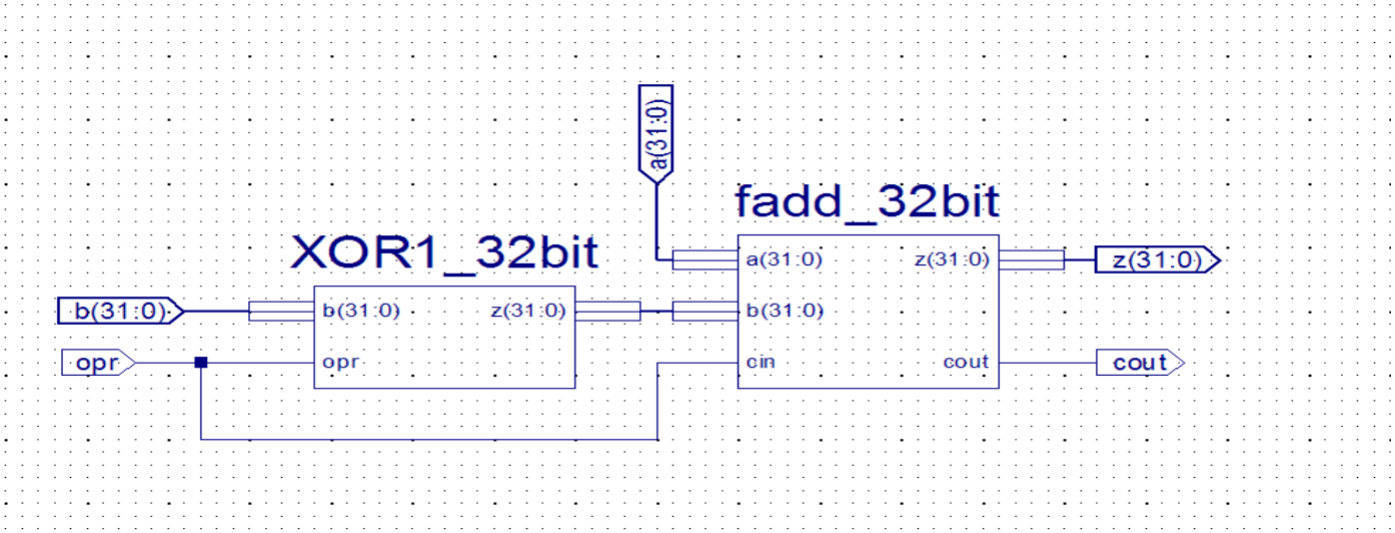

Figure 9: 32-bit subtractor

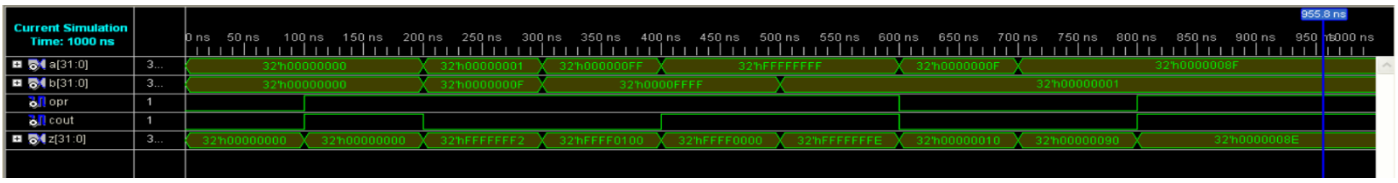

Figure 10: waveform of 32-bit subtractor

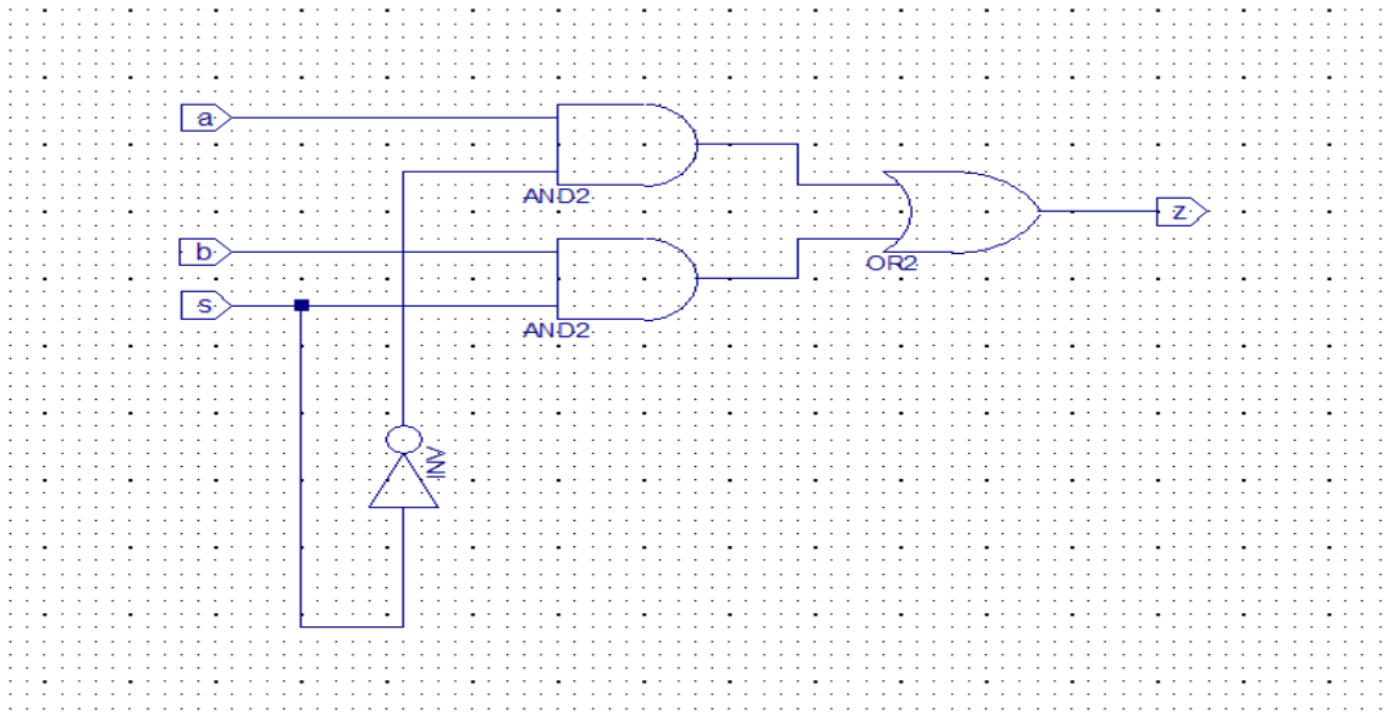

Figure 11: 1-bit 2-to-1 mux

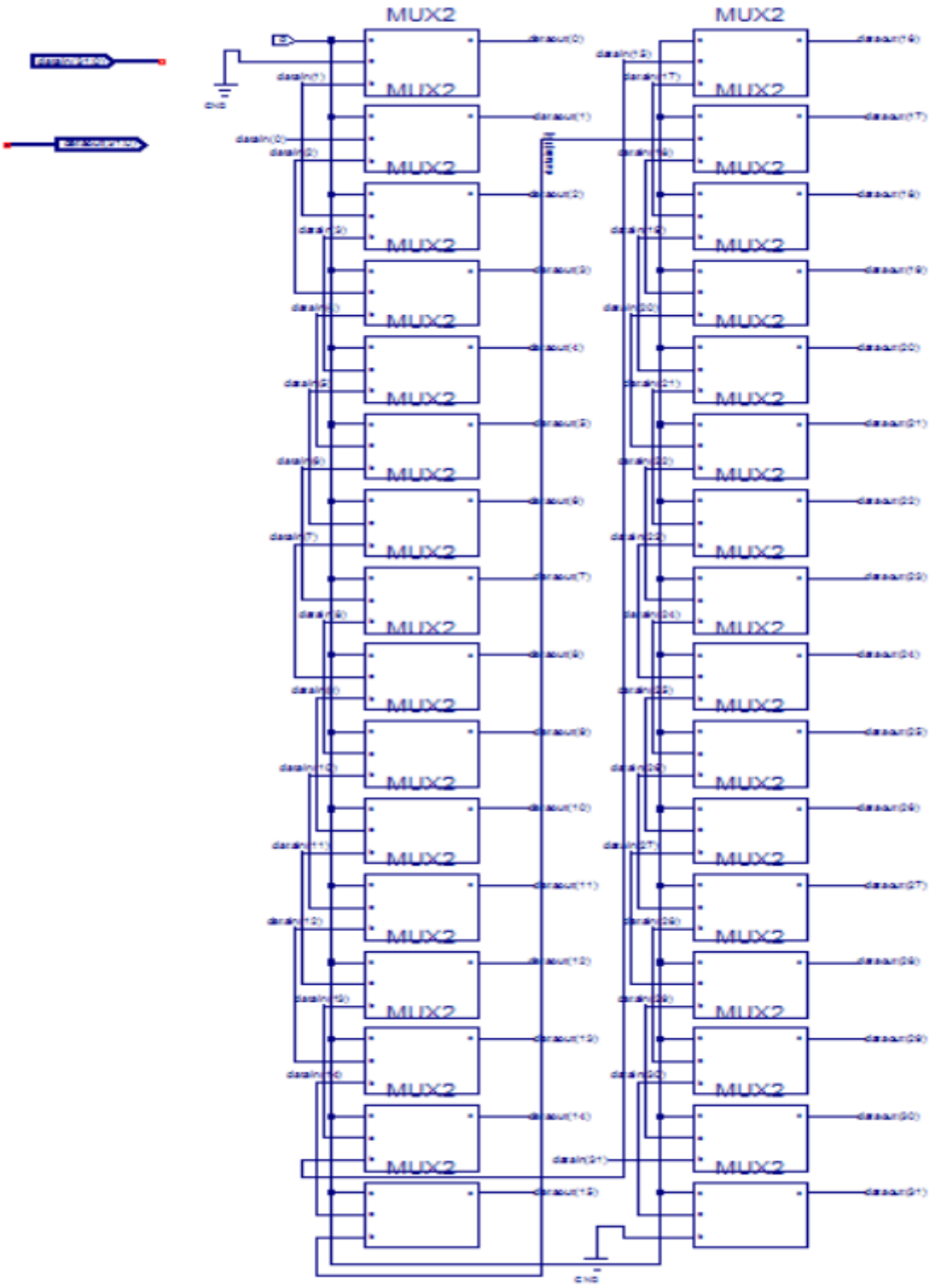

Figure 12: 32-bit logical shifter

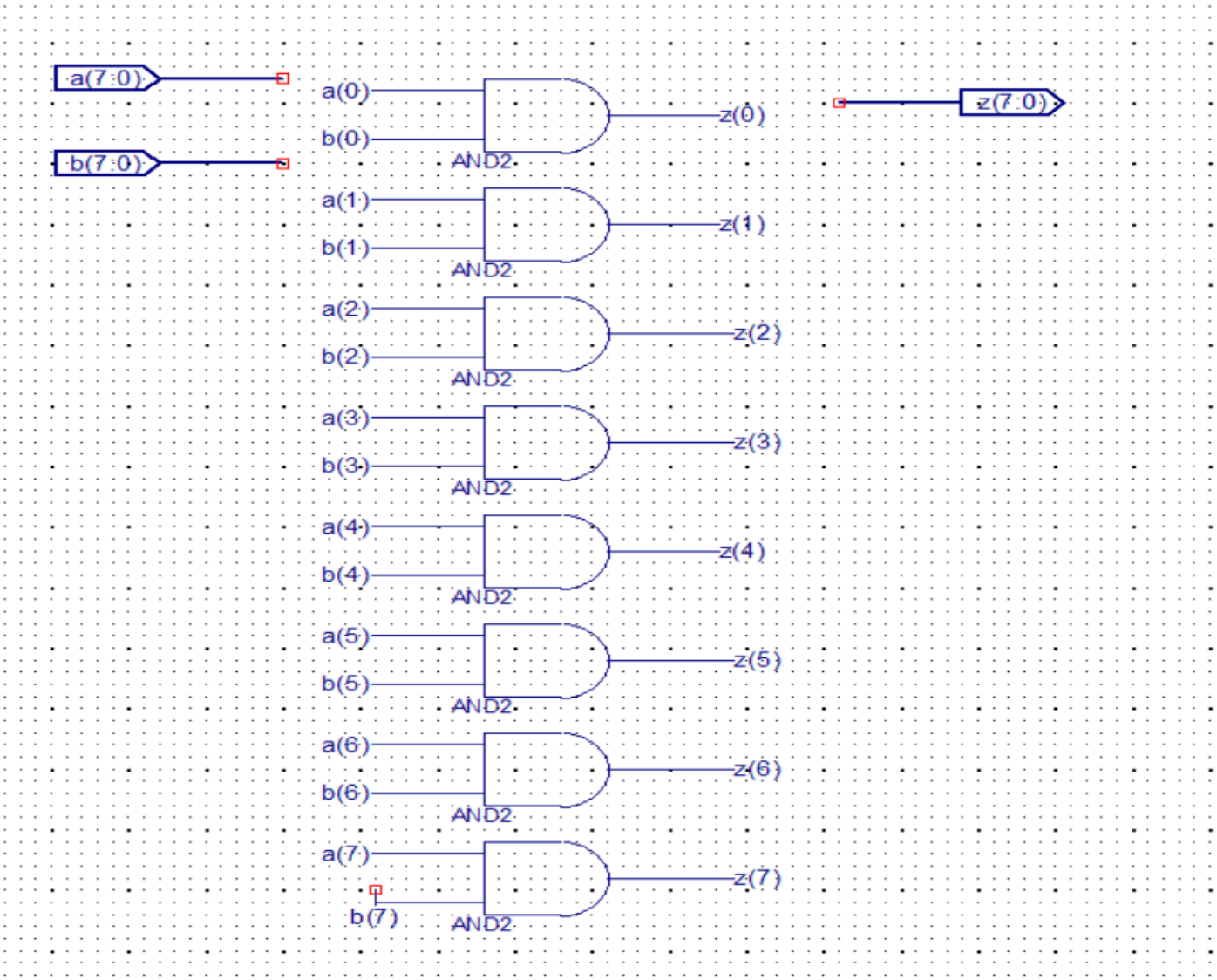

Figure 13: 8-bit and

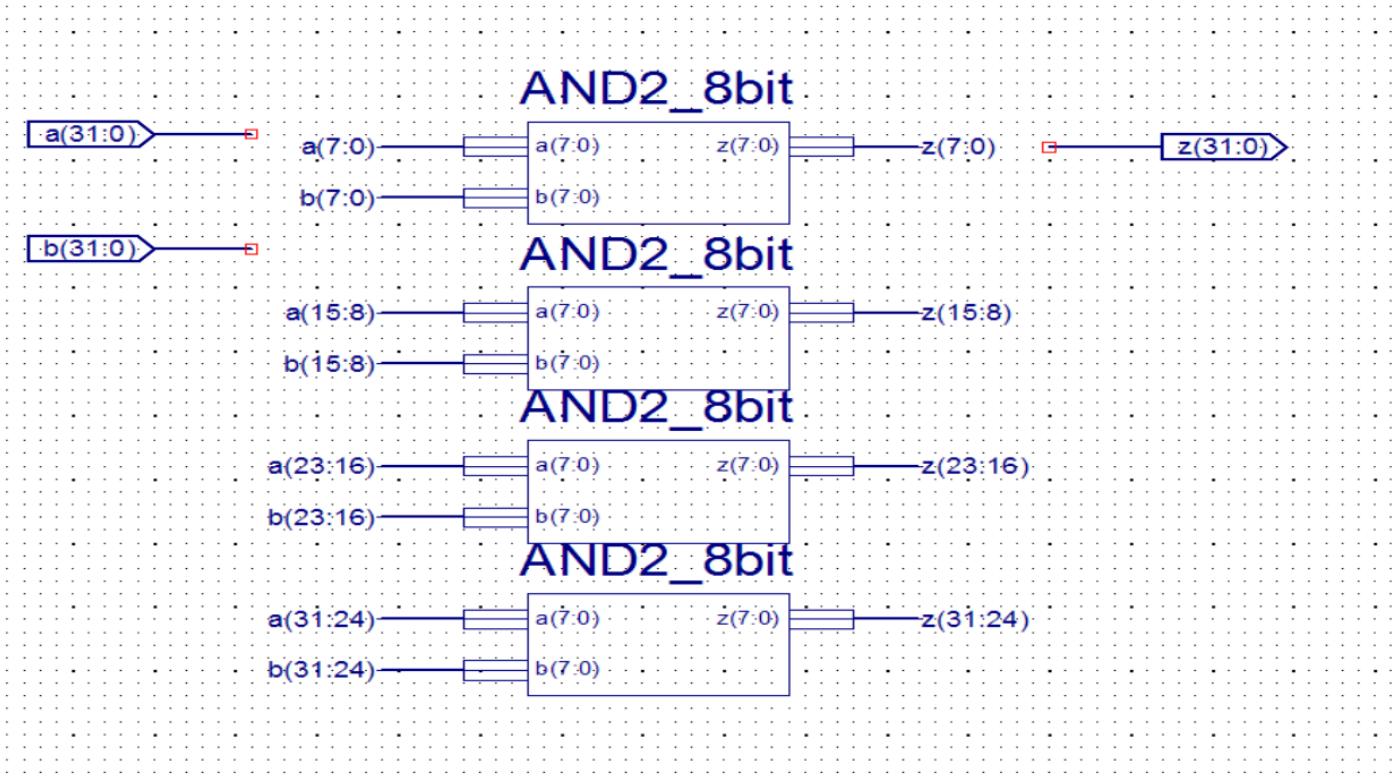

Figure 14: 32-bit and

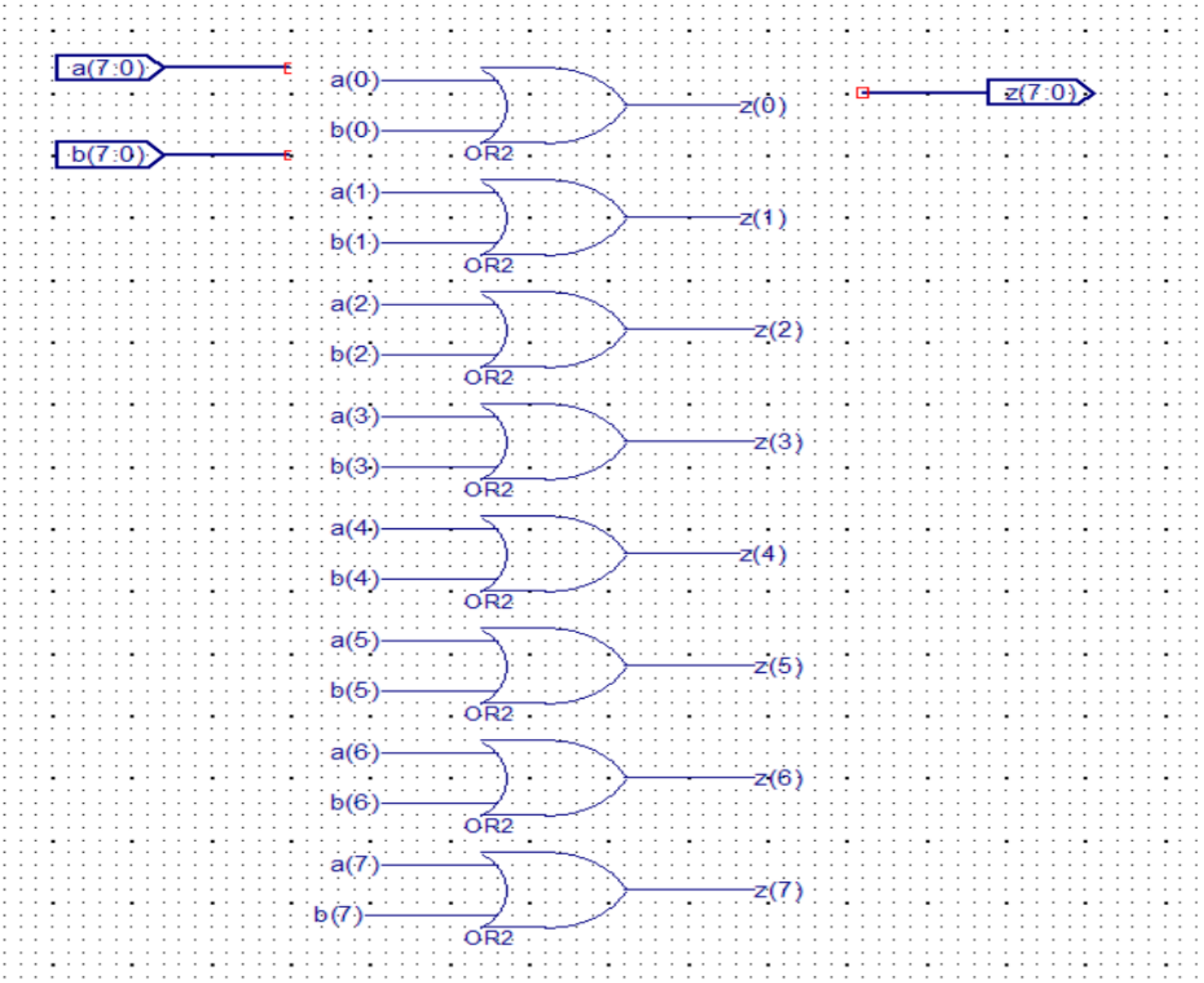

Figure 15: 8-bit or

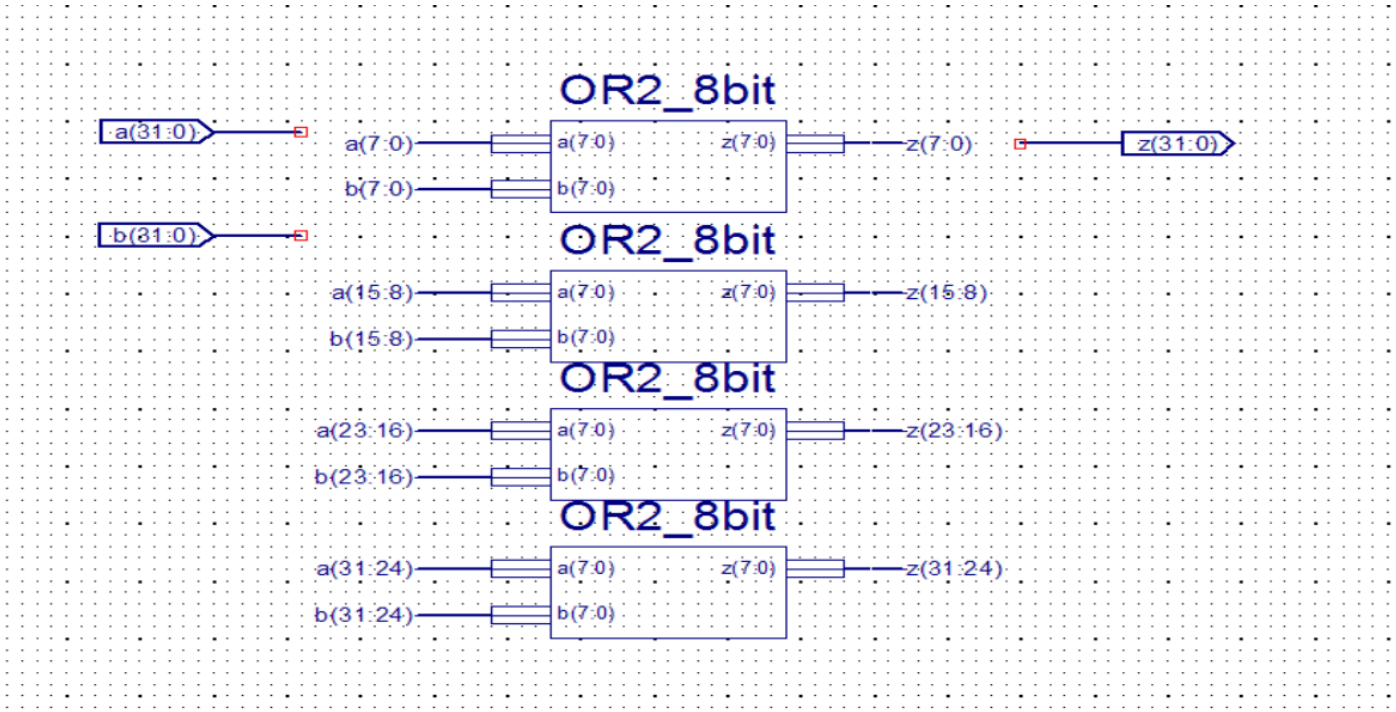

Figure 16: 32-bit or

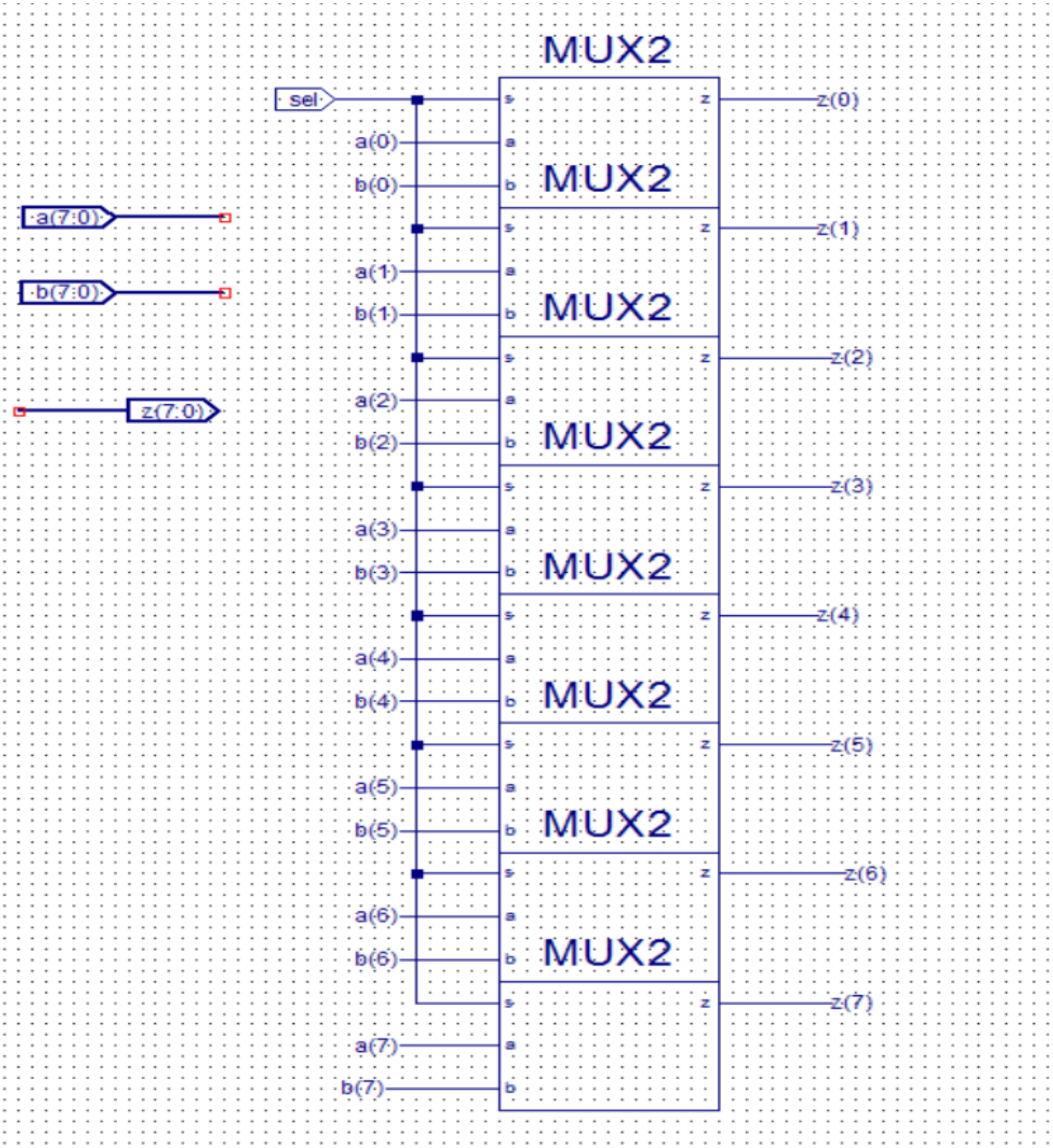

Figure 16: 8-bit 2-to-1 mux

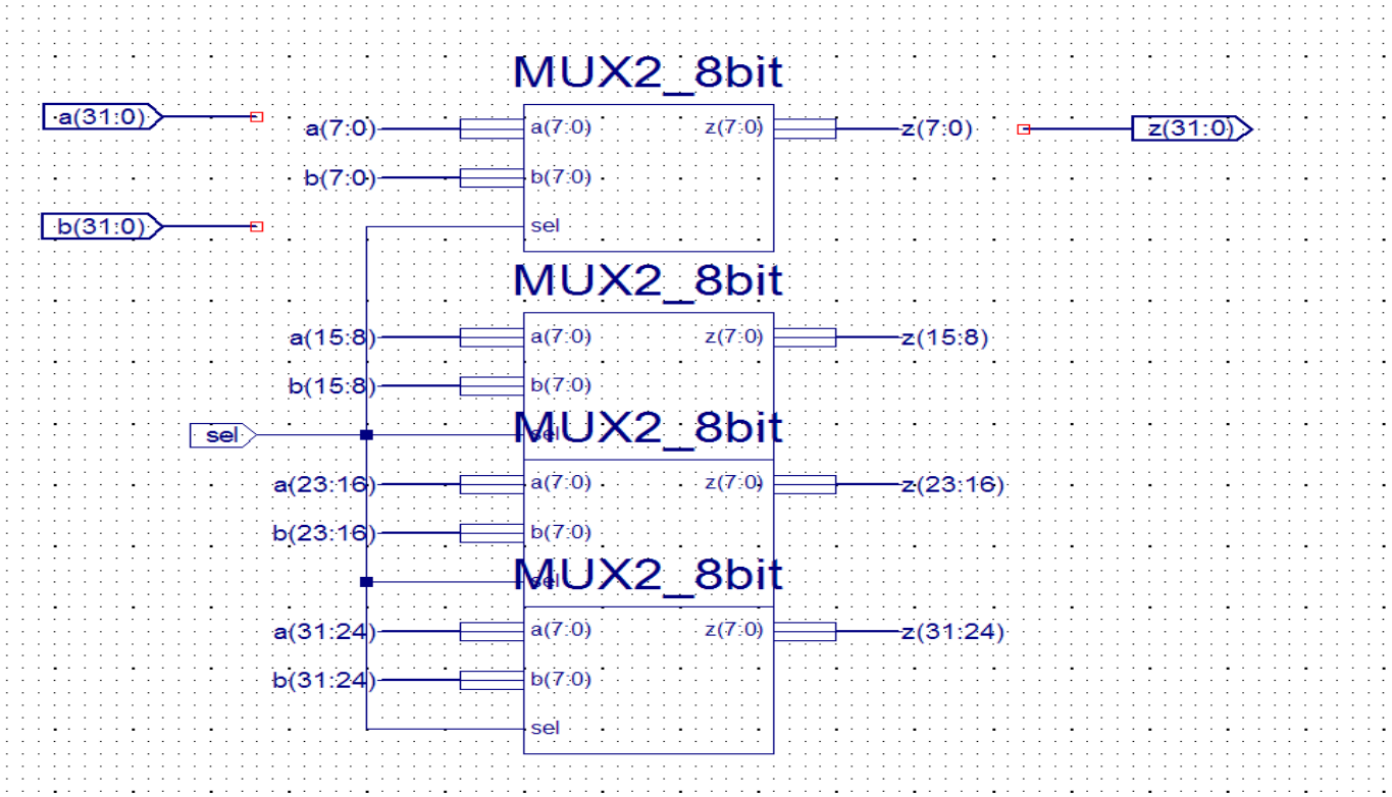

Figure 17: 32-bit 2-to-1 mux

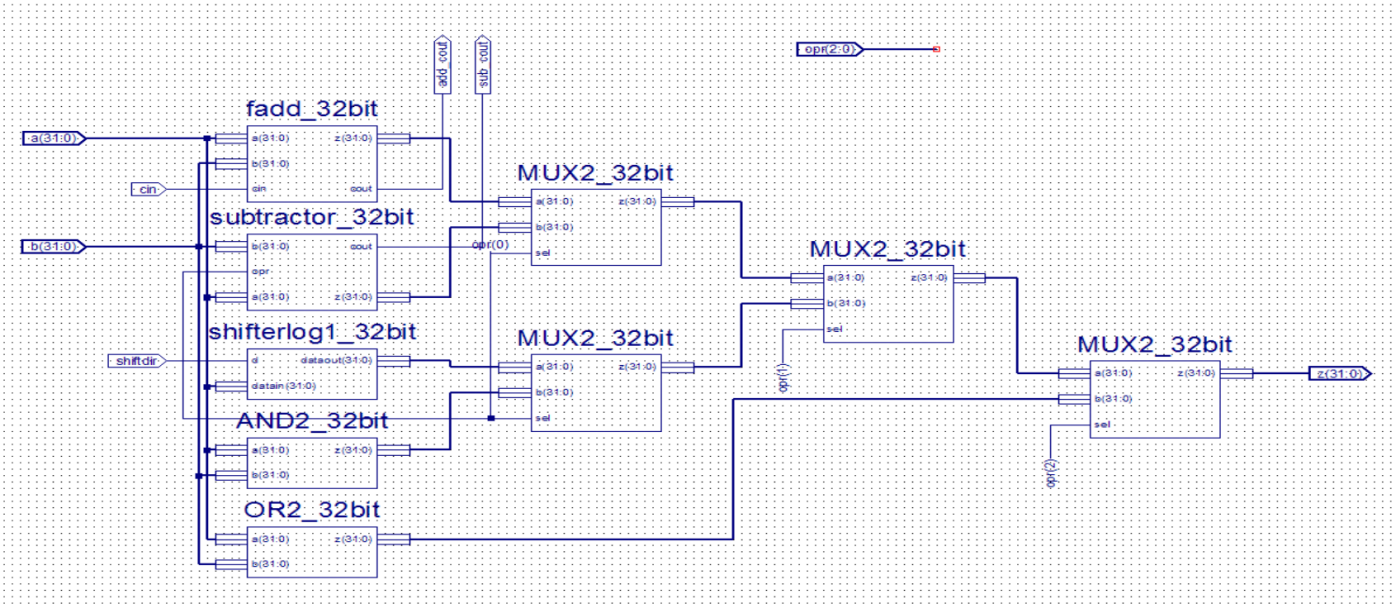

Figure 18: 32-bit ALU

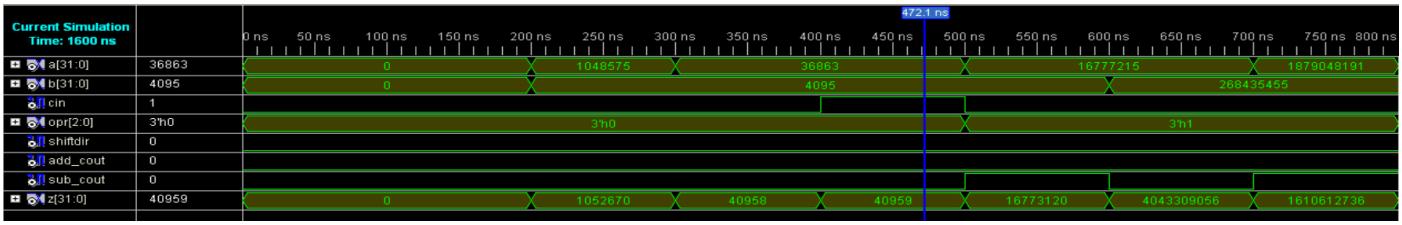

Figure 19: waveform of 32-bit ALU (1)

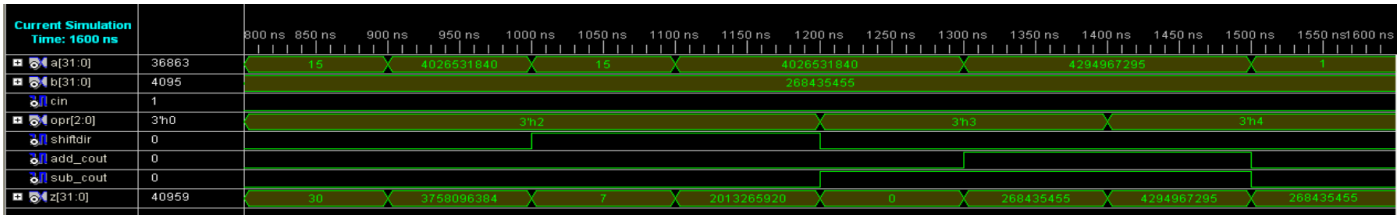

Figure 20: waveform of 32-bit ALU (2)

```
Release 10.1 Map K.31 (nt)
Xilinx Mapping Report File for Design 'ALUsch_32bit'

Design Information
------------------
Command Line   : map -ise C:/yzhou477/yzhou477.ise -intstyle ise -p
xa2s300e-ft256-6 -cm area -pr off -k 4 -c 100 -tx off -o ALUsch_32bit_map.ncd
ALUsch_32bit.ngd ALUsch_32bit.pcf
Target Device  : xa2s300e
Target Package : ft256
Target Speed   : -6
Mapper Version : aspartan2e -- $Revision: 1.46 $
Mapped Date    : Sat Jan 25 20:24:16 2025

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Logic Utilization:
  Number of 4 input LUTs:           288 out of  6,144    4%
Logic Distribution:
    Number of occupied Slices:                        145 out of  3,072    4%
    Number of Slices containing only related logic:   145 out of    145  100%
    Number of Slices containing unrelated logic:        0 out of    145    0%
       *See NOTES below for an explanation of the effects of unrelated logic
Total Number of 4 input LUTs:       288 out of  6,144    4%
   Number of bonded IOBs:           103 out of    178   57%

Peak Memory Usage:  136 MB
Total REAL time to MAP completion:  6 secs
Total CPU time to MAP completion:   5 secs

NOTES:

   Related logic is defined as being logic that shares connectivity - e.g. two
   LUTs are "related" if they share common inputs.  When assembling slices,
   Map gives priority to combine logic that is related.  Doing so results in
   the best timing performance.

   Unrelated logic shares no connectivity.  Map will only begin packing
   unrelated logic into a slice once 99% of the slices are occupied through
   related logic packing.

   Note that once logic distribution reaches the 99% level through related
   logic packing, this does not mean the device is completely utilized.
   Unrelated logic packing will then begin, continuing until all usable LUTs
   and FFs are occupied.  Depending on your timing budget, increased levels of
   unrelated logic packing may adversely affect the overall timing performance
   of your design.

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Section 1 - Errors
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Section 3 - Informational
Section 4 - Removed Logic Summary
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Figure 21: map report of 32-bit ALU

32-bit ALU Verilog:

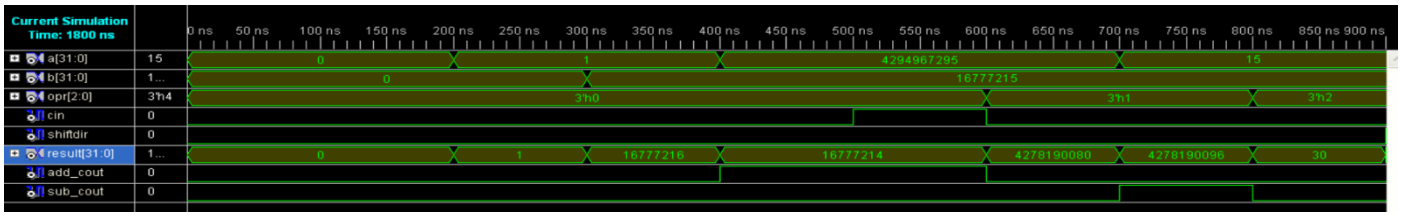

Figure 22: waveform of 32-bit ALU verilog (1)

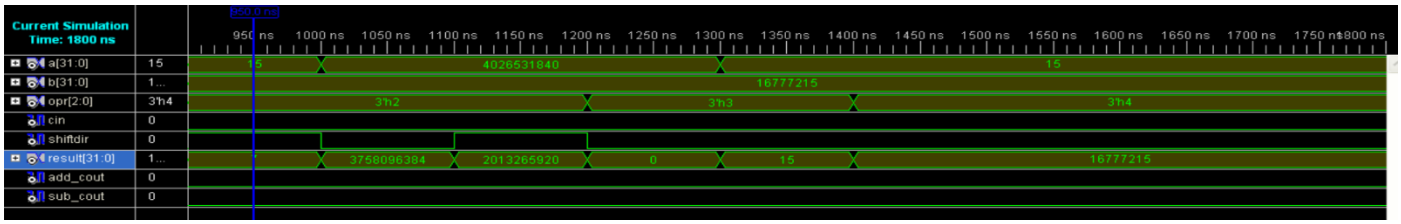

Figure 23: waveform of 32-bit ALU verilog (2)

```
Design Information
------------------
Command Line   : map -ise C:/yzhou477/yzhou477.ise -intstyle ise -p
xa2s300e-ft256-6 -cm area -pr off -k 4 -c 100 -tx off -o ALUv_32bit_map.ncd
ALUv_32bit.ngd ALUv_32bit.pcf
Target Device  : xa2s300e
Target Package : ft256
Target Speed   : -6
Mapper Version : aspartan2e -- $Revision: 1.46 $
Mapped Date    : Sat Jan 25 20:53:03 2025

Design Summary
--------------
Number of errors:      0
Number of warnings:    1
Logic Utilization:
  Number of 4 input LUTs:           194 out of  6,144    3%
Logic Distribution:
    Number of occupied Slices:                          99 out of  3,072    3%
    Number of Slices containing only related logic:     99 out of     99  100%
    Number of Slices containing unrelated logic:         0 out of     99    0%
        *See NOTES below for an explanation of the effects of unrelated logic
Total Number of 4 input LUTs:       194 out of  6,144    3%
   Number of bonded IOBs:           102 out of    178   57%

Peak Memory Usage:  135 MB
Total REAL time to MAP completion:  8 secs
Total CPU time to MAP completion:   6 secs

NOTES:

   Related logic is defined as being logic that shares connectivity - e.g. two
   LUTs are "related" if they share common inputs.  When assembling slices,
   Map gives priority to combine logic that is related.  Doing so results in
   the best timing performance.

   Unrelated logic shares no connectivity.  Map will only begin packing
   unrelated logic into a slice once 99% of the slices are occupied through
   related logic packing.

   Note that once logic distribution reaches the 99% level through related
   logic packing, this does not mean the device is completely utilized.
   Unrelated logic packing will then begin, continuing until all usable LUTs
   and FFs are occupied.  Depending on your timing budget, increased levels of
   unrelated logic packing may adversely affect the overall timing performance
   of your design.

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Section 5 - Removed Logic
Section 6 - IOB Properties
Section 7 - RPMs
Section 8 - Guide Report
```

Figure 24: map report of 32-bit ALU Verilog

Comment:

In my design, Verilog gates (194) are much less than schematic gates (288). This means there is some logical redundancy in my schematic design.