

DDR 内存

1、简介（概述）

DDR_SDRAM，即双倍速率同步动态随机存储器，人们习惯称为 DDR，是在 SDRAM 内存基础上发展而来的，相比普通 RAM 具有双倍的读取速率。在即时存储/读取数据时，可以使用板子上自带的 DDR 内存(1Gib, DDR2)，从而实现数据的快速存储和读取。

板子上的 DDR2 内存使用单一 rank + 16 位宽的数据通路，只需要一位片选信号，使用它时，可以调用 IP 核(MIG_7series)，也使用官方提供的 DDR-to-SRAM 模块，实现存储时 SRAM->DDR 的转化，和读取时 DDR->SRAM 的转化。

2、使用方法

步骤

（一）使用官方提供的 DDR-to-SRAM 模块：

- ① 导入附件中的 DDR-to-SRAM 模块：Ram2Ddr.vhd
- ② 导入调试好的 MIG_7series IP 核文件：mig_7series_0.xci
- ③ 为导入的 IP 核解压缩
- ④ 创建 200MHz 的时钟信号（使用 clk_wiz IP 核，比较简单，不提及）
- ⑤ 搞清楚 RAM 和 DDR 内存接口的含义
- ⑥ 在顶层模块中定义 DDR 内存接口信息：（下左图）
- ⑦ 定义 RAM2DDR 模块中 RAM 接口信息：（下右图）

<pre>// DDR2 Memory Signals ***** output [12:0] ddr2_addr, // Address * output [2:0] ddr2_ba, // Bank * output ddr2_ras_n, // Row En * output ddr2_cas_n, // Column En * output ddr2_we_n, // Write En * output ddr2_cke, // Clk En * output ddr2_ck_p, // Clk Posedge * output ddr2_ck_n, // Clk Negedge * output ddr2_cs_n, // Chip Select En * output [1:0] ddr2_dm, // High/Low Flag * output ddr2_odt, // On-Die Termination * inout [15:0] ddr2_dq, // Data * inout [1:0] ddr2_dqs_p, // Data Clk Posedge * inout [1:0] ddr2_dqs_n // Data Clk Negedge * //*****</pre>	<pre>// RAM Memory Signals ***** wire mem_ub; // RAM high bits * wire mem_lb; // RAM low bits * wire mem_cen; // RAM en * wire mem_oen; // RAM read en * wire mem_wen; // RAM write en * wire [2:0] mem_bank; // Bank * wire [26:0] mem_a; // Address * wire [15:0] mem_dq; // Data wire * wire [15:0] mem_dq_i; // Data in * wire [15:0] mem_dq_o; // Data out * //*****</pre>
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⑦ 创建 RAM2DDR 实例：（下图）

```
Ram2Ddr Ram(  
    .clk_200MHz_i(clk200),           // Clk 200MHz  
    .rst_i(rst),                     // Reset  
    .device_temp_i(chipTemp),        // Temp data  
  
    .ram_ub(mem_ub), .ram_lb(mem_lb),  
    .ram_a(mem_a), .ram_dq_i(mem_dq_i),  
    .ram_oen(mem_oen), .ram_wen(mem_wen),  
    .ram_dq_o(mem_dq_o), .ram_cen(mem_cen),  
  
    .ddr2_odt(dds2_odt), .ddr2_dq(dds2_dq),  
    .ddr2_addr(dds2_addr), .ddr2_ba(dds2_ba),  
    .ddr2_cs_n(dds2_cs_n), .ddr2_dm(dds2_dm),  
    .ddr2_ck_n(dds2_ck_n), .ddr2_cke(dds2_cke),  
    .ddr2_we_n(dds2_we_n), .ddr2_ck_p(dds2_ck_p),  
    .ddr2_ras_n(dds2_ras_n), .ddr2_cas_n(dds2_cas_n),  
    .ddr2_dqs_p(dds2_dqs_p), .ddr2_dqs_n(dds2_dqs_n)  
);
```

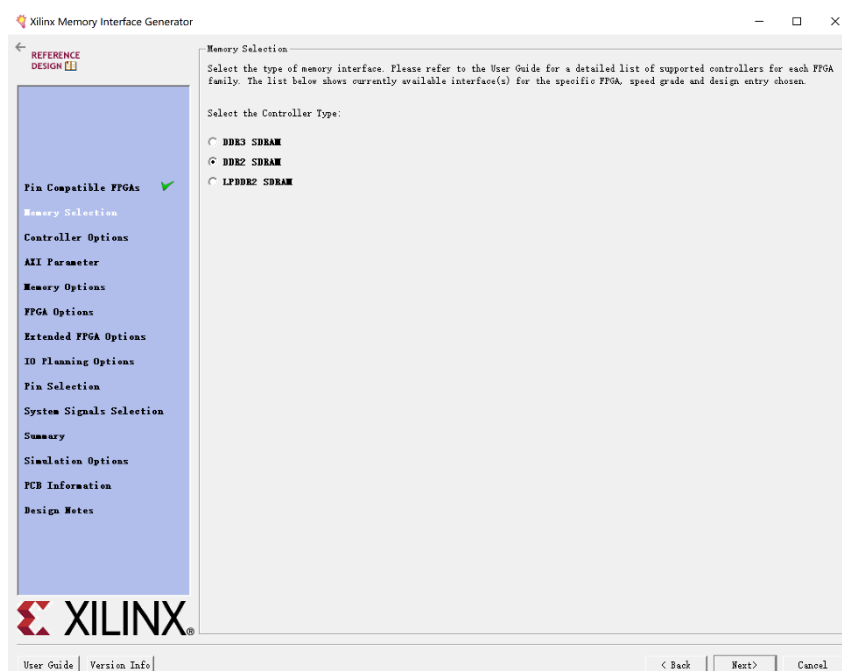
⑧ 主要的 RAM 操作接口为：

- a. mem_a -> 1 位标准信号 + 26 位地址信号
- b. mem_dq_i -> 16 位写入数据
- c. mem_dq_o -> 16 位读取数据
- d. mem_oen -> 读取使能信号
- e. mem_wen -> 写入使能信号
- f. mem_cen -> RAM 使能信号

⑨ 只需要调用 RAM 的几个接口，进行数据输入输出即可。

（二）自己调试 MIG IP 核：

- ① 打开 IP Catalog，搜索 mig
- ② 添加并定制 MIG IP 核：（具体参数如下图）
- ③ 使用该 IP 核，实现 DDR 操作，可以参考案例。



REFERENCE
DESIGN

Pin Compatible FPGAs ✓
Memory Selection ✓
Controller Options
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Pin Selection
System Signals Selection
Summary
Simulation Options
PCB Information
Design Notes

Options for Controller 0 - DDR2 SDRAM

Clock Period: Choose the clock period for the desired frequency. The allowed period range(3000 - 5000) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information. 3333 ps 300.03 MHz

PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. 4:1

Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above. Components

Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RDRAM II. MT47H64M16HR-25E Create Custom Part

Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above. 16

ECC: MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported. Disabled

Data Mask: Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs (DDR3 SDRAM, DDR2 SDRAM) will not use Data Mask. ☒

ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received. Strict

Memory Details: 1Gb, x16, row:13, col:10, bank:3, data bits per strobe:8, with data mask, single rank

User Guide Version Info < Back Next> Cancel

REFERENCE
DESIGN

Pin Compatible FPGAs ✓
Memory Selection ✓
Controller Options ✓
AXI Parameter
Memory Options
FPGA Options
Extended FPGA Options
IO Planning Options
Pin Selection
System Signals Selection
Summary
Simulation Options
PCB Information
Design Notes

Memory Options for Controller 0 - DDR2 SDRAM

Input Clock Period: Select the period for the PLL input clock (CLKIN). MIG determines the allowable input clock periods based on the Memory Clock Period entered above and the clocking guidelines listed in the User Guide. The generated design will use the selected Input Clock and Memory Clock Periods to generate the required PLL parameters. If the required input clock period is not available, the Memory Clock Period must be modified. 5000 ps (200 MHz)

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

Burst Type
The ordering of accesses with in a burst is determined based on the burst length, the burst type Sequential and the starting column address. Sequential

Output Drive Strength
Selecting reduced strength will reduce all outputs to approximately 60 percent of the drive strength. Fullstrength

Controller Chip Select Pin
The Chip Select (CS#) pin can be tied low externally to save one pin in the address/command group when this selection is set to 'Disable'. Disable is only valid for single rank configurations. Enable

RTT (nominal) - ODT
This feature allows to apply internal termination resistance of the memory module for signals DQ, DQS/DQS#, LDQS/LDQS#, VDQS/VDQS# and LDM/LDM. This improves the signal integrity of the memory channel. 50ohms

Memory Address Mapping Selection

User Address

☐ ROW BANK COLUMN

☒ BANK ROW COLUMN

User Guide Version Info < Back Next> Cancel

REFERENCE DESIGN [1]

Pin Compatible FPGAs ✓
Memory Selection ✓
Controller Options ✓
AXI Parameter
Memory Options ✓
FPGA Options
Extended FPGA Options
IO Planning Options
Pin Selection
System Signals Selection
Summary
Simulation Options
PCB Information
Design Notes

System Clock No Buffer

Reference Clock
Choose the desired reference clock configuration. Reference clock can be Differential or Single-Ended.

Reference Clock Use System Clock

System Reset Polarity
Choose the desired System Reset Polarity.

System Reset Polarity ACTIVE LOW

Debug Signals Control
This feature allows various debug signals present in the IP to be monitored on the ChipScope tool. The debug signals include status signals of various PHY calibration stages. Enabling this feature will connect all the debug signals to the ChipScope ILA and VIO cores in the example design top module. A part of each bus in the debug interface has been grounded so that users can replace the grounded signals with the required signals.

Debug Signals for Memory Controller OFF

This selects the value of Sample Data depth for Chipscope ILA used in Debug logic.

Sample Data Depth 1024

Internal Vref
Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This option can only be used at 800 Mbps and lower data rates. This can free 2 pins per bank where inputs are used. This setting has no effect on banks with only outputs.

Internal Vref ☒

IO Power Reduction
Significantly reduces average IO power by automatically disabling DQ/DQS IBUFs and internal terminations during WRITES and periods of inactivity.

IO Power Reduction ON

XADC Instantiation
The memory interface uses the temperature reading from the XADC block to perform temperature compensation and keep the read DQS centered in the data window. There is one XADC block per device. If the XADC is not currently used anywhere in the design, enable this option to have the block instantiated. If the XADC is already used, disable this MIG option. The user is then required to provide the temperature value to the top level 12-bit device_temp_i input port. Refer to Answer Record 51687 or the UG586 for detailed information.

XADC Instantiation Disabled

User Guide Version Info

< Back Next> Cancel

REFERENCE DESIGN [1]

Internal Termination for High Range Banks
Select the internal termination (IR_TERM) impedance for the High Range (HR) banks used in the interface.

Internal Termination Impedance 50 Ohms

REFERENCE DESIGN [1]

Pin/Bank Selection Mode

☐ New Design: Pick the optimum banks for a new design
☒ Fixed Pin Out: Pre-existing pin out is known and fixed

REFERENCE DESIGN [1]

Pin Compatible FPGAs ✓
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Pin Selection
System Signals Selection
Summary
Simulation Options
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Design Notes

Pin Selection For Controller 0 - DDR2 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr2_dq[0]	34	T3	R7	SSTL18_II
2	ddr2_dq[1]	34	T3	V6	SSTL18_II
3	ddr2_dq[2]	34	T3	B8	SSTL18_II
4	ddr2_dq[3]	34	T3	U7	SSTL18_II
5	ddr2_dq[4]	34	T3	V7	SSTL18_II
6	ddr2_dq[5]	34	T3	B6	SSTL18_II
7	ddr2_dq[6]	34	T3	U6	SSTL18_II
8	ddr2_dq[7]	34	T3	B5	SSTL18_II
9	ddr2_dq[8]	34	T1	T5	SSTL18_II
10	ddr2_dq[9]	34	T1	U3	SSTL18_II
11	ddr2_dq[10]	34	T1	V5	SSTL18_II
12	ddr2_dq[11]	34	T1	U4	SSTL18_II
13	ddr2_dq[12]	34	T1	V4	SSTL18_II
14	ddr2_dq[13]	34	T1	T4	SSTL18_II
15	ddr2_dq[14]	34	T1	V1	SSTL18_II
16	ddr2_dq[15]	34	T1	T3	SSTL18_II
17	ddr2_dm[0]	34	T3	T6	SSTL18_II
18	ddr2_dm[1]	34	T1	V1	SSTL18_II
19	ddr2_dqs_p[0]	34	T3	U9	DIFF_SSTL18_II
20	ddr2_dqs_n[0]	34	T3	V9	DIFF_SSTL18_II

INFO: Press Validate to proceed.

Validate Read XDC/UCF Save PinOut

User Guide Version Info

< Back Next> Cancel

(具体参数参照参考案例，接口过多，不再罗列)
(也可以直接导入板子的接口信息，方法见资料④)

注意事项

- ① 如果要使用 DDR 内存，切记要仔细阅读资料①
 - ② 如果选择自己调试 IP 核，要阅读资料①中参数栏，并阅读资料③
 - ③ 正常情况下，调用以下接口足以解决问题，其他接口初始化为 0 即可：
 - a. mem_a -> 1 位标准信号(1'b0) + 26 位地址信号
 - b. mem_dq_i -> 16 位写入数据
 - c. mem_dq_o -> 16 位读取数据
 - d. mem_oen -> 读取使能信号
 - e. mem_wen -> 写入使能信号
 - f. men_cen -> RAM 使能信号
 - g. chipTemp\mem_ub\mem_lb-> 0
 - ④ 注意 26 位的写入\读取地址，需要即使的更新，避免出现错误。
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