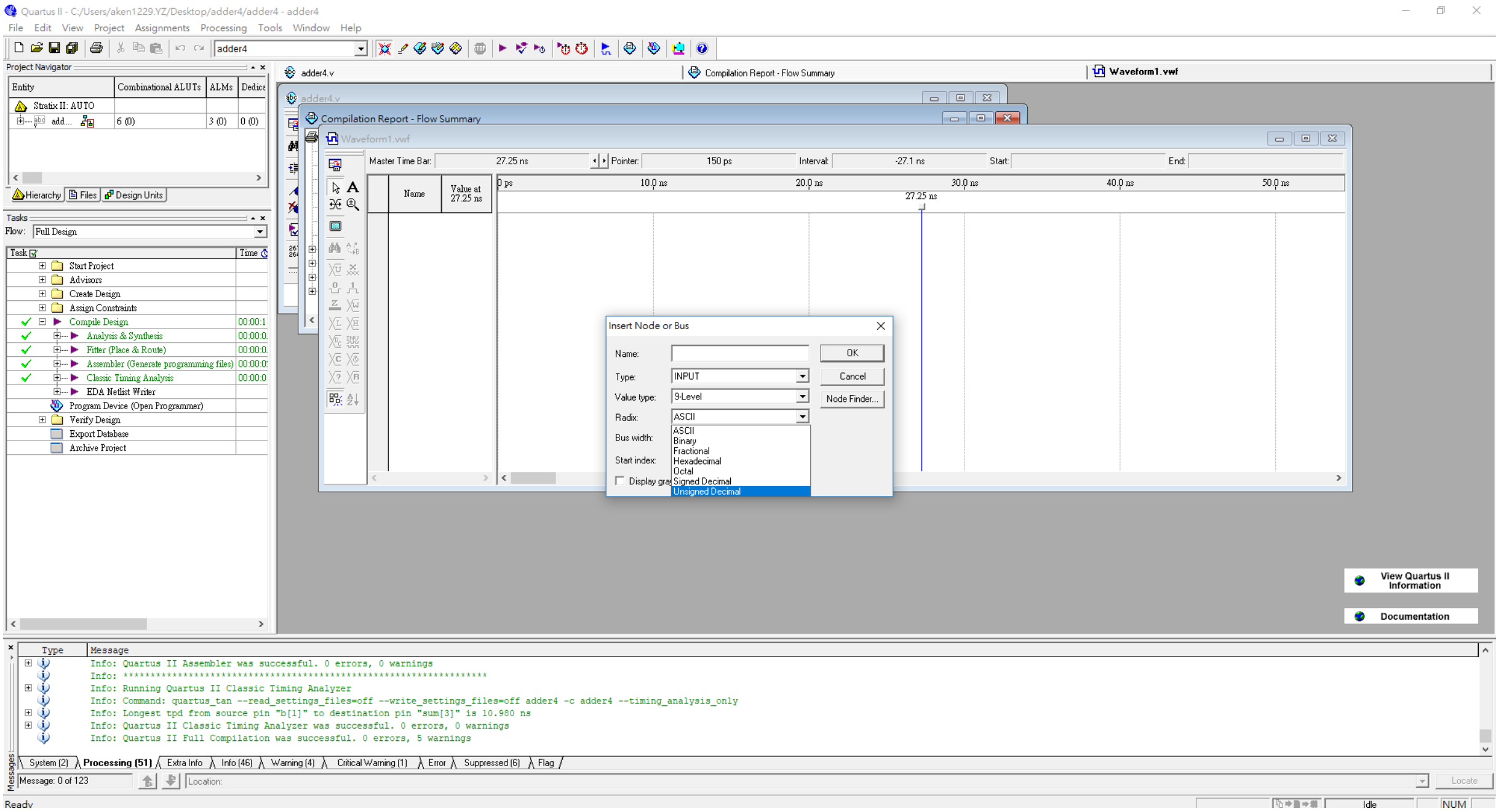
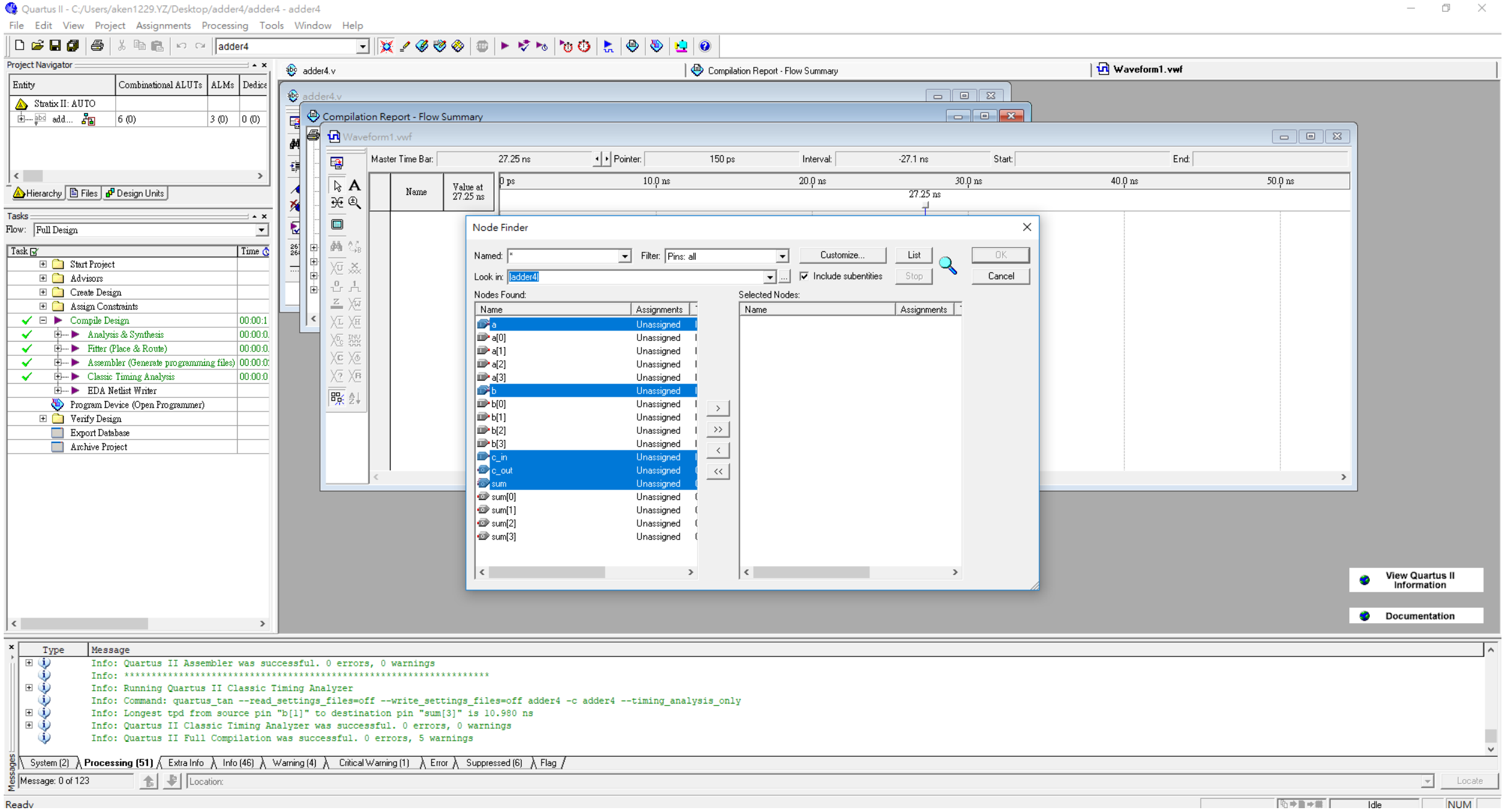
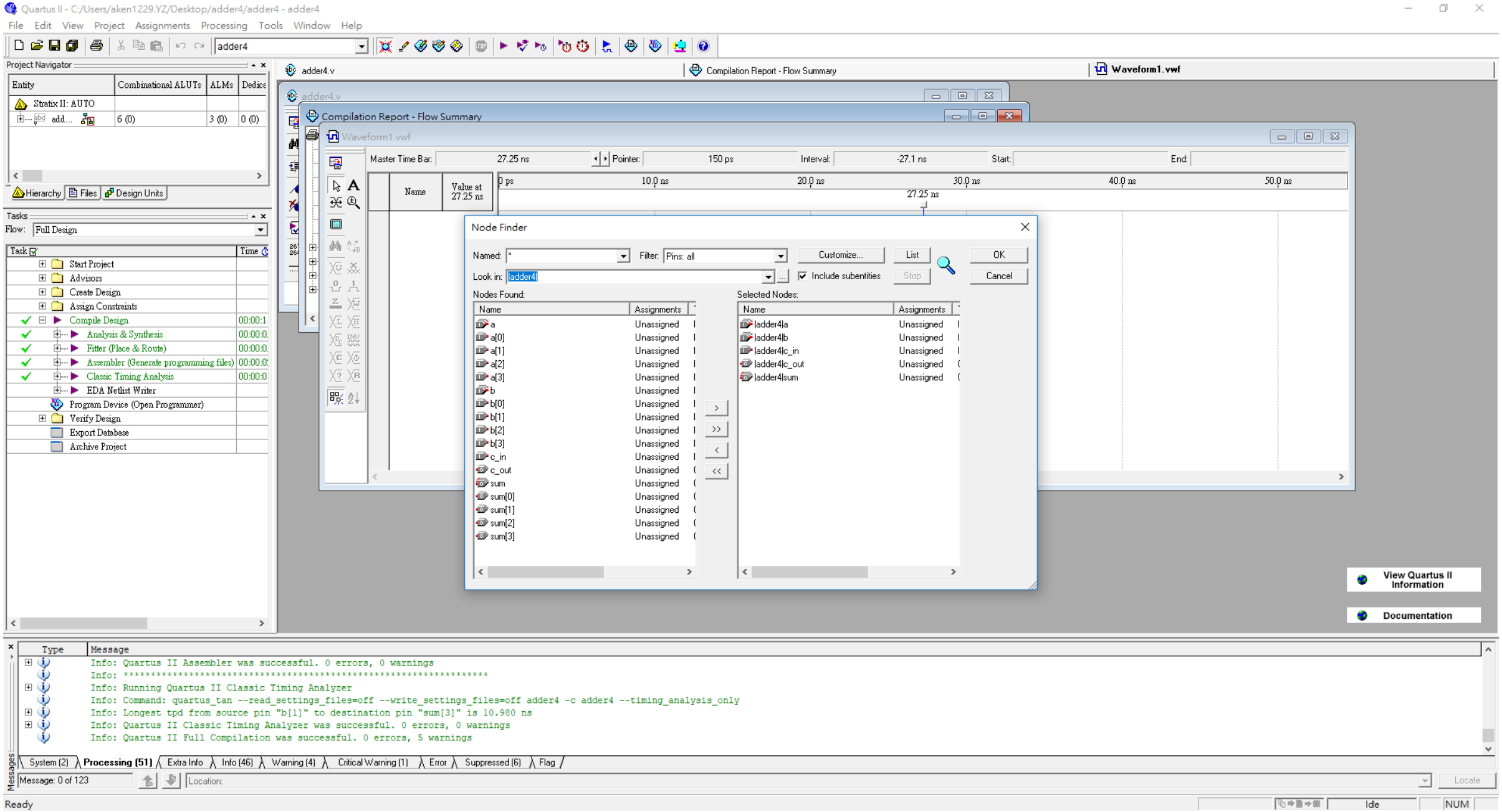
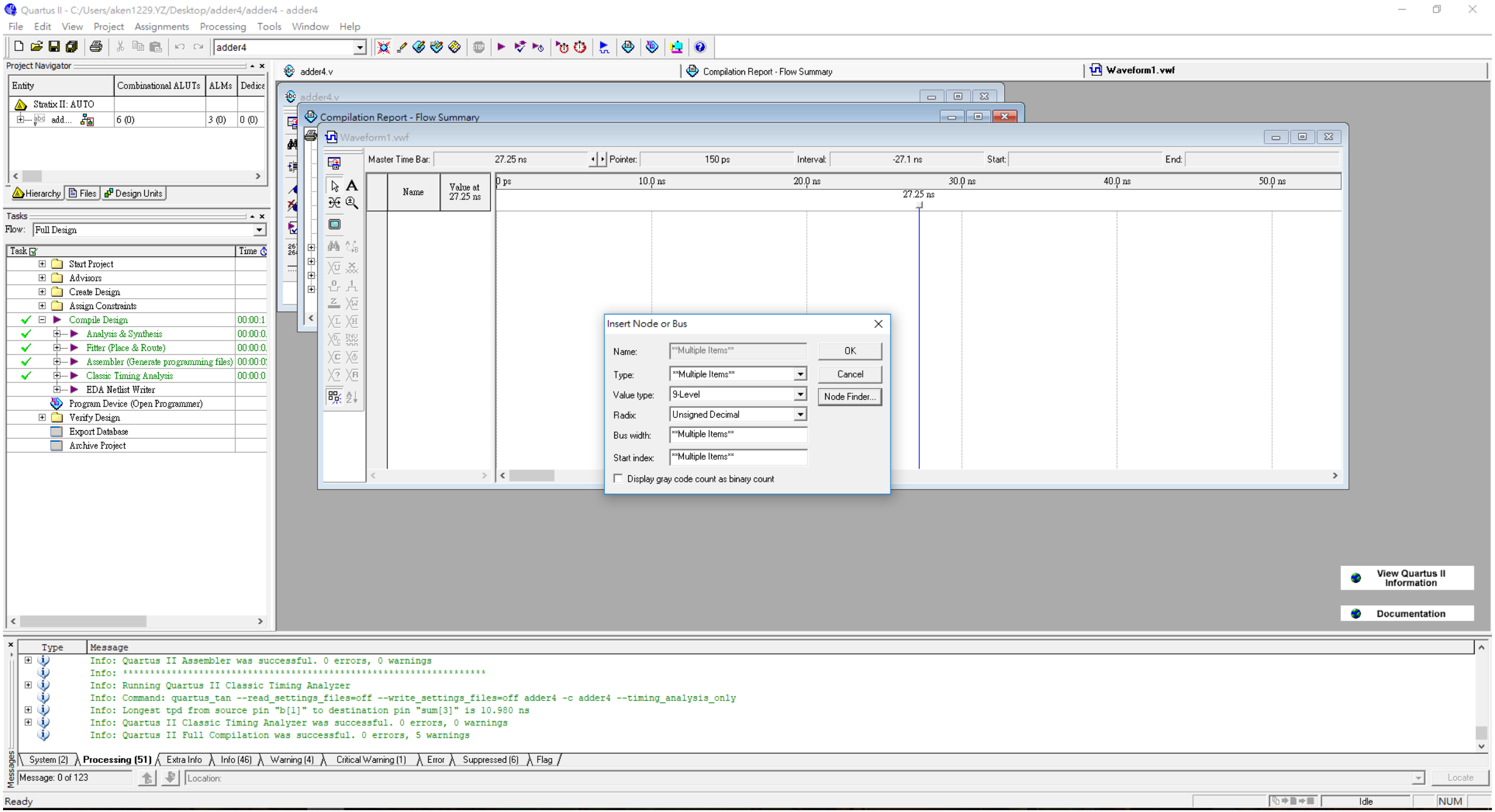
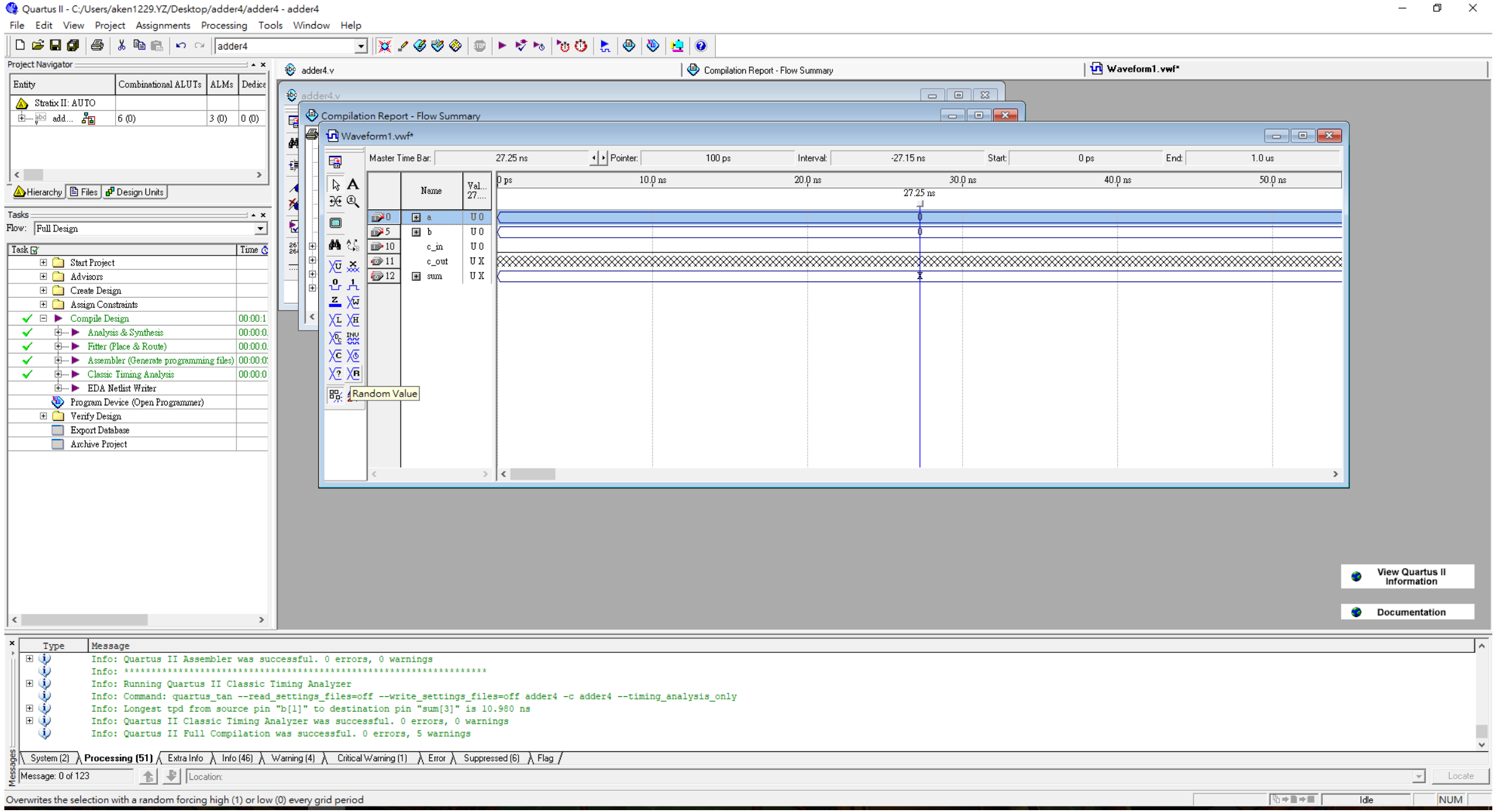
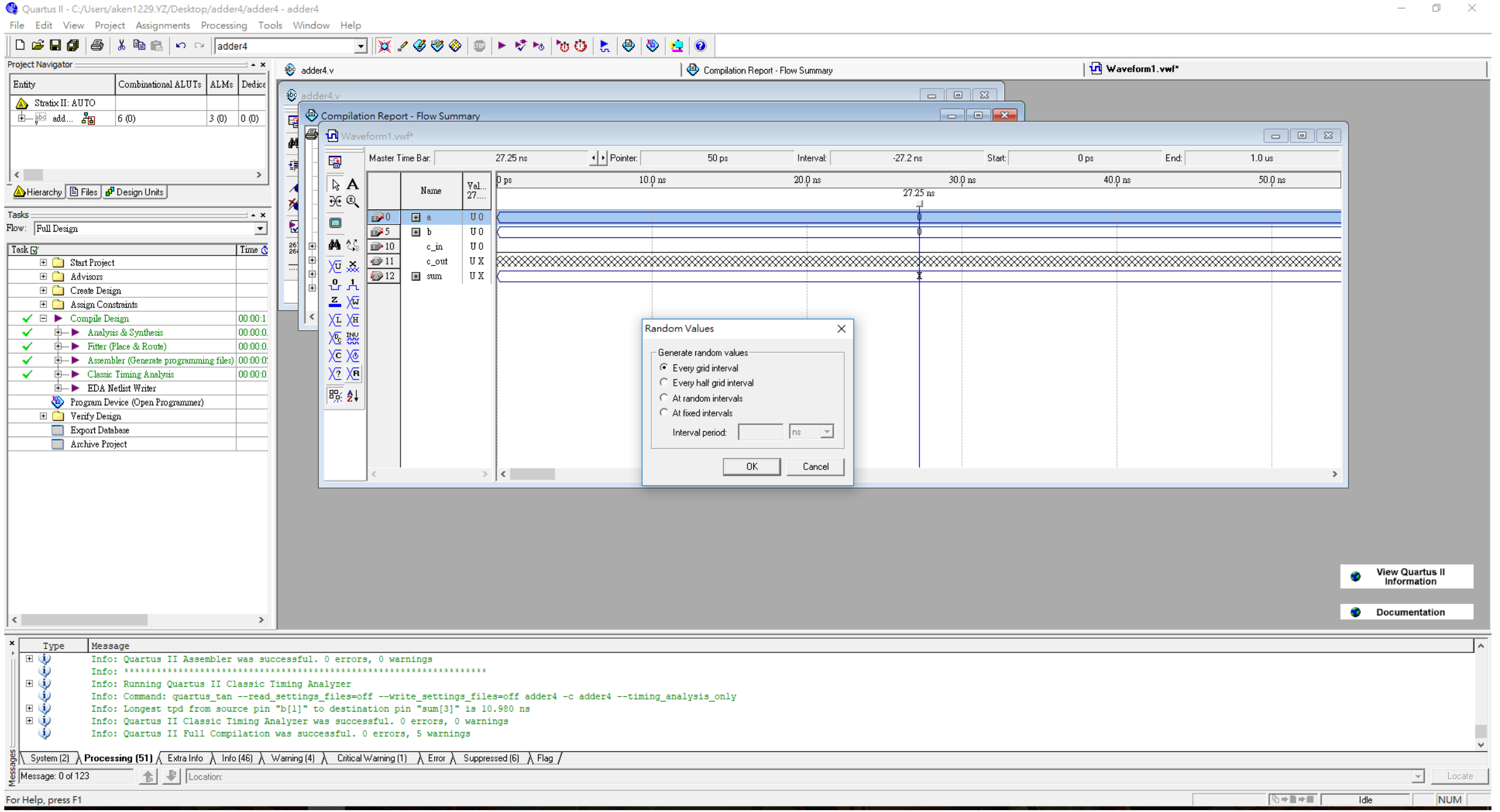

Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity
Combinational ALUTs
ALMs
Stratix II: AUTO
6 (0)
3 (0)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Full Design
Task
Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
Waveform1.vwf
Master Time Bar: 27.25 ns
Pointer: 150 ps
Interval: -27.1 ns
Start:
End:
Name
Value at 27.25 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
Insert Node or Bus
Name:
Type: INPUT
Value type: 9-Level
Radix: ASCII
Bus width:
Start index:
Display gra
OK
Cancel
Node Finder...
ASCII
Binary
Fractional
Hexadecimal
Octal
Signed Decimal
Unsigned Decimal
View Quartus II Information
Documentation
Type
Message
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: **
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off adder4 -c adder4 --timing_analysis_only
Info: Longest tpd from source pin "b[1]" to destination pin "sum[3]" is 10.980 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings
System (2)
Processing (51)
Extra Info
Info (46)
Warning (4)
Critical Warning (1)
Error
Suppressed (6)
Flag
Messages
Message: 0 of 123
Location:
Locate
Ready
Idle
NUM

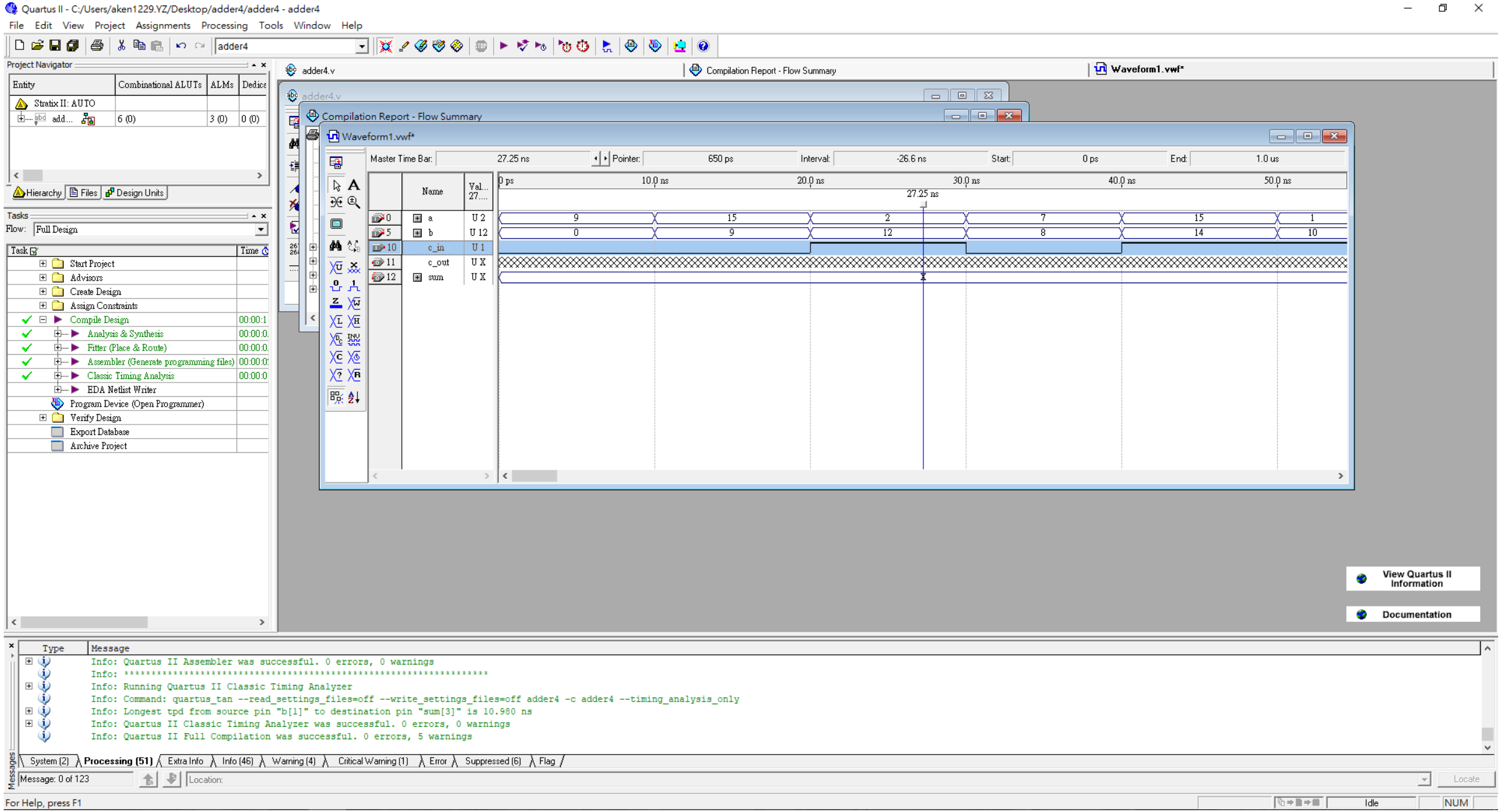

Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity
Combinational ALUTs
ALMs
Stratix II: AUTO
add...
6 (0)
3 (0)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Full Design
Task
Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
Waveform1.vwf
Master Time Bar: 27.25 ns
Pointer: 150 ps
Interval: -27.1 ns
Start:
End:
Name
Value at 27.25 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
Node Finder
Named: *
Filter: Pins: all
Customize...
List
OK
Look in: adder4
Include subentities
Stop
Cancel
Nodes Found:
Selected Nodes:
Name
Assignments
a Unassigned
a[0] Unassigned
a[1] Unassigned
a[2] Unassigned
a[3] Unassigned
b Unassigned
b[0] Unassigned
b[1] Unassigned
b[2] Unassigned
b[3] Unassigned
c_in Unassigned
c_out Unassigned
sum Unassigned
sum[0] Unassigned
sum[1] Unassigned
sum[2] Unassigned
sum[3] Unassigned
View Quartus II Information
Documentation
Type
Message
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: **
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off adder4 -c adder4 --timing_analysis_only
Info: Longest tpd from source pin "b[1]" to destination pin "sum[3]" is 10.980 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings
System (2) Processing (51) Extra Info Info (46) Warning (4) Critical Warning (1) Error Suppressed (6) Flag
Message: 0 of 123
Location:
Locate
Ready
Idle
NUM

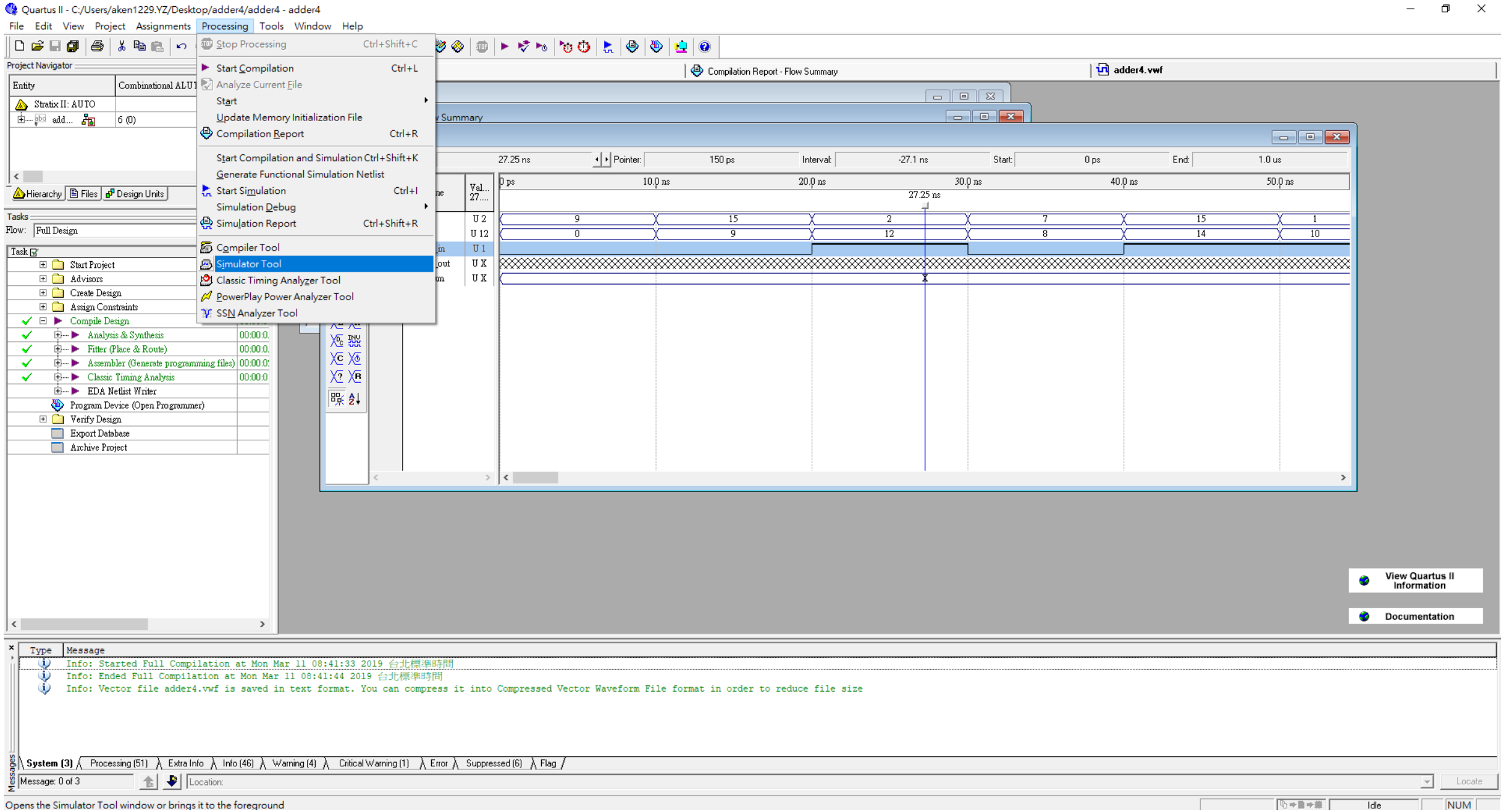

Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity
Combinational ALUTs
ALMs
Stratix II: AUTO
add...
6 (0)
3 (0)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Full Design
Task
Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
Waveform1.vwf
Master Time Bar: 27.25 ns
Pointer: 150 ps
Interval: -27.1 ns
Start:
End:
Name
Value at 27.25 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
Node Finder
Named: *
Filter: Pins: all
Customize...
List
OK
Look in: |adder4|
Include subentities
Stop
Cancel
Nodes Found:
Selected Nodes:
Name
Assignments
a Unassigned
a[0] Unassigned
a[1] Unassigned
a[2] Unassigned
a[3] Unassigned
b Unassigned
b[0] Unassigned
b[1] Unassigned
b[2] Unassigned
b[3] Unassigned
c_in Unassigned
c_out Unassigned
sum Unassigned
sum[0] Unassigned
sum[1] Unassigned
sum[2] Unassigned
sum[3] Unassigned
|adder4|a Unassigned
|adder4|b Unassigned
|adder4|c_in Unassigned
|adder4|c_out Unassigned
|adder4|sum Unassigned
View Quartus II Information
Documentation
Type
Message
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: **
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off adder4 -c adder4 --timing_analysis_only
Info: Longest tpd from source pin "b[1]" to destination pin "sum[3]" is 10.980 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings
System (2) Processing (51) Extra Info Info (46) Warning (4) Critical Warning (1) Error Suppressed (6) Flag
Message: 0 of 123
Location:
Locate
Ready
Idle
NUM

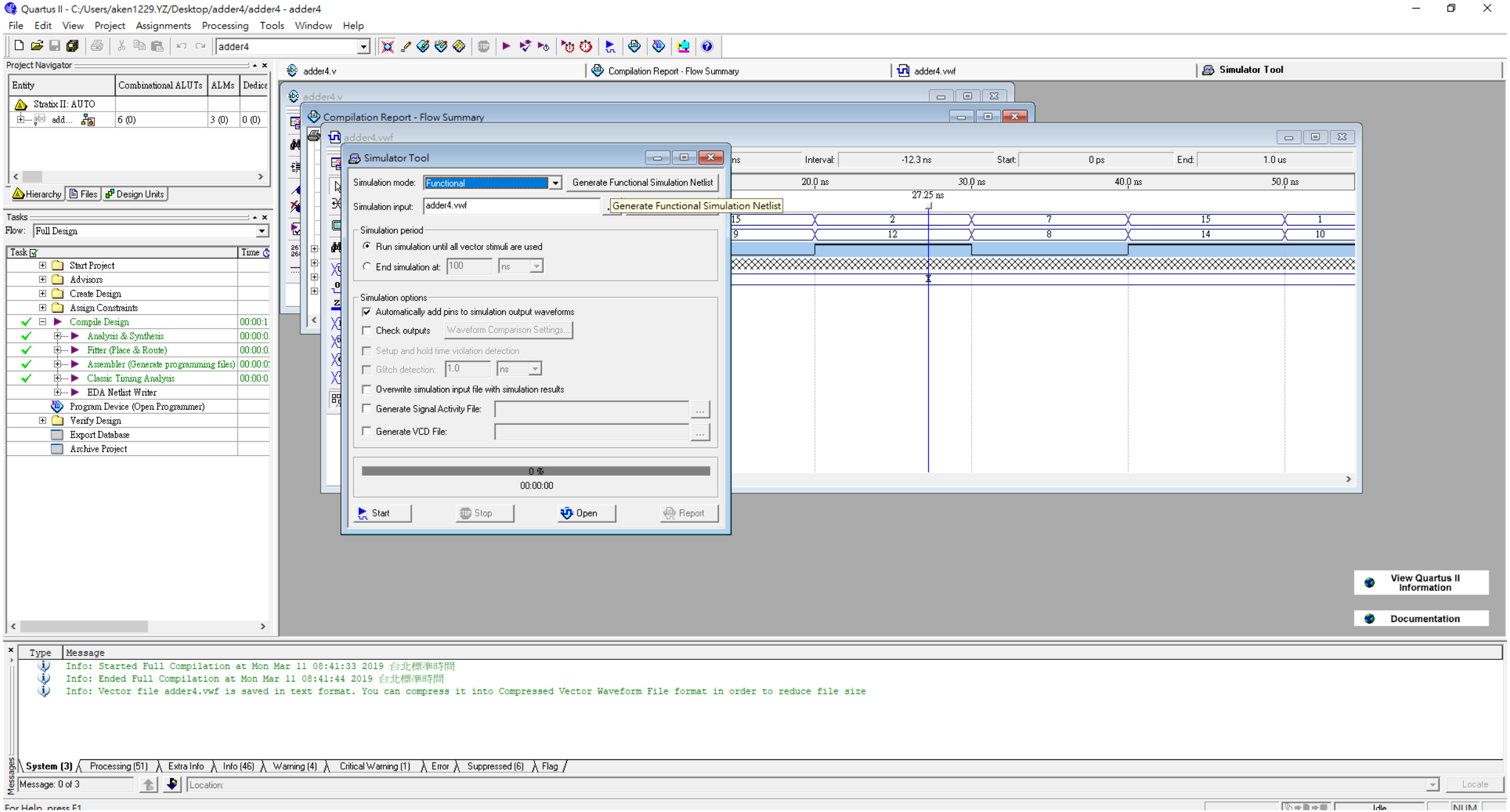

Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity
Combinational ALUTs
ALMs
Stratix II: AUTO
6 (0)
3 (0)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Full Design
Task
Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
Waveform1.vwf
Master Time Bar:
27.25 ns
Pointer:
150 ps
Interval:
-27.1 ns
Start:
End:
Name
Value at 27.25 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
Insert Node or Bus
Name:
Multiple Items
Type:
Multiple Items
Value type:
9-Level
Radix:
Unsigned Decimal
Bus width:
Multiple Items
Start index:
Multiple Items
Display gray code count as binary count
OK
Cancel
Node Finder...
View Quartus II Information
Documentation
Type
Message
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: **
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off adder4 -c adder4 --timing_analysis_only
Info: Longest tpd from source pin "b[1]" to destination pin "sum[3]" is 10.980 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings
System (2)
Processing (51)
Extra Info
Info (46)
Warning (4)
Critical Warning (1)
Error
Suppressed (6)
Flag
Message: 0 of 123
Location:
Locate
Ready
Idle
NUM

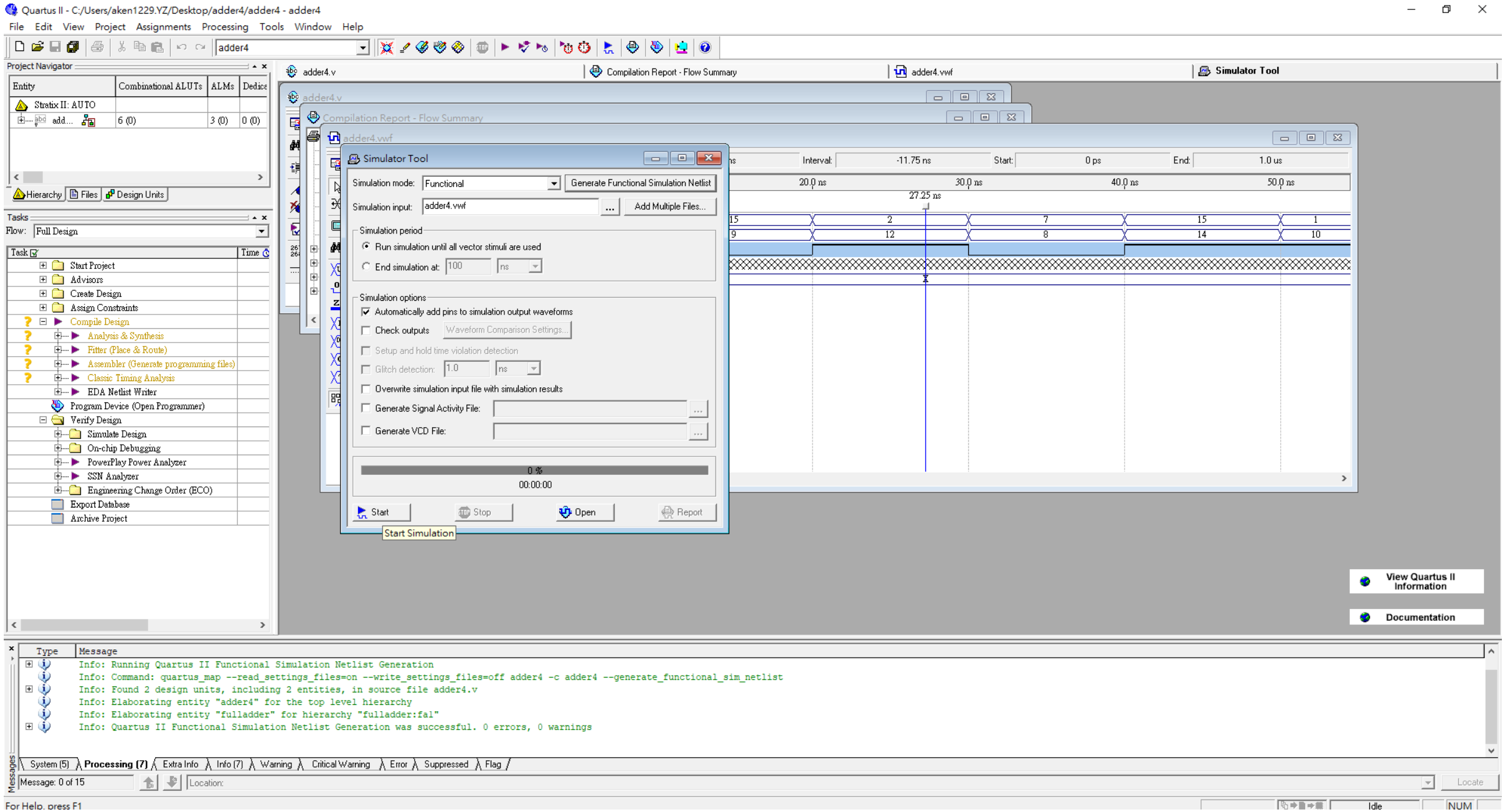

Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity
Combinational ALUTs
ALMs
Stratix II: AUTO
add...
6 (0)
3 (0)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Full Design
Task
Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
Waveform1.vwf*
Master Time Bar: 27.25 ns
Pointer: 100 ps
Interval: -27.15 ns
Start: 0 ps
End: 1.0 us
Name
Val... 27....
a
b
c_in
c_out
sum
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
Random Value
View Quartus II Information
Documentation
Type
Message
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off adder4 -c adder4 --timing_analysis_only
Info: Longest tpd from source pin "b[1]" to destination pin "sum[3]" is 10.980 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings
System (2)
Processing (51)
Extra Info
Info (46)
Warning (4)
Critical Warning (1)
Error
Suppressed (6)
Flag
Message: 0 of 123
Location:
Locate
Overwrites the selection with a random forcing high (1) or low (0) every grid period
Idle
NUM

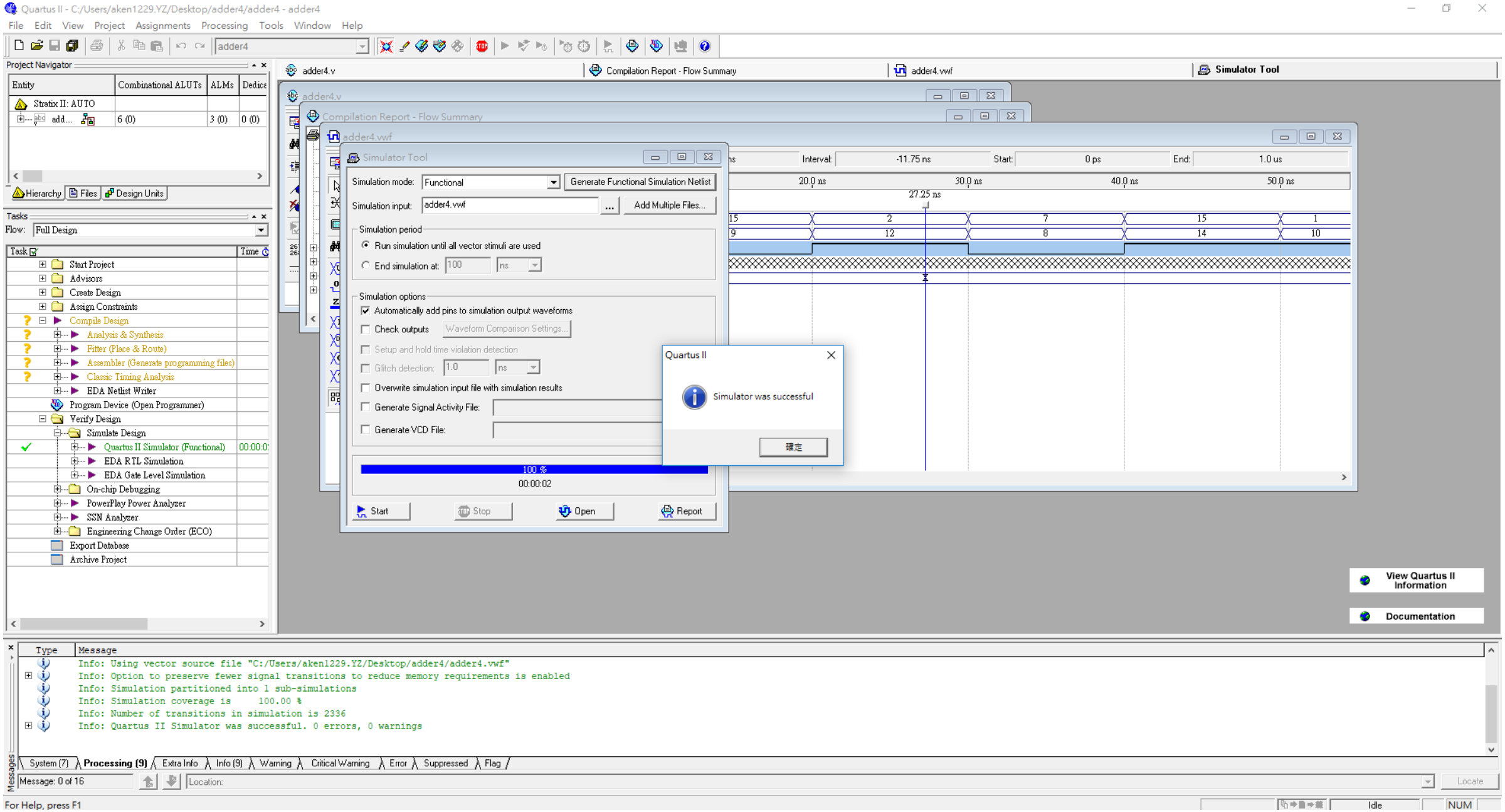

Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity | Combinational ALUTs | ALMs | Dedic
Stratix II: AUTO
add... 6 (0) 3 (0) 0 (0)
Hierarchy Files Design Units
Tasks
Flow: Full Design
Task Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design 00:00:1
Analysis & Synthesis 00:00:0
Fitter (Place & Route) 00:00:0
Assembler (Generate programming files) 00:00:0
Classic Timing Analysis 00:00:0
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
Waveform1.vwf*
Master Time Bar: 27.25 ns Pointer: 50 ps Interval: -27.2 ns Start: 0 ps End: 1.0 us
Name
a
b
c_in
c_out
sum
0 ps 10.0 ns 20.0 ns 30.0 ns 40.0 ns 50.0 ns
27.25 ns
Random Values
Generate random values
Every grid interval
Every half grid interval
At random intervals
At fixed intervals
Interval period:
ns
OK
Cancel
View Quartus II Information
Documentation
Type Message
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off adder4 -c adder4 --timing_analysis_only
Info: Longest tpd from source pin "b[1]" to destination pin "sum[3]" is 10.980 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings
System (2) Processing (51) Extra Info Info (46) Warning (4) Critical Warning (1) Error Suppressed (6) Flag
Message: 0 of 123
Location:
Locate
For Help, press F1
Idle
NUM

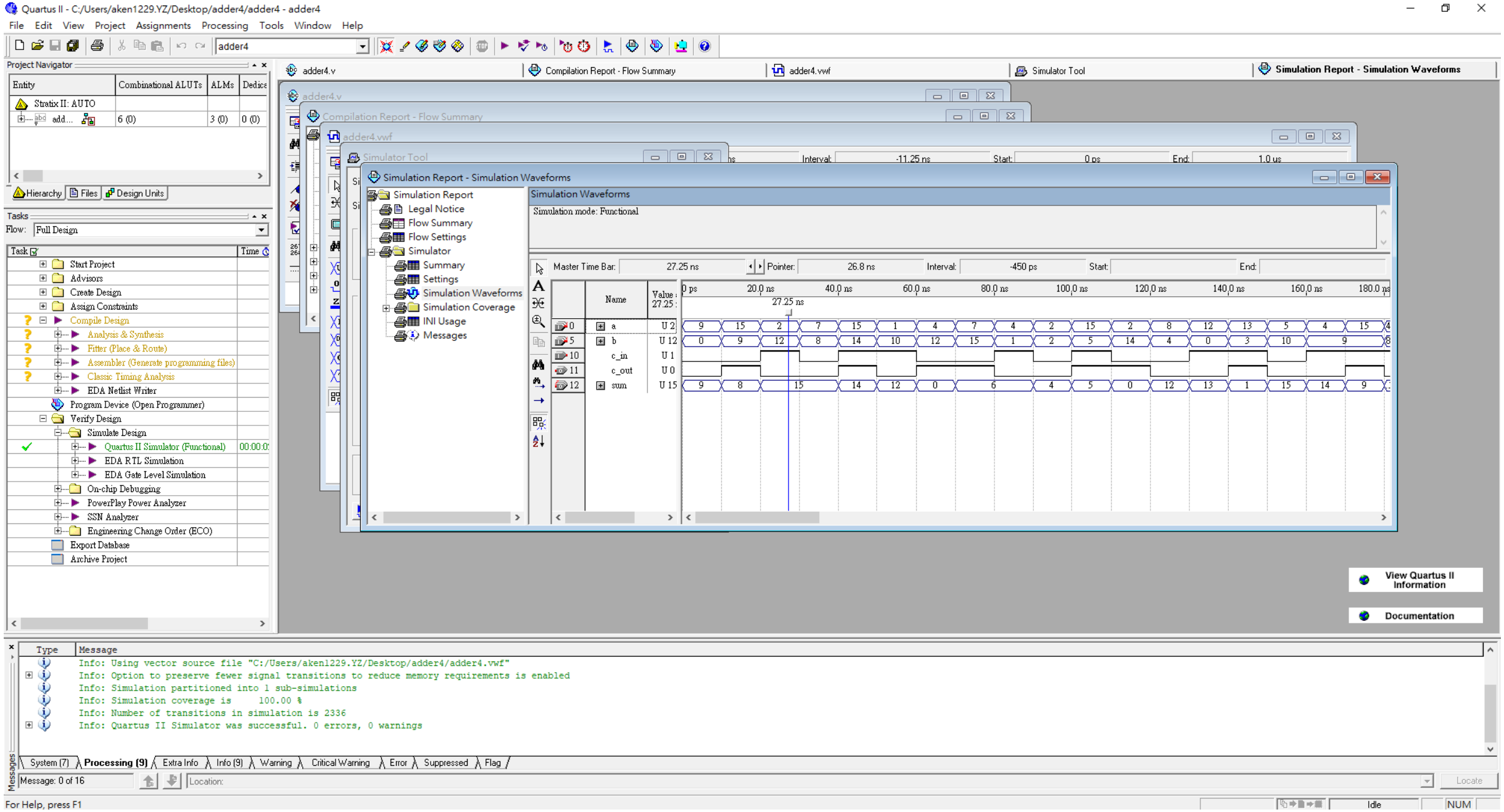

Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity
Combinational ALUTs
ALMs
Stratix II: AUTO
add...
6 (0)
3 (0)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Full Design
Task
Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
Waveform1.vwf*
Master Time Bar: 27.25 ns
Pointer: 650 ps
Interval: -26.6 ns
Start: 0 ps
End: 1.0 us
Name
Val... 27....
a
b
c_in
c_out
sum
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
View Quartus II Information
Documentation
Type
Message
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off adder4 -c adder4 --timing_analysis_only
Info: Longest tpd from source pin "b[1]" to destination pin "sum[3]" is 10.980 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings
System (2)
Processing (51)
Extra Info
Info (46)
Warning (4)
Critical Warning (1)
Error
Suppressed (6)
Flag
Message: 0 of 123
Location:
Locate
For Help, press F1
Idle
NUM


Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report Ctrl+R
Start Compilation and Simulation Ctrl+Shift+K
Generate Functional Simulation Netlist
Start Simulation Ctrl+I
Simulation Debug
Simulation Report Ctrl+Shift+R
Compiler Tool
Simulator Tool
Classic Timing Analyzer Tool
PowerPlay Power Analyzer Tool
SSN Analyzer Tool
Project Navigator
Entity
Stratix II: AUTO
Hierarchy Files Design Units
Tasks
Flow: Full Design
Task
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Export Database
Archive Project
Compilation Report - Flow Summary
adder4.vwf
Pointer: 150 ps
Interval: -27.1 ns
Start: 0 ps
End: 1.0 us
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
View Quartus II Information
Documentation
Type Message
Info: Started Full Compilation at Mon Mar 11 08:41:33 2019 台北標準時間
Info: Ended Full Compilation at Mon Mar 11 08:41:44 2019 台北標準時間
Info: Vector file adder4.vwf is saved in text format. You can compress it into Compressed Vector Waveform File format in order to reduce file size
System (3) Processing (51) Extra Info Info (46) Warning (4) Critical Warning (1) Error Suppressed (6) Flag
Message: 0 of 3
Location:
Locate
Opens the Simulator Tool window or brings it to the foreground
Idle
NUM


Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity
Combinational ALUTs
ALMs
Stratix II: AUTO
6 (0)
3 (0)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Full Design
Task
Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
adder4.vwf
Simulator Tool
Simulation mode: Functional
Generate Functional Simulation Netlist
Simulation input: adder4.vwf
Simulation period
Run simulation until all vector stimuli are used
End simulation at: 100 ns
Simulation options
Automatically add pins to simulation output waveforms
Check outputs
Waveform Comparison Settings...
Setup and hold time violation detection
Glitch detection: 1.0 ns
Overwrite simulation input file with simulation results
Generate Signal Activity File:
Generate VCD File:
0 %
00:00:00
Start
Stop
Open
Report
Interval: -12.3 ns
Start: 0 ps
End: 1.0 us
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
View Quartus II Information
Documentation
Type
Message
Info: Started Full Compilation at Mon Mar 11 08:41:33 2019 台北標準時間
Info: Ended Full Compilation at Mon Mar 11 08:41:44 2019 台北標準時間
Info: Vector file adder4.vwf is saved in text format. You can compress it into Compressed Vector Waveform File format in order to reduce file size
System (3)
Processing (51)
Extra Info
Info (46)
Warning (4)
Critical Warning (1)
Error
Suppressed (6)
Flag
Message: 0 of 3
Location:
Locate
For Help, press F1
Idle
NUM


Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity
Combinational ALUTs
ALMs
Stratix II: AUTO
add...
6 (0)
3 (0)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Full Design
Task
Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Simulate Design
On-chip Debugging
PowerPlay Power Analyzer
SSN Analyzer
Engineering Change Order (ECO)
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
adder4.vwf
Simulator Tool
Simulation mode: Functional
Generate Functional Simulation Netlist
Simulation input: adder4.vwf
Add Multiple Files...
Simulation period
Run simulation until all vector stimuli are used
End simulation at: 100 ns
Simulation options
Automatically add pins to simulation output waveforms
Check outputs
Waveform Comparison Settings...
Setup and hold time violation detection
Glitch detection: 1.0 ns
Overwrite simulation input file with simulation results
Generate Signal Activity File:
Generate VCD File:
0 %
00:00:00
Start
Stop
Open
Report
Start Simulation
Interval: -11.75 ns
Start: 0 ps
End: 1.0 us
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
View Quartus II Information
Documentation
Type
Message
Info: Running Quartus II Functional Simulation Netlist Generation
Info: Command: quartus_map --read_settings_files=on --write_settings_files=off adder4 -c adder4 --generate_functional_sim_netlist
Info: Found 2 design units, including 2 entities, in source file adder4.v
Info: Elaborating entity "adder4" for the top level hierarchy
Info: Elaborating entity "fulladder" for hierarchy "fulladder:fa1"
Info: Quartus II Functional Simulation Netlist Generation was successful. 0 errors, 0 warnings
System (5)
Processing (7)
Extra Info
Info (7)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 15
Location:
Locate
For Help, press F1
Idle
NUM


Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Combinational ALUTs
ALMs
Stratix II: AUTO
Hierarchy
Files
Design Units
Tasks
Flow: Full Design
Task
Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Simulate Design
Quartus II Simulator (Functional)
EDA RTL Simulation
EDA Gate Level Simulation
On-chip Debugging
PowerPlay Power Analyzer
SSN Analyzer
Engineering Change Order (ECO)
Export Database
Archive Project
adder4.v
Compilation Report - Flow Summary
adder4.vwf
Simulator Tool
Simulation mode: Functional
Generate Functional Simulation Netlist
Simulation input: adder4.vwf
Add Multiple Files...
Simulation period
Run simulation until all vector stimuli are used
End simulation at: 100 ns
Simulation options
Automatically add pins to simulation output waveforms
Check outputs
Waveform Comparison Settings...
Setup and hold time violation detection
Glitch detection: 1.0 ns
Overwrite simulation input file with simulation results
Generate Signal Activity File:
Generate VCD File:
100 %
00:00:02
Start
Stop
Open
Report
Quartus II
Simulator was successful
確定
Interval: -11.75 ns
Start: 0 ps
End: 1.0 us
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.25 ns
View Quartus II Information
Documentation
Type
Message
Info: Using vector source file "C:/Users/aken1229.YZ/Desktop/adder4/adder4.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 100.00 %
Info: Number of transitions in simulation is 2336
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (7)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
Locate
For Help, press F1
Idle
NUM


Quartus II - C:/Users/aken1229.YZ/Desktop/adder4/adder4 - adder4
File Edit View Project Assignments Processing Tools Window Help
adder4
Project Navigator
Entity | Combinational ALUTs | ALMs | Dedica
Stratix II: AUTO
add... 6 (0) 3 (0) 0 (0)
Hierarchy Files Design Units
Tasks
Flow: Full Design
Task | Time
Start Project
Advisors
Create Design
Assign Constraints
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Verify Design
Simulate Design
Quartus II Simulator (Functional) 00:00:0
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adder4.v
Compilation Report - Flow Summary
adder4.vwf
Simulator Tool
Simulation Report - Simulation Waveforms
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 27.25 ns Pointer: 26.8 ns Interval: -450 ps Start: End:
Name
a
b
c_in
c_out
sum
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Documentation
Type Message
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