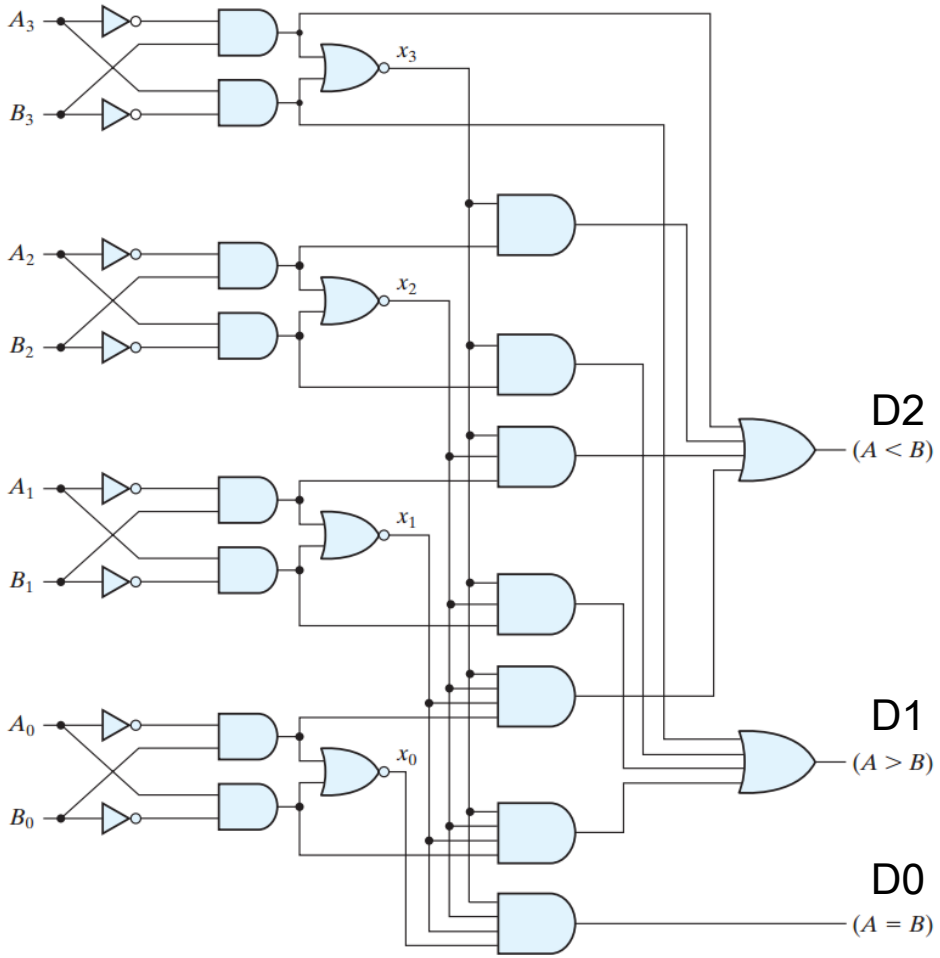
HW1 Bonus: 4-bit magnitude comparator

- Using gate-level Verilog to implement this design



Output results :

- A<B : D = 3'b100
- A>B : D = 3'b010
- A=B : D = 3'b001