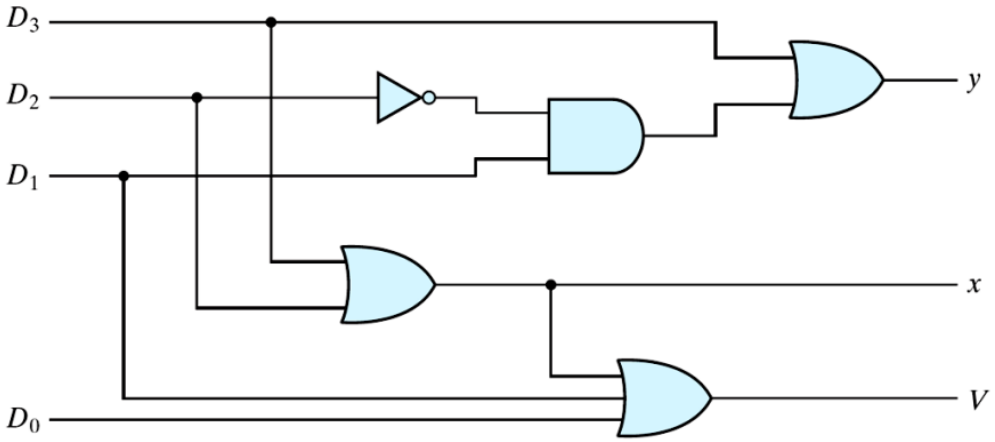
Homework 1 : Priority Encoder

- Design a priority encoder using gate-level Verilog



Truth Table of a Priority Encoder

LSB Inputs			MSB	Outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1