ADSP-BF561 EZ-KIT Lite®
Evaluation System Manual

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Analog Devices, Inc.
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Norwood, Mass. 02062-9106

ANALOG DEVICES

Copyright Information

Printed in the USA.

Limited Warranty

The EZ-KIT Lite evaluation system is warranted against defects in materials and workmanship for a period of one year from the date of purchase from Analog Devices or from an authorized dealer.

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Regulatory Compliance

The ADSP-BF561 EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The ADSP-BF561 EZ-KIT Lite evaluation system has been appended to Analog Devices Development Tools Technical Construction File referenced "DSPTOOLS1" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

CONTENTS

PREFACE

PREFACE

Thank you for purchasing the ADSP-BF561 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for Blackfin® processors.

The Blackfin processors are embedded processors that support a Media Instruction Set Computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics towards delivering signal processing performance in a microprocessor-like environment.

The evaluation board is designed to be used in conjunction with the VisualDSP++® development environment to test the capabilities of the ADSP-BF561 Blackfin processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C and ADSP-BF561 assembly
- Load, run, step, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF561 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF561 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster

communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to `http://www.analog.com/dsp/tools/`.

ADSP-BF561 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The ADSP-BF561 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF561 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a users program to 41 KB of internal memory for code space with no restrictions for data space.

The board features:

- Analog Devices ADSP-BF561 processor
  - 256-pin Mini-BGA package
  - 30 MHz CLKIN oscillator
- Synchronous Dynamic Random Access Memory (SDRAM)
  - 64 MB (16M x 16 bits x 2 chips)
- Flash Memory
  - 8 MB (4M x 16 bits)

- Analog Audio Interface
  - AD1836 A – Analog Devices 96 kHz audio codec
  - 4 input RCA phono jacks (2 Stereo Channels)
  - 6 output RCA phono jacks (3 Stereo Channels)
- Analog Video Interface
  - ADV7183A video decoder w/ 3 input RCA phono jacks
  - ADV7179 video encoder w/ 3 output RCA phono jacks
- Universal Asynchronous Receiver/Transmitter (UART)
  - ADM3202 RS-232 line driver/receiver
  - DB9 male connector
- LEDs
  - 20 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 16 general purpose (amber), and 1 USB monitor (amber)
- Push Buttons
  - 5 push buttons with debounce logic: 1 reset, 4 programmable flags
- Expansion Interface
  - `PPI0`, `PPI1`, `SPI`, `EBIU`, `Timers11-0`, `UART`, Programmable Flags, `SPORT0`, `SPORT1`
- Other Features
  - JTAG ICE 14-pin header

The EZ-KIT Lite board holds 8 MB of flash memory, which can be used to store user-specific boot code, allowing the board to run as a stand-alone unit. The board also holds 512-Mb SDRAM, which can be used at runtime. For more information see "External Memory" on page 1-6.

SPORT0 interfaces with the AD1836A audio codec, allowing you to create audio signal processing applications. SPORT0 also attaches to an off-board connector to allow communication with other serial devices. For information about SPORT0, see "SPORT0 Audio Interface" on page 2-3.

The Parallel Peripheral Interfaces (PPIs) of the processor connect to both a video encoder and video decoder, allowing you to create video signal processing applications. For information on how the board utilizes the processor's PPIs, see "PPI Interfaces" on page 2-6.

The UART of the processor connects to an RS232 Line Driver and a DB9 male connector, allowing you to interface with a PC or other serial device. For information about the UART, see "UART Port" on page 2-8.

Additionally, the EZ-KIT Lite board provides access to most of the processor's peripheral ports. Access is provided in the form of a three-connector expansion interface. For information about the expansion interface, see "Expansion Interface" on page 2-8.

Purpose of This Manual

The *ADSP-BF561 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes the operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF561 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

The product software installation is detailed in the *VisualDSP++ Installation Quick Reference Card*.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts (such as the *ADSP-BF561 Blackfin Processor Hardware Reference* and *Blackfin Processor Instruction Set Reference*) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and user's or getting started guides. For the locations of these documents, see "Related Documents".

Manual Contents

The manual consists of:

- Chapter 1, "Using EZ-KIT Lite" on page 1-1
  Describes the EZ-KIT Lite functionality from a programmer's perspective and provides an easy-to-access memory map
- Chapter 2, "EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components.

- Appendix A, "Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "Schematics" on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.

This appendix is not part of the online Help. The online Help viewers should go to the PDF version of the ADSP-BF561 EZ-KIT Lite Evaluation System Manual located in the `Docs\EZ-KIT Lite Manuals` folder on the installation CD to see the schematics. Alternatively, the schematics can be found on the Analog Devices Web site, `www.analog.com/processors`.

What's New in This Manual

This revision of the *ADSP-BF561 EZ-KIT Lite Evaluation System Manual* provides an updated listing of related documents and updated licensing information.

Technical or Customer Support

You can reach DSP Tools Support in the following ways.

- Visit the Embedded Processing and DSP products Web site at `http://www.analog.com/processors/technicalSupport`
- E-mail tools questions to `dsptools.support@analog.com`
- E-mail processor questions to `dsp.support@analog.com`
- Phone questions to **1-800-ANALOGD**

- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:

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Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
USA
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Supported Processors

This EZ-KIT Lite evaluation system supports the Analog Devices ADSP-BF561 Blackfin embedded processors.

Product Information

You can obtain product information from the Analog Devices Web site, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at `www.analog.com`. Our Web site provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit www.myanalog.com to sign up. Click **Register** to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

Processor Product Information

For information on embedded processors and DSPs, visit our Web site at www.analog.com/processors, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- E-mail questions or requests for information to
  dsp.support@analog.com
- Fax questions or requests for information to
  1-781-461-3010 (North America)
  +49 (89) 76 903-557 (Europe)
- Access the FTP Web site at
  ftp ftp.analog.com or ftp 137.71.23.21
  ftp://ftp.analog.com

Related Documents

For information on product related development software, see the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF561 Blackfin Embedded Symmetric Multi-Processor Datasheet	General functional description, pinout, and timing
ADSP-BF561 Blackfin Processor Hardware Reference	Description of internal processor architecture and all register functions
Blackfin Processor Instruction Set Reference	Description of all allowed processor assembly instructions

Table 2. Related VisualDSP++ Publications

Title	Description
VisualDSP++ User's Guide	Description of VisualDSP++ features and usage
VisualDSP++ Assembler and Preprocessor Manual	Description of the assembler function and commands
VisualDSP++ C/C++ Complier and Library Manual for Blackfin Processors	Description of the complier function and commands for Blackfin processors
VisualDSP++ Linker & Utilities Manual	Description of the linker function and commands
VisualDSP++ Loader Manual	Description of the loader/splitter function and commands

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

All documentation is available online. Most documentation is available in printed form.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:

`http://www.analog.com/processors/resources/technicalLibrary`

Online Technical Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, the Dinkum Abridged C++ library, and Flexible License Manager (FlexLM) network license manager software documentation. You can easily search across the entire VisualDSP++ documentation set for any topic of interest. For easy printing, supplementary `.PDF` files of most manuals are provided in the `Docs` folder on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
`.CHM`	Help system files and manuals in Help format
`.HTM` or `.HTML`	Dinkum Abridged C++ library and FlexLM network license manager software documentation. Viewing and printing the `.HTML` files requires a browser, such as Internet Explorer 4.0 (or higher).
`.PDF`	VisualDSP++ and processor manuals in Portable Documentation Format (PDF). Viewing and printing the `.PDF` files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

If documentation is not installed on your system as part of the software installation, you can add it from the VisualDSP++ CD at any time by running the Tools installation. Access the online documentation from the VisualDSP++ environment, Windows® Explorer, or the Analog Devices Web site.

Accessing Documentation From VisualDSP++

To view VisualDSP++ Help, click on the **Help** menu item or go to the Windows task bar and navigate to the VisualDSP++ documentation via the **Start** menu.

To view ADSP-BF561 EZ-KIT Lite Help, which is part of the VisualDSP++ Help system, use the **Contents** or **Search** tab of the Help window.

Accessing Documentation From Windows

In addition to any shortcuts you may have constructed, there are many ways to open VisualDSP++ online Help or the supplementary documentation from Windows.

Help system files (`.CHM`) are located in the `Help` folder, and `.PDF` files are located in the `Docs` folder of your VisualDSP++ installation CD-ROM. The `Docs` folder also contains the Dinkum Abridged C++ library and the FlexLM network license manager software documentation.

Your software installation kit includes online Help as part of the Windows® interface. These help files provide information about VisualDSP++ and the ADSP-BF561 EZ-KIT Lite evaluation system.

Accessing Documentation From Web

Download manuals at the following Web site:
`http://www.analog.com/processors/resources/technicalLibrary/manuals`.

Select a processor family and book title. Download archive (`.ZIP`) files, one for each manual. Use any archive management software, such as WinZip, to decompress downloaded files.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**) and follow the prompts.

VisualDSP++ Documentation Set

To purchase VisualDSP++ manuals, call **1-603-883-2430**. The manuals may be purchased only as a kit.

If you do not have an account with Analog Devices, you are referred to Analog Devices distributors. For information on our distributors, log onto `http://www.analog.com/salesdir/continent.asp`.

Hardware Tools Manuals

To purchase EZ-KIT Lite and In-Circuit Emulator (ICE) manuals, call **1-603-883-2430**. The manuals may be ordered by title or by product number located on the back cover of each manual.

Processor Manuals

Hardware reference and instruction set reference manuals may be ordered through the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**), or downloaded from the Analog Devices Web site. Manuals may be ordered by title or by product number located on the back cover of each manual.

Data Sheets

All data sheets (preliminary and production) may be downloaded from the Analog Devices Web site. Only production (final) data sheets (Rev. 0, A, B, C, and so on) can be obtained from the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**); they also can be downloaded from the Web site.

To have a data sheet faxed to you, call the Analog Devices Faxback System at **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. If the data sheet you want is not listed, check for it on the Web site.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

Additional conventions, which apply only to specific chapters, may appear throughout this document.

1 USING EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-BF561 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "Example Programs" on page 1-12
  Provides information about the example programs included in the ADSP-BF561 EZ-KIT Lite evaluation system.
- "Flash Programmer Utility" on page 1-12
  Highlights the advantages of the Flash Programmer utility of VisualDSP++.
- "Background Telemetry Channel" on page 1-13
  Highlights the advantages of the Background Telemetry Channel feature of VisualDSP++.
- "VisualDSP++ Interface" on page 1-13
  Describes the target options facilities of the EZ-KIT Lite system.

For more detailed information about programming the ADSP-BF561 Blackfin processor, see the documents referred to as "Related Documents".

Package Contents

Your ADSP-BF561 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF561 EZ-KIT Lite board
- *VisualDSP++ Installation Quick Reference Card*
- CD containing:
  - VisualDSP++ software
  - ADSP-BF561 EZ-KIT Lite software
  - USB driver files
  - Example programs
  - *ADSP-BF561 EZ-KIT Lite Evaluation System Manual* (this document)

- Universal 7.5V DC power supply
- USB 2.0 cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF561 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before using the board.

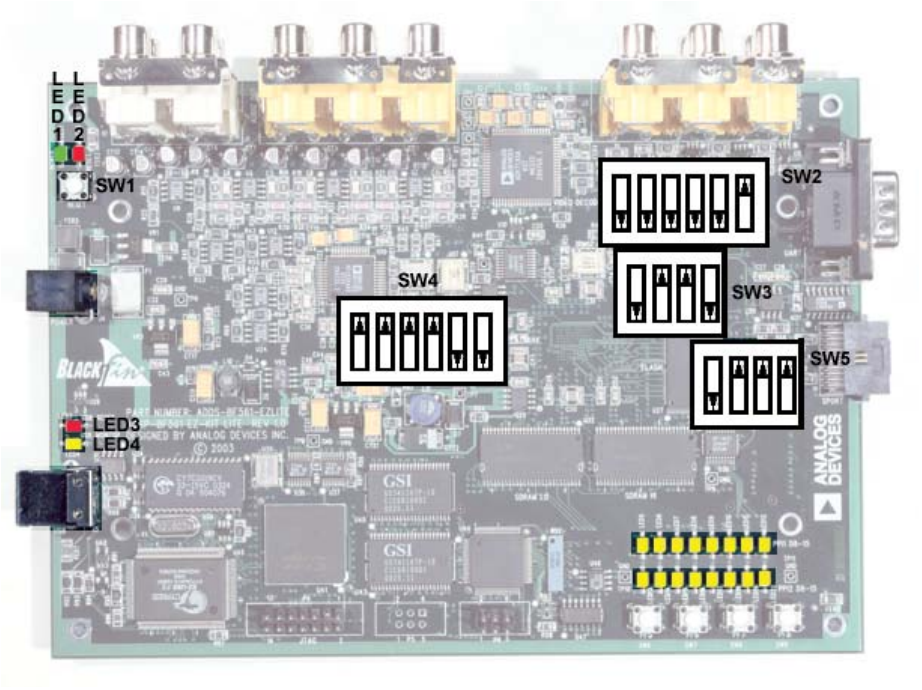

Figure 1-1. EZ-KIT Lite Hardware Setup

Installation and Session Startup

For correct operation, install the software and hardware in the order presented in the *VisualDSP++ Installation Quick Reference Card*.

1. Verify that the yellow USB monitor LED (LED4, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. From the **Start** menu, navigate to the VisualDSP++ environment via the **Programs** menu.
   If you are running VisualDSP++ for the first time, the **New Session** dialog box appears on the screen (skip the rest of the procedure and go to step 3).
   If you have run VisualDSP++ previously, the last opened session appears on the screen.
   To switch to another session, via the **Session List** dialog box, hold down the **Ctrl** key while starting VisualDSP++ (go to step 5).
3. In **Debug target**, select **Blackfin Emulators/EZ-KIT Lites**.
   In **Platform**, select the appropriate EZ-KIT Lite via a debug agent (**ADSP-BF561 EZ-KIT Lite via Debug Agent**).
   In **Session name**, type a new name or accept the default.
4. Click **OK** to return to the **Session List**.
5. Highlight the session and click **Activate**.

Evaluation License Restrictions

The ADSP-BF561 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF561 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a users program to 41 KB of internal memory for code space with no restrictions for data space.

The EZ-KIT Lite hardware must be connected and powered up to use VisualDSP++ with a valid evaluation or permanent license.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

External Memory

EZ-KIT Lite board includes two types of external memory, 64-MB SDRAM and 8-MB flash. Table 1-1 shows the memory map of these devices. The complete configuration of the ADSP-BF561 processor internal SRAM is detailed in Figure 1-2.

Table 1-1. EZ-KIT Lite External Memory Map

Start Address	End Address	Description
0x00000000	0x3FFFFFF	SDRAM Bank 0; see "External Memory" on page 1-6
0x20000000	0x207FFFFF	ASYNC Memory Bank 0; see "External Memory" on page 1-6.
All other locations		Not used

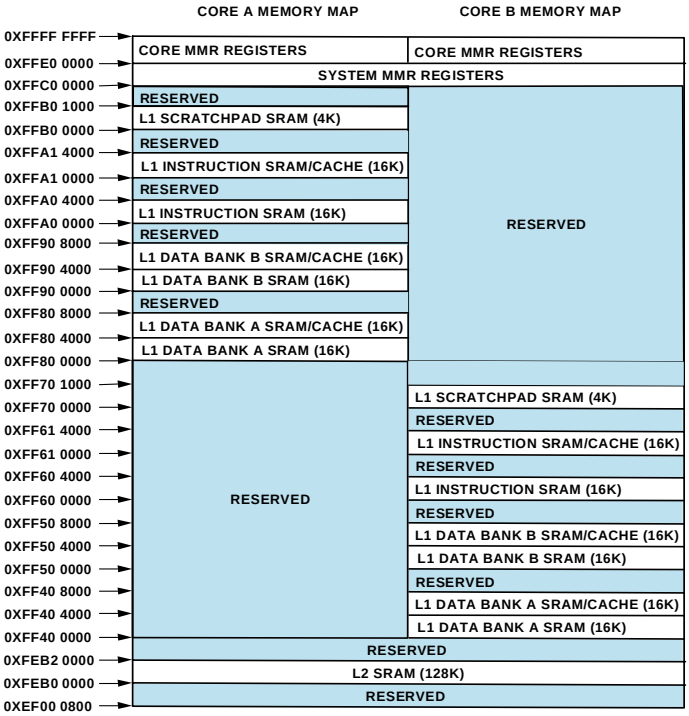

Figure 1-2. ADSP-BF561 Processor Internal Memory Map

The 8 MB of flash memory is organized as 4M x 16 bit and mapped into a ADSP-BF561 processor's ASYNC Memory Bank 0 (~AMS0, memory select signal connects to the flash memory's output enable pin).

The 64 MB of SDRAM is organized as 16M x 32 bits wide. The processor's memory select pin ~SMS0 is configured for the SDRAM. Three SDRAM control registers must be initialized in order to access the SDRAM memory.

When in a VisualDSP++ EZ-KIT Lite session, you can automatically configure the SDRAM registers by selecting the **Use XML reset values** box on the **Target Options** dialog box, which is accessible through the **Settings**

pull-down menu. The values for the EBIU_SDGCTL, EBIU_SDBCTL, and EBIU_SDRRC registers have been set in the ADSP-BF561.xml file found in your VisualDSP\SYSTEM folder under the RegReset tag. These values can be changed to be more optimal depending on the SCLK frequency.

The values in Table 1-2 are programmed by default whenever Bank 0 is accessed through the debugger (for example, when viewing memory windows or loading a program). The numbers are derived for maximum flexibility and work for a system clock frequency between 60 MHz and 133 MHz.

Table 1-2. EZ-KIT Lite Session SDRAM Default Settings

Register	Value	Function
EBIU_SDGCTL	0x0091998D	Calculated with SCLK = 133 MHz
EBIU_SDBCTL	0x00000013	
EBIU_SDRRC	0x000001CF	Calculated with SCLK = 120 MHz

The EBIU_SDGCTL register can only be written once after the processor comes out of reset. Therefore, the user code should not reinitialize this register. Clearing the **Use XML reset values** checkbox allows manual configuration of the EBIU registers. For more information, see "Target Options" on page 1-14.

Automatic configuration of the SDRAM is not optimized for a specific SCLK frequency. Table 1-3 shows the optimized configuration for the SDRAM registers using a 120 MHz SCLK. The frequency of 120 MHz is the maximum SCLK frequency when using a 600 MHz core frequency, the maximum frequency for the EZ-KIT Lite. Only the SDRRC register needs to be modified in the user code to achieve maximum performance.

Table 1-3. SDRAM Optimum Settings[1]

Register	Value
EBIU_SDGCTL	0x0091998D
EBIU_SDBCTL	0x00000013
EBIU_SDRRC	0x000003A0

1 Calculated with SCLK = 120 MHz

For more information about the memory connection on the EZ-KIT Lite, see "External Bus Interface Unit" on page 2-3.

An example program is included in the EZ-KIT installation directory to demonstrate how to set up the SDRAM interface.

LEDs and Push Buttons

The EZ-KIT Lite provides four push buttons and sixteen LEDs for general-purpose IO.

Sixteen LEDs labeled LED5 through LED20 are controlled by the processor's programmable flags PF32 through PF47 (equivalent to PPI0 D15-8 and PPI1 D15-8). These LEDs are accessed through the Flag 2 registers. First, the direction must be configured to output by setting the bits of the FIO2_DIR register to "1". Then the value of the LEDs can be modified using one the FIO2_FLAG_D, FIO2_FLAG_C, FIO2_FLAG_S, or FIO2_FLAG_T registers.

The four general-purpose push buttons are labeled SW6 through SW9. These connect to the programmable flags PF8-5. A status of each individual button can be read through the FIO0_FLAG_D register. When the corresponding bit of the register reads "1", a switch is being pressed-on. When the switch is released, the bit reads "0". A connection between the

push button and PF input is established through the SW4 DIP switch. For information on how to disconnect the switch from the programmable flag and use it for another objective, see "Push Button Enable Switch (SW4)".

An example program is included in the EZ-KIT installation directory to demonstrate the functionality of the LEDs and push buttons.

Audio Interface

The AD1836A audio codec provides three channels of stereo audio output and two channels of multichannel 96 kHz input. The SPORT0 interface of the processor links with the stereo audio data input and output pins of the AD1836A codec. The processor is capable of transferring data to the audio codec in Time-Division Multiplexed (TDM) or Two-Wire Interface (TWI) mode.

The TWI mode allows the codec to operate with a 96 kHz sample rate but restricts the output to two channels. TDM mode can operate at a maximum of 48 kHz sample rate but allows simultaneous use of all input and output channels. When using TWI mode, the TSCLK0 and RSCLK0 pins, as well as the TFS0 and RFS0 pins of the processor, must be tied together externally to the processor. This is accomplished with the SW4 DIP switch. See "Push Button Enable Switch (SW4)" on page 2-12 for more information.

The AD1836A audio codec's internal configuration registers are configured using the processor's PF4 programmable flag pin is used as the select for this device. For more information on how to configure the multichannel codec, download the datasheet from Analog Devices website, www.analog.com.

The AD1836A codec reset is controlled by the processor's programmable flag PF15. When PF15 is "0", the reset is asserted. When PF15 is "1", the reset is de-asserted. Note, when PF15 is not driven (configured as input), the AD1836A reset is asserted due to the pull-down resistor. See "Programmable Flags" on page 2-4 for more information.

Example programs are included in the EZ-KIT installation directory to demonstrate the AD1836A codec operation.

Video Interface

The board supports video input and output applications. The ADV7179 video encoder provides up to three output channels of analog video, while the ADV7183A video decoder provides up to three input channels of analog video. The video encoder connects to the Parallel Peripheral Interface 1 (PPI1), while the video decoder connects to the Parallel Peripheral Interface 0, (PPI0). Each PPI interface has an individual clock that is configured by the SW5 switch settings. See "PPI Clock Select Switch (SW5)" on page 2-13 for more information.

Both the encoder and the decoder connect to the Parallel Peripheral Interfaces (PPI input clock) of the ADSP-BF561 processor. For additional information on the video interface hardware, refer to "PPI Interfaces" on page 2-6.

For the video interface to be operational, the following basic steps must be performed.

1. Configure the SW2 DIP switch as required by the application. Refer to "Video Configuration Switch (SW2)" on page 2-10 for details.
2. De-assert the video device's reset by setting a corresponding programmable flag "High". Note that PF14 controls the ADV7179 encoder's reset, while PF13 controls the ADV7183A decoder's reset.

3. If using the decoder:
   - Enable device by driving programmable flag output `PF2` to "`0`".
   - Select `PPI0` clock; for details, refer to "PPI Clock Select Switch (SW5)" on page 2-13.
4. Program internal registers of the video device in use. Both video encoder and decoder use a 2-wire serial interface to access internal registers. The `PF0` programmable flag functions as a serial clock (SCL), and `PF1` functions as a serial data (SDAT).
5. Program the ADSP-BF561 processor's PPI interfaces (configuration registers, DMA, and so on).

Example programs are included in the EZ-KIT installation directory to demonstrate the capabilities of the video interface.

Example Programs

Example programs are provided with the ADSP-BF561 EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in the `\...\Blackfin\EZ-KITs\ADSP-BF561\Examples` subdirectory of the VisualDSP++ installation directory. Please refer to the readme file provided with each example for more information.

Flash Programmer Utility

The ADSP-BF561 EZ-KIT Lite evaluation system includes a Flash Programmer utility. The utility allows you to program the flash memory on the EZ-KIT Lite. The Flash Programmer is installed with VisualDSP++. Once the utility is installed, it is accessible from the **Tools** pull-down menu.

The Flash Programmer driver is core-specific (core A) and must be loaded to the core A in order to operate correctly. The Flash Programmer relies on the user to set the correct core focus. To set up the correct core, select the core A in the multiprocessor window before opening the Flash Programmer interface.

For more information on the Flash Programmer utility, refer to the online Help.

Background Telemetry Channel

The ADSP-BF561 USB debug agent supports the Background Telemetry Channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting processor execution.

The BTC allows to view a variable as it is updated or changed, all while the processor continues to execute. For increased performance of the BTC, including faster reading and writing, please check out our latest line of processor emulators at `www.analog.com/Analog_Root/productPage/productHome/0,2121,EMULATORS,00.html`. For more information about the Background Telemetry Channel, see the *VisualDSP++ User's Guide* or online Help.

VisualDSP++ Interface

This section provides information on the following parts of the VisualDSP++ graphical user interface:

- "Target Options" on page 1-14
- "Restricted Software Breakpoints" on page 1-17

Target Options

Choosing **Target Options** from the **Settings** menu opens the **Target Options** dialog box (Figure 1-3). Use target options to control certain aspects of the processor on the ADSP-BF561 EZ-KIT Lite evaluation system.

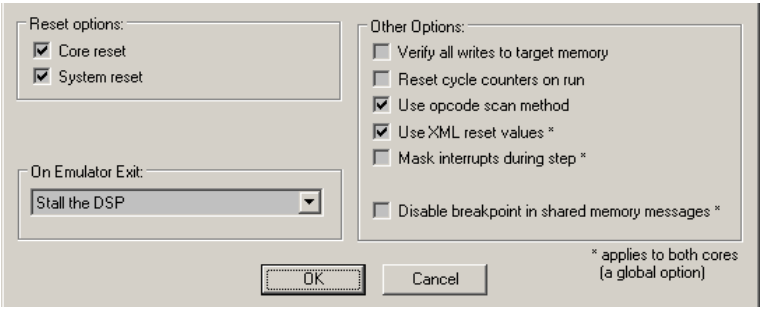

Figure 1-3. Target Options Dialog Box

Reset Options

Reset options control how the processor behaves when a reset occurs. The reset options are described in Table 1-4.

Table 1-4. Reset Options

Option	Description
Core reset	Resets the core when the debugger executes a reset. Note that a core reset of either core effects both cores as does a system reset.
System reset	Resets the peripherals when the debugger executes a reset.

On Emulator Exit

This target option controls processor behavior when VisualDSP++ relinquishes processor control (for example, when exiting VisualDSP++). The option is described in Table 1-5.

Table 1-5. On Emulator Exit Target Options

Option	Description
On Emulator Exit	Determines the state the processor is left in when the board relinquishes control of the processor: **Reset DSP and Run** causes the processor to reset and begin execution from its reset vector location. **Run from current PC** causes the processor to begin running from its current location. **Stall the DSP** resets the processor and then writes a `JUMP 0` to the first location in internal memory so the processor is stuck in a tight loop after exiting.

XML File

These read-only fields show the version information for the processor-specific XML file, in the `\...\SYSTEM\ADSP-BF561.xml` subdirectory of the VisualDSP++ installation directory, as well as the parser program (Table 1-6).

Table 1-6. XML File Information

Option	Description
XML File Version	The version of the processor's XML file.
XML Parser Version	The version of the program that parses the XML file.

Other Options

Table 1-7 describes other available target options.

Table 1-7. Miscellaneous Target Options

Option	Description
Verify all writes to target memory	Validates all memory writes to the processor. After each write, a read is performed and the values are checked for a matching condition. Enable this option during initial program development to locate and fix initial build problems (such as attempting to load data into non-existent memory). Clear this option to increase performance while loading executable files, since VisualDSP++ does not perform the extra reads that are required to verify each write.
Reset cycle counters on run	Resets the cycle count registers to zero before a **Run** command is issued. Select this option to count the number of cycles executed between breakpoints in a program.
Use opcode scan method	Enables the debugger to use a highly optimized JTAG scan method. This provides extremely fast communication between the EZ-KIT Lite and the processor. In certain circumstances, this causes JTAG scan failures. Typically, JTAG scan failures occur when using this method combined with debugging situations that hold off or stall the core (such as debugging, loading, or viewing external memory). Clearing this option uses a less optimized JTAG scan method.
Use XML reset values	Uses a section in the processor-specific `.XML` file located in the installation's `system` folder. The file defines registers that are reset to certain values; the values are read at startup and subsequently used to set the registers when a reset is performed through VisualDSP++. Applies to both processors.
Mask interrupts during step	Disables interrupts while single stepping through code. Applies to both processors.
Disable breakpoints in shared memory messages	Suppress a warning message caused by setting a breakpoint in shared memory. Applies to both processors.

Restricted Software Breakpoints

The EZ-KIT Lite development system restricts breakpoint placement when certain conditions are met. That is, under some conditions, breakpoints cannot be placed effectively. Such conditions depend on bus architecture, pipeline depth, and ordering of the EZ-KIT Lite and its target processor.

2 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF561 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the configuration of the ADSP-BF561EZ-KIT Lite and explains how the board components interface with the processor.
- "Jumper and DIP Switch Settings" on page 2-10
  Shows the location and describes the function of the configuration jumpers and switches.
- "LEDs and Push Buttons" on page 2-14
  Shows the location and describes the function of the LEDs and push buttons.
- "Connectors" on page 2-17
  Shows the location and gives the part number for all of the connectors on the board. Also, the manufacturer and part number information is given for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

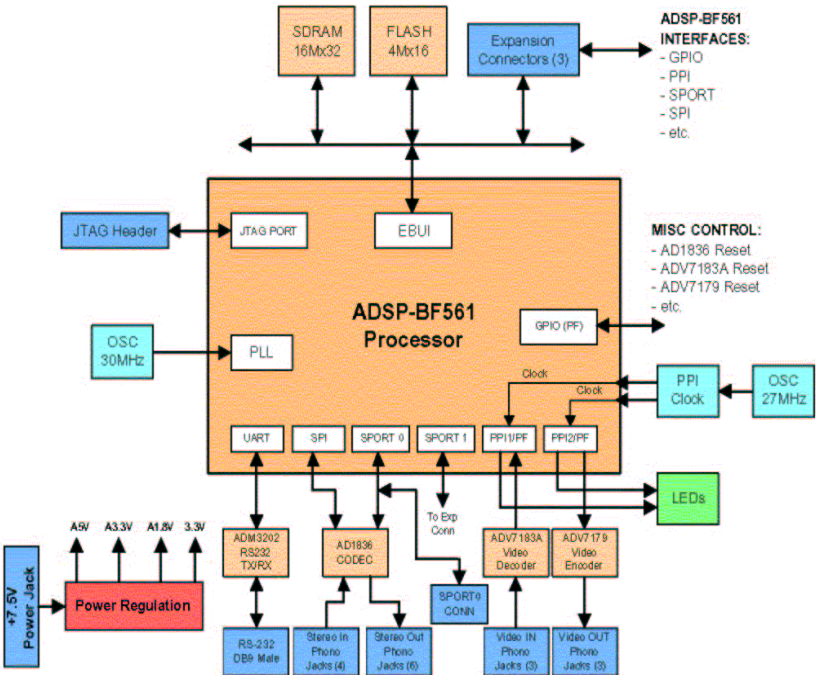

Figure 2-1. System Architecture

The EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-BF561 Blackfin processor. The processor has IO voltage of 3.3V. The core voltage and the core clock rate can be set on the fly by the processor. The input clock is 30 MHz.

External Bus Interface Unit

The External Bus Interface Unit (EBIU) connects an external memory to the ADSP-BF561 processor. It includes a 32-bit wide data bus, an address bus (A25-A2), and a control bus. All 8-bit, 16-bit, and 32-bit accesses are supported. On the EZ-KIT Lite board, the EBI unit is connected to SDRAM and flash memory. For more information on using the external memory see "External Memory" on page 1-6.

All of the address, data, and control signals are available externally via the extender connectors (J3-J1). The pinout of these connectors can be found in Appendix B, "Schematics" on page B-1.

SPORT0 Audio Interface

The SPORT0 interface connects to the AD1836A audio codec, the SPORT connector (P3), and the expansion interface. The AD1836A codec uses both the primary and secondary data transmit and receive pins to input and output data from the audio input and outputs.

The pinout of the SPORT connector and the expansion interface connectors can be found in Appendix B, "Schematics" on page B-1.

SPI Interface

The processor's Serial Peripheral Interconnect (SPI) interface connects to the AD1836A audio codec and the expansion interface. The SPI connection to the AD1836A is used to access the control registers of the device. The PF4 flag of the processor acts as the devices select for the SPI port.

The SPI signals are available on the expansion interface. The pinout for the expansion interface can be found in Appendix B, "Schematics" on page B-1.

Programmable Flags

The processor has 48 programmable flag pins (PFs). Many of the flags have a multiple functionality, depending on the processor's setup. Table 2-1 shows how the programmable flag pins are used on the EZ-KIT Lite.

Table 2-1. Programmable Flag Connections

Processor PF Pin	Processor Function	EZ-KIT Function
PF0	SPI Select S, Timer 0	Serial clock for programming ADV7179 video encoder and ADV7183A video decoder.
PF1	SPI Select 1, Timer 1	Serial data for programming ADV7179 video encoder and ADV7183A video decoder.
PF2	SPI Select 2, Timer 2	ADV7183A video decoder's ~OE.
PF3	SPI Select 3, Timer 3	ADV7183A Field pin. See "Video Configuration Switch (SW2)" on page 2-10.
PF4	SPI Select 4, Timer 4	AD1836A audio codec's SPI Select.
PF5	SPI Select 5, Timer 5	Push Button (SW6). See "LEDs and Push Buttons" on page 1-9 and "Push Button Enable Switch (SW4)" on page 2-12 for information on how to disable the push button.
PF6	SPI Select 6, Timer 6	Push Button (SW7). See "LEDs and Push Buttons" on page 1-9 and "Push Button Enable Switch (SW4)" on page 2-12 for information on how to disable the push button.
PF7	SPI Select 7, Timer 7	Push Button (SW8). See "LEDs and Push Buttons" on page 1-9 and "Push Button Enable Switch (SW4)" on page 2-12 for information on how to disable the push button.
PF8		Push Button (SW9). See "LEDs and Push Buttons" on page 1-9 and "Push Button Enable Switch (SW4)" on page 2-12 for information on how to disable the push button.

Table 2-1. Programmable Flag Connections (Cont'd)

Processor PF Pin	Processor Function	EZ-KIT Function
PF9-PF12		Not used
PF13		ADV7183A video decoder's reset
PF14		ADV7179 video encoder's reset
PF15		AD1836 codec's reset
PF16		Sport 0 Transmit Frame Sync
PF17		Sport 0 Transmit Data Secondary
PF18		Sport 0 Transmit Data Primary
PF19		Sport 0 Receive Frame Sync
PF20		Sport 0 Receive Data Secondary
PF21		Sport 1 Transmit Frame
PF22		Sport 1 Transmit Data Secondary
PF23		Sport 1 Transmit Data Primary
PF24		Sport 1 Receive Frame Sync
PF25		Sport 1 Receive Data Secondary
PF26		UART Transmit
PF27		UART Receive
PF28		Sport 0 Receive Serial Clock
PF29		Sport 0 Transmit Serial Clock
PF30		Sport 1 Receive Serial Clock
PF31		Sport 1 Transmit Serial Clock
PF39-32	PPI1 data 15-8	LED20-13
PF47-40	PPI0 data 15-8	LED12-5

PPI Interfaces

The ADSP-BF561 processor employs two independent Parallel Peripheral Interfaces (PPIs), PPI0 and PPI1. Each PPI interface is a half-duplex, bi-directional bus consisting of 16 bits of data, a dedicated input clock, and synchronization signals. The ADSP-BF561 EZ-KIT Lite board utilizes the PPI interfaces for video input and video output.

The PPI0 interface is configured to input video data from the ADV7183A video decoder device: bits 7-0 connect to the video decoder's data outputs. The PPI1 interface is configured to output video data to the ADV7179 video encoder device: bits 7-0 connect to the video encoder's data inputs.

Each PPI interface has a dedicated clock input configured independently by the SW5 switch. The clock source can be one of the following: 27 MHz crystal oscillator, ADV7183A video decoder's clock output, or external clock from the expansion interface. See "PPI Clock Select Switch (SW5)" on page 2-13 for more information about the switch.

The SW2 switch allows flexible connectivity between dedicated synchronization IOs (SYNC1 and SYNC2 of each PPI interface) and the encoder's and decoder's horizontal and vertical synchronization pins. See "Video Configuration Switch (SW2)" on page 2-10 for more information about the switch. For a detailed description of the ADSP-BF561 processor's PPI interfaces, refer to the *ADSP-BF561 Blackfin Processor Hardware Reference*.

Table 2-2 describes the PPI pins and their use on the EZ-KIT Lite board.

Table 2-2. PPI Connections

Processor PPI Pin	Other PRocessor Function	EZ-KIT Function
PPI0 bits 7-0		ADV7183A data outputs P15-8
PPI1 bits 7-0		ADV7179 data inputs P7-0
PPI0 SYNC1	Timer 8	ADV7179 HSYNC. For more information, see "Video Configuration Switch (SW2)" on page 2-10.

Table 2-2. PPI Connections (Cont'd)

Processor PPI Pin	Other PRocessor Function	EZ-KIT Function
PPI0 SYNC2	Timer 9	ADV7179 VSYNC. For more information, see "Video Configuration Switch (SW2)" on page 2-10.
PPI0 Clock		A choice of ADV7183A output clock, a local 27 MHz oscillator, or an external clock from ADSP-BF533/BF561 EZ-KIT Extender 1 board.
PPI1 SYNC1	Timer 10	ADV7183A HSYNC. For more information, see "Video Configuration Switch (SW2)" on page 2-10.
PPI1 SYNC2	Timer 11	ADV7183A VSYNC. For more information, see "Video Configuration Switch (SW2)" on page 2-10.
PPI1 Clock		A choice of ADV7183A output clock, a local 27 MHz oscillator, or an external clock from ADSP-BF53x/BF561 EZ-Extender 1.

Video Output (PPI1)

The PPI1 interface is configured as output and connects to the on-board video encoder device, ADV7179. The ADV7179 encoder generates three analog video channels on DAC A, DAC B, and DAC C. The PPI1 bits 7-0 connect to P7-0 of the encoder's pixel inputs. The encoder's input clock is fixed and comes from an on-board 27 MHz oscillator.

The encoder's synchronization signals, HSYNC and VSYNC, can be configured as inputs or outputs. Video Blanking control signal is at level "1". The HSYNC and VSYNC signals can connect to the ADSP-BF561 processor's PPI1 interface SYNC1 and SYNC2 via the SW2 switch, as described in "Video Configuration Switch (SW2)" on page 2-10.

Video Input (PPI0)

The PPI0 interface is configured as input and connect to the on-board video decoder device, ADV7183A. The ADV7183A decoder receives three analog video channels on AIN1, AIN4, and AIN5 input. The decoder's pixel data outputs P15-8 drive the PPI0 inputs 8-0. The decoder's 27 MHz pixel clock output can be selected to drive any of the PPI clocks, as shown in Table 2-7 on page 2-13.

Synchronization outputs of the decoder, HS/HACTIVE, VS/VACTIVE, and FIELD can connect to the processor's PPI1 SYNC1, SYNC2, and PF3 flag via the SW2 DIP switch, as described in "Video Configuration Switch (SW2)" on page 2-10.

UART Port

The processor's Universal Asynchronous Receiver/Transmitter (UART) port connects to the ADM3202 RS232 line driver as well as to the expansion interface. The RS232 line driver is attached to the DB9 male connector, allowing you to interface with a PC or other serial device.

Expansion Interface

The expansion interface consists of the three 90-pin connectors, J3-1. Table 2-3 shows the interfaces each connector provides. For the exact pinout of these connectors, refer to Appendix B, "Schematics" on page B-1. The mechanical dimensions of the connectors can be obtained from Technical or Customer Support.

Table 2-3. Connector Interfaces

Connector	Interfaces
J1	5V, G ND, Address, Data, PPI0 3-0, PF15-6, PF4
J2	3.3V, GND, SPI, NMI, PPI0 SYNC3-1, SPORT0, SPORT1, PF15-0, EBUI control signals
J3	5V, 3.3V, GND, UART, PPI1 15-0, Reset, Video control signals

Limits to the current and to the interface speed must be taken into consideration when you use the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a 6-pin interface. The JTAG emulation port of the processor also connects to the USB debugging interface. When an emulator connects to the board at P4, the USB debugging interface is disabled. See "JTAG (P4)" on page 2-20 for more information about the JTAG connector.

To learn more about available emulators, contact Analog Devices (see "Product Information").

Jumper and DIP Switch Settings

This section describes the operation of the jumpers and DIP switches. The jumper and DIP switch locations are shown in Figure 2-2.

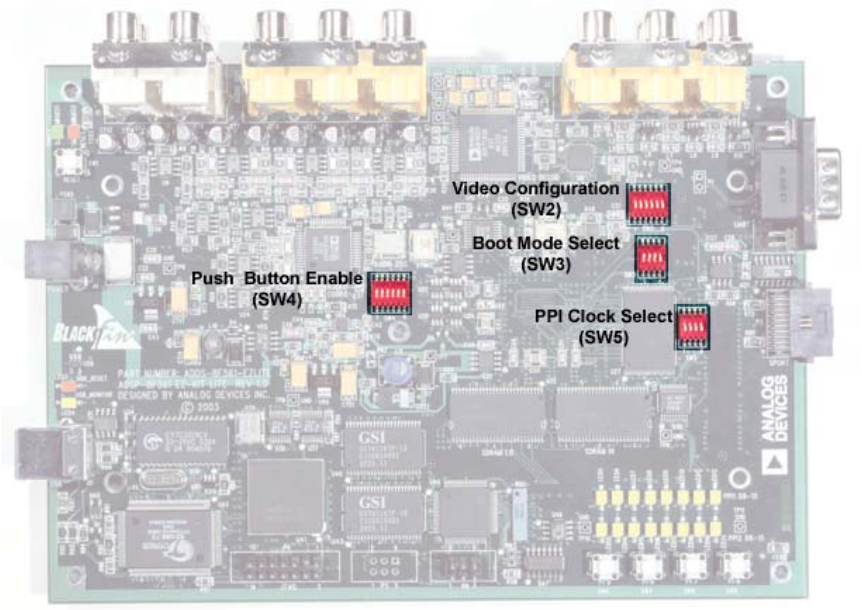

Figure 2-2. DIP Switch Locations

Video Configuration Switch (SW2)

The video configuration switch (SW2) controls how some video signals from the ADV7183A video decoder and ADV7179 video encoder are routed to the processor's PPIs. The switch also determines if the PF2 pin controls the ~OE signal of the ADV7183A video decoder outputs. Table 2-4 shows which processor's signals are connected to the encoder and decoder when in the "ON" position.

Table 2-4. Video Configuration Switch (SW2)

Switch Position (Default)	Processor Signal	Video Signal
1 (OFF)	PPI1 SYNC1	ADV7179
2 (OFF)	PPI0 SYNC1	ADV7183A
3 (OFF)	PPI1 SYNC2	ADV7183A
4 (OFF)	PPI1 SYNC2	ADV7179
5 (OFF)	PF3 (FIELD)	ADV7183A
6 (ON)	PF2	ADV7183A

Positions 1 thorough 5 of SW2 determine how and if the SYNC1, SYNC2, and FIELD control signals of the PPI0 and PPI1 interfaces are routed to the processor's PPIs. In standard configuration of the encoder and decoder, this is not necessary because the processor is capable of reading the embedded control information, which is in the data stream.

Position 6 of SW2 determines whether PF2 connects to the ~OE signal of the ADV7183A. When the switch is "OFF", PF2 can be used for other operations, and the decoder output enable is held "HIGH" with a pull-up resistor.

Boot Mode Switch (SW3)

The SW3 switch positions 1 and 2 set the ADSP-BF561 processor's boot mode as described in Table 2-5. Position 3 sets the processor's PLL on boot. When SW3 position 3 is "ON", the PLL is in bypass.

Table 2-5. Boot Mode Select Switch (SW3)

Position 1 BMODE0	Position 2 BMODE1	Boot Mode
ON	ON	Reserved
ON	OFF	Flash memory

Table 2-5. Boot Mode Select Switch (SW3) (Cont'd)

Position 1 BMODE0	Position 2 BMODE1	Boot Mode
OFF	ON	8-bit SPI PROM
OFF	OFF	16-bit SPI PROM

Push Button Enable Switch (SW4)

The push button enable switch (SW4) positions 1 through 4 allow to disconnect the drivers associated with the push buttons from the PF pins of the processor. Positions 5 and 6 connect the transmit and receive frame syncs and clocks of SPORT0. This is important when the AD1836A video decoder and the processor are communicating in Two-Wire Interface (TWI) mode. Table 2-6 shows which PF is driven when the switch is in the "ON" position.

Table 2-6. Push Button Enable Switch (SW4)

Switch Position	Default Setting	Pin #	Signal (Side 1)	Pin #	Signal (Side 2)
1	ON	1	SW6	12	PF5
2	ON	2	SW7	11	PF6
3	ON	3	SW8	10	PF7
4	ON	4	SW9	9	PF8
5	OFF	5	TFS0	8	RFS0
6	OFF	6	RSCLK0	7	TSCLK0

PPI Clock Select Switch (SW5)

The SW5 switch controls a clock selection of PPI interfaces, as described in Table 2-7 and Table 2-8.

Table 2-7. PPICLK1 Clock Source Setup

SW5 Position 1 PPI0_CKSEL0	SW5 Position 2 PPI0_CKSEL1	PPICLK1 Source
ON	ON	27 MHz Oscillator (default)
OFF	ON	ADV7183 Clock Out
X	OFF	Expansion Interface

Table 2-8. PPICLK2 Clock Source Setup

SW5 Position 3 PPI1_CKSEL0	SW5 Position 4 PPI1_CKSEL1	PPICLK2 Source
ON	ON	27 MHz Oscillator (default)
OFF	ON	ADV7183 Clock Out
X	OFF	Expansion Interface

Test DIP Switches (SW10 and SW11)

Two DIP switches (SW10 and SW11) are located on the bottom of the board. The switches are used only for testing and should be in the "OFF" position.

LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 2-3 shows the locations of the LEDs and push buttons on the board.

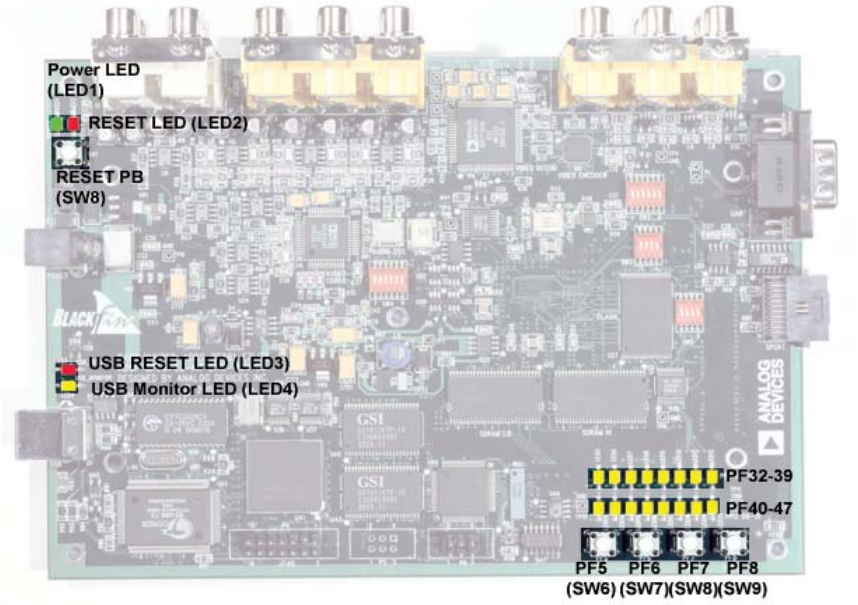

Figure 2-3. LED and Push Button Locations

Reset Push Button (SW1)

The RESET push button resets all of the ICs on the board. One exception is the USB interface chip (U34). The chip is not being reset when the push button is pressed after the USB cable has been plugged in and communication with the PC has been initialized correctly. Once communication is initialized, the only way to reset the USB is by powering down the board.

Programmable Flag Push Buttons (SW9–6)

Four push buttons, SW9-6, are provided for general-purpose user input. The buttons connect to the processor's programmable flag pins PF8-5. The push buttons are active "HIGH" and, when pressed, send a High (1) to the processor. Refer to "LEDs and Push Buttons" on page 1-9 for more information on how to use the PFs when programming the processor. The push button enable switch (SW4) is capable of disconnecting the push buttons from the PF (refer to "Push Button Enable Switch (SW4)" on page 2-12). The programmable flag signals and their corresponding switches are shown in Table 2-9.

Table 2-9. Programmable Flag Switches

Processor Programmable Flag Pin	Push Button Reference Designator
PF5	SW6
PF6	SW7
PF7	SW8
PF8	SW9

Power LED (J7)

When J7 is lit (green), it indicates that power is being properly supplied to the board.

Reset LEDs (LED2 and LED3)

When LED2 is lit, it indicates that the master reset of all the major ICs is active. When LED3 is lit, the USB interface chip (U34) is being reset. The USB chips only reset on power-up, or if USB communication has not been initialized.

USB Monitor LED (LED4)

The USB monitor LED (LED4) indicates that USB communication has been initialized successfully and you may connect to the processor using a VisualDSP++ EZ-KIT Lite session. This should take approximately 15 seconds. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver.

When VisualDSP++ is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

User LEDs (LED12–5, LED20–13)

Sixteen LEDs are connected to the ADSP-BF561 processor's programmable flags. Eight LEDs labeled LED5 through LED12 are controlled by programmable flags PF40 through PF47 (equivalent to PPI0 D15-8). Eight LEDs labeled LED13 through LED20 are controlled by programmable flags PF32 through PF39 (equivalent to PPI1 D15-8). To learn how to use the flash memory when programming the LEDs, refer to "LEDs and Push Buttons" on page 1-9.

Table 2-10. User LEDs

LED Reference Designator	Flash Port Name	LED Reference Designator	Flash Port Name
LED5	PB40	LED13	PB32
LED6	PB41	LED14	PB33
LED7	PB42	LED15	PB34
LED8	PB43	LED16	PB35
LED9	PB44	LED17	PB36
LED10	PB45	LED18	PB37
LED11	PB46	LED19	PB38
LED12	PB47	LED20	PB39

Connectors

This section describes the connector functionality and provides information about mating connectors. The locations of the connectors are shown in Figure 2-4.

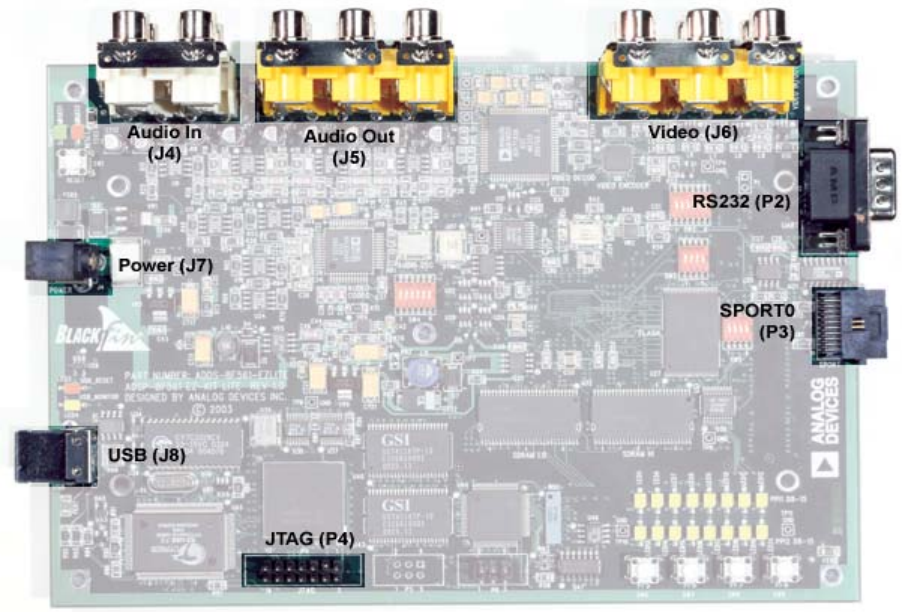

Figure 2-4. Connector Locations

Expansion Interface (J3–1)

Three board-to-board connector footprints provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the expansion interface, see on page 2-8. For the availability and pricing of the J1, J2, and J3 connectors, contact Samtec.

Part Description	Manufacturer	Part Number
90 Position 0.05" Spacing, SMT (J1, J2, J3)	Samtec	SFC-145-T2-F-D-A
Mating Connector		
90 Position 0.05” Spacing (Through Hole)	Samtec	TFM-145-x1 Series
90 Position 0.05” Spacing (Surface Mount)	Samtec	TFM-145-x2 Series
90 Position 0.05” Spacing (Low Cost)	Samtec	TFC-145 Series

Audio (J4 and J5)

Part Description	Manufacturer	Part Number
2x2 RCA Jacks (J4)	SWITCHCRAFT	PJRAS2X2S01
3x2 RCA Jacks (J5)	SWITCHCRAFT	PJRAS3X2S01
Mating Connector		
Two channel RCA interconnect cable	Monster Cable	BI100-1M

Video (J6)

Part Description	Manufacturer	Part Number
3x2 RCA Jacks (J6)	SWITCHCRAFT	PJRAS3X2S01

Power (J7)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board. The power connector supplies DC power to the board. The following table shows the power connector pinout.

Part Description	Manufacturer	Part Number
2.5 mm Power Jack (J7)	SWITCHCRAFT	RAPC712
	Digi-Key	SC1152-ND
Mating Power Supply (shipped with EZ-KIT Lite)		
7.5V Power Supply	GlobTek	TR9CC2000LCP-Y

The power connector supplies DC power to the EZ-KIT Lite board. Table 2-11 shows the power supply specifications.

Table 2-11. Power Supply Specification

Terminal	Connection
Center pin	+7.5 VDC@3Amps
Outer Ring	GND

USB (J8)

The USB connector is a standard Type B USB receptacle.

Part Description	Manufacturer	Part Number
Type B USB receptacle (J8)	Mill-Max	897-30-004-90-000
	Digi-Key	ED90003-ND
Mating Assembly		
USB cable (provided with kit)	Assmann	AK672-5
	Digi-Key	AK672-5ND

RS232 (P2)

The RS232-compatible connector is described in Table 2-12.

Table 2-12. RS232 Connector

Part Description	Manufacturer	Part Number
DB9, Male, Right Angle (P2)	Digi-Key	A2096-ND
Mating Assembly		
2m Female to Female cable	Digi-Key	AE1016-ND

SPORT0 (P3)

The SPORT0 connector is linked to a 20-pin connector. The connector's pinout can be found in "Schematics" on page B-1. For pricing and availability of the connectors, contact AMP.

Part Description	Manufacturer	Part Number
20-position AMPMODU system 50 receptacle (P3)	AMP	104069-1
Mating Connectors		
20-position ribbon cable connector	AMP	111196-4
20-position AMPMODU system 20 connector	AMP	2-487937-0
20-position AMPMODU system 20 connector (w/o lock)	AMP	2-487938-0
Flexible film contacts (20 per connector)	AMP	487547-1

JTAG (P4)

The JTAG header is the connecting point for a JTAG in-circuit emulator

pod. When an emulator is connected to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

A BILL OF MATERIALS

The bill of materials corresponds to the board schematics on page B-1. Please check the latest schematics on the Analog Devices website, http://www.analog.com/Processors/Processors/DevelopmentTools/technicalLibrary/manuals/DevToolsIndex.html#Evaluation%20Kit%20Manuals.

Ref.#	Description	Reference Designator	Manufacturer	Part Number
1	10MHZ SMT OSC003 3V	U35	RALTRON	C04310-10.00
2	74LVC14A SOIC14 HEX-INVER-SCHMITT-TRIGGER	U47	TI	74LVC14AD
3	IDT74FCT3244APY SSOP20 3.3V-OCTAL-BUFFER	U13,U30	IDT	IDT74FCT3244APY
4	CY7C64603-128 PQFP128 USB-TX/RX MICROCONTROLLER	U45	CYPRESS	CY7C64603-128NC
5	MMBT4401 SOT-23 NPN TRANSISTOR 200MA	Q1	FAIRCHILD	MMBT4401
6	ADP3331ART SOT23-6 ADJ 200MA REGULATOR	VR7	ANALOG DEVICES	ADP3331ART
7	CY7C1019BV33-15VC SOJ32 128K X 8 SRAM	U38	CYPRESS	CY7C1019BV33-12VC
8	12.0MHZ THR OSC006 CRYSTAL	Y1	DIG01	300-6027-ND
9	DSM2150F5V TQFP80 FLASH-ICP	U44	ST MICRO	DSM2150F5V
10	SN74AHC1G00 SOT23-5 SINGLE-2-INPUT-NAND	U28,U34,U39,U42	TI	SN74AHC1G00DBVR

Ref.#	Description	Reference Designator	Manufacturer	Part Number
11	12.288MHZ SMT OSC003 TS201/21262	U16	DIG01	SG-8002CA-PCC-ND
12	LT1765 SO-8 ADJUSTABLE-3A-SWITCH-REG	VR5	LINEAR TECH	LT1765ES8
13	GS74116 TSOP44 256Kx16 SRAM	U40,U43	GSI TECHNOL-OGY	GS74116ATP-10
14	NDS8434A SO-P-MOSFET	U29	FAIRCHILD SEMI	NDS8434A
15	MT48LC16M16A2TG-75 TSOP54 256MB-SDRAM	U32-33	MICRON	MT48LC16M16A2TG-75
16	27MHZ SMT OSC003	U17	EPSON	SG-8002CA MP
17	XC2S150E FT256 XILINX-SPARTANIIE-FPGA	U41	XILINX	XC2S150E-7FT256C
18	IDT2305-1DC SOIC8 1 TO 5 ZERO DELAY CLK BUF	U19-20	INTEGRATED SYS	ICS9112AM-16
19	SN74LVC1G32 SOT23-5 SINGLE-2 INPUT OR GATE	U10	TI	SN74LVC1G32DBVR
20	M29W64OD TSOP48 64MBIT 8/16-BIT FLASH MEM	U27	ST MICRO	M29W640DT 90N1
21	30.0000MHZ SMT OSC003 OSCILLATOR	U14	EPSON	SG-8002CA30.000M

Ref.#	Description	Reference Designator	Manufacturer	Part Number
22	BF561 24LC32 “U31” SEE 1000220	U31	MICROCHIP	24LC32A-I/SN “U31”
23	1000pF 50V 5% 1206 CERM	C153,C160	AVX	12065A102JAT2A
24	2200pF 50V 5% 1206 NPO	C46,C76-81	AVX	12065A222JAT050
25	ADM708SAR SOIC8 VOLTAGE-SUPERVISOR	U46	ANALOG DEVICES	ADM708SAR
26	ADP3338AKC-33 SOT-223 3.3V-1.0AMP REGULATOR	VR3	ANALOG DEVICES	ADP3338AKC-3.3
27	ADP3339AKC-5 SOT-223 5V-1.5A REGULATOR	VR1	ANALOG DEVICES	ADP3339AKC-5-REEL
28	ADP3339AKC-33 SOT-223 3.3V 1.5A REGULATOR	VR6	ANALOG DEVICES	ADP3339AKC-3.3-RL
29	ADP3336ARM MSOP8 ADJ 500MA REGULATOR	VR2,VR4	ANALOG DEVICES	ADP3336ARM-REEL
30	10MA AD1580BRT SOT23D 1.2V-SHUNT-REF	D1	ANALOG DEVICES	AD1580BRT
31	ADG752BRT SOT23-6 CMOS-SPDT-SWITCH	U22-23,U25-26	ANALOG DEVICES	ADG752BRT
32	AD8061ART SOT23-5 300MHZ-AMP	U1-3	ANALOG DEVICES	AD8061ART-REEL

Ref.#	Description	Reference Designator	Manufacturer	Part Number
33	ADM3202ARN SOIC16 RS232-TXRX	U21	ANALOG DEVICES	ADM3202ARN
34	AD8606AR SOIC8 OPAMP	U5-7,U9,U11-12,U1,U24	ANALOG DEVICES	AD8606AR
35	AD1836AAS MQFP52 MULTI-CHAN-NEL-96KHZ-CODEC	U15	ANALOG DEVICES	AD1836AAS
36	ADSP-BF561SKBC-600 256 DUEL BLACKFIN DSP	U48	ANALOG DEVICES	ADSP-BF561SKBC-600
37	ADV7179 LFCSP40 VIDEO ENCODER	U8	ANALOG DEVICES	ADV7179KCP
38	ADV7183AKST LQFP80	U4	ANALOG DEVICES	ADV7183AKST
39	RUBBER FEET BLACK	MH1-5	MOUSER	517-SJ-5018BK
40	PWR2.5MM_JACKCON005RA	J7	SWITCHCRAFT	SC1152-ND12
41	USB 4PIN CON009 USB	J8	MILL-MAX	897-30-004-90-000000
42	RCA 2X2 CON013	J4	SWITCHCRAFT	PJRAS2X2S01
43	.05 10X2 CON014 RA	P3	AMP	104069-1
44	SPST-MOMENTARYSWT0136MM	SW1,SW6-9	PANASONIC	EVQ-PAD04M

Ref.#	Description	Reference Designator	Manufacturer	Part Number
45	DIP12 SWT014	J7	DIGI-KEY	CKN3063-ND
46	0.05 45X2 CON019 SMT SOCKET	J1-3	SAMTEC	SFC-145-T2-F-D-A
47	DIP6 SWT017	SW2,SW4,SW10	DIG01	CKN1364-ND
48	RCA 3X2 CON024 RA	J5-6	SWITCHCRAFT	PJRAS3X2S01
49	DIP4 SWT018 4PIN-SMT-SWT	SW3,SW5,SW11	DIG01	CKN1363-ND
50	0.00 1/8W 5% 1206	R43-44, R55, R71-73, R80, R90, R133,R159, R163, R223-225, R228, R247	YAGEO	0.0ECT-ND
51	AMBER-SMT LED001 GULL-WING	LED4-20	PANASONIC	LN1461C-TR
52	330pF 50V 5% 805 NPO	C82,C84,C86,C92-100	AVX	08055A331JAT

Ref.#	Description	Reference Designator	Manufacturer	Part Number
53	0.01uF 100V 10% 805 CERM	C3, C5, C28, C41, C49, C69-70, C74-75, C101,C112-114,C127,C134, C136-138, C140-141, C146, C149-150, C154, C156-157, C165-166, C168, C173-174, C176, C180-182, C185-188, C190, C200-203, C249, C256	AVX	08051C103KAT2A
54	0.22uF 25V 10% 805 CERM	C104, C106-108, C125, C129, C143, C162	AVX	08053C224FAT
55	0.1uF 50V 10% 805 CERM	C1-2, C4, C12, C19-20, C22, C27, C29-30, C35, C37, C48, C51-60, C65-66, C71, C73, C83, C85, C87-91, C102, C109-111, C115, C122-124, C126, C131-132, C135, C139, C145, C147-148, C151-152, C155, C158-159, C164,C167,C171-172,C175, C177-179, C183-184, C189, C191, C233, C236, C241	AVX	08055C104KAT
56	0.001uF 50V 5% 805 NPO	C23,C25,C33,C36, C38-40,C67-68,	AVX	08055A102JAT2A
57	10uF 16V 10% C TANT	CT17-18,CT20-21, CT23-24	SPRAGUE	293D106X9016C2T

Ref.#	Description	Reference Designator	Manufacturer	Part Number
58	10K 100MW 5% 805	R2, R7, R11-12, R14, R24, R42, R45-47, R52, R57, R78, R85, R91, R96-98, R131, R143, R158, R160-162, R167-170, R174-177, R179, R181-183, R185, R189-190, R196, R198-203, R205-206, R208, R212, R221-222, R229, R239-241, R246, R248-251	AVX	CR21-103J-T
59	33 100MW 5% 805	R39,R41,R59-61, R165-166,R172	AVX	CR21-330JTR
60	4.7K 100MW 5% 805	R86	AVX	CR21-4701F-T
61	1M 100MW 5% 805	R76,R209	AVX	CR21-1004F-T
62	1.5K 100MW 5% 805	R1,R94	AVX	CR21-1501F-T
63	1.2K 1/8W 5% 1206	R23	DALE	CRCW1206-122JRT1
64	49.9K 1/8W 1% 1206	R108-113	AVX	CR32-4992F-T
65	2.21K 1/8W 1% 1206	R88-89	AVX	CR32-2211F-T
66	100pF 100V 5% 1206 NPO	C6-11,C26,C34, C61-63,C72	AVX	12061A101JAT2A
67	10uF 16V 10% B TANT	CT1-4,CT15-16	AVX	TAJB106K016R
68	100 100MW 5% 805	R242-245	AVX	CR21-101J-T

Ref.#	Description	Reference Designator	Manufacturer	Part Number
69	220pf 50V 10% 1206 NPO	C13-18	AVX	12061A221JAT2A
70	600 100MHZ 200MA 603 0.50 BEAD	FER18-21	MURATA	BLM11A601SPT
71	2A S2A_RECT DO-214AA SILICON RECTIFIER	D2-3,D7	GENERALSEMI	S2A
72	600 100MHZ 500MA 1206 0.70 BEAD	FER2-4,FER6-12,FER14-16	DIGI-KEY	240-1019-1-ND
73	237 1/8W 1% 1206	R25-26,R53-54	AVX	CR32-2370F-T
74	750K 1/8W 1% 1206	R132,R156,R164,R173	DALE/VISHAY	CRCW12067503FRT1
75	5.76K 1/8W 1% 1206	R8,R15-16,R40, R49-50,R58,	PHYCOMP	9C12063A5761FKHFT
76	11.0K 1/8W 1% 1206	R144-149	DALE	CRCW12061102FRT1
77	120PF 50V 5% 1206 NPO	C103,C105,C128, C130,C142,C144, C161,C163	PHILLIPS	1206CG121J9B200
78	75 1/8W 5% 1206	R4-6,R100-102,R104-105,R107,R114, R134-135	PHILIPS	9C12063A75R0JLHFT
79	30PF 100V 5% 1206	C221-222	AVX	12061A300JAT2A
80	68UF 6.3V 20% D TANT	CT22	PANASONIC	ECS-TOJD686R

Ref.#	Description	Reference Designator	Manufacturer	Part Number
81	340K 1/8W 1% 805	R211	DALE	CRCW0805-3403FT
82	698K 1/8W 1% 805	R210	DALE	CRCW0805-6983FT
83	680PF 50V 1% 805 NPO	C116-121	AVX	08055A681FAT2A
84	10UF 25V +80-20% 1210 Y5V	C31,C47,C50	MURATA	GRM235Y.5V106Z025
85	2.74K 1/8W 1% 1206	R150-155	DALE	CRCW12062741FRT1
86	5.49K 1/8W 1% 1206	R17-22,R27,R30-31, R34-35,R38	PANASONIC	ERJ-8ENF5491V
87	3.32K 1/8W 1% 1206	R137-142	DALE	CRCW12063321FRT1
88	1.65K 1/8W 1% 1206	R28-29,R32-33,R36-37	PANASONIC	ERJ-8ENF1651V
89	10UF 16V 20% CAP002 ELEC	CT5-14	DIG01	PCE3062TR-ND
90	2A SL22 DO-214AA SCHOTTKY	D6	GENERAL SEMI	SL22
91	53.6K 1/10W 1% 805	R75	PHILIPS	9C08052A5362FKRT/R
92	332K 1/10W 1% 805	R207	PHILIPS	9C08052A3323FKRT/R
93	10UH 47 +/-20 IND001	L11	DIG01	445-1202-2-ND

Ref.#	Description	Reference Designator	Manufacturer	Part Number
94	10K 31MW 5% RNET8	RN3	CTS	746X101103J
95	10K 50MW 5% BGA36	RN2	CTS	RT130B7
96	0.00 100MW 5% 805	R66,R74,R77,R79,R81,R83-84,R87,R99, R103,R106,R178, R192, R252	VISHAY	CRCW0805 0.0 RT1
97	190 100MHZ 5A FER002	FER5	MURATA	DLW5BSN191SQ2
98	3.32K 100MW 1% 805	R194-195, R227	DIG01	P3.32KCCTR-ND
99	22 1/10W 5% 805	R67-68,R187-188, R204,R226	VISHAY/DALE	CRCW0805220JRT1
100	0.68UH 0.72 10% 805	L1-4,L6,L8	MURATA	LQG21NR68K10T1
101	82NF 50V 5% 805 X7R	C64	AVX	08055C823JAT2A
102	1A ZHCS1000 SOT23D SCHOTTKY	D5	ZETEX	ZHCS1000
103	2.2UH 0.63 10% 805	L5,L7,L9	MURATA	LQG21N2R2K10
104	0.47UF 16V 10% 805	C218,C230	AVX	0805YC474KAT2A
105	1UF 10V 10% 805	C21,C24,C32,C44-45	AVX	0805ZC105KAT2A
106	10UF 6.3V 10% 805	C208,C217,C219, C243,C255	AVX	080560106KAT2A

Ref.#	Description	Reference Designator	Manufacturer	Part Number
107	4.7UF 6.3V 10% 805	C169	AVX	08056D475KAT2A
108	0.1UF 10V 10% 402	C192-199,C206, C209-213,C215, C220,C224-226, C234-235, C237-238,C242, C244-245,C248, C250,C253, C258-259	AVX	0402ZD104KAT2A
109	0.01UF 16V 10% 402	C204-205,C207,C214,C216, C223,C227-229,C231-232,C239-240, C246-247,C251-252,C254,C257	AVX	0402YC103KAT2A
110	1.5UH45MOHM20%IND0032.8A	L10	TYCO	DS6630-1R5M
111	100MA CMDSH-3 SOD-323 SUPERMINI SCHOTTKY	D4	CENTRAL SEMI	CMDSH-3
112	0.18uF 25V 10% 805 CERM	C170	AVX	08053C184KAT2A
113	100uF 10V 10% C TANT-LOW-ESR	CT19	AVX	TPSC107K010R0075
114	2.2uF 10V 10% 805 CERM	C43	AVX	0805ZD225KAT2A
115	76.8K 100MW 1% 1206	R48	DALE	CRCW1206-7682FRT1

Ref.#	Description	Reference Designator	Manufacturer	Part Number
116	147K 100MW 1% 1206	R56	DALE	CRCW1206-1473FRT1
117	10 62.5MW/R 5% RA8/38V RESISTOR ARRAY	RN1,RN4-12	PANASONIC	EXB-38V100JV
118	17.4K 1/10W 1% 805	R180	PANASONIC	ERJ-6ENF1742V
119	ADSP-BF561-EZLITE PCB		ANALOD DEVICES	
120	DB9 9PIN DB9M RIGHT ANGLE MALE	P2	3M	787203-2
121	1K 1/8W 5% 1206	R10,R95,R115-118,R136	AVX	CR32-102J-T
122	100K 1/8W 5% 1206	R9,R13,R157	DALE	CR1206-1003FRT1
123	22 1/8W 5% 1206	R92-93	DALE	CRCW1206220JRT1
124	270 1/8W 5% 1206	R120,R193,R197,R213-220, R230-237	AVX	CR32-271J-T
125	680 1/8W 5% 1206	R119	AVX	CR32-681J-T
126	10.0K 1/8W 1% 1206	R186	DALE	CRCW1206-1002FRT1
127	150 1/8W 1% 1206	R3	PANASONIC	ERJ-8ENF1500V

Ref.#	Description	Reference Designator	Manufacturer	Part Number
128	RED-SMT LED001 GULL-WING	LED2-3	PANASONIC	LN1261C
129	GREEN-SMT LED001 GULL-WING	LED1	PANASONIC	LN1361C
130	604 1/8W 1% 1206	R125-130	DALE	CRCW12066040FRT1
131	1uF 25V 20% A TANT -55+125	CT25-28	PANASONIC	ECS-T1EY105R
132	ADG774A QSOP16 QUICKSWITCH-257	U36-37	ANALOG DEVICES	ADG774ABRQ
133	IDC 2X1 IDC2X1 GOLD	P1		
134	IDC 7X2 IDC7X2 HEADER	P4	BERG	54102-T08-07
135	2.5A RESETABLE FUS001	F1	RAYCHEM CORP.	SMD250-2

ADSP-BF561 EZ-KIT Lite Schematic

Approvals		Date
Drawn	JSZ	10/10/03
Checked		
Engineering		

ANALOG DEVICES
20 Cotton Road
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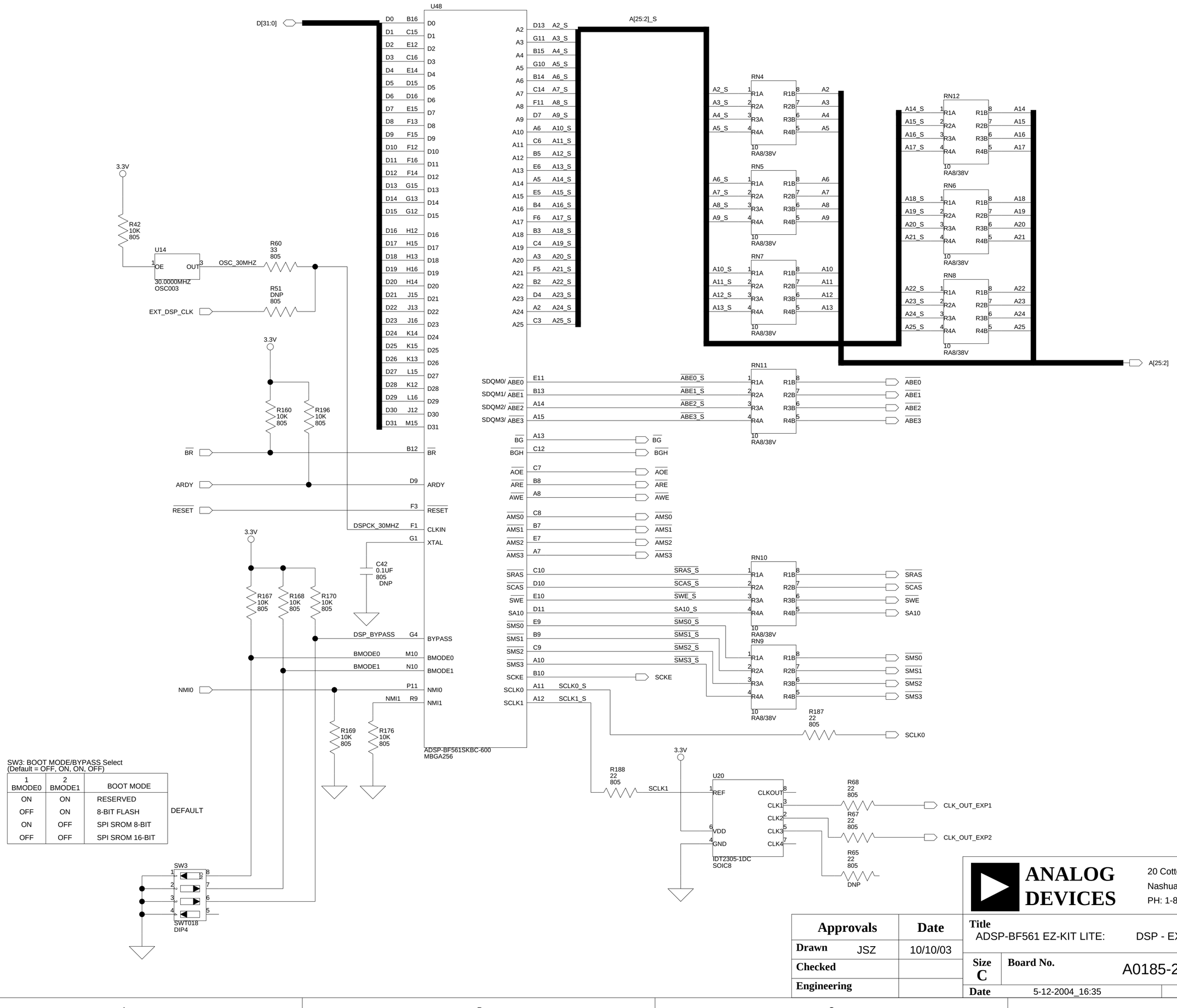
Title: ADSP-BF561 EZ-KIT LITE: TITLE			
Size: C	Board No.: A0185-2003		Rev: 1.3A
Date: 12-16-2003_11:50		Sheet 1 of 18	



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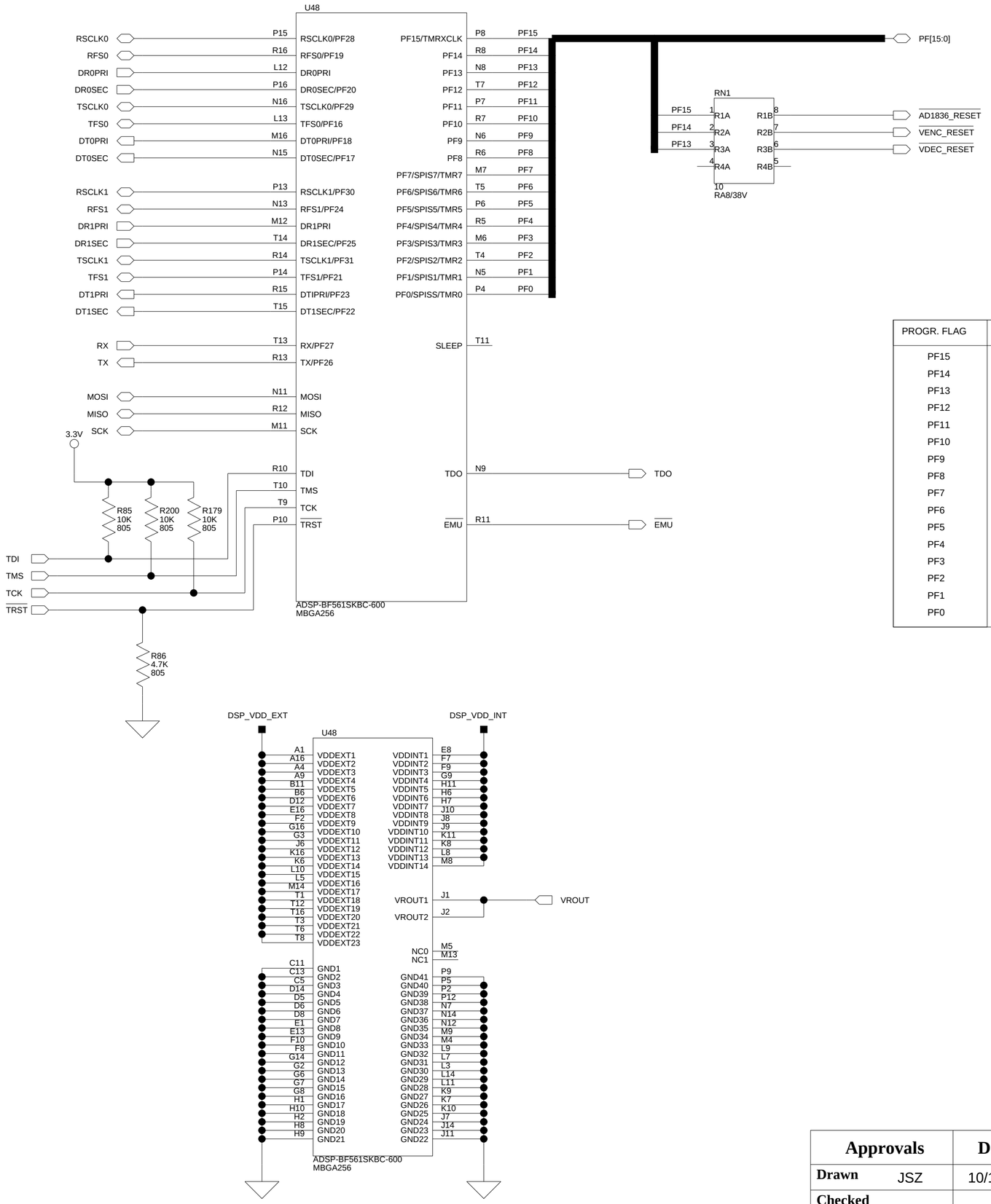
Title
ADSP-BF561 EZ-KIT LITE: DSP - EXT MEM INTERFACE

Size	Board No.	Rev
C	A0185-2003	1.3A

Date 5-12-2004_16:35 Sheet 2 of 18



PROGR. FLAG	FUNCTION
PF15	AD1836 CODEC RESET
PF14	ADV7179 VIDEO ENCODER RESET
PF13	ADV7183A VIDEO DECODER RESET
PF12	GENERAL PURPOSE
PF11	GENERAL PURPOSE
PF10	GENERAL PURPOSE
PF9	GENERAL PURPOSE
PF8	GENERAL PURPOSE / PUSH BUTTON STATUS INPUT
PF7	GENERAL PURPOSE / PUSH BUTTON STATUS INPUT
PF6	GENERAL PURPOSE / PUSH BUTTON STATUS INPUT/ UART SIGNAL
PF5	GENERAL PURPOSE / PUSH BUTTON STATUS INPUT/ UART SIGNAL
PF4	GENERAL PURPOSE / AD1836 LATCH SIGNAL
PF3	GENERAL PURPOSE / VIDEO DECODER FIELD
PF2	GENERAL PURPOSE / VIDEO DECODER OUTPUT ENABLE
PF1	GENERAL PURPOSE / I2C SERIAL DATA
PF0	GENERAL PURPOSE / I2C SERIAL CLOCK

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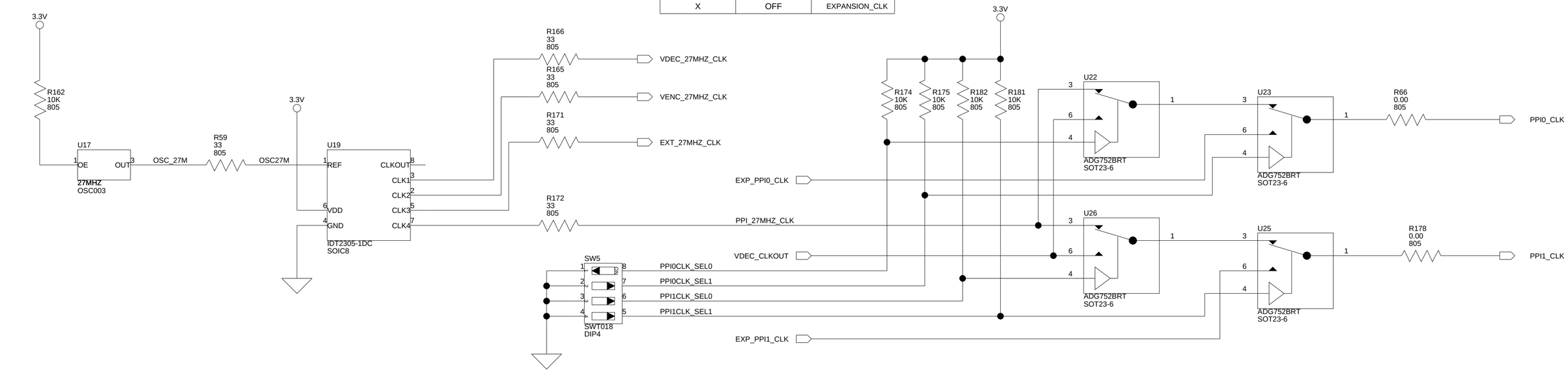
Title: ADSP-BF561 EZ-KIT LITE: DSP - PROGR. FLAGS, SPI

Size	Board No.	Rev
C	A0185-2003	1.3A

Date: 5-6-2004_16:04 Sheet 3 of 18

SW5: PPI CLK Routing Select
(Default: 1 = OFF, 2 = ON, 3 = ON, 4 = ON)

1 or 3 PPIxCLK_SEL0	2 or 4 PPIxCLK_SEL1	PPIxCLK
ON	ON	PPI_27MHZ_CLK
OFF	ON	VDEC_CLKOUT
X	OFF	EXPANSION_CLK



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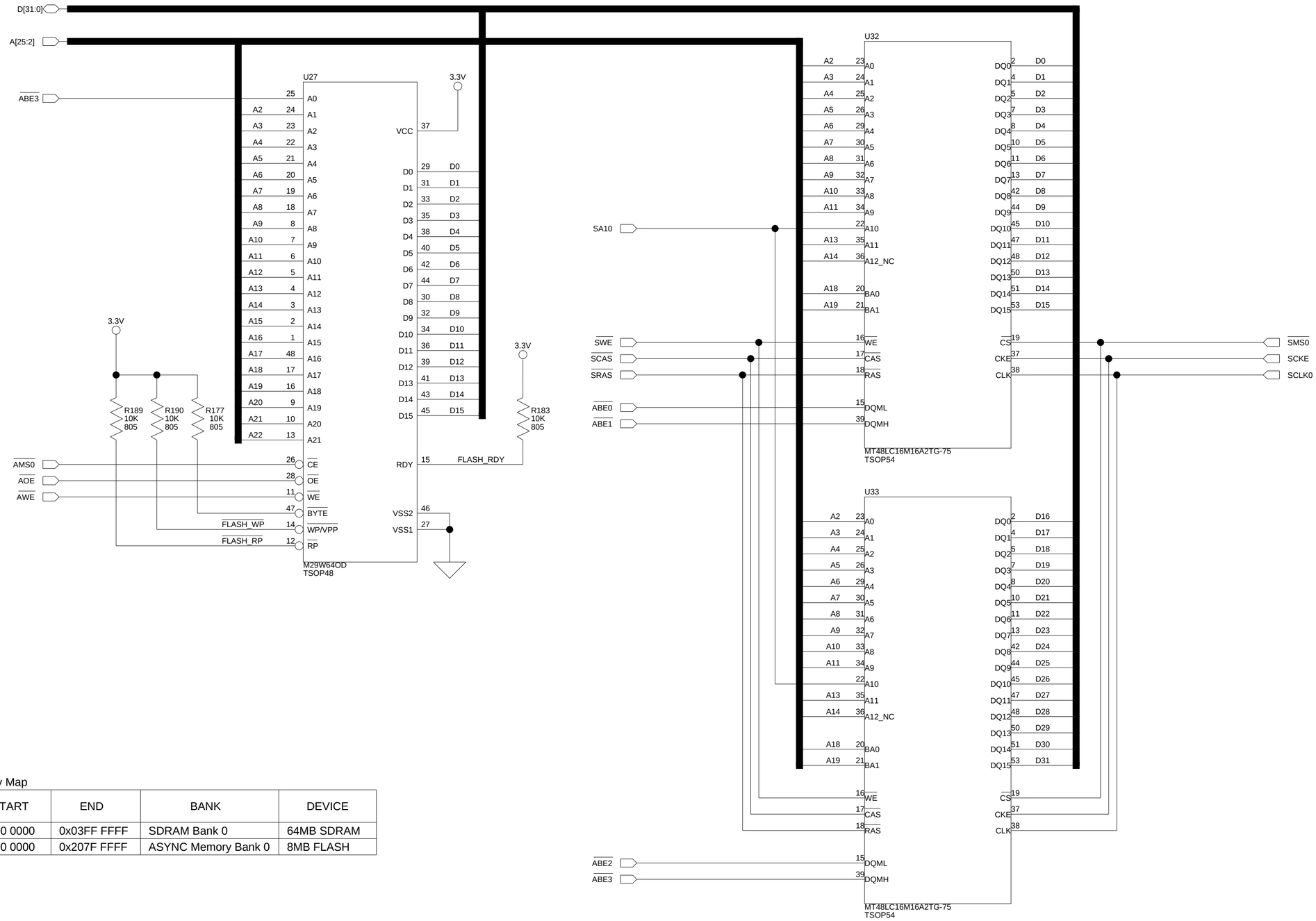
Title: ADSP-BF561 EZ-KIT LITE: DSP - PPI0 AND PPI1

Size	Board No.	Rev
C	A0185-2003	1.3A

Date: 5-12-2004_16:32 Sheet 4 of 18

FLASH A (8MB)
4M x 16

SDRAM 64MB
(256Mb x 2 Chips)



Memory Map

START	END	BANK	DEVICE
0x0000 0000	0x03FF FFFF	SDRAM Bank 0	64MB SDRAM
0x2000 0000	0x207F FFFF	ASYNC Memory Bank 0	8MB FLASH

Approvals		Date
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Engineering		

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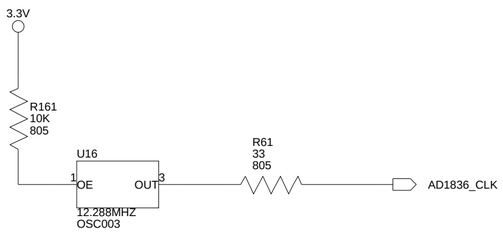
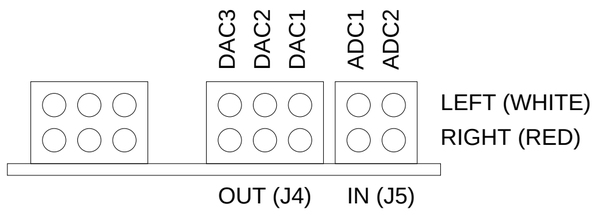
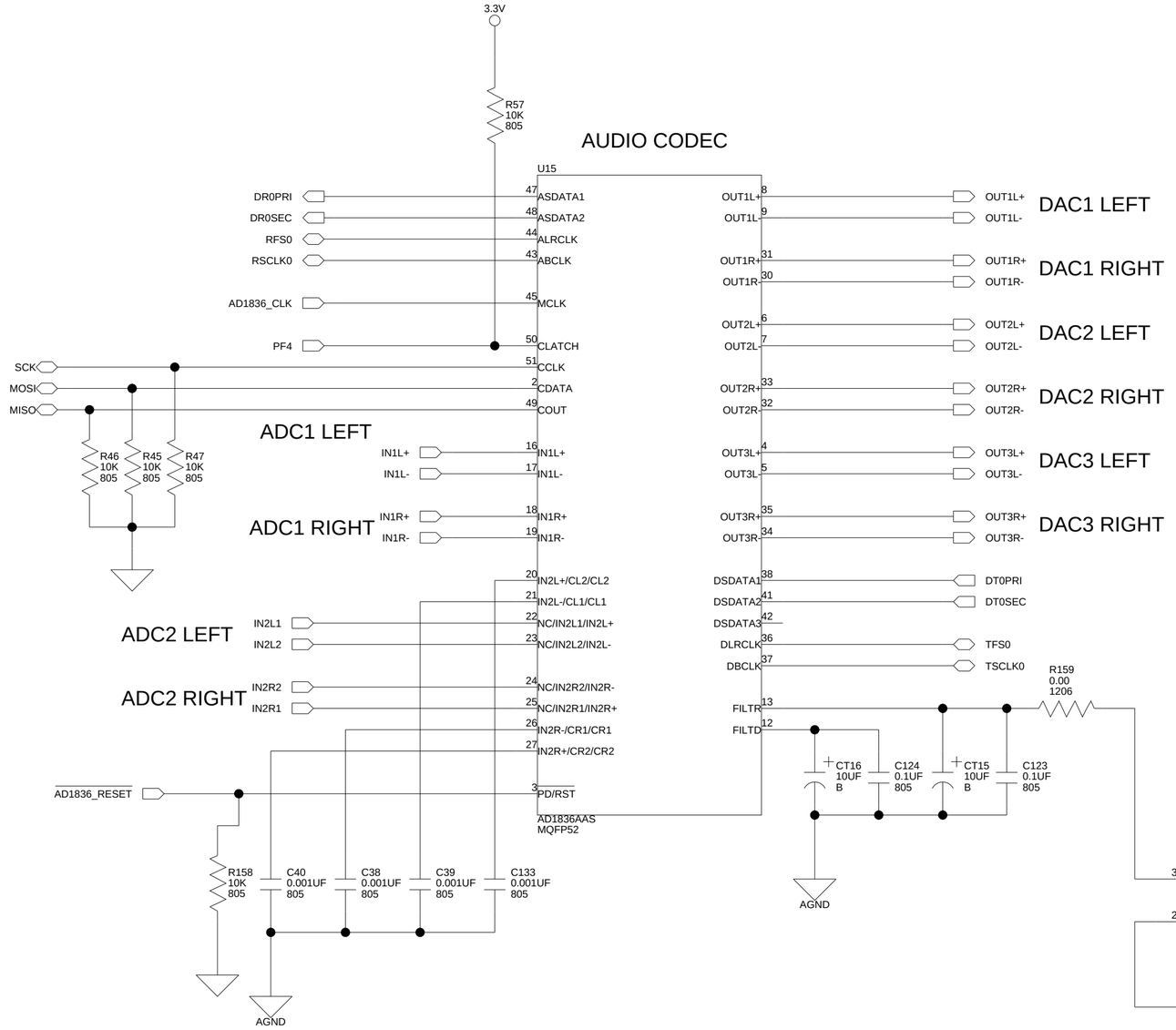
Title: ADSP-BF561 EZ-KIT LITE: MEMORY - FLASH & SDRAM

Size	Board No.	Rev
C	A0185-2003	1.3A

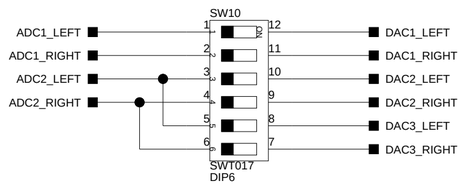
Date: 12-16-2003_11:03 Sheet 5 of 18

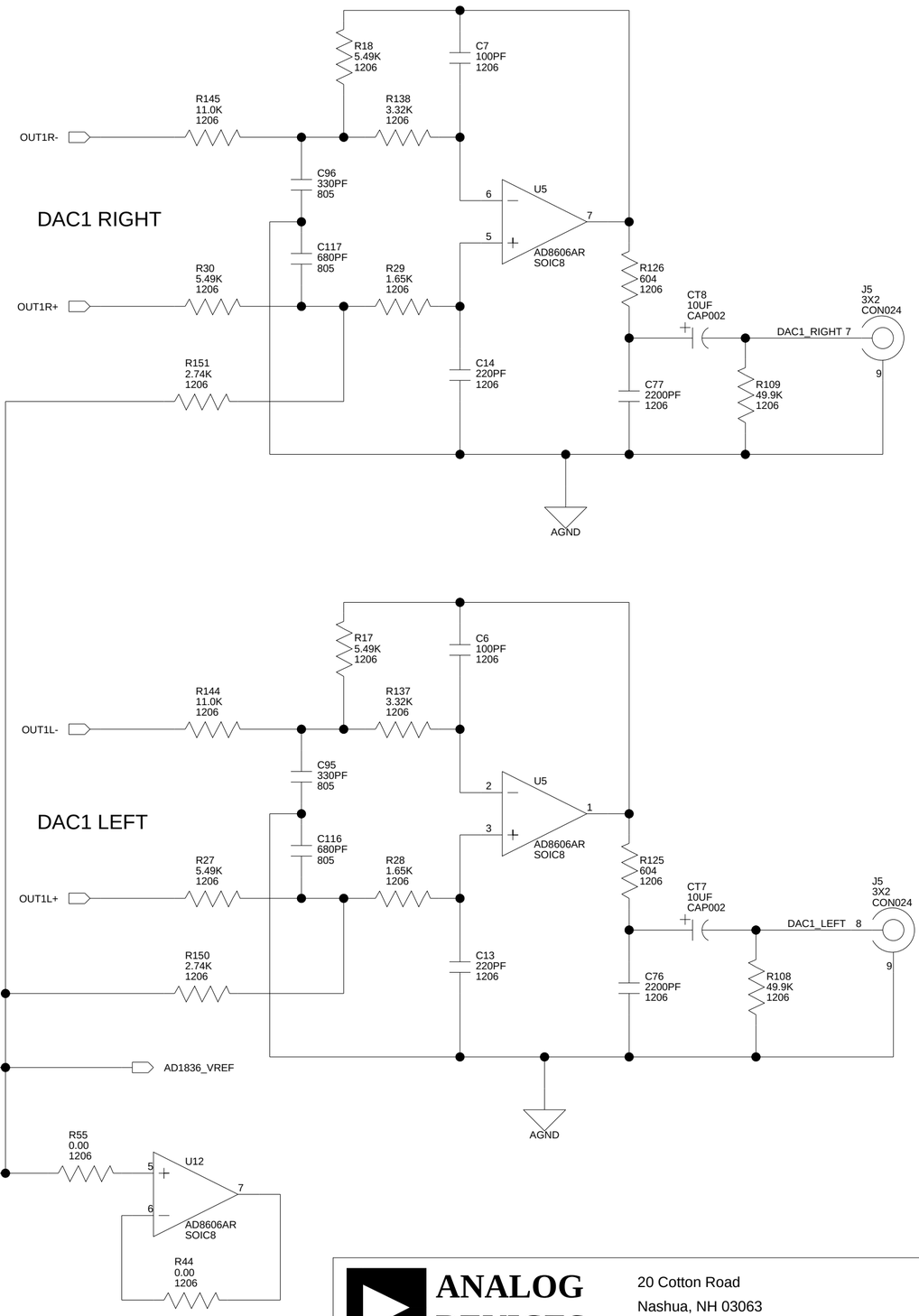






SW10: Audio Loopback
For Test Purposes
Default = All Off





Approvals		**Date**
Drawn	JSZ	10/10/03
Checked		
Engineering		

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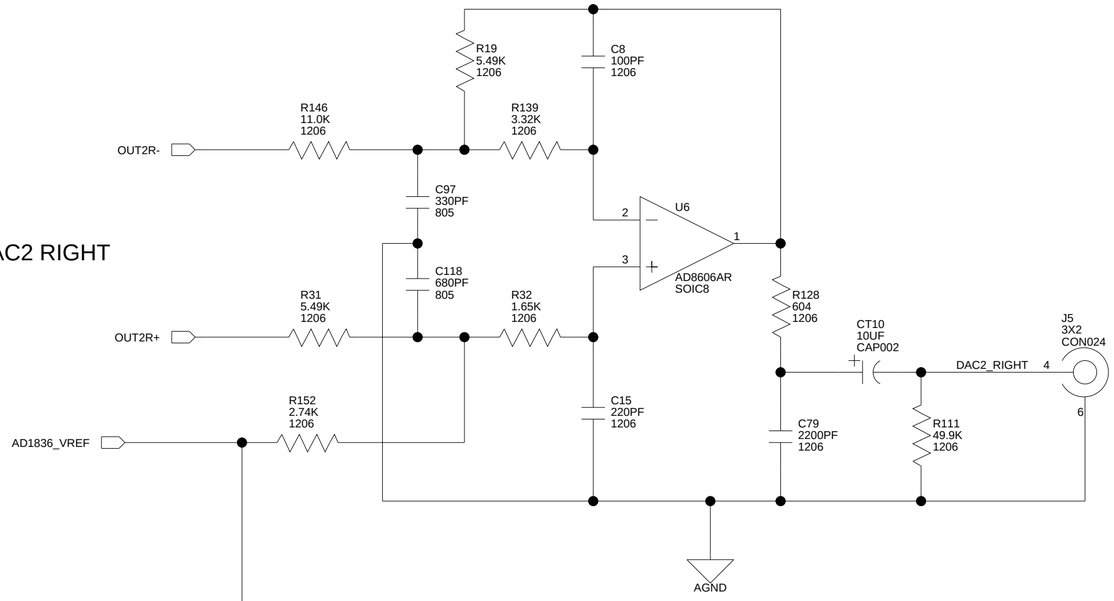
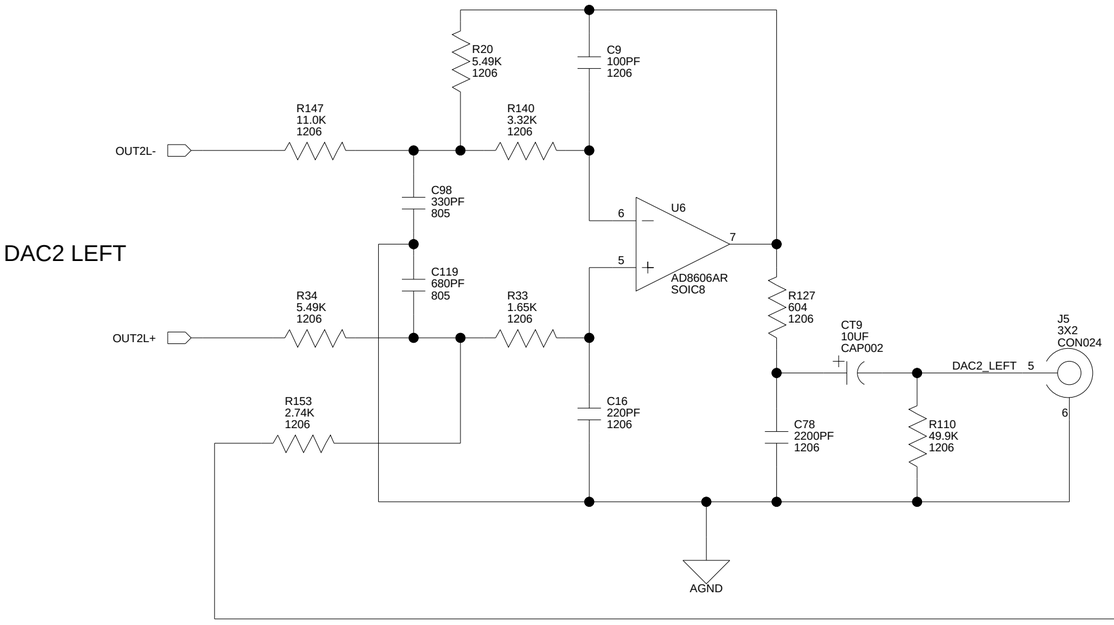
Title ADSP-BF561 EZ-KIT LITE: AUDIO CODEC

Size	**Board No.**	**Rev**
C	A0185-2003	1.3A
Date 5-12-2004_16:35	**Sheet** 6 **of** 18	

DAC2 RIGHT



DAC2 LEFT



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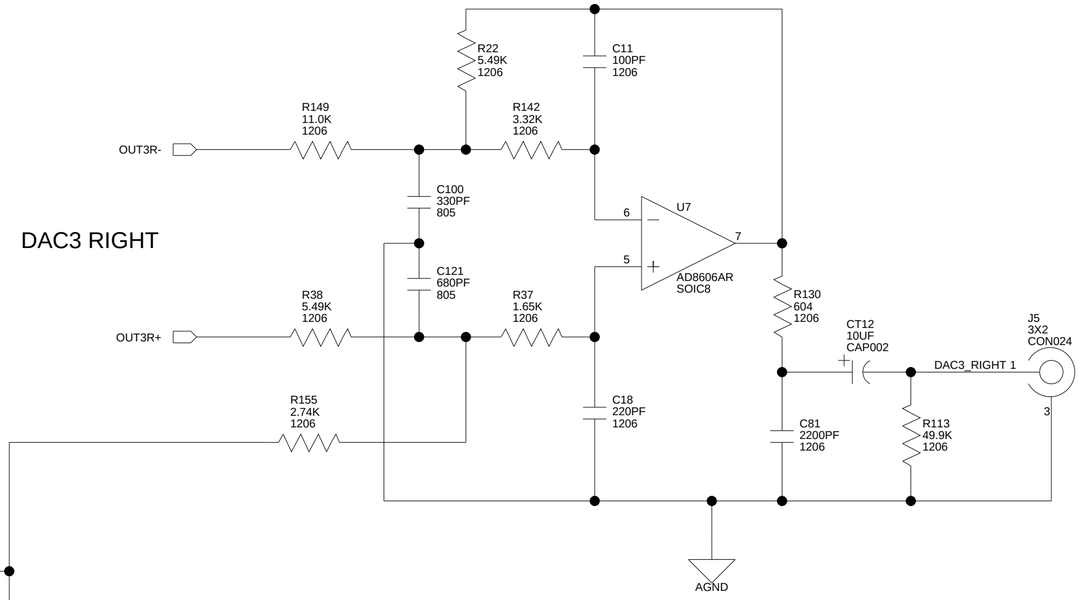
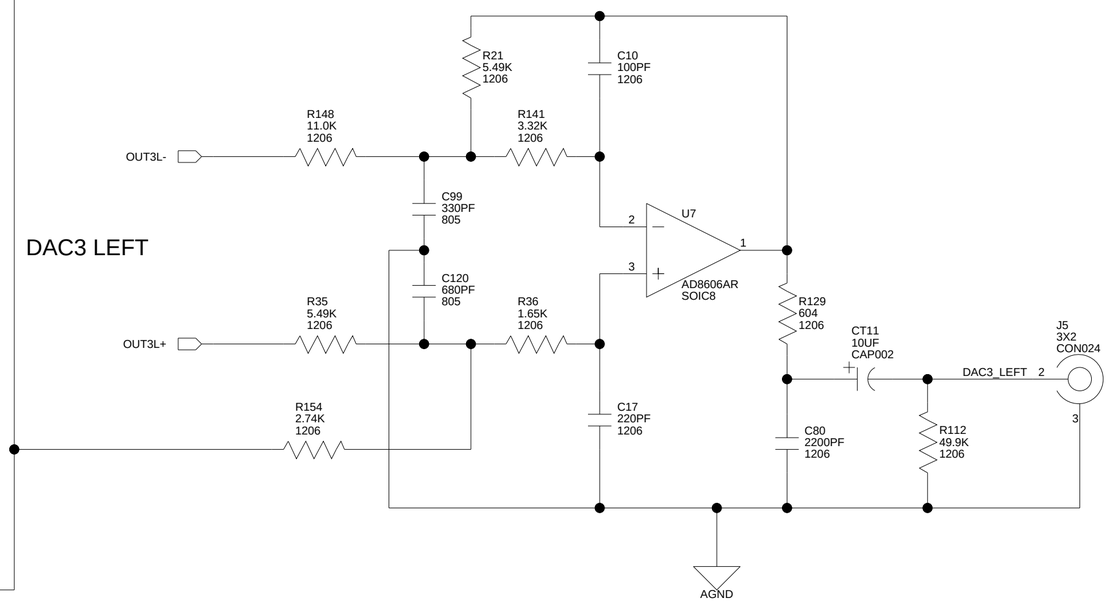


DAC3 LEFT



Approvals		Date
Drawn	JSZ	10/10/03
Checked		
Engineering		

ANALOG DEVICES
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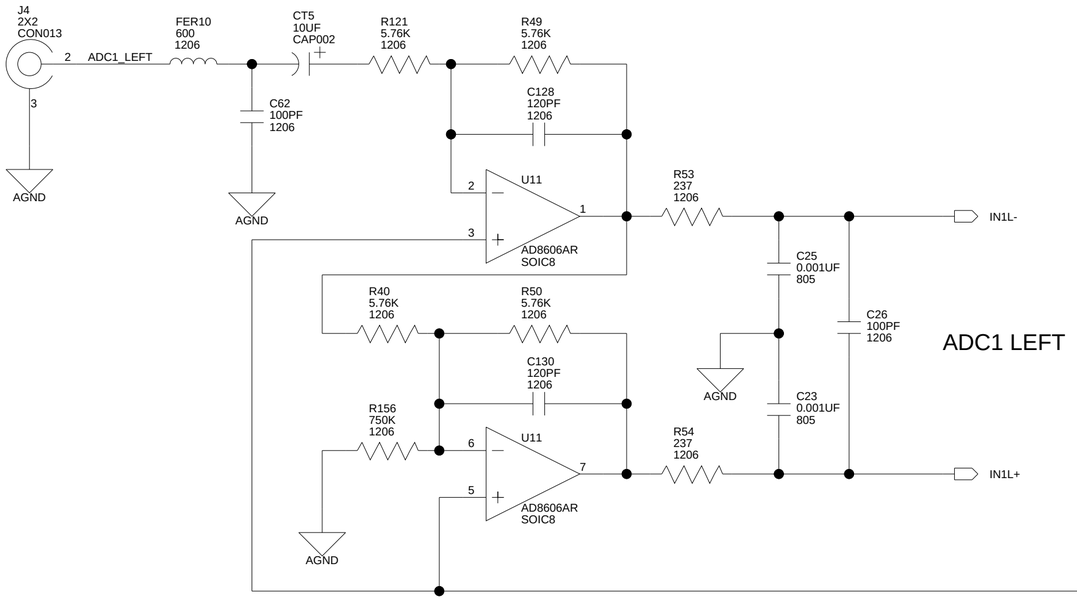
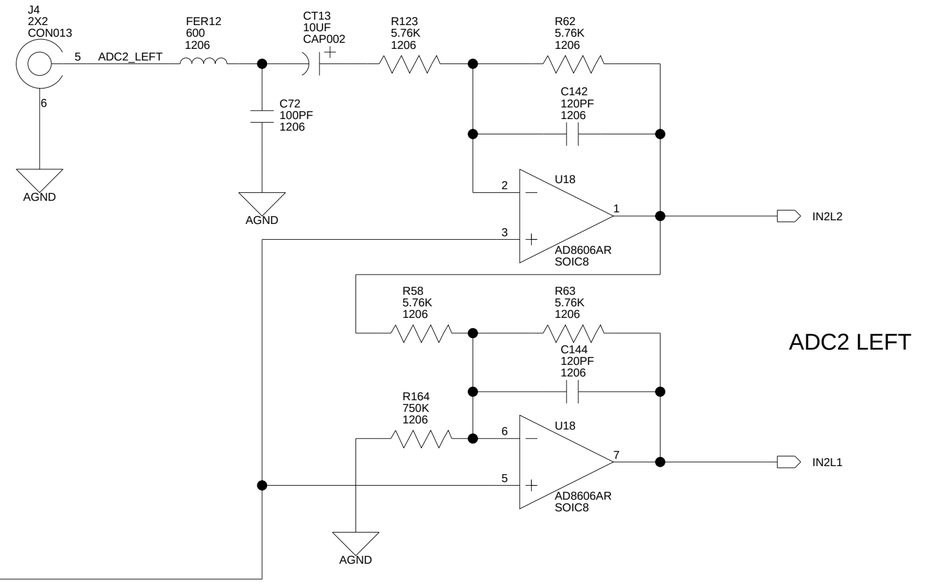
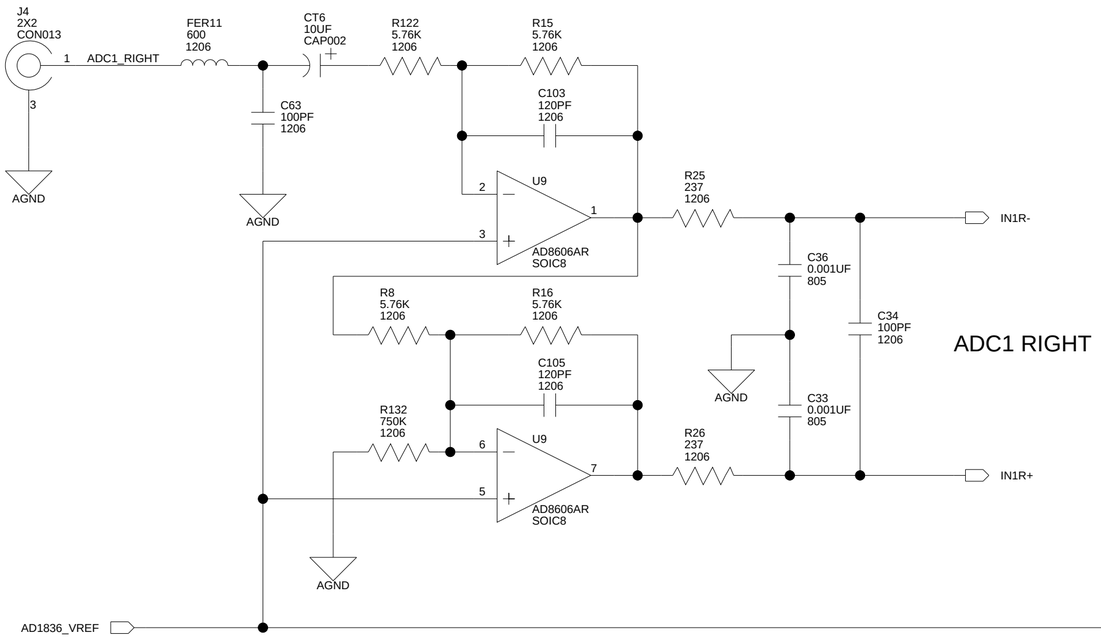
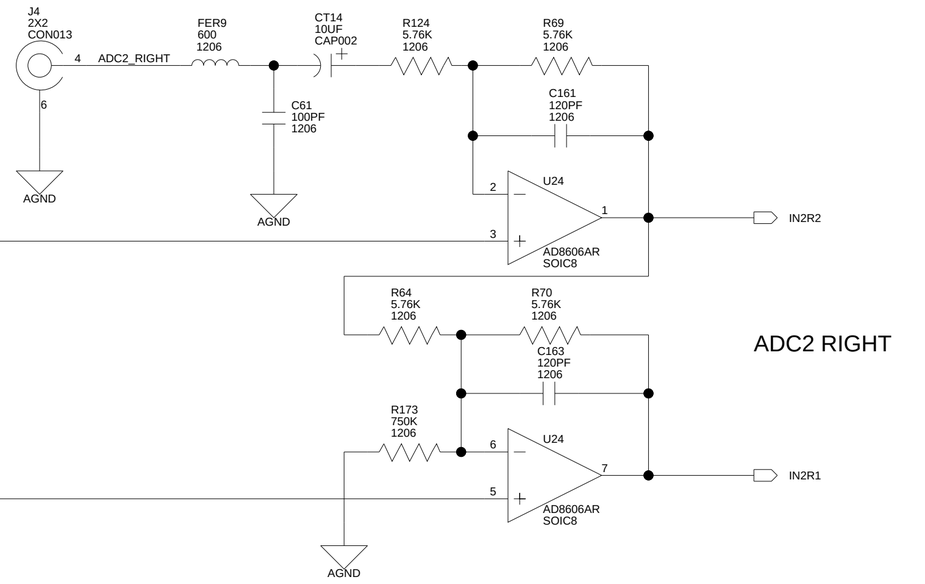
Title: ADSP-BF561 EZ-KIT LITE: AUDIO OUT			
Size: C	Board No.: A0185-2003		Rev: 1.3A
Date: 12-10-2003_18:18		Sheet 7 of 18	









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Title ADSP-BF561 EZ-KIT LITE: AUDIO IN

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C	A0185-2003	1.3A

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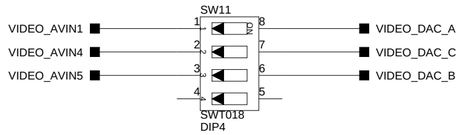
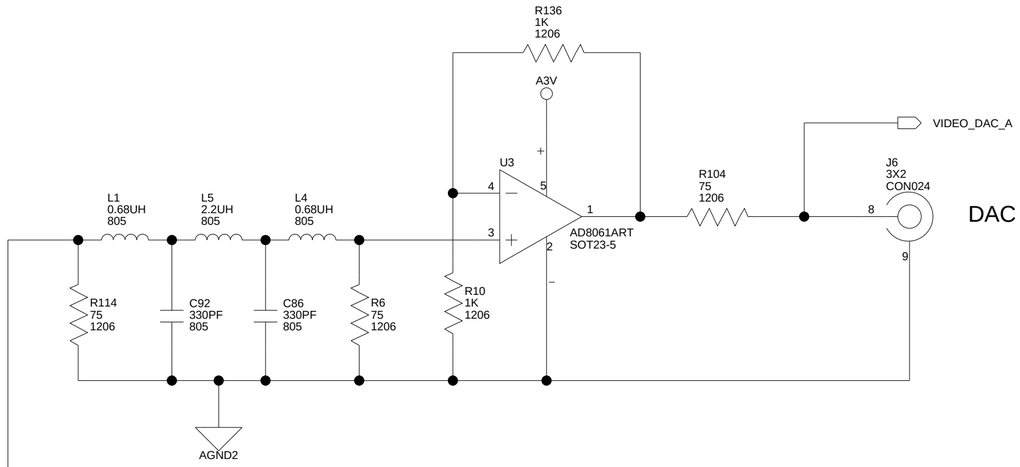
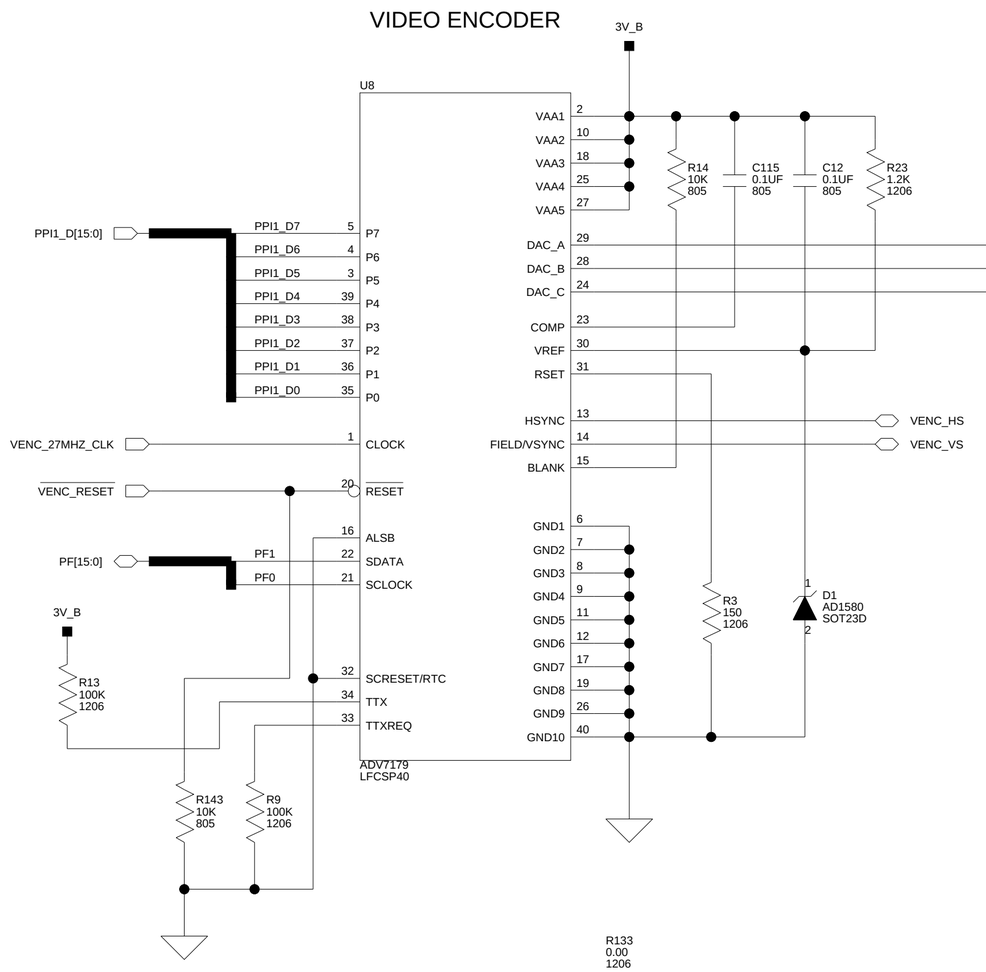


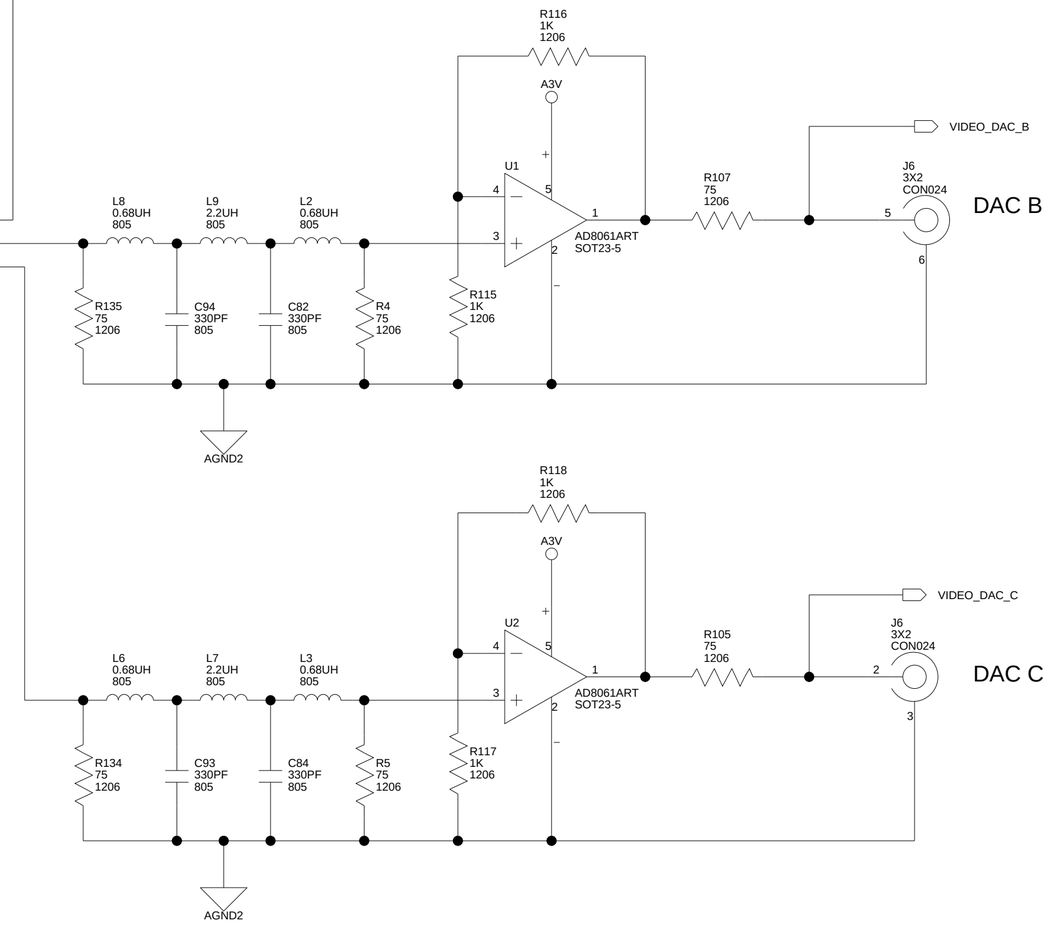
SW11: Video Loopback
For Test Purposes
Default = All Off



DAC A

	DAC A	DAC B	DAC C
Composite Video	CVSB	CVSB	C
Component Video	G	B	R
Differential Component Video	Y	U	V
S Video	Y		C





DAC B

DAC C

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Title: ADSP-BF561 EZ-KIT LITE: VIDEO ENCODER (VIDEO OUT)

Size	Board No.	Rev
C	A0185-2003	1.3A

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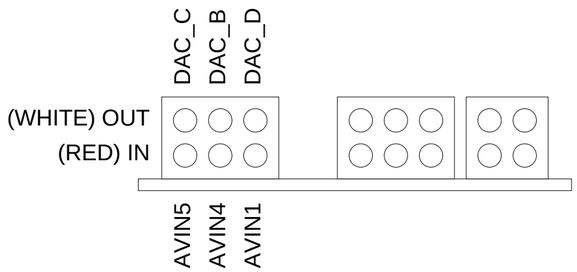
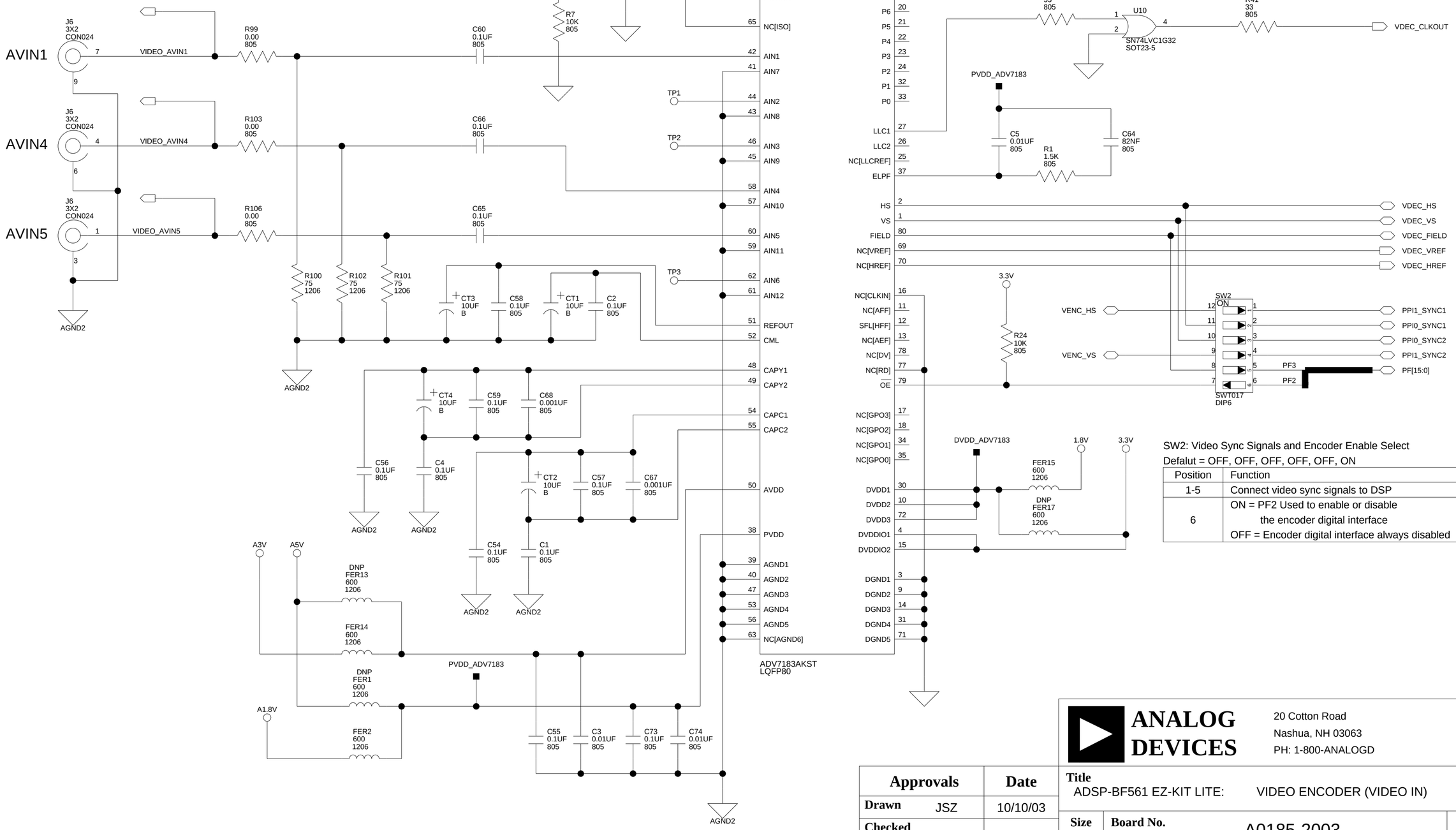


	AVIN1	AVIN4	AVIN5
Composite Video	CVBS	CVBS	CVBS
Differential Component Video	Y	V	U
S Video	Y	C	

VIDEO DECODER

Note: Signal Names in brackets refer to ADV7183KST



SW2: Video Sync Signals and Encoder Enable Select

Defalut = OFF, OFF, OFF, OFF, OFF, ON

Position	Function
1-5	Connect video sync signals to DSP
6	ON = PF2 Used to enable or disable the encoder digital interface OFF = Encoder digital interface always disabled

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Title ADSP-BF561 EZ-KIT LITE: VIDEO ENCODER (VIDEO IN)

Size	Board No.	Rev
C	A0185-2003	1.3A

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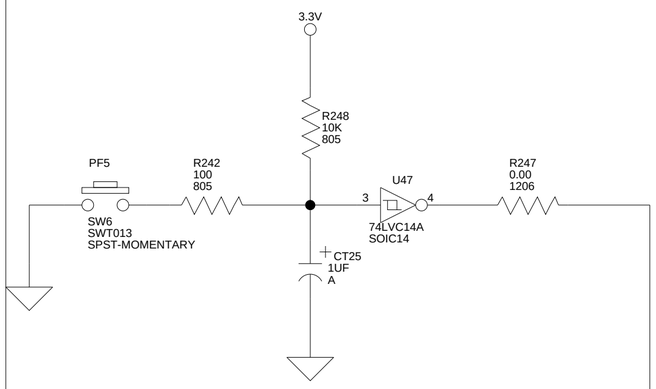

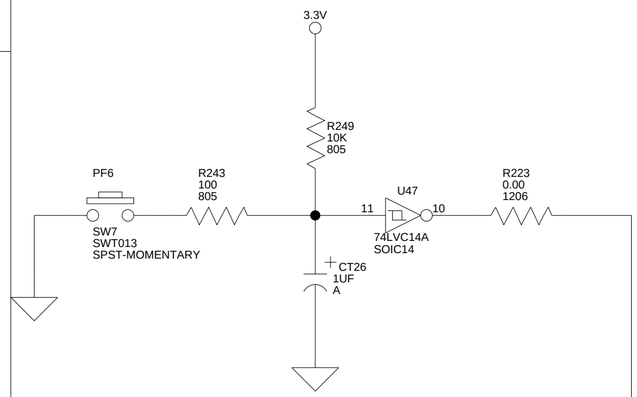

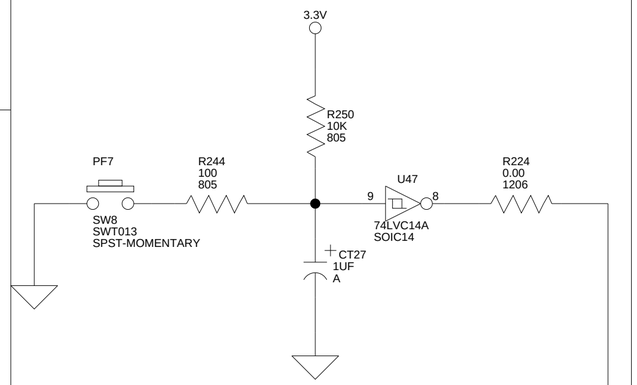

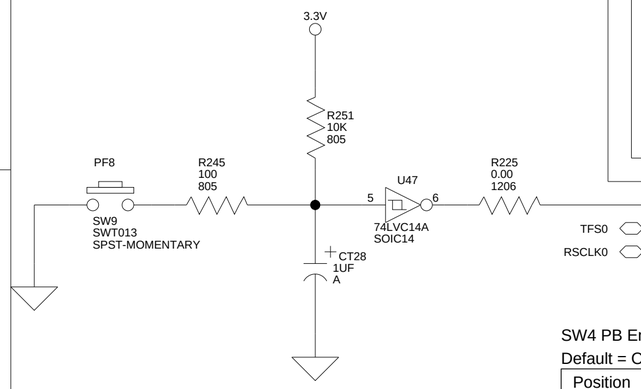

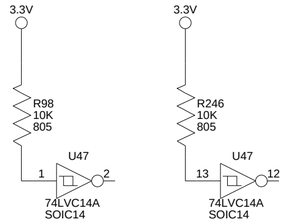

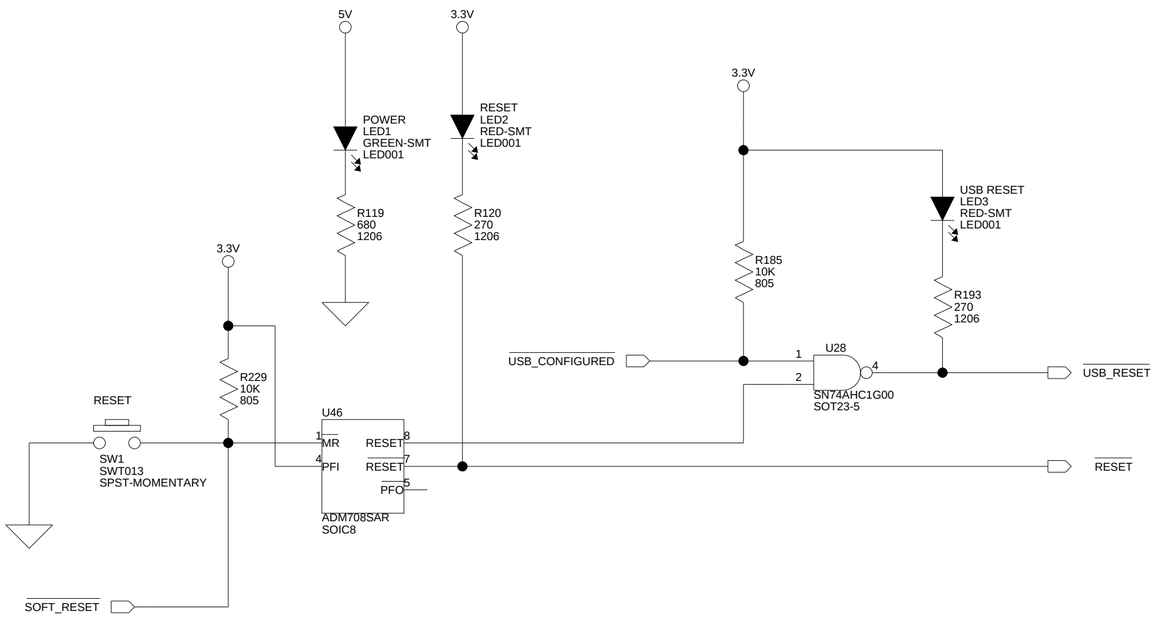

NOTE: Remove R192 when populating R191 and R184

UART

SW4 PB Enable Switch

Default = ON, ON, ON, ON, OFF, OFF

Position	Function
1-4	Connects the push buttons to the Programmable Flags of the DSP Useful if using the PFs for another purpose.
5,6	OFF, OFF = AD1836A -> TDM Mode ON, ON = AD1836A -> I2S Mode

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Title ADSP-BF561 EZ-KIT LITE: RESET, PUSH-BUTTON SWITCHES, UART

Size	Board No.	Rev
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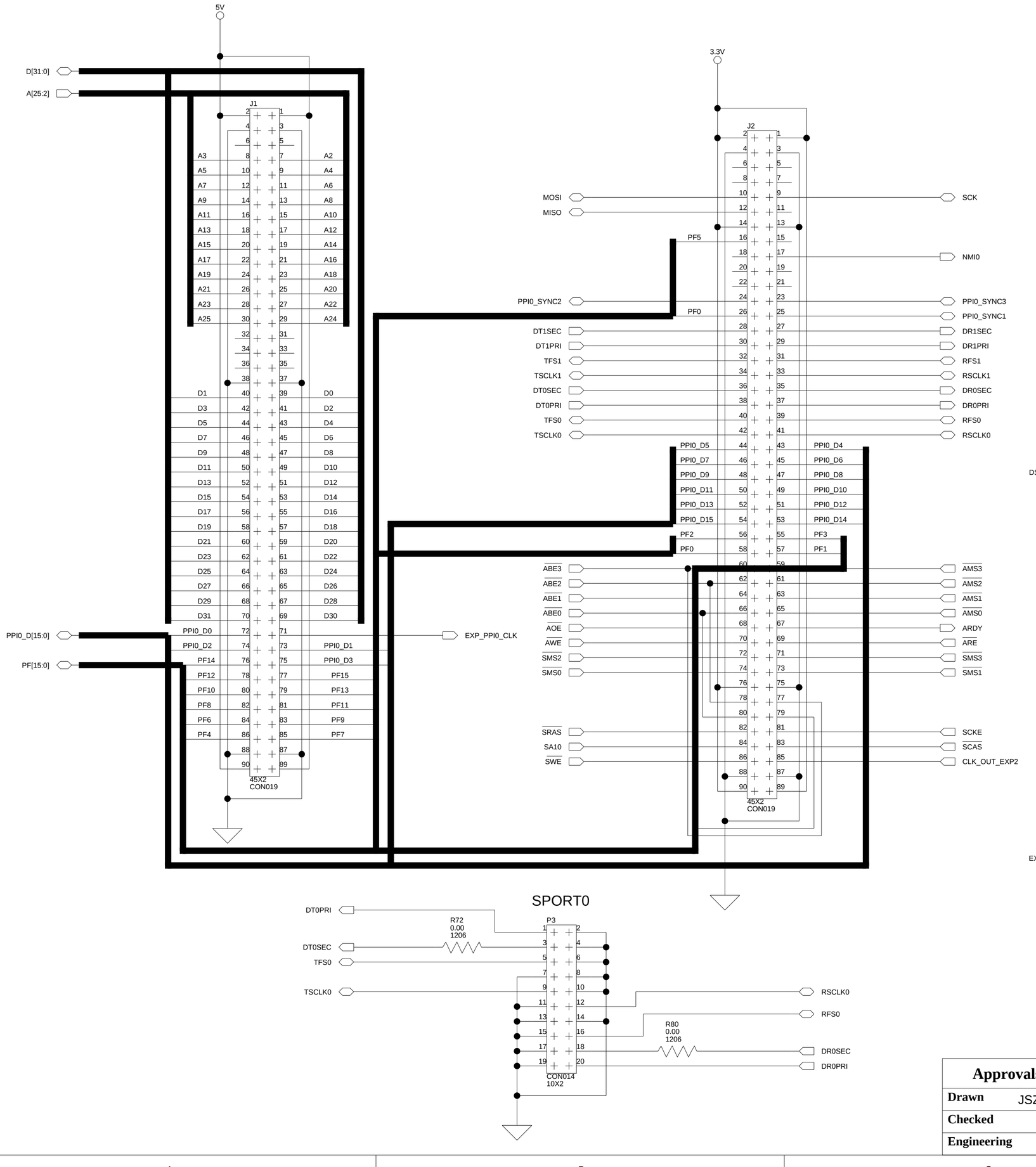
EXPANSION INTERFACE (TYPE B)



SPORT0

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Drawn JSZ	10/10/03
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Title ADSP-BF561 EZ-KIT LITE: EXTENDER CARD CONNECTORS

Size	Board No.	Rev
C	A0185-2003	1.3A

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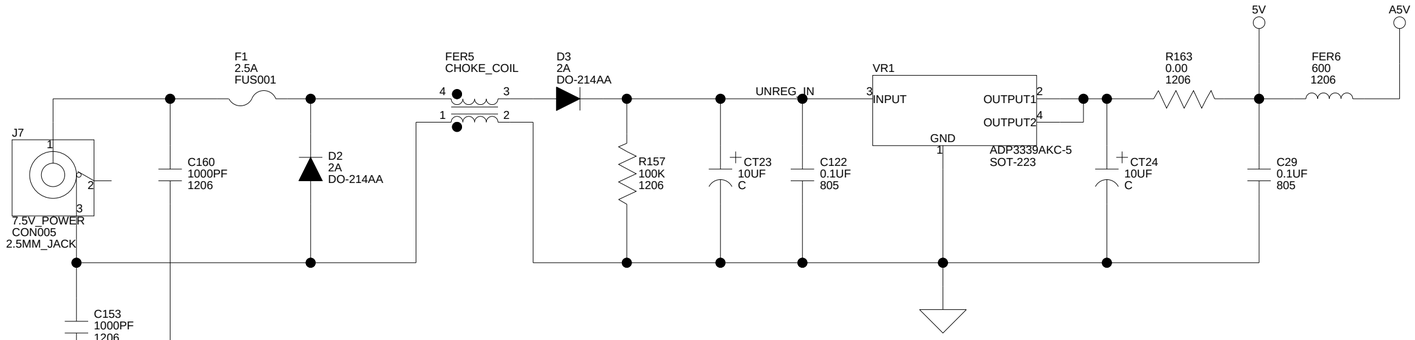

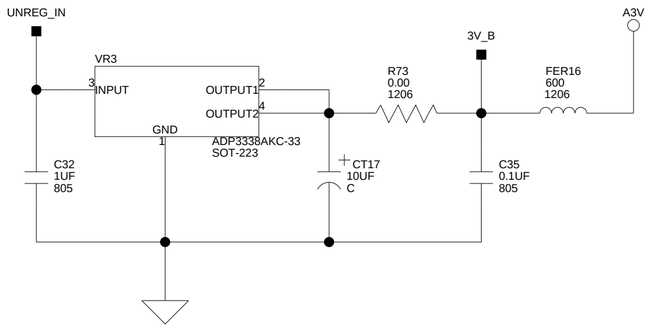

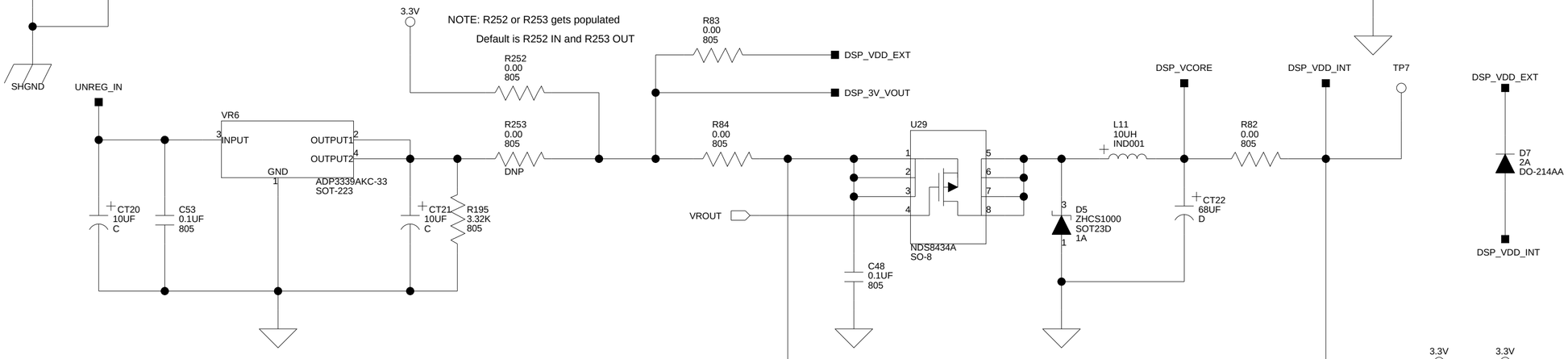

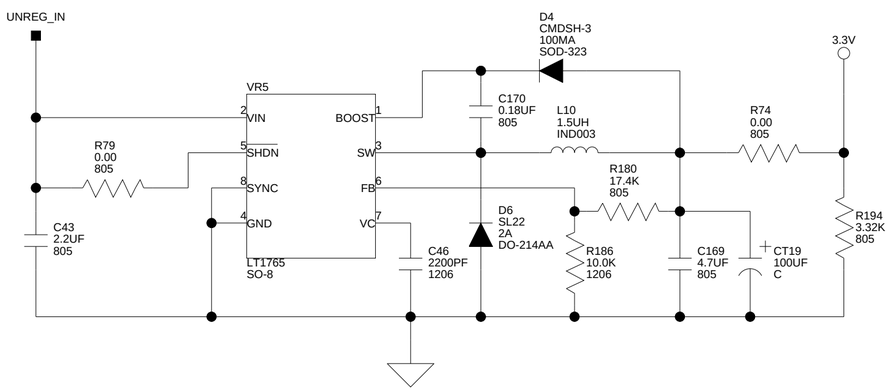

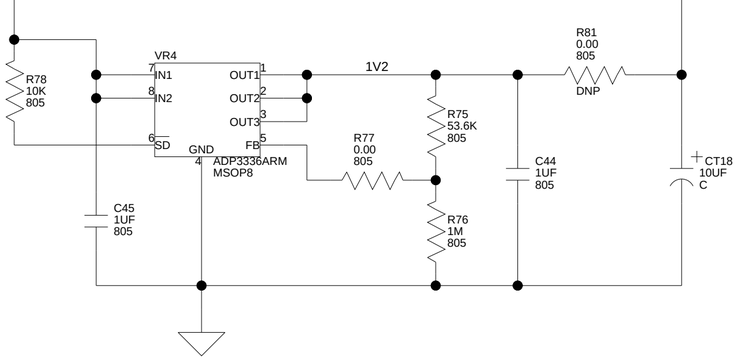

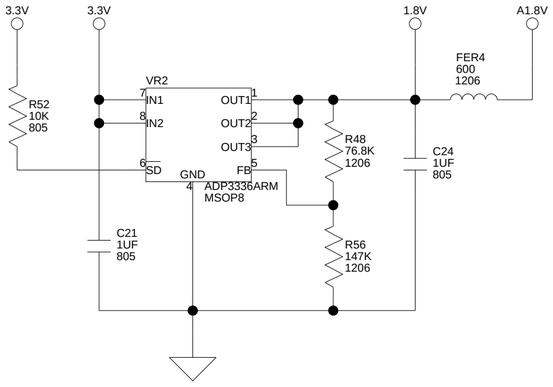

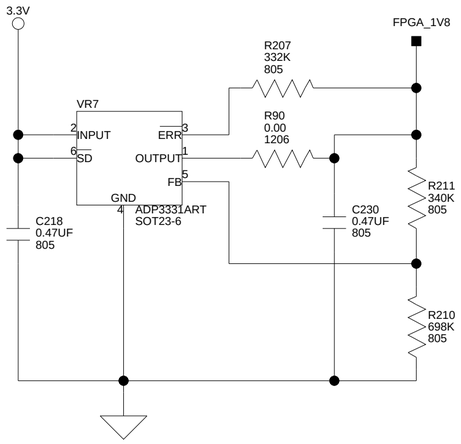

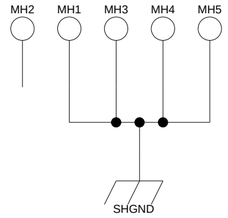

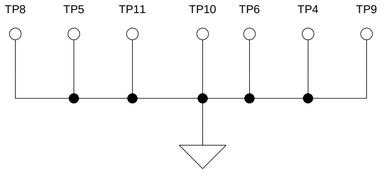

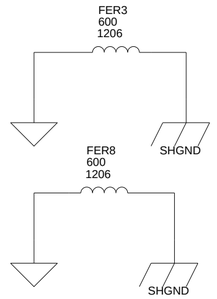

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Title ADSP-BF561 EZ-KIT LITE: POWER

Size	Board No.	Rev
C	A0185-2003	1.3A

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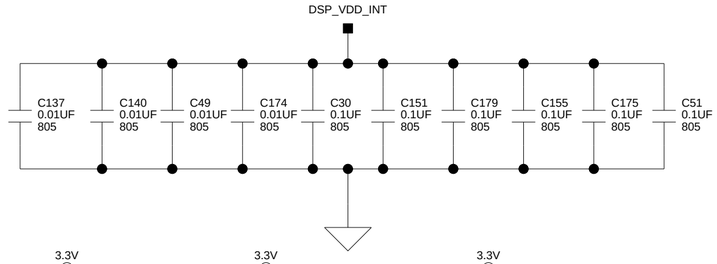

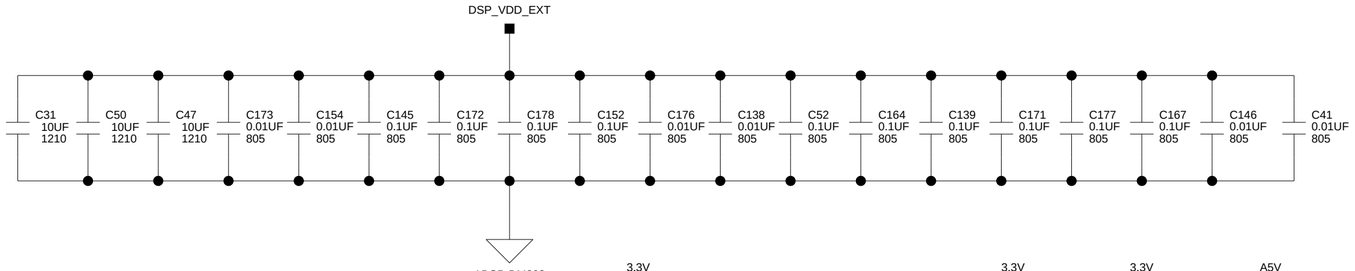

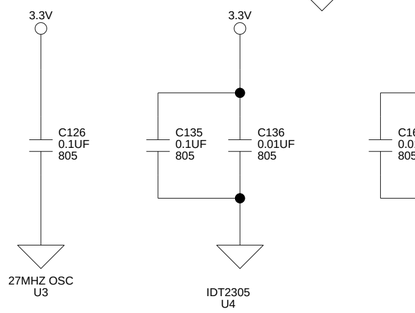

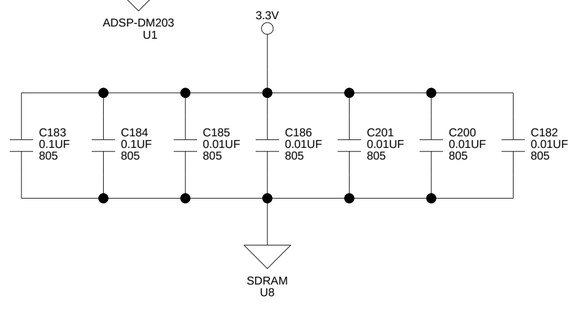

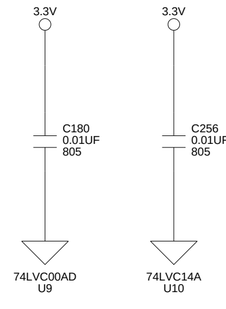

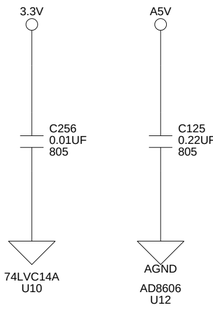

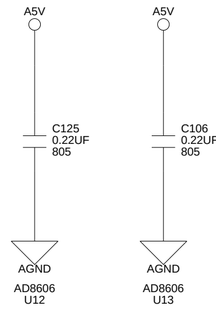

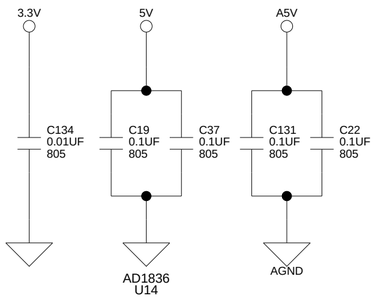

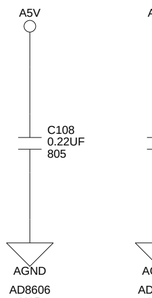

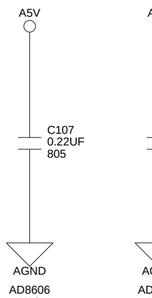

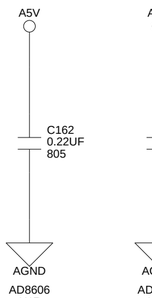

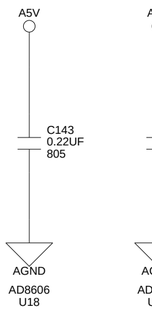

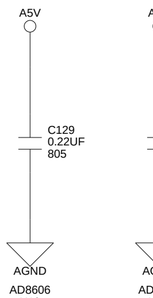

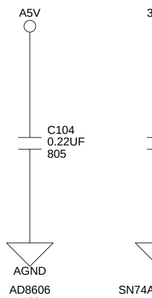

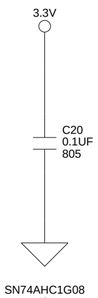

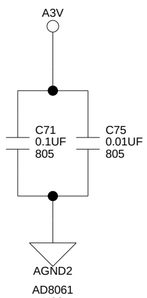

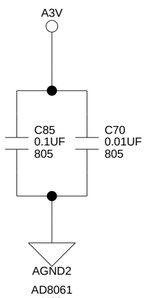

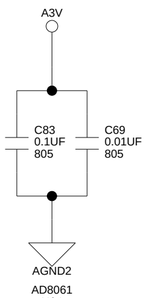

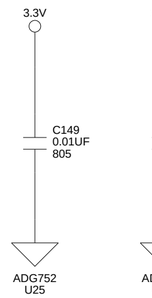

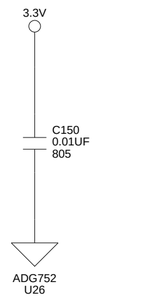

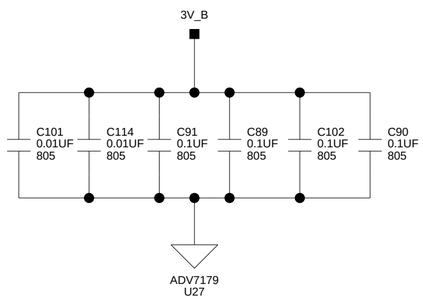

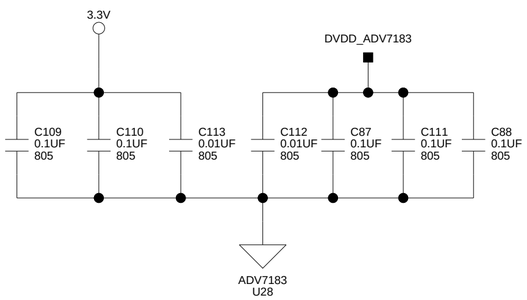

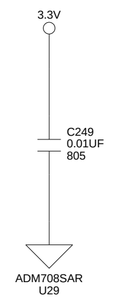

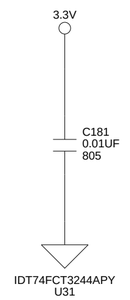

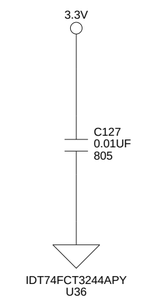

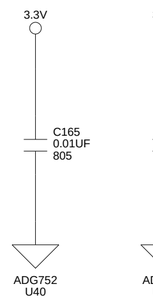

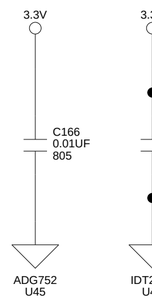

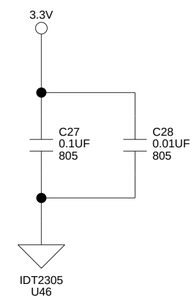

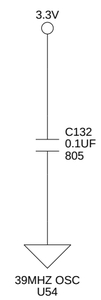

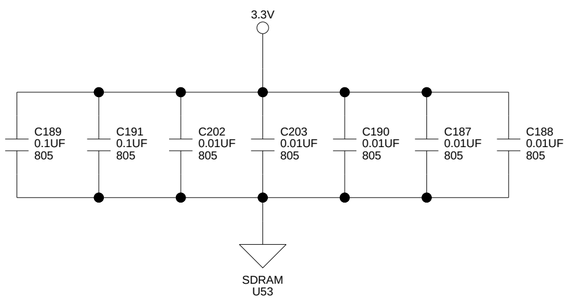

Approvals		Date
Drawn	JSZ	10/10/03
Checked		
Engineering		

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Nashua, NH 03063
PH: 1-800-ANALOGD

Title: ADSP-BF561 EZ-KIT LITE: DECOUPLING CAPS

Size	Board No.	Rev
C	A0185-2003	1.3A

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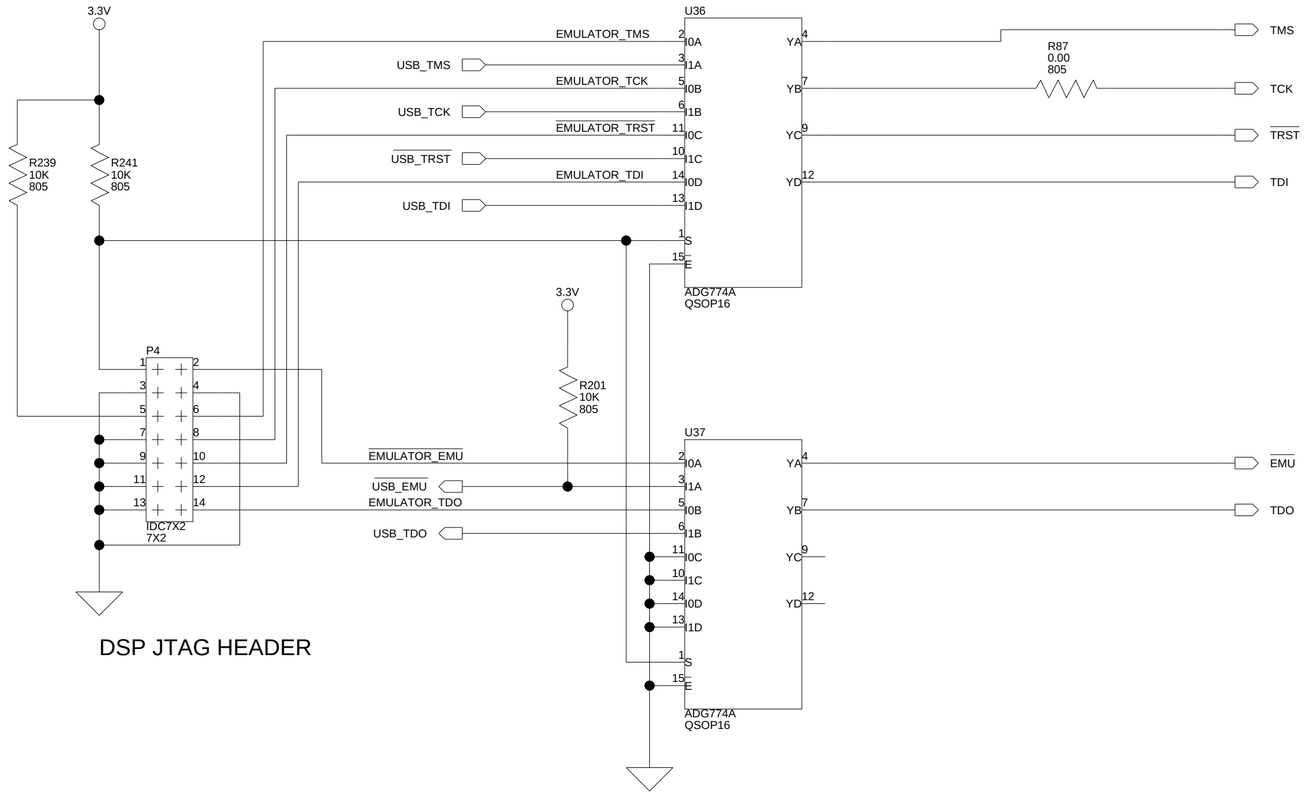
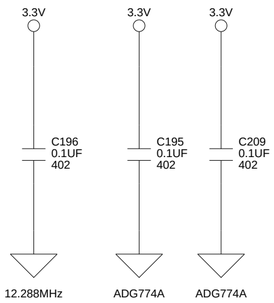
All USB interface circuitry is considered propreitary andh has been omitted from this schematic

When designin your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com



DSP JTAG HEADER



Approvals	**Date**
Drawn JSZ	10/10/03
Checked	
Engineering	

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Nashua, NH 03063
PH: 1-800-ANALOGD

Title ADSP-BF561 EZ-KIT LITE: DEBUG AGENT - JTAG

Size	**Board No.**	**Rev**
C	A0185-2003	1.3A

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