# Zafar Takhirov

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## Education

**Boston University** Boston, MA
*PhD Computer Engineering* May 2017, GPA 3.5/4.0

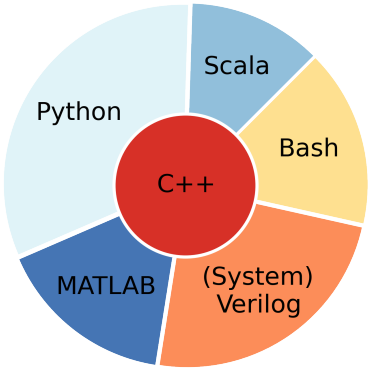
**Boston University** Boston, MA
*M.S. Computer Engineering* May 2012, GPA 3.49/4.0

**Russian-Tajik (Slavic) University**
Dushanbe, Tajikistan May 2008
*Specialist, Linguistics* GPA 5.0/5.0

## Skills

**Programming Languages**

C++, Python, (System)Verilog, MATLAB, Bash, Scala/Chisel, LaTeX, GNU Make




**Tools**

Git, Emacs, Cadence RTL Compiler, Cadence SOC Encounter, Icarus Verilog, GTKWave, Inkscape

**Foreign Languages**

English, Russian, Tajik, Turkish, German

## Relevant Coursework

- Computer Organization, Architecture
- Advanced Digital Design in Verilog
- VLSI, VLSI Project
- Microprocessors
- RF/Analog Design
- Photonics

## Links

**GitHub**: zafartahirov
**LinkedIn**: zafartakhirov
**blog.**zafar.cc
**resume.**zafar.cc

## Work Experience

**Research Assistant** 09/2011 – Now
*Boston University, Boston, MA*
Worked on tunable and adaptive systems; developed energy-efficient mechanism to achieve 40% lower energy dissipation

**CTO & Co-Founder** 05/15 – 02/16
*Avicennas Group, Inc., New York City, NY*
Manage the team of 5 developers (remote) to develop a healthcare travel system

**Mixed-Signal Verification Engineer** 02/14 – 02/15
*Analog Devices, Inc.*
Initiated the implementation of UVM-based verification as well as functional safety discussion (ISO 26262)

**Mixed-Signal Design Engineering Intern** 05/13 – 12/13
*Analog Devices, Inc.*
Develop Real-Number Modeling approach to speed up analog simulations by 1000x

**Teaching Fellow / Guest Lecturer** 2011–2015
*Boston University: Logic Design, Computer Architecture*
Designed final projects, provided lab help, and delivered guest lectures on Verilog to undergraduate and graduate students.

## Research

**Designing Energy-Efficient Computing Systems using Equalization and Machine Learning** 2012–Present

This research focuses on designing energy-efficient hardware for mobile applications by utilizing feedback equalization and machine learning algorithms to dynamically adapt to energy budgets.

[2016] Takhirov, Z., Joshi, A. J. *"On Feedback Equalization in Digital Logic for the Above-Threshold Voltage Range"*, TVLSI'16, **in preparation**

[2016] Takhirov, Z., Wang, J., Saligrama, V., and Joshi, A. J. *"Energy-Efficient Adaptive Classifier Design for Mobile Systems"*, ISLPED'16, **under review**

[2013] Takhirov, Z., Nazer, B., and Joshi, A. J. *"Energy-efficient pass-transistor-logic using decision feedback equalization"*, ISLPED'13

[2012] Takhirov, Z., Nazer, B., and Joshi, A. J. *"Error mitigation in digital logic using a feedback equalization with Schmitt trigger (FEST) circuit"*, ISQED'12

[2011] Takhirov, Z., Nazer, B., and Joshi, A. J. *"A preliminary look at error avoidance in digital logic via feedback equalization"*, Allerton'11

## Projects

**RISC-V & Accelerator System Design** *in progress*
**"NSFW" Programming Language** *in progress*
**Quadcopter with Machine Learning Navigation** Spring 2015
**Background Subtraction on FPGA** Fall 2013
**Handwriting Calculator using ANN on FPGA** Fall 2013