ZAFAR M. TAKHIROV

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SKILLS

- Programming languages: C/C++, Assembly, Python, Verilog HDL, SystemVerilog, SPICE;
- Applications/Tools: Xilinx ISE, Cadence Virtuoso/Encounter, HSPICE, Spectre, UVM, RNM;
- Natural Languages: English, Tajik, German, Russian, Turkish;

WORK AND RESEARCH EXPERIENCE

Boston University Sep, 2011 - Present
Research Assistant *Boston, MA*

· Thesis: Error Mitigation in ultra-low power digital circuits using feedback systems and dynamic voltage and frequency scaling (DVFS)
· Introduced a novel approach to ultra-low-power equalized computation using pass-transistor logic that allowed for up to 30% lower energy consumption
· Developed a novel approach to error mitigation (FEST), tested on Spartan 6 FPGA and taped-out ASIC using GF 130nm technology. Results showed up to 40% reduction in power dissiption in FIR filters
· Developed equalized interconnect for manycore systems; ASIC taped-out using UMC 130nm technology
· Worked on error-correcting codes in sub-micron technology nodes

Analog Devices, Inc. Feb, 2014 - Feb, 2015
Mixed-Signal Verification Engineer *San Jose, CA*

· Designed mixed-signal blocks using Cadence Virtuoso and Verilog HDL
· Created real-number models (RNM) for analog blocks and digital systems (SystemVerilog)
· Was responsible for verification strategy and methodologies (UVM, Formal Verification, RNM)
· Wrote scripts to automate simulation flow using BASH and Python

Analog Devices, Inc. May, 2013 - Dec,2013
Mixed-Signal Design Engineering Intern *San Jose, CA*

· Designed mixed-signal blocks using Cadence Virtuoso and Verilog
· Was involved in complete digital design flow (RTL, simulation, synthesis, fault analysis, timing, DRC, LVS), as well as test vector generation and fault injection
· Was involved in real-number modeling and behavioral model generation and simulation

EDUCATION

Boston University 2012 - Present
Ph.D., Electrical and Computer Engineering

· Dissertation (projected): "Error Mitigation in Ultra-Low Power Many-Core Digital Systems"

Boston University 2009 - 2012
M.S., Electrical and Computer Engineering *GPA: 3.5*

· Thesis: "Equalization in High Speed Communications Networks"

Russian-Tajik (Slavonic) University 2003 - 2008
Specialist, Linguistics *GPA: 4.0*

· Thesis: "Neologisms and Slang in German Languages"

PUBLICATIONS

- Z. Takhirov, B. Nazer and A. Joshi, "Energy-Efficient Pass-Transistor-Logic Using Decision Feedback Equalization," *International Symposium on Low Power Electronics and Design (ISLPED)*, 2013.
- A. Joshi, C. Chen, Z. Takhirov, B. Nazer, "A Multi-Layer Approach to Green Computing: Designing Energy-Efficient Digital Circuits and Manycore Architectures," *Proc. Workshop on Lighter-than-Green Dependable Multicore Architectures (LGDMA)*. Held in conjunction with *International Green Computing Conference (IGCC)*, 2012 **(Invited Paper)**.
- Z. Takhirov, B. Nazer and A. Joshi, "Error Mitigation in Digital Logic using Feedback Equalization with Schmitt Trigger (FEST) Circuit," *Proc. IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2012.
- Z. Takhirov, B. Nazer and A. Joshi, "A Preliminary Look at Error Avoidance in Digital Logic Via Feedback Equalization," *in Proc. Allerton-11*, September 2011. **(Invited Paper)**.

OTHER PROJECTS

- **RISC-V Manycore System Tapeout:** *(In progress)* 64-core RISC-V processor using photonic interconnect. Research in progress - tapeout scheduled December 2015 using 40nm process technology.
- **"NSFW" Programming Language:** *(In progress)* Toy programming language (esoteric) created using Flex, Bison, and LLVM. Currently in progress and is scheduled for August 2015.
- **Hardware Background Subtraction DSP using FPGA:** *(Complete)* Implemented image background subtraction algorithm on Xilinx Spartan 6 chip (using Verilog HDL). Two step process was developed: dynamic background detection and background subtraction using background filtering.
- **Handwriting Calculator using ANN on FPGA:** *(Complete)* Using Verilog HDL a hardware ANN was developed and trained to recognize handwritten digits.
- **Microstrip PCB 1-GHz Receiver/Transmitter (ASIC/PCB):** *(Complete)* Designed using Altium ISE. Design included HF PLL synthesizer, patch antena, RF power amplifier. Testing performed using Agilent instrumentation (oscilloscope, spectrum/network/logic analyzers).

TEACHING EXPERIENCE

- Teaching Fellow for Logic Design course (09/2010 to 12/2012): Taught 100 students the basics of digital logic design, Verilog programming, as well as supervised final projects. Main topics included: SPI/I2C communication, single-cycle processors, and image filters development on FPGAs.
- Teaching Fellow for Computer Architecture course (09/2012 to 12/2012): Taught 45 students RISC architecture, microprocessor design (pipelining, multi-cycle execution, instruction set design) design-for-test, as well as microprocessor test automation.