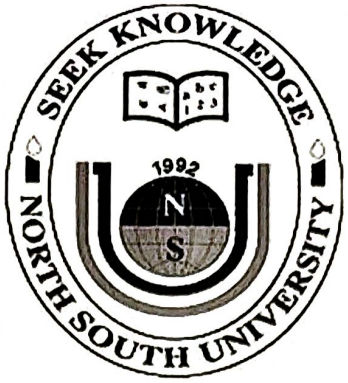


North South University
Department of Electrical & Computer Engineering

PROJECT REPORT

Course Code: *CSE231L*

Course Title: *Digital Logic Design Lab*

Section: *04*

Project Name:

Display "CSE231-9" in 7 Segment Display

Date of Submission: *April, 2022*

Submitted by Group Number: *09*

Group members:

1. ***Zobaer Ahammod Zamil*, ID: *2021796642***
2. *Al Nahian Niloy*, **ID:** *2031445642*
3. *Osmita Monzur Subonty*, **ID:** *2011708642*

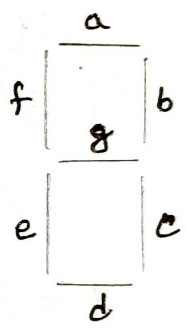
Course Instructor: Md. Shahriar Hussain (HSM)

Submitted To: Md. Anisur Rahman Asif

We have to print "CSE231-9" in 7 segment display. Here is the truth table for it, where A, B, C will be input and, a, b, c, d, e, f, g will be output.

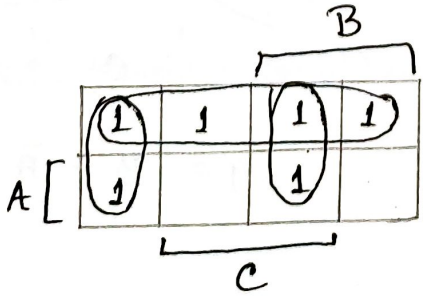
Truth Table :

A	B	C	a	b	c	d	e	f	g	output
0	0	0	1	0	0	1	1	1	0	C
0	0	1	1	0	1	1	0	1	1	S
0	1	0	1	0	0	1	1	1	1	E
0	1	1	1	1	0	1	1	0	1	2
1	0	0	1	1	1	1	0	0	1	3
1	0	1	0	1	1	0	0	0	0	1
1	1	0	0	0	0	0	0	0	1	-
1	1	1	1	1	1	1	0	1	1	9



7 segment display

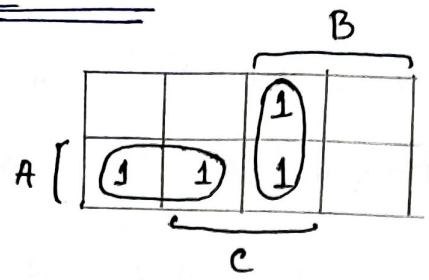
K-maps :



$a = \bar{A} + BC + \bar{B}\bar{C}$

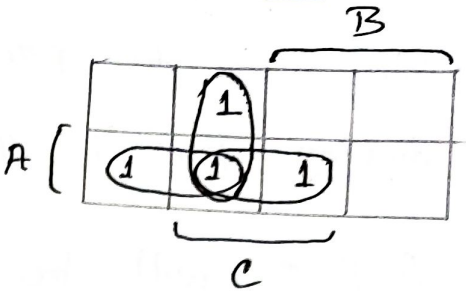
for a

For b :



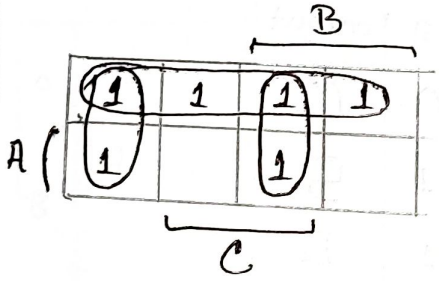
$b = A\bar{B} + BC$

For c :



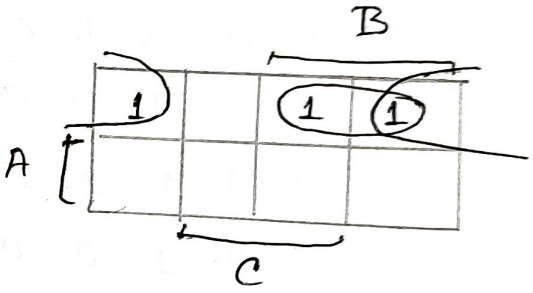
$c = A\bar{B} + AC + \bar{B}C$

For d :



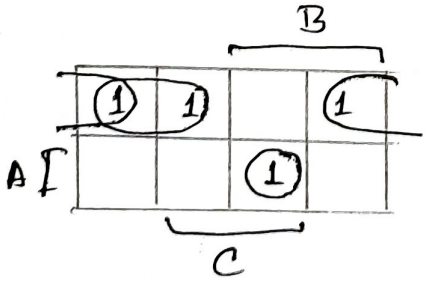
$d = \bar{A} + BC + \bar{B}\bar{C}$

For e :



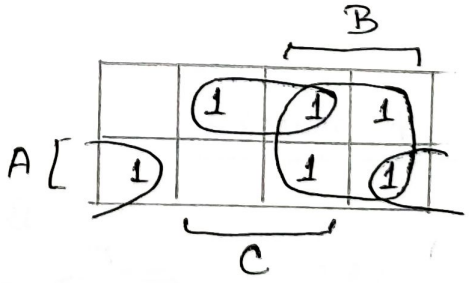
$e = \bar{A}B + \bar{A}\bar{C}$

For f :



$f = ABC + \bar{A}\bar{B} + \bar{A}\bar{C}$

For g :



$g = B + \bar{A}C + A\bar{C}$

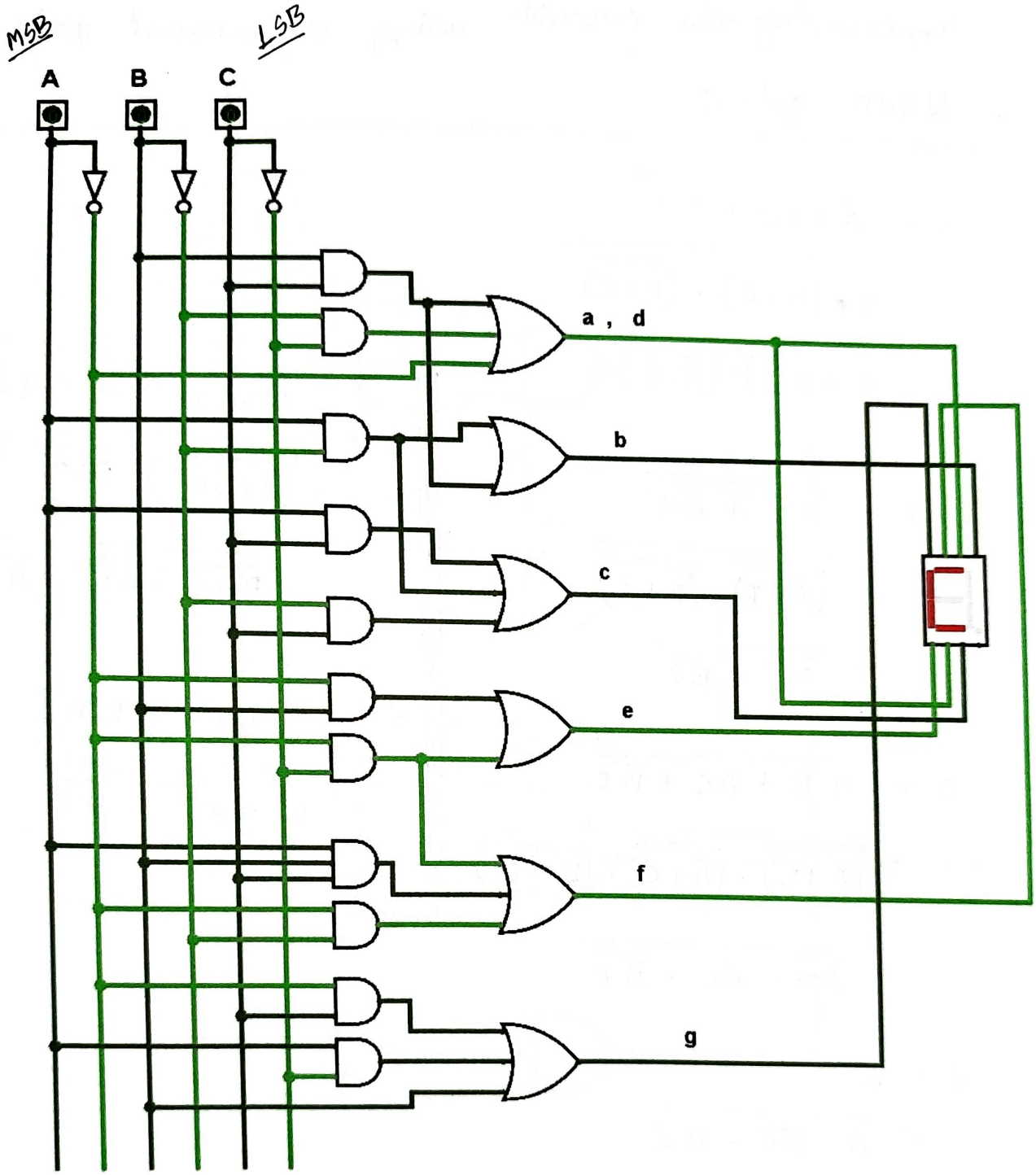


Figure P.1: ***Implementation of 7 segment circuit using Basic GATES***

Implementing the circuit using universal gate NAND gates:

$$a = \overline{\overline{A + BC + \bar{B}\bar{C}}}$$

$$= A \cdot \overline{\overline{(\bar{B}+\bar{C})} \cdot \overline{(B+C)}}$$

$$= A \cdot (\bar{B}\cdot\bar{C}) \cdot (\bar{\bar{B}}\cdot\bar{\bar{C}})$$

$$b = \overline{\overline{A\bar{B} + BC}}$$

$$= \overline{\overline{(\bar{A}+B)} \cdot \overline{(\bar{B}+\bar{C})}}$$

$$= \overline{A\bar{B} \cdot \bar{B}C}$$

$$c = \overline{\overline{A\bar{B} + AC + \bar{B}C}}$$

$$= \overline{\overline{(\bar{A}+B)} \cdot \overline{(\bar{A}+\bar{C})} \cdot \overline{(B+\bar{C})}}$$

$$= \overline{A\bar{B} \cdot \bar{A}C \cdot \bar{B}C}$$

$$d = a$$

$$= \overline{A \cdot \bar{B}\bar{C} \cdot \bar{B}\bar{\bar{C}}}$$

$$e = \overline{\overline{\bar{A}B + \bar{A}\bar{C}}}$$

$$= \overline{\overline{A+\bar{B}} \cdot \overline{A+C}}$$

$$= \overline{\bar{A}B \cdot \bar{A}\bar{C}}$$

$$f = \overline{\overline{ABC + \bar{A}\bar{B} + \bar{A}\bar{C}}}$$

$$= \overline{\overline{(\bar{A}+\bar{B}+\bar{C})} \cdot \overline{A+B} \cdot \overline{A+C}}$$

$$= \overline{ABC \cdot \bar{A}\bar{B} \cdot \bar{A}\bar{C}}$$

$$g = B + \bar{A}C + A\bar{C}$$

$$= \overline{\bar{B} \cdot \bar{A}C \cdot A\bar{C}}$$

NAND

P-5

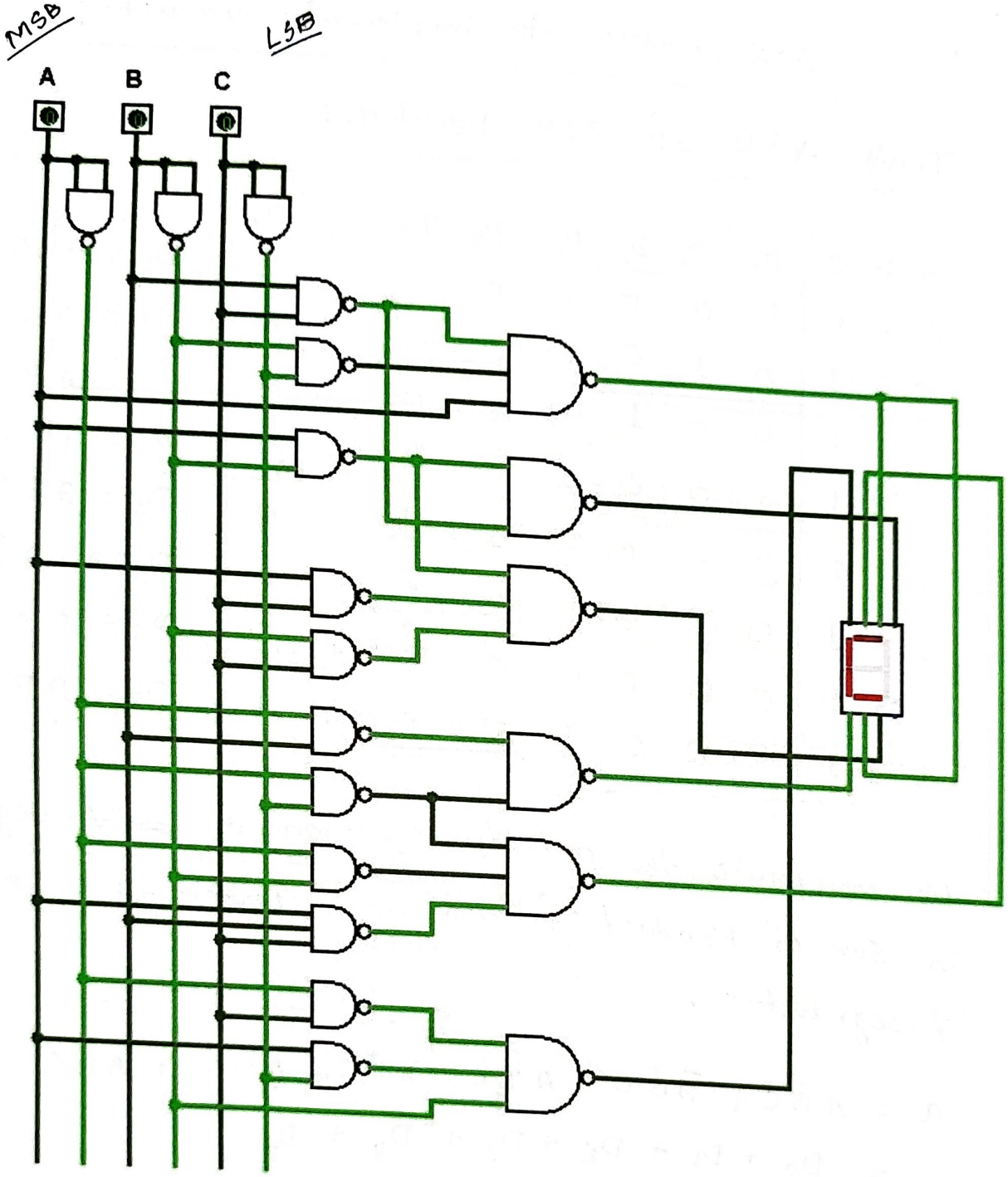


Figure P.2: ***Implementation of 7 segment circuit using Universal GATE (NAND GATE)***

P-6

Using 3:8 Decoders to implement circuit:

Truth table of 3:8 Decoders:

A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

$D_0 = \bar{A}\bar{B}\bar{C}$

$D_1 = \bar{A}\bar{B}C$

$D_2 = \bar{A}B\bar{C}$

$D_3 = \bar{A}BC$

$D_4 = A\bar{B}\bar{C}$

$D_5 = A\bar{B}C$

$D_6 = AB\bar{C}$

$D_7 = ABC$

We can write the outputs equation of ~~se~~ 7-segment in sum of Product form, from Truth table of 7-segment.

$$a = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + ABC$$
$$= D_0 + D_1 + D_2 + D_3 + D_4 + D_7$$

$$b = \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C + ABC = D_3 + D_4 + D_5 + D_7$$

$$c = \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + ABC = D_1 + D_4 + D_5 + D_7$$

$$d = a = D_0 + D_1 + D_2 + D_3 + D_4 + D_7$$

$$e = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC = D_0 + D_2 + D_3$$

$$f = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC = D_0 + D_1 + D_2 + D_7$$

$$g = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C} + ABC$$
$$= D_1 + D_2 + D_3 + D_4 + D_6 + D_7$$

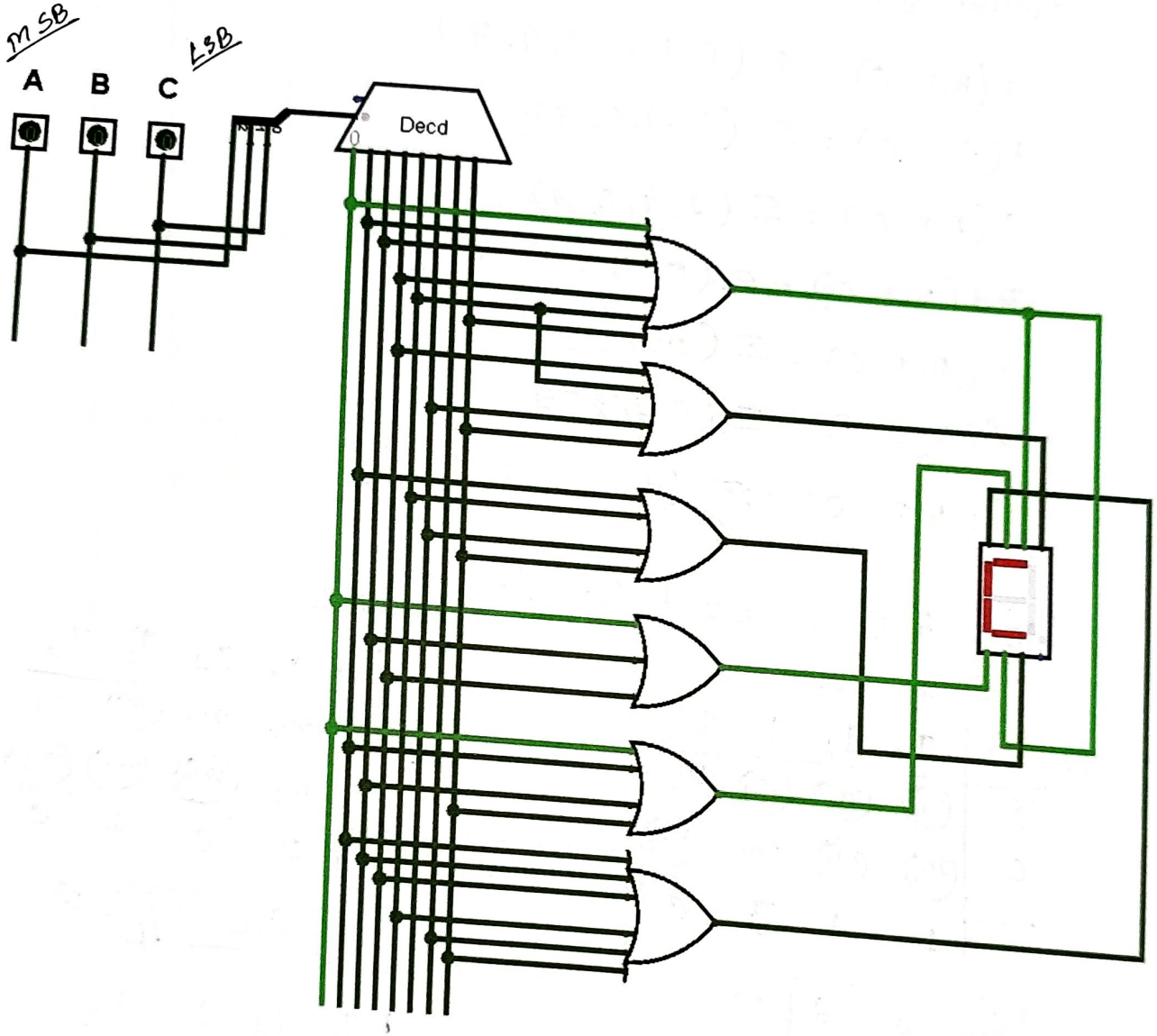


Figure P.3: ***Implementation of 7 segment circuit using 3 to 8 Line Decoder***

P-8

Implementing 8 circuit using 8×1 MUX :

output functions are,

$a(A,B,C) = \Sigma(0,1,2,3,4,7)$

$b(A,B,C) = \Sigma(3,4,5,7)$

$c(A,B,C) = \Sigma(1,4,5,7)$

$d(A,B,C) = \Sigma(0,1,2,3,4,7)$

$e(A,B,C) = \Sigma(0,2,3)$

$f(A,B,C) = \Sigma(0,1,2,7)$

$g(A,B,C) = \Sigma(1,2,3,4,6,7)$

Let, A, B be select bit for all.

	I_0	I_1	I_2	I_3
$\bar{C}$	m_0	m_2	m_4	m_6
C	m_1	m_3	m_5	m_7
	1	1	$\bar{C}$	C

for a, d

	I_0	I_1	I_2	I_3
$\bar{C}$	m_0	m_2	m_4	m_6
C	m_1	m_3	m_5	m_7
	0	C	1	C

for b

	I_0	I_1	I_2	I_3
$\bar{C}$	m_0	m_2	m_4	m_6
C	m_1	m_3	m_5	m_7
	C	0	1	C

for c

	I_0	I_1	I_2	I_3
$\bar{C}$	m_0	m_2	m_4	m_6
C	m_1	m_3	m_5	m_7
	1	$\bar{C}$	0	C

for f

	I_0	I_1	I_2	I_3
$\bar{C}$	m_0	m_2	m_4	m_6
C	m_1	m_3	m_5	m_7
	$\bar{C}$	1	0	0

for e

	I_0	I_1	I_2	I_3
$\bar{C}$	m_0	m_2	m_4	m_6
C	m_1	m_3	m_5	m_7
	C	1	$\bar{C}$	1

for g

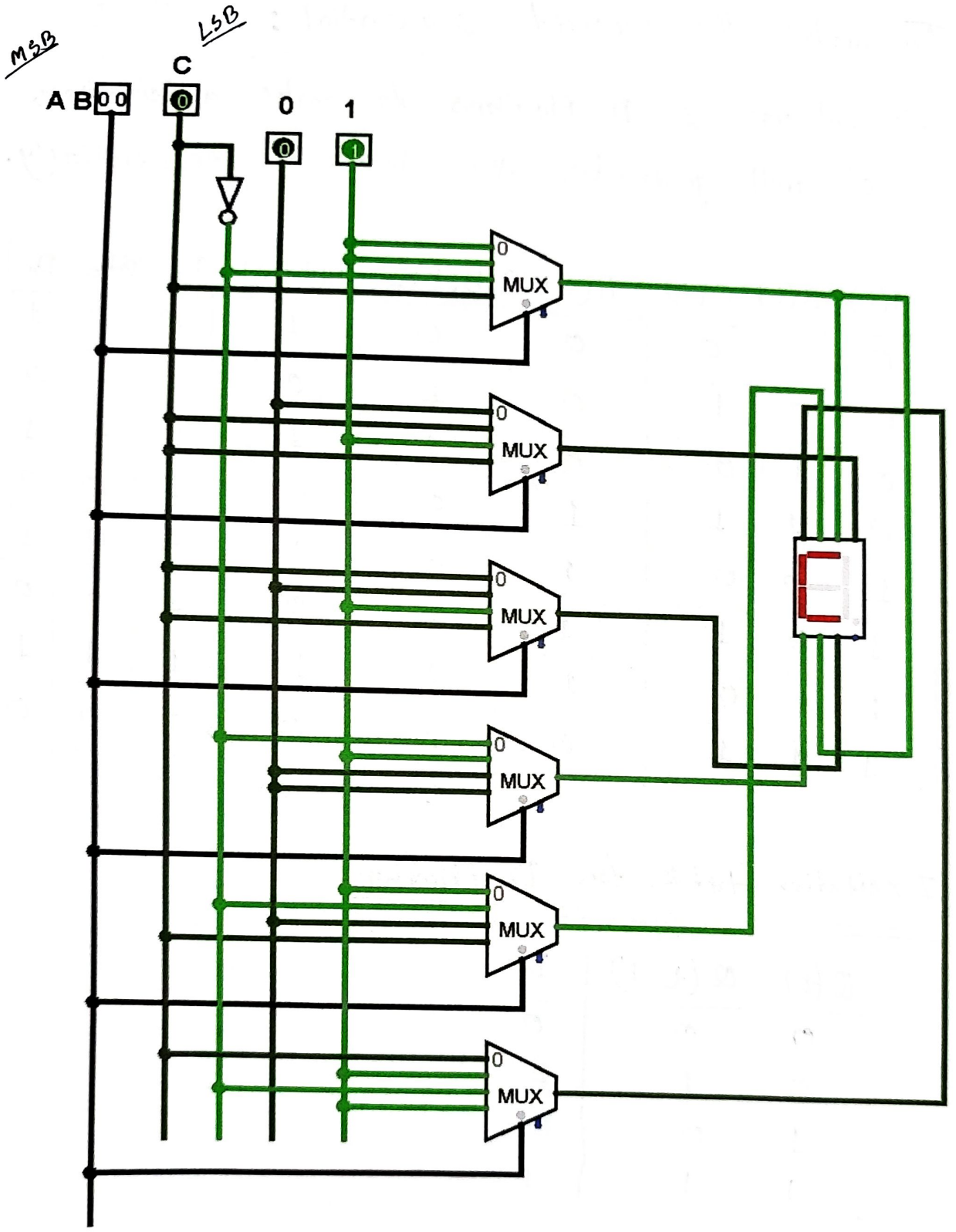


Figure P.4: ***Implementation of 7 segment circuit using 4:1 Multiplexers***

To make the circuit sequential :

We will use 3 D-Flipflops to make a counter which will generate the inputs sequentially.

A(t)	B(t)	C(t)	A(t+1)	B(t+1)	C(t+1)	D_A	D_B	D_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

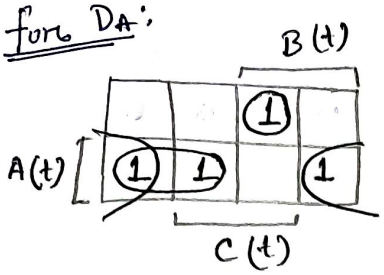
Excitation table for D-flipflop :

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

After using this counter, we can see the output "CSE231-9" sequentially.

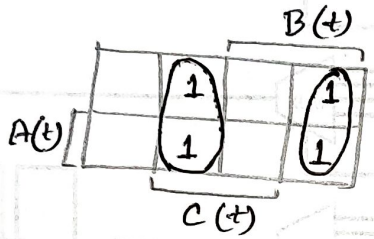
K-maps :

for D_A :

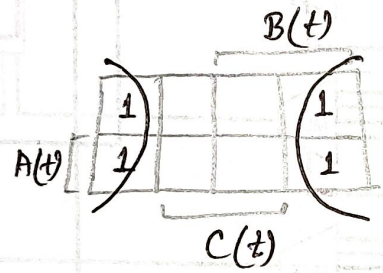


$$D_A = A(t)\cdot\bar{B}(t) + A(t)\,\bar{C}(t) + \bar{A}(t)\cdot B(t)\,C(t)$$

for D_B :



$$D_B = \bar{B}(t)\,C(t) + B(t)\,\bar{C}(t)$$



$$D_C = \bar{C}(t)$$

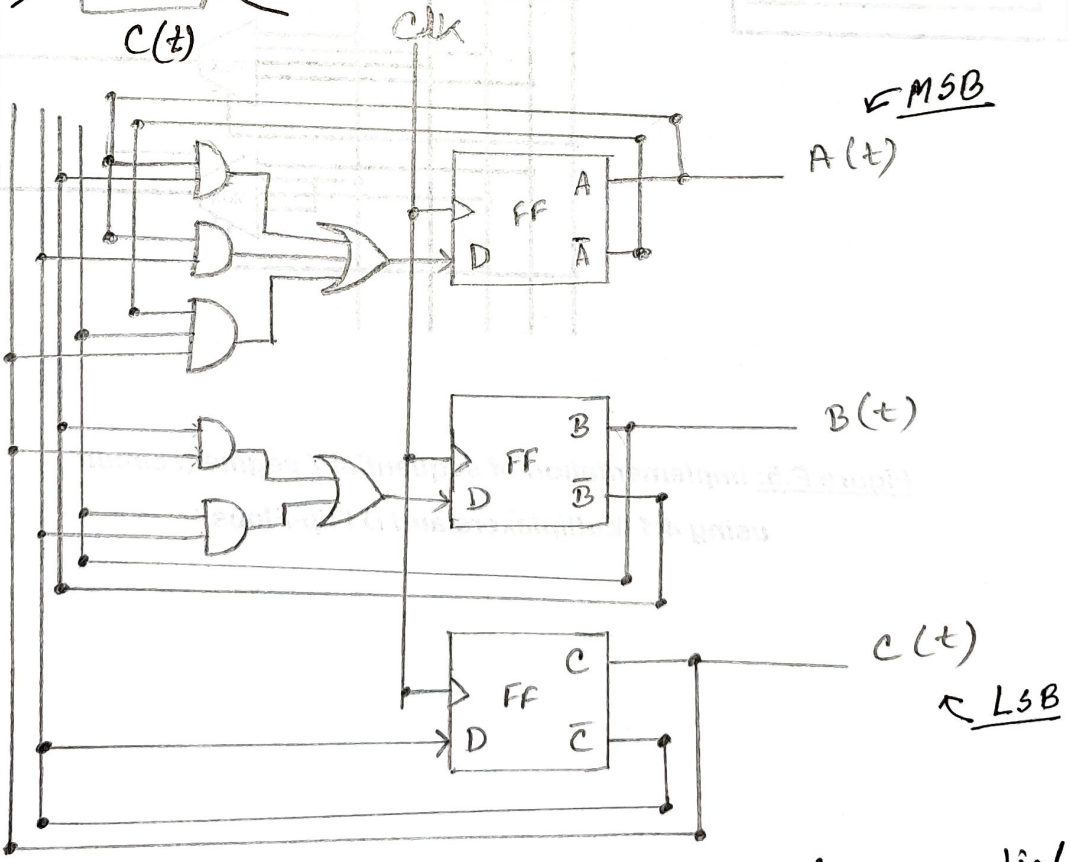


Fig: Counter for 7 segment sequential circuit

P-12

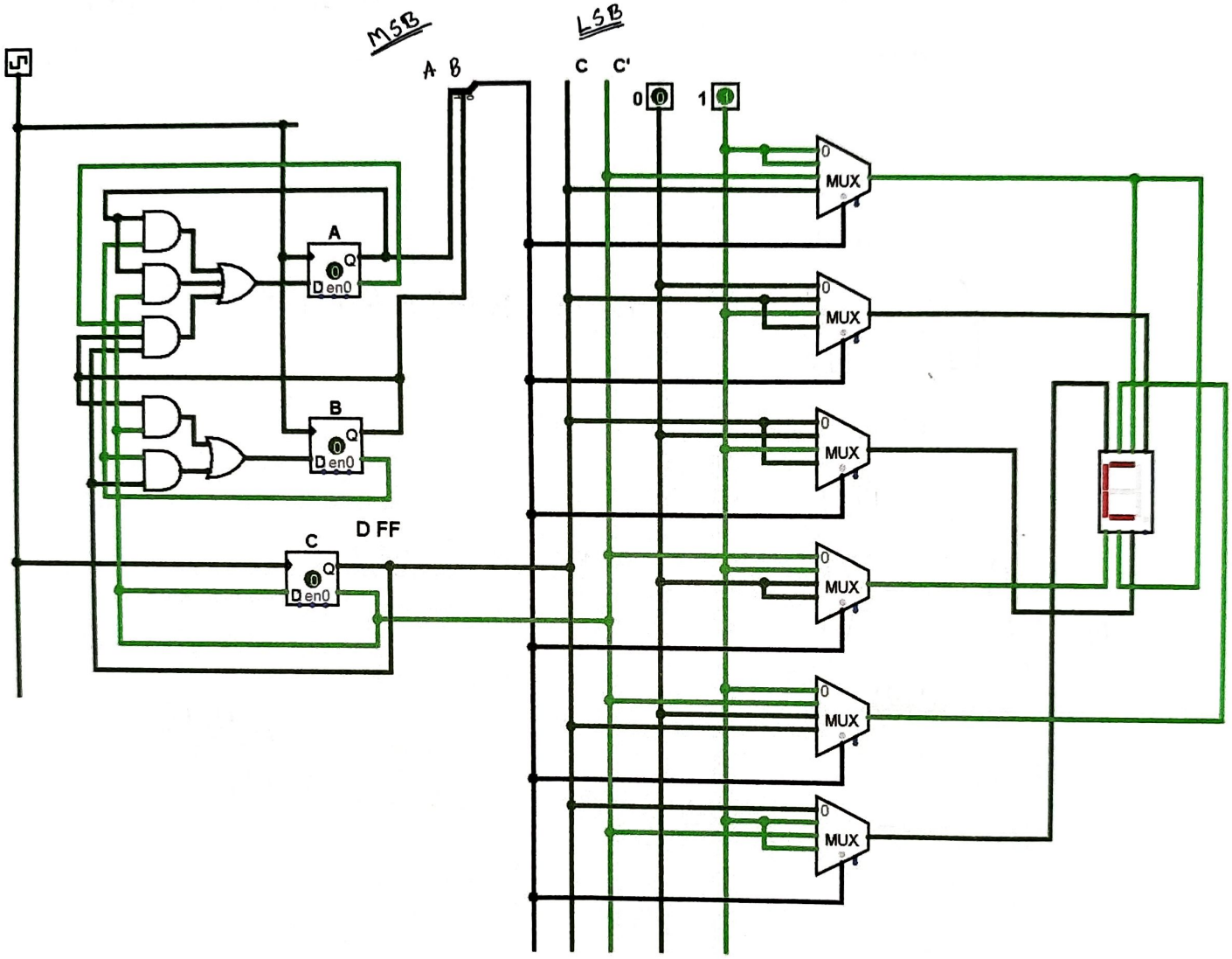


Figure P.5: ***Implementation of sequential 7 segment circuit using 4:1 Multiplexers and D Flip-Flops***