ECE260B Winter 22

Synthesis

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Announcement

- Resuming In-person lecture next week.
  - All the lecture will be recorded and will be posted right after class
  - Office hours will be still in remote

- Discussion tab etiquette
  - Describe the title in detail, e.g., good: “missing nmos / pmos in hspice sim”, vs. bad: “HW1 Q2”
  - Before posting a question
    1. Please see previous discussion thread first
    2. Please watch demonstration video + homework explanation video during class

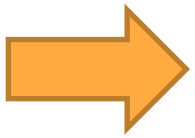
Synthesis

aes_rcon.v (~/cs241data/design/aes_cipher_top/rtl) - G

File Edit Tools Syntax Buffers Window Help

```
`timescale 1ns / 10ps

module aes_rcon(clk, kld, out);
input           clk;
input           kld;
output  [31:0]  out;
reg     [31:0]  out;
reg     [3:0]   rcnt;
wire    [3:0]   rcnt_next;

always @(posedge clk)
        if(kld)         out <= #1 32'h01_00_00_00;
        else            out <= #1 frcon(rcnt_next);

assign rcnt_next = rcnt + 4'h1;
always @(posedge clk)
        if(kld)         rcnt <= #1 4'h0;
        else            rcnt <= #1 rcnt_next;

function [31:0] frcon;
input   [3:0]   i;
case(i) // synopsys parallel_case
   4'h0: frcon=32'h01_00_00_00;
   4'h1: frcon=32'h02_00_00_00;
```

behavioral code (RTL description)



synthesis

aes_cipher_top.out.v (~/lab2/run0) - GVIM4

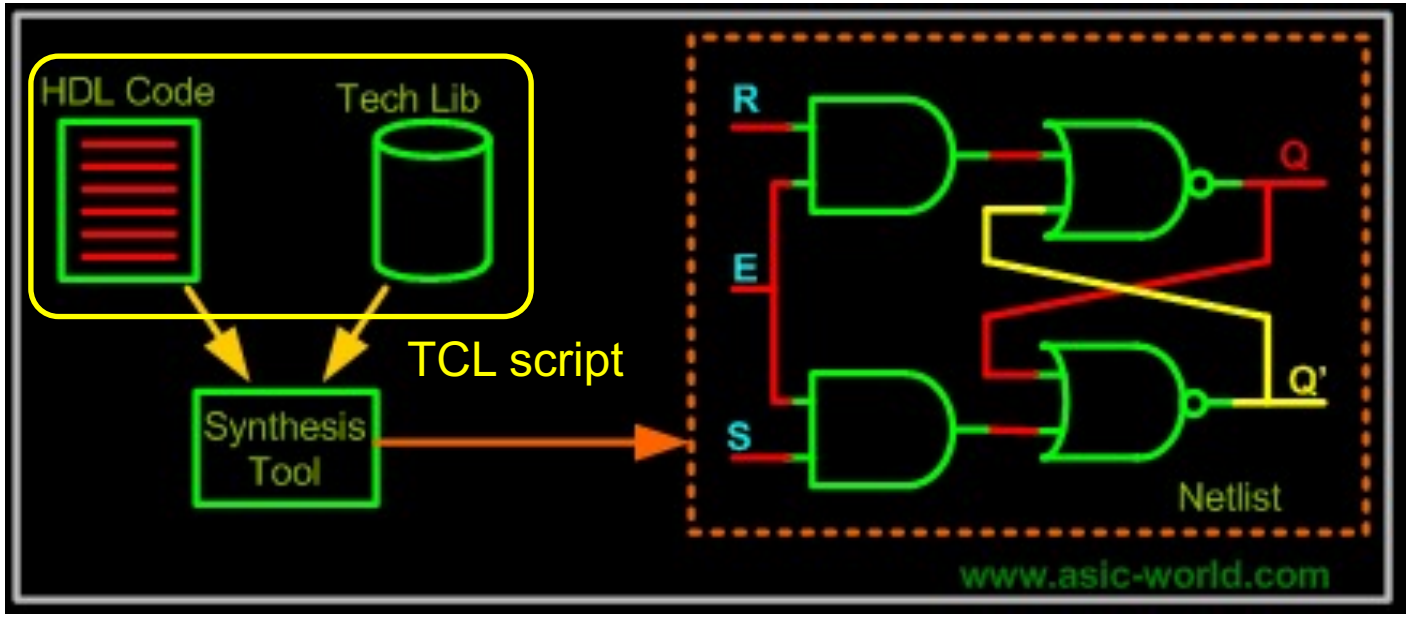
File Edit Tools Syntax Buffers Window Help

```
//////////////////////////////////////////////////////////////////
// Created by: Synopsys DC Ultra(TM) in wire load mode
// Version   : K-2015.06-SP2
// Date      : Wed Dec 15 12:51:16 2021
//////////////////////////////////////////////////////////////////


module aes_rcon ( clk, kld, out );
  output [31:0] out;
  input clk, kld;
  wire   n_Logic0_, N71, N72, N73, N74, N75, N78, n1, n2, n3, n5, n15, n18,
         n19, n4, n6, n7, n8, n9, n10, n11, n12, n13, n14;
  wire   [3:0] rcnt;

  DFQD1 out_reg_23_ ( .D(n_Logic0_), .CP(clk), .Q(out[23]) );
  DFQD1 out_reg_22_ ( .D(n_Logic0_), .CP(clk), .Q(out[22]) );
  DFQD1 out_reg_21_ ( .D(n_Logic0_), .CP(clk), .Q(out[21]) );
  DFQD1 out_reg_20_ ( .D(n_Logic0_), .CP(clk), .Q(out[20]) );
  DFQD1 out_reg_19_ ( .D(n_Logic0_), .CP(clk), .Q(out[19]) );
  DFQD1 out_reg_18_ ( .D(n_Logic0_), .CP(clk), .Q(out[18]) );
  DFQD1 out_reg_17_ ( .D(n_Logic0_), .CP(clk), .Q(out[17]) );
  DFQD1 out_reg_16_ ( .D(n_Logic0_), .CP(clk), .Q(out[16]) );
  DFQD1 out_reg_15_ ( .D(n_Logic0_), .CP(clk), .Q(out[15]) );
```

gate-level netlist

- Synthesis: generating gate-level netlist by using STD cells

Commercial Synthesis Tools



- Synopsys Design Compiler (DC): will be used in this class
- Cadence Genus
- TCL script: provides the RTL code and libs for synthesis tool

Example of run_dc.tcl

1)
2)
3)

run_dc.tcl (~/lab2/run0) - GVIM

```
set top_module aes_cipher_top
set rtlPath "/home/linux/ieng6/ee260bwi22/ee260bwi22/cs241data/design/aes_cipher_top/rtl"

# Target library
set target_library /home/linux/ieng6/ee260bwi22/ee260bwi22/cs241data/libraries/db/tcbn65gpluswc.db
set link_library $target_library
set symbol_library {}
set wire_load_mode enclosed
set timing_use_enhanced_capacitance_modeling true

set search_path [concat $rtlPath $search_path]
set link_library [concat * $link_library ]

set synthetic_library {}
set link_path [concat  $link_library $synthetic_library]
set dont_use_cells 1
set dont_use_cell_list ""

remove_design -all
```

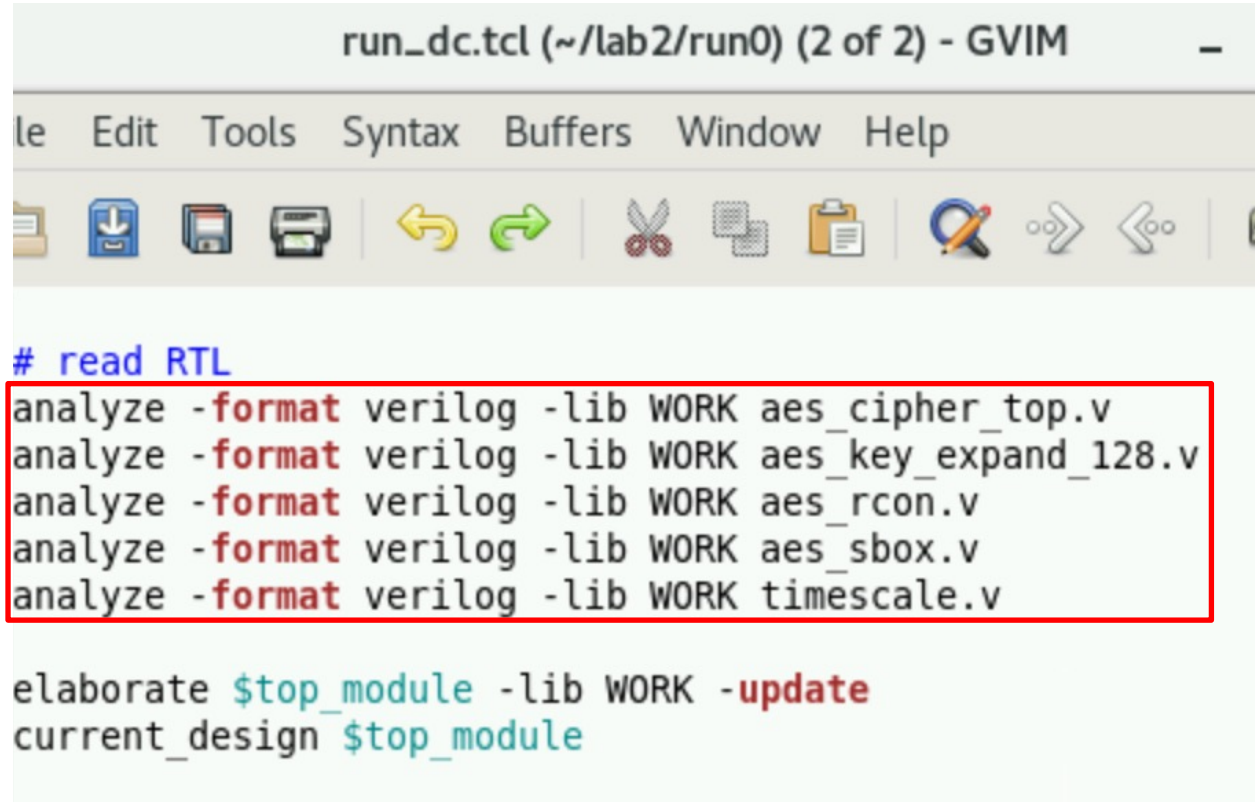
- 1) top module name for RTL
- 2) RTL path
- 3) Technology library (db file, this is the same contents with lib file)

Example of Library Files

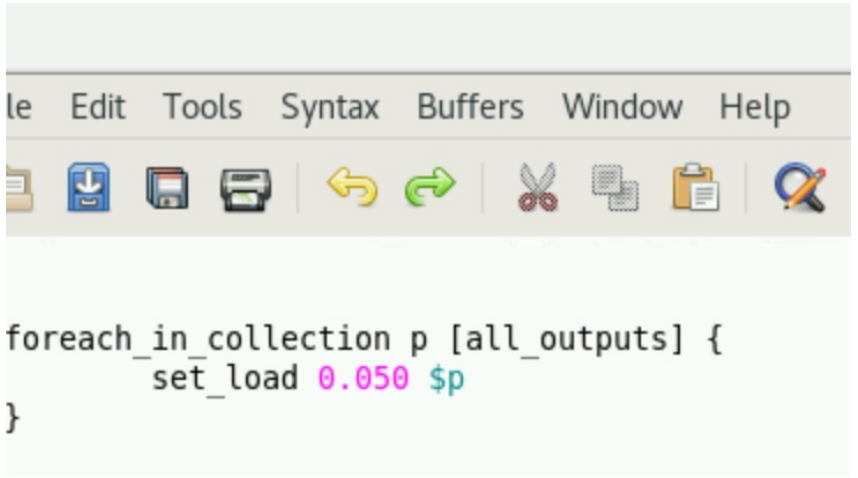
- tcbn65gpluswc.lib (or .db): worst corner (0.9V 125℃)
- tcbn65gplustc.lib (or .db): typical corner (1V 25℃)
- tcbn65gplusbc.lib (or .db): best corner (1.1V 0℃)

- Can combine both for setup (w/ worst case lib) and hold time (w/ best case lib) analysis together
  - set_operating_conditions -max my_WORST_lib -max_library tcbn65gpluswc.lib
    -min my_BEST_lib -min_library tcbn65gplusbc.lib

Example of run_dc.tcl



4)



5)

- 4) RTL list
- 5) estimated output capacitance (unit: pF)

Example of run_dc.tcl

```
6) write -format verilog -hier -output [format "%s%s" $top_module .out.v]

   # Write Reports
7) redirect [format "%s%s%s" log/ $top_module _area.rep] { report_area }
8) redirect -append [format "%s%s%s" log/ $top_module _area.rep] { report_reference }
9) redirect [format "%s%s%s" log/ $top_module _power.rep] { report_power }
10)redirect [format "%s%s%s" log/ $top_module _timing.rep] \
```

up to three characters can be included, each word is separated by "/"

- 6) output gate netlist
- 7) area report
- 8) type of STD cells used (-append: add on the previous report)
- 9) power report
- 10) timing report

Other Options in run_dc.tcl

- “set_driving_cell -lib cell BUFFD8 -pin Z [all inputs]”
  - Assume that all of your inputs are driven by BUFFD8 cell

- “ungroup -flatten -all
  - RTL will be fully flattened for optimization
  - In a big system design, it can be slow compared to hierarchical synthesis

- “compile_ultra -no_autoungroup”
  - RTL hierarchy is maintained
  - Might be less optimized than flattened design

- set_false_path -from [get_ports ”reset"]
  - Exclude reset path from the timing calculation

sdc file

aes_cipher_top.sdc (~/lab2/run0) - GVIM1

File Edit Tools Syntax Buffers Window Help

```
set clock_cycle 1.2
set io_delay 0.2

set clock_port clk

create_clock -name clk -period $clock_cycle [get_ports $clock_port]

set_input_delay -clock [get_clocks clk] -add_delay -max $io_delay [get_ports {key[52]}]
set_input_delay -clock [get_clocks clk] -add_delay -max $io_delay [get_ports {key[45]}]
set_input_delay -clock [get_clocks clk] -add_delay -max $io_delay [get_ports {key[38]}]
```

period in ns

input delay, i.e., delay from clock rising edge to the delivered moment at the input pin

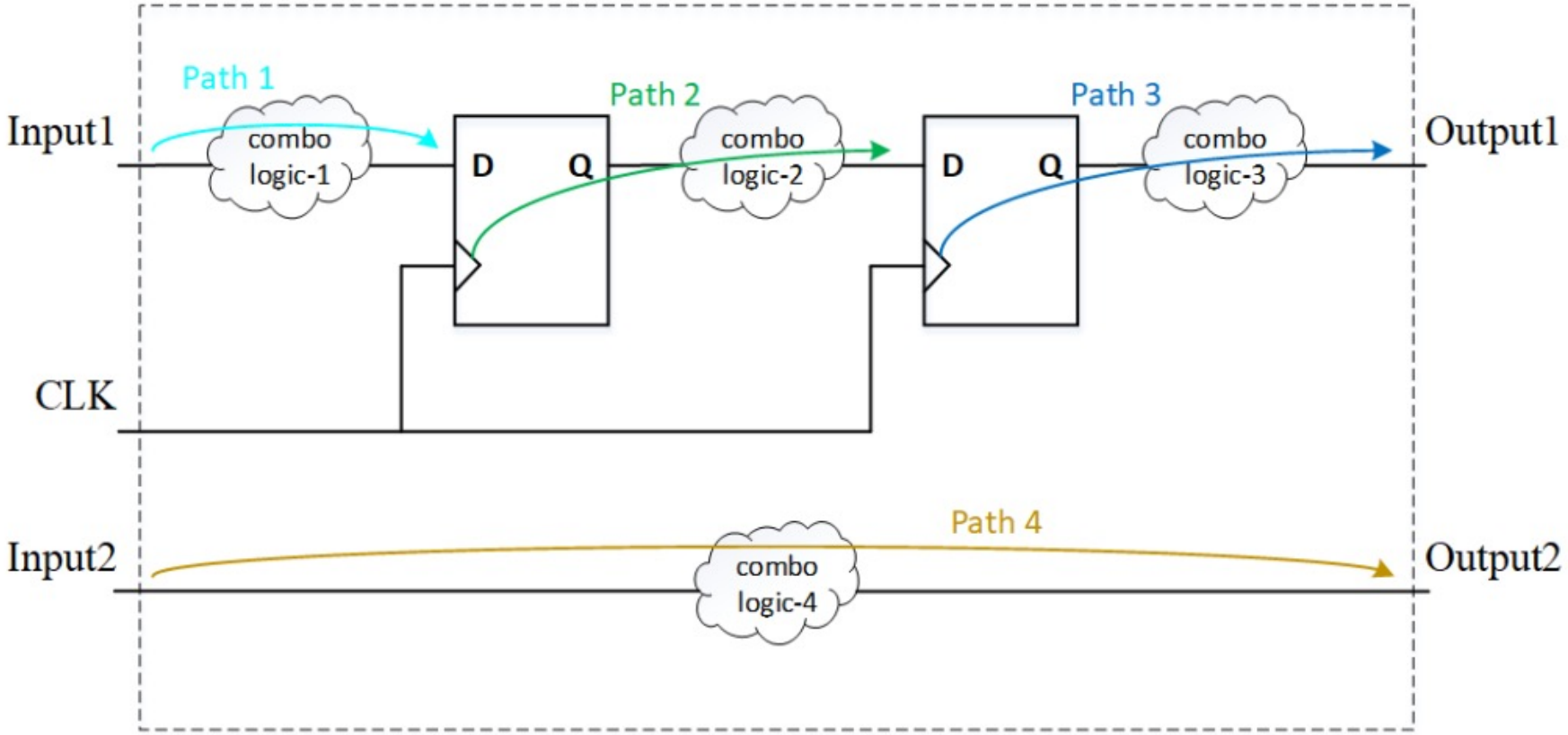
- This file can be included inside the run_dc.tcl file
- create_clock: clock from external source through a port
- create_generated_clock: clock generated internally
  - e.g., create_generated_clock -name my_clk_div2 -source $clk_port -divide_by 4 [get_pins CLK_SLOW_reg/Q]

Alternative Option for Input / Output Delay

```
set_input_delay  $io_delay -clock $clock_port [all_inputs]
set_output_delay $io_delay -clock $clock_port [all_outputs]
```

- set up all the inputs' and outputs' delay together as shown above

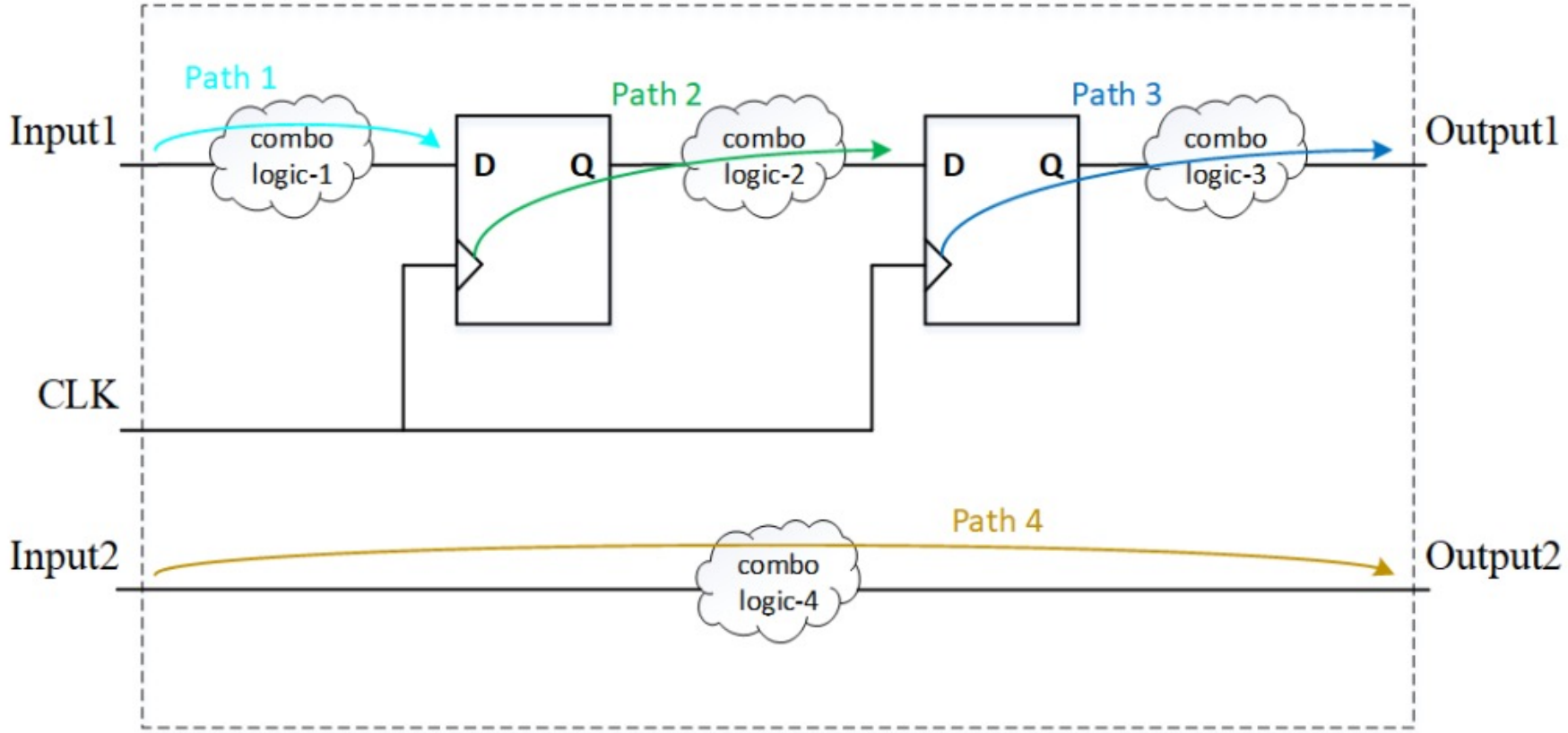
Cases of Delay Paths



https://vlsitutorials.com/constraining-timing-paths-in-synthesis-part-1/

- Startpoint
  - Input port (except a clock port) - Clock pin of flip-flop
- Endpoint
  - Output port - Any input pin (D) of a flip-flop

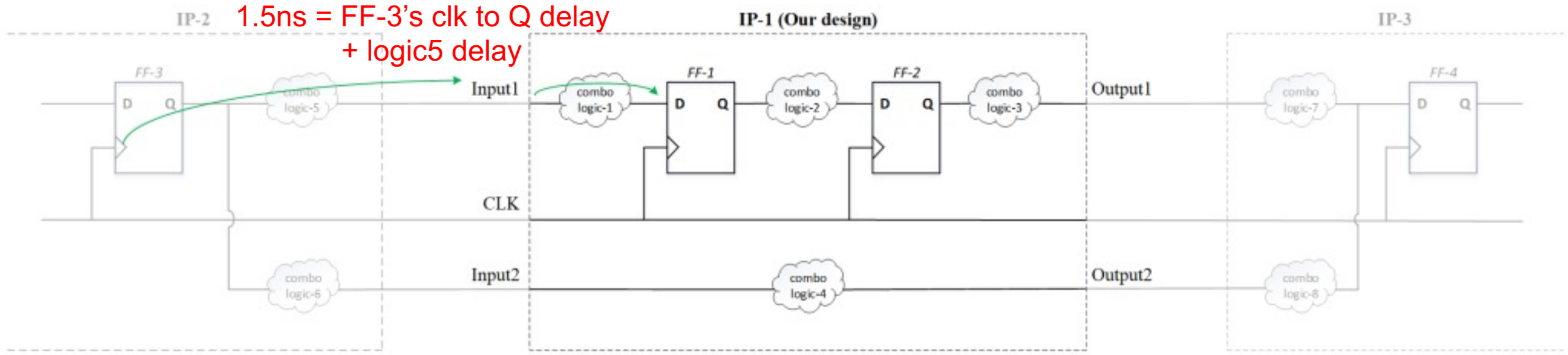
Cases of Delay Paths



https://vlsitutorials.com/constraining-timing-paths-in-synthesis-part-1/

- Path 1: Starts from an input port and ends in an input pin of flip-flop.
- Path 2: Starts from a clock pin of flip-flop and ends in an input pin of flip-flop.
- Path 3: Starts from a clock pin of flip-flop and ends in an output port.
- Path 4: Starts from an input port and ends in an output port.

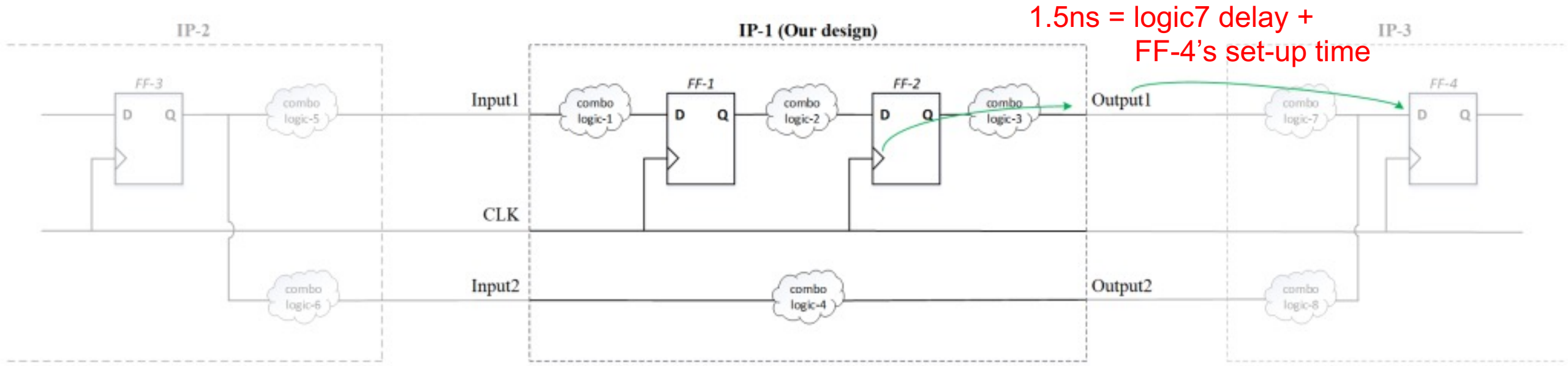
set_input_delay



https://vlsitutorials.com/constraining-timing-paths-in-synthesis-part-1/

- set_input_delay -max 1.5 -clock CLK [get_ports Input1]
- This time is reserved for the input signal delivered to the input of current block
- Thus, "clock_period - input_delay" is assigned for the for combo logic-1

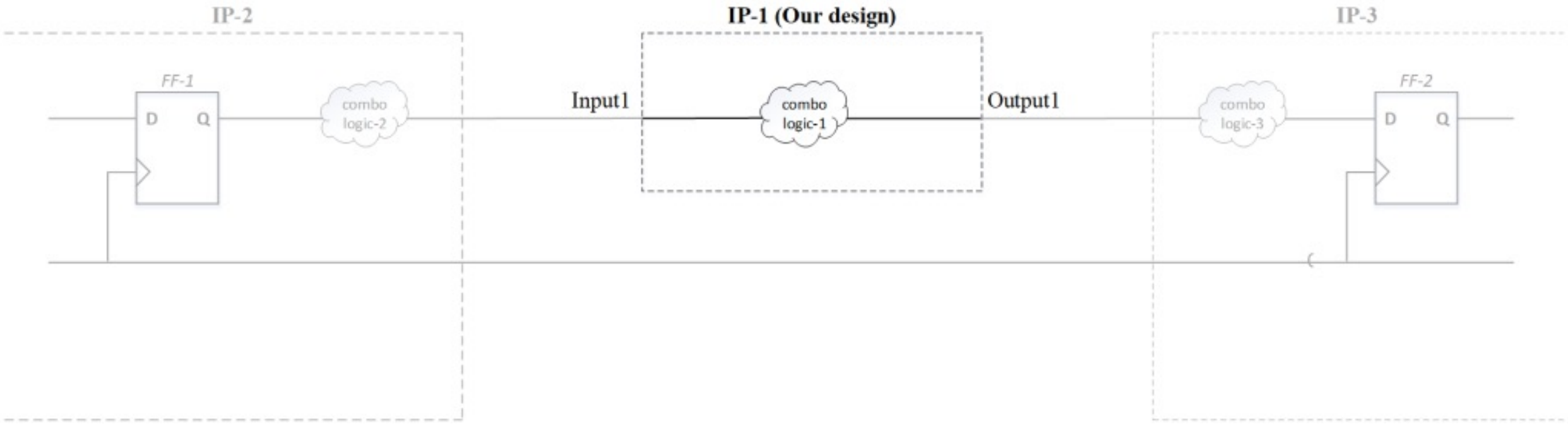
set_output_delay



https://vlsitutorials.com/constraining-timing-paths-in-synthesis-part-1/

- set_output_delay -max 1.5 -clock CLK [get_ports Output1]
- This time is reserved for the output signal delivered to the next block's input of flip flop
- Thus, the last logic part has only "clock_period - output_delay"

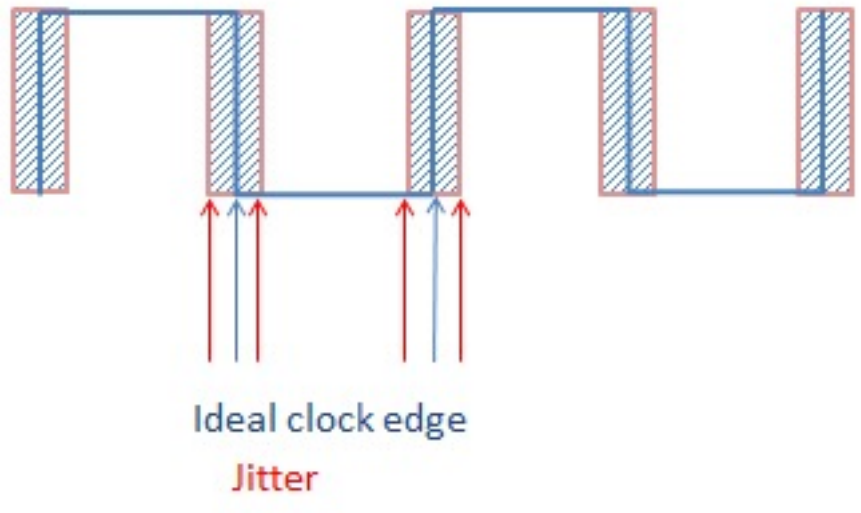
Design with Only Combinational Logics



virtual clock

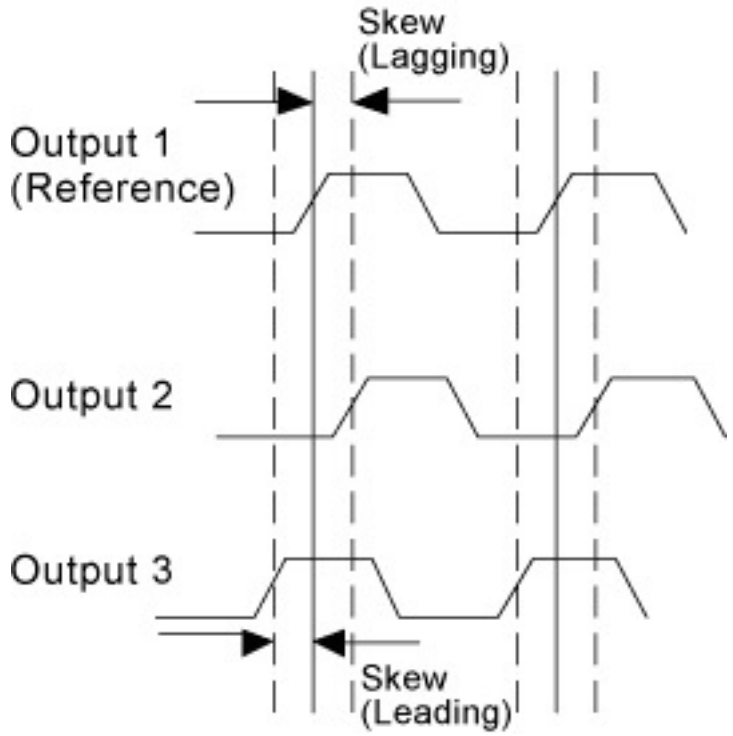
- create_clock -name VCLK -period 5
- set_input_delay -max 2 -clock VCLK [get_ports Input2]
- set_output_delay -max 2.5 -clock VCLK [get_ports Output2]

Clock Uncertainty



Clock jitter

https://vlsi.pro/clock-jitter/



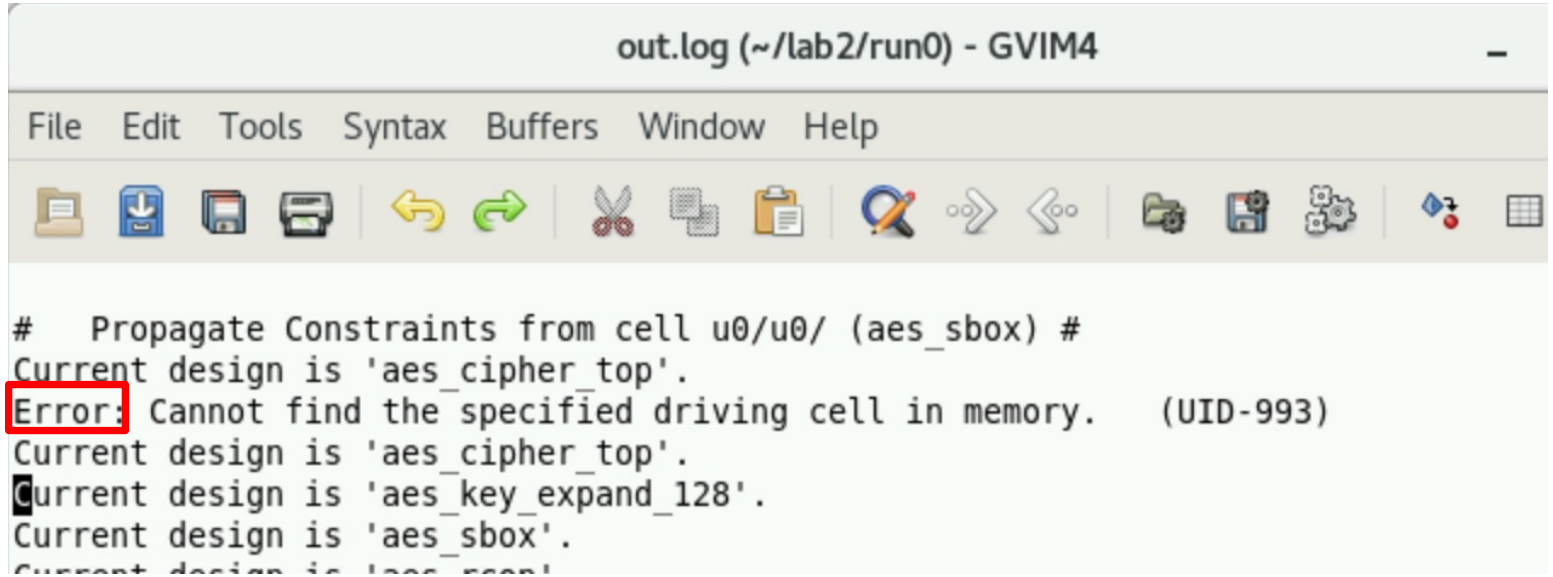
Clock skew

http://electronicsgurukulam.blogspot.com/2012/11/clock-skew-and-jitter-in-digital.html?m=1

- set_clock_uncertainty $T_{uncertain}$ [get_clocks <*clock*>]
  - To consider clock slew and jitter

Excuting run_dc.tcl

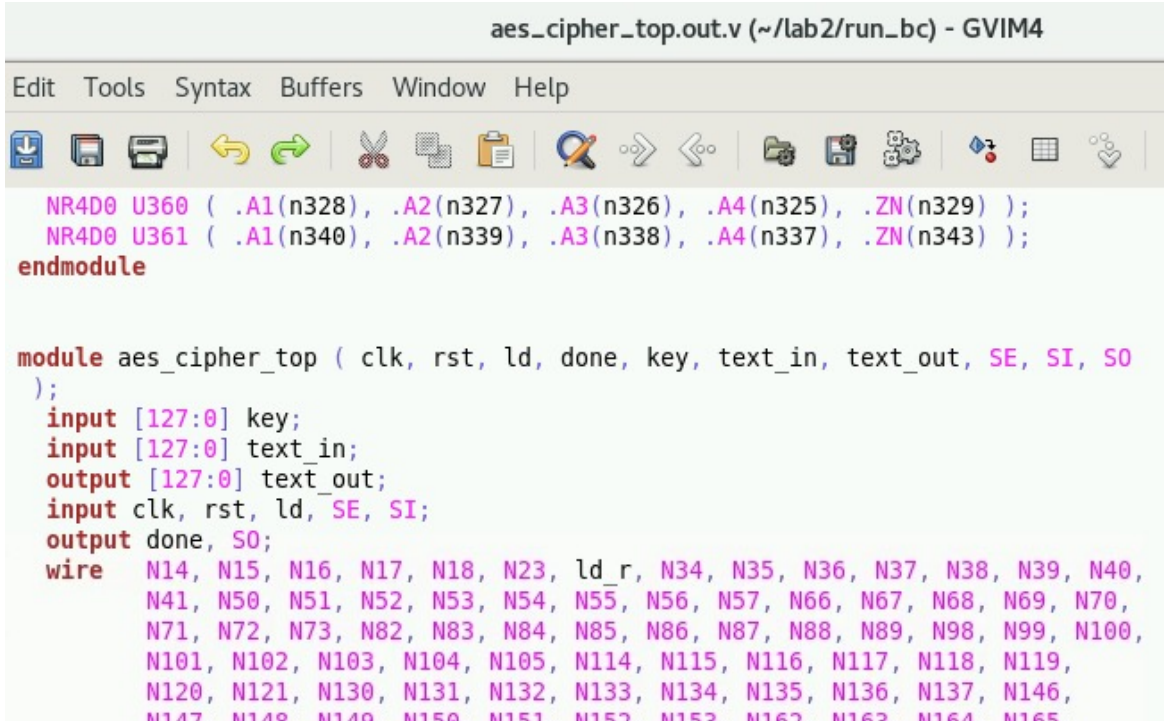
- type “dc_shell”
- <command> –help in the dc_shell to see manual for each <command>
- type “source run_dc.tcl”
- or “source run_dc.tcl > out.log” to save your output messages
- type “exit” to close dc_shell



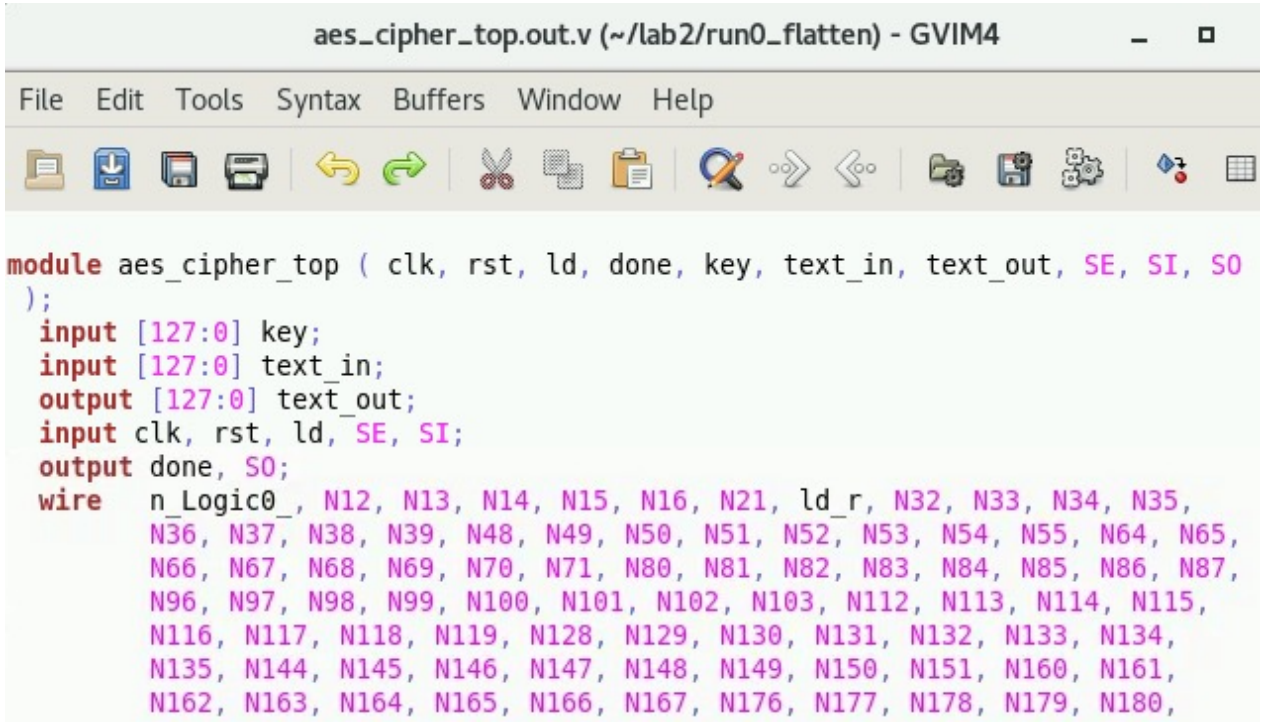
Tip: Grep Errors

- grep “ERROR|Error|error” log_filename > error.log
- grep “WARN|Warn|warn” log_filename > warning.log
- Type “[command] –help” to get some manual

aes_cipher_top.out.v



Unflattened out.v file



flattened out.v file

- many other modules are included

- only top module is included

Power Report

aes_cipher_top_power.rep (~/lab2/run0/l

File Edit Tools Syntax Buffers Window Help

```
   Voltage Units = 1V
   Capacitance Units = 1.000000pf
   Time Units = 1ns
   Dynamic Power Units = 1mW    (derived from V,C,T units)
   Leakage Power Units = 1nW


  Cell Internal Power  =   5.6852 mW   (70%)
  Net Switching Power  =   2.4310 mW   (30%)
                         ---------
Total Dynamic Power    =   8.1162 mW  (100%)

Cell Leakage Power     = 187.2281 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------
```

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	3.8463	1.1770	3.6722e+04	5.0600	(60.94%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	1.8390	1.2540	1.5051e+05	3.2434	(39.06%)	
Total	5.6852 mW	2.4309 mW	1.8723e+05 nW	8.3034 mW		

- Internal power:
  - dynamic power inside cells (gates)
- Switching power:
  - dynamic power from outside cells, e.g., wire load

Area Report

```
Number of ports:                          391
Number of nets:                          1673
Number of cells:                         1175
Number of combinational cells:            768
Number of sequential cells:               390
Number of macros/black boxes:               0
Number of buf/inv:                         79
Number of references:                      68

Combinational area:              20989.440305
Buf/Inv area:                     1814.400064
Noncombinational area:            4443.479995
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire lo

Total cell area:                 25432.920300
Total area:                 undefined
1

****************************************
Report : reference
Design : aes_cipher_top
Version: I-2013.12-SP1
Date   : Thu Dec 16 18:57:29 2021
****************************************
```

```
Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
AOI21D0            tcbn65gpluswc
                                   2.160000       1      2.160000
AOI21D1            tcbn65gpluswc
                                   2.160000       8     17.280001
AOI22D0            tcbn65gpluswc
                                   2.520000      12     30.240000
AOI22D1            tcbn65gpluswc
                                   2.520000      20     50.400000
AOI221D0           tcbn65gpluswc
                                        ⋮

aes_sbox_9                       865.440016       1    865.440016  h
aes_sbox_10                      894.240017       1    894.240017  h
aes_sbox_11                      871.200016       1    871.200016  h
aes_sbox_12                      891.000017       1    891.000017  h
aes_sbox_13                      860.400017       1    860.400017  h
aes_sbox_14                      861.480017       1    861.480017  h
aes_sbox_15                      842.760016       1    842.760016  h
aes_sbox_16                      855.360017       1    855.360017  h
aes_sbox_17                      856.440016       1    856.440016  h
aes_sbox_18                      854.640016       1    854.640016  h
aes_sbox_19                      868.320017       1    868.320017  h
--------------------------------------------------------------------------------
Total 68 references                                   25432.920300
```

un-flattened case reports including sub-modules' area

Timing Report (Setup Time)

```
Startpoint: u0/w_reg_3__10_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: u0/w_reg_3__18_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Point                          Fanout       Cap     Trans      Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                          0.000      0.000
clock network delay (ideal)                                    0.000      0.000
u0/w_reg_3__10_/CP (DFD1)                             0.000    0.000      0.000 r
u0/w_reg_3__10_/Q (DFD1)                              0.164    0.130      0.130 r
u0/wo_3_10_ (net)                40          0.036               0.000      0.130 r
u0/u1/a_2_ (aes_sbox_3)                                        0.000      0.130 r
u0/u1/a_2_ (net)                             0.036             0.000      0.130 r
u0/u1/U243/ZN (INVD1)                                 0.087    0.065      0.194 f
u0/u1/n23 (net)                  26          0.023             0.000      0.194 f
                                                                 ⋮
U1734/Z (CKBD1)                                       0.010    0.015      0.677 r
n1392 (net)                       1          0.001             0.000      0.677 r
sa12_reg_5_/D (DFQD1)                                 0.010    0.000      0.677 r
data arrival time                                                        0.677

clock clk (rise edge)                                          1.200      1.200
clock network delay (ideal)                                    0.000      1.200
clock uncertainty                                             -0.120      1.080
sa12_reg_5_/CP (DFQD1)                                         0.000      1.080 r
library setup time                                            -0.012      1.068
data required time                                                       1.068
-----------------------------------------------------------------------------
data required time                                                       1.068
data arrival time                                                       -0.677
-----------------------------------------------------------------------------
slack (MET)                                                              0.392
```

- slow path is listed first

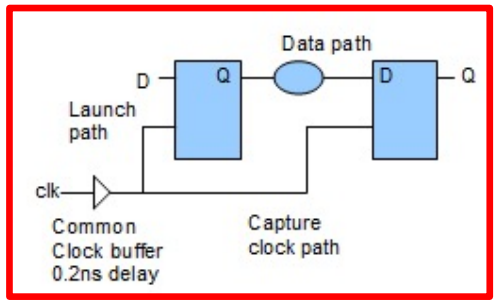
delay in your path

Time budget you have

Time slack: should be positive value or 0

Timing Report (Hold Time)

```
Path 10: MET Hold Check with Pin text_out_reg_38_/CP
Endpoint:   text_out_reg_38_/D (v) checked with  leading edge of 'clk'
Beginpoint: u0/w_reg_2__6_/Q   (v) triggered by  leading edge of 'clk'
Path Groups: {reg2reg}
Analysis View: BC_VIEW
Other End Arrival Time          0.054
+ Hold                          0.013
+ Phase Shift                   0.000
- CPPR Adjustment               0.000
= Required Time                 0.067
  Arrival Time                  0.148
  Slack Time                    0.081
     Clock Rise Edge                     0.000
     = Beginpoint Arrival Time           0.000
     Timing Path:
     +-------------------------------------------------------------------------------+
     |          Pin          | Edge |  Net   |  Cell   | Delay | Arrival | Required |
     |                       |      |        |         |       |  Time   |   Time   |
     |-----------------------+------+--------+---------+-------+---------+----------|
     | clk                   |  ^   | clk    |         |       |   0.000 |   -0.081 |
     | CTS_ccl_a_buf_00003/I |  ^   | clk    | CKBD16  | 0.011 |   0.011 |   -0.071 |
     | CTS_ccl_a_buf_00003/Z |  ^   | CTS_1  | CKBD16  | 0.042 |   0.053 |   -0.028 |
     | u0/w_reg_2__6_/CP     |  ^   | CTS_1  | DFQD1   | 0.001 |   0.054 |   -0.028 |
     | u0/w_reg_2__6_/Q      |  v   | w2[6]  | DFQD1   | 0.068 |   0.122 |    0.041 |
     | U822/A1               |  v   | w2[6]  | XOR2D0  | 0.000 |   0.122 |    0.041 |
     | U822/Z                |  v   | N489   | XOR2D0  | 0.026 |   0.148 |    0.067 |
     | text_out_reg_38_/D    |  v   | N489   | DFQD1   | 0.000 |   0.148 |    0.067 |
     +-------------------------------------------------------------------------------+
```



Data path: Arrival time should be higher than required time

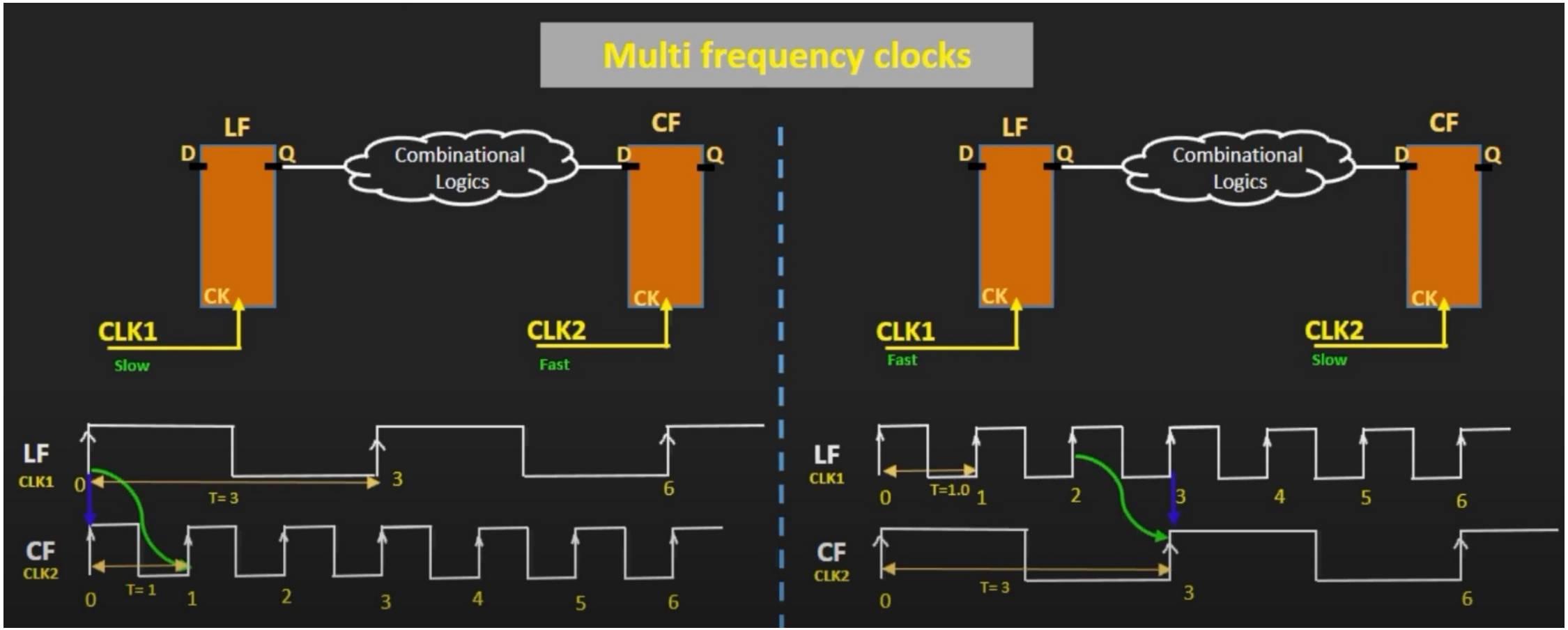
```
Clock Rise Edge                     0.000
= Beginpoint Arrival Time           0.000
Other End Path:
+-------------------------------------------------------------------------------+
|          Pin          | Edge |  Net   |  Cell   | Delay | Arrival | Required |
|                       |      |        |         |       |  Time   |   Time   |
|-----------------------+------+--------+---------+-------+---------+----------|
| clk                   |  ^   | clk    |         |       |   0.000 |    0.081 |
| CTS_ccl_a_buf_00003/I |  ^   | clk    | CKBD16  | 0.011 |   0.011 |    0.092 |
| CTS_ccl_a_buf_00003/Z |  ^   | CTS_1  | CKBD16  | 0.042 |   0.053 |    0.135 |
| text_out_reg_38_/CP   |  ^   | CTS_1  | DFQD1   | 0.001 |   0.054 |    0.135 |
+-------------------------------------------------------------------------------+
```

CLK path: Arrival time should be smaller than required time

Note: for this sim, clock uncertainty was not included. But, should be included like below

```
Path 1: MET Hold Check with Pin col_num[(
CK
Endpoint:   col_num[0].output_fifo_instar
leading edge of 'my_clk'
Beginpoint: ofifo_rd
leading edge of 'my_clk'
Path Groups: {my_clk}
Analysis View: fastView
Other End Arrival Time          0.124
+ Hold                          0.003
+ Phase Shift                   0.000
- CPPR Adjustment               0.000
+ Uncertainty                   0.019
= Required Time                 0.146
  Arrival Time                  0.203
  Slack Time                    0.057
```

FYI) Setup Timing Check with Multi-Frequency



- Summary: Tool considers always the worst-case setup scenario as default

https://www.youtube.com/watch?v=UufBe_JE_Jw

HW3

Prob1 (Script given)

- part 1: synthesize aes_cipher_top with typ. Report timing/area/power
- part 2: synthesize with bst corner. Compare timing/area/power
- part 3: change clock period from 1.2 to 1.6ns. Compare timing/area/power

Prob2 (unflatten Script given)

- synthesize mpeg2 with unflatten and flatten options. Compare timing/area/power

Prob3 (Script given)

- Placement aware synthesize for aes_cipher_top. Compare timing/area/power against Prob1's part1

Prob4 (Script not given)

- Synthesize W1/example2 (3-term carry save adder) to maximize the frequency with wc. input & output delay is the same as part1

Q & A

- typo corrected in “set_input_delay” page

- hold time clock uncertainty issue

  Uncertainty is also included in hold time analysis

- how switching power computed ?

  wiring cap + all TR caps on the output nodes

- async interface timing checked ?

  set_clock_groups -async -group my_clk -group my_WCLK_ML

HW3

Prob1 (Script given)

- part 1: synthesize aes_cipher_top with typ. Report timing/area/power
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- Synthesize W1/example2 (3-term carry save adder) to maximize the frequency with wc. input & output delay is the same as part1