

数字集成电路静态时序分析基础

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概述

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数字芯片与FPGA设计流程

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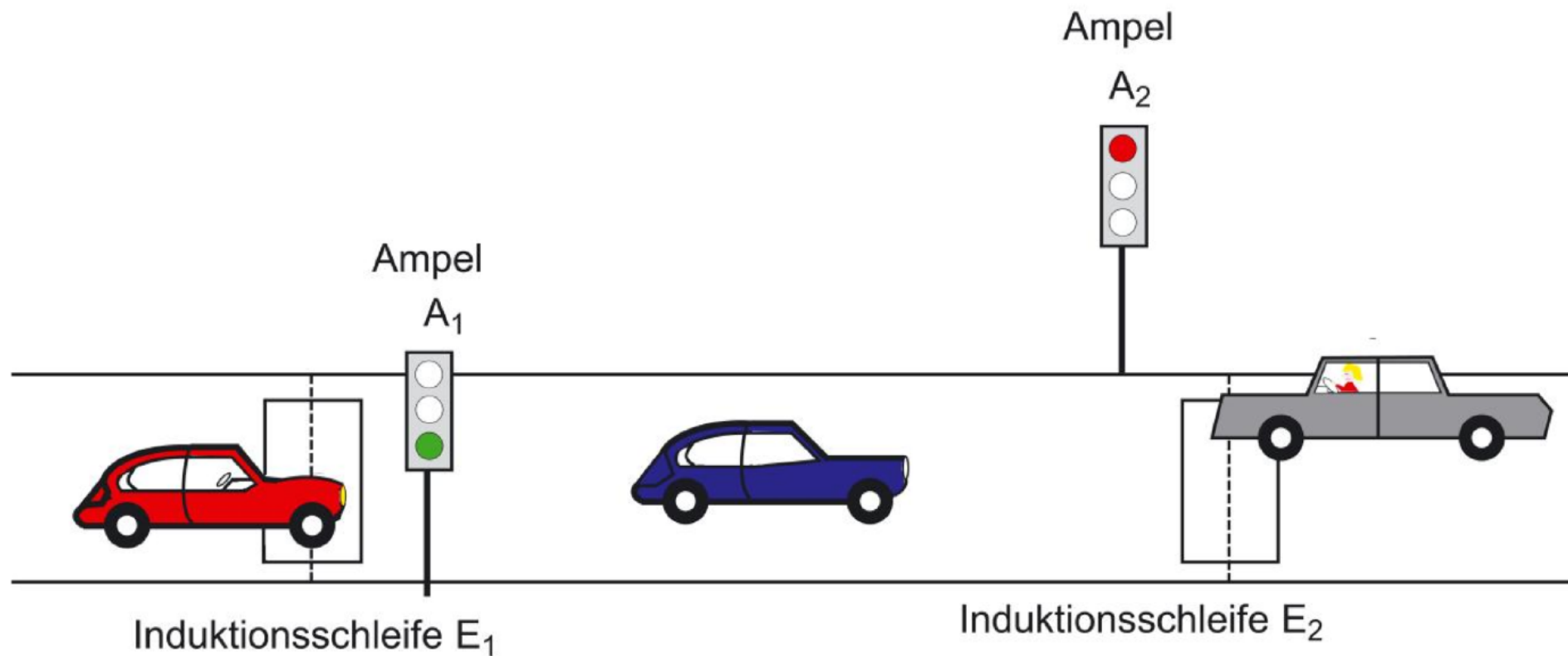
静态时序分析概述

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课程内容规划

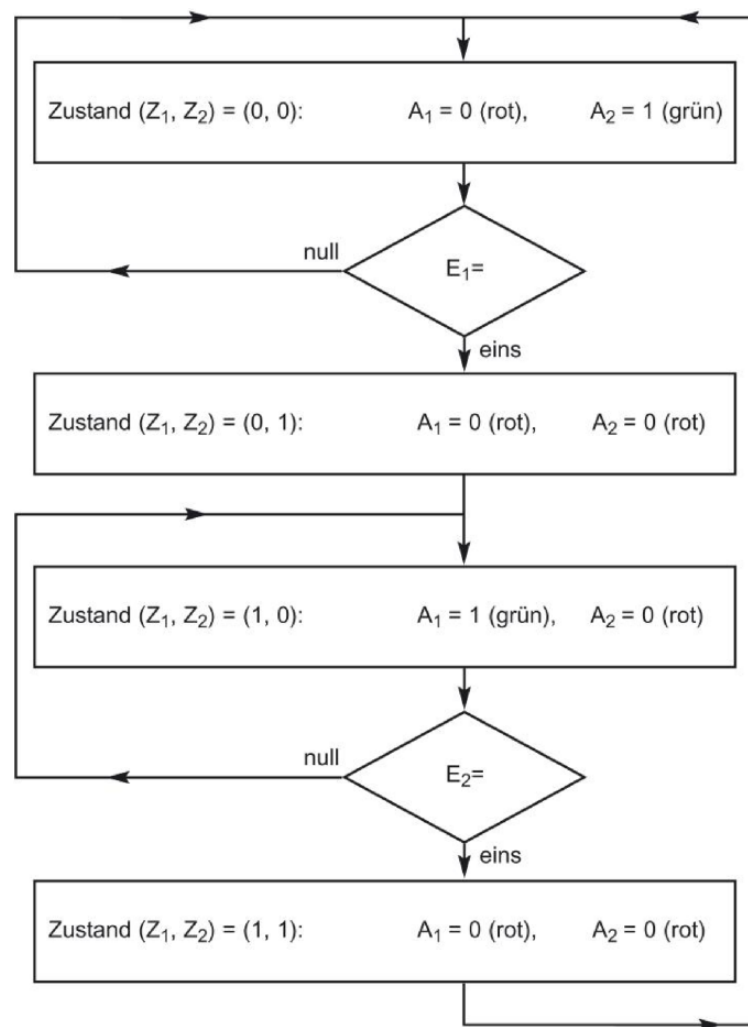
1 数字芯片与FPGA设计流程

数字芯片设计流程



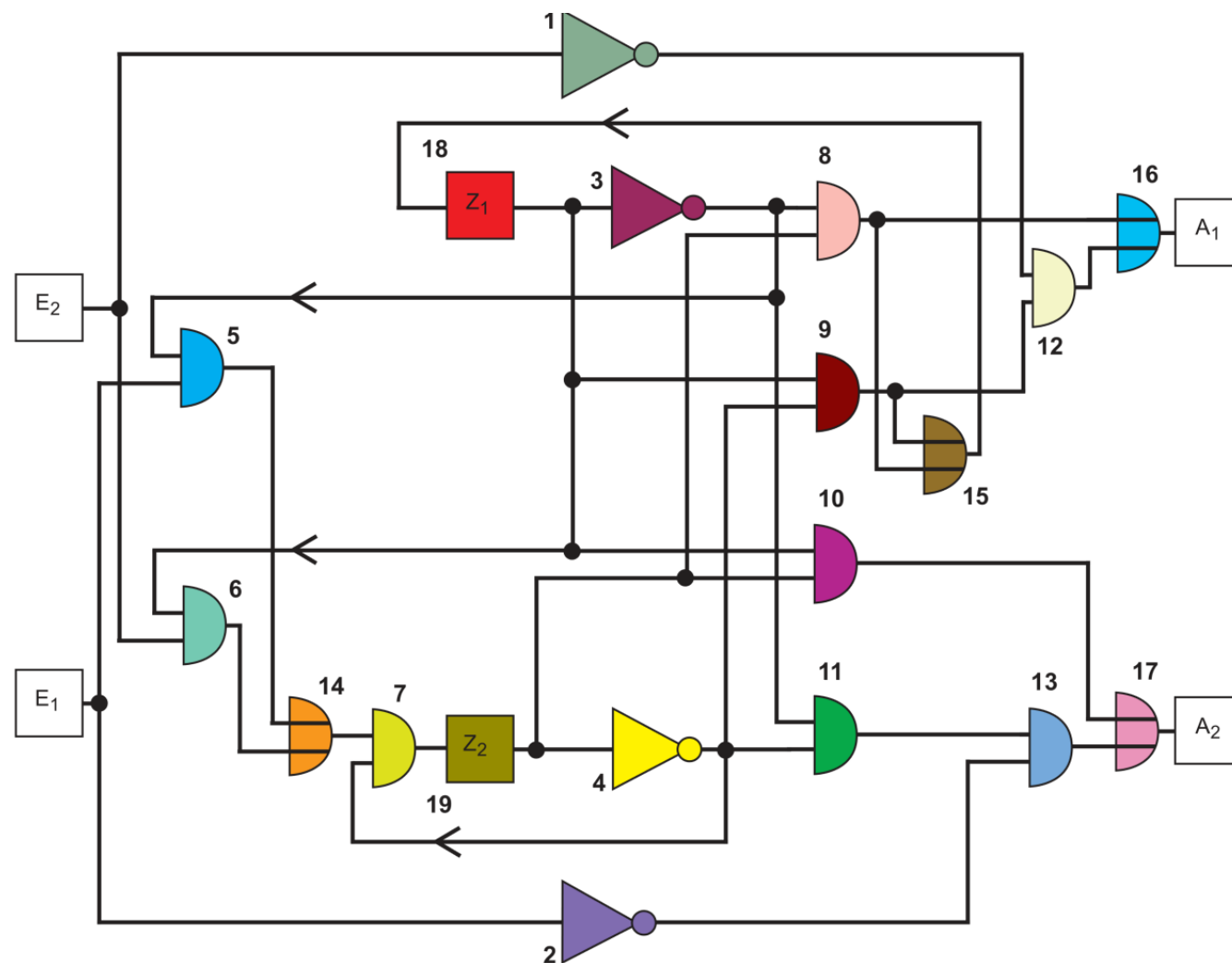
引用自Prof. Jens Vygen @University of Bonn的《Combinatorial Optimization and Applications in VLSI Design》课程。

数字芯片设计流程



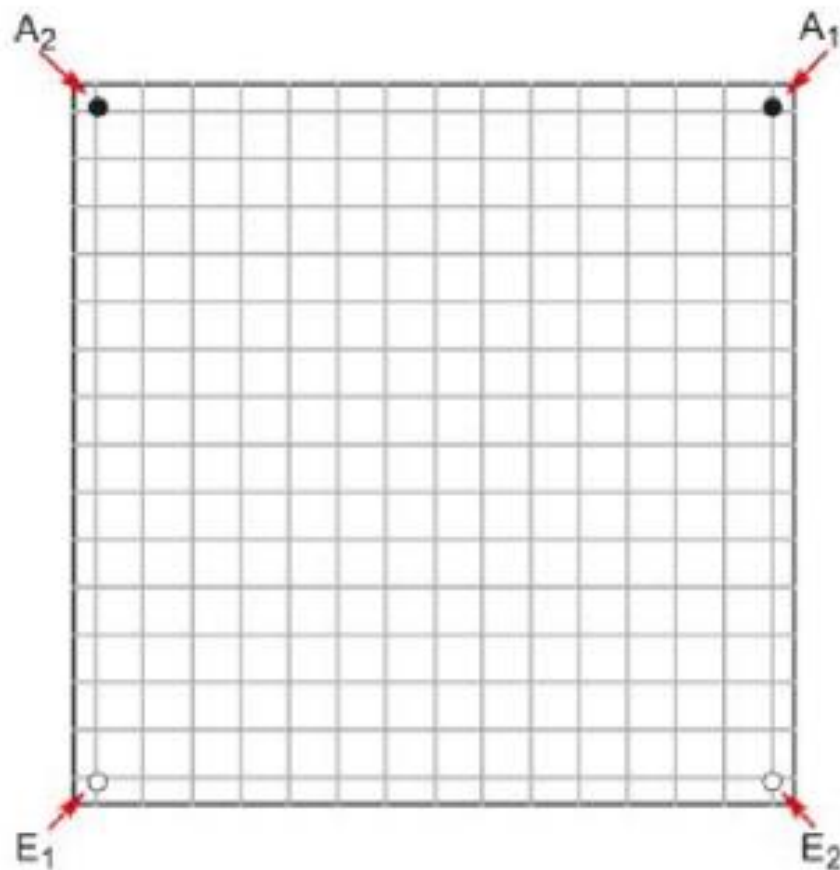
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数字芯片设计流程



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数字芯片设计流程



Inverter



Und - Bauteile



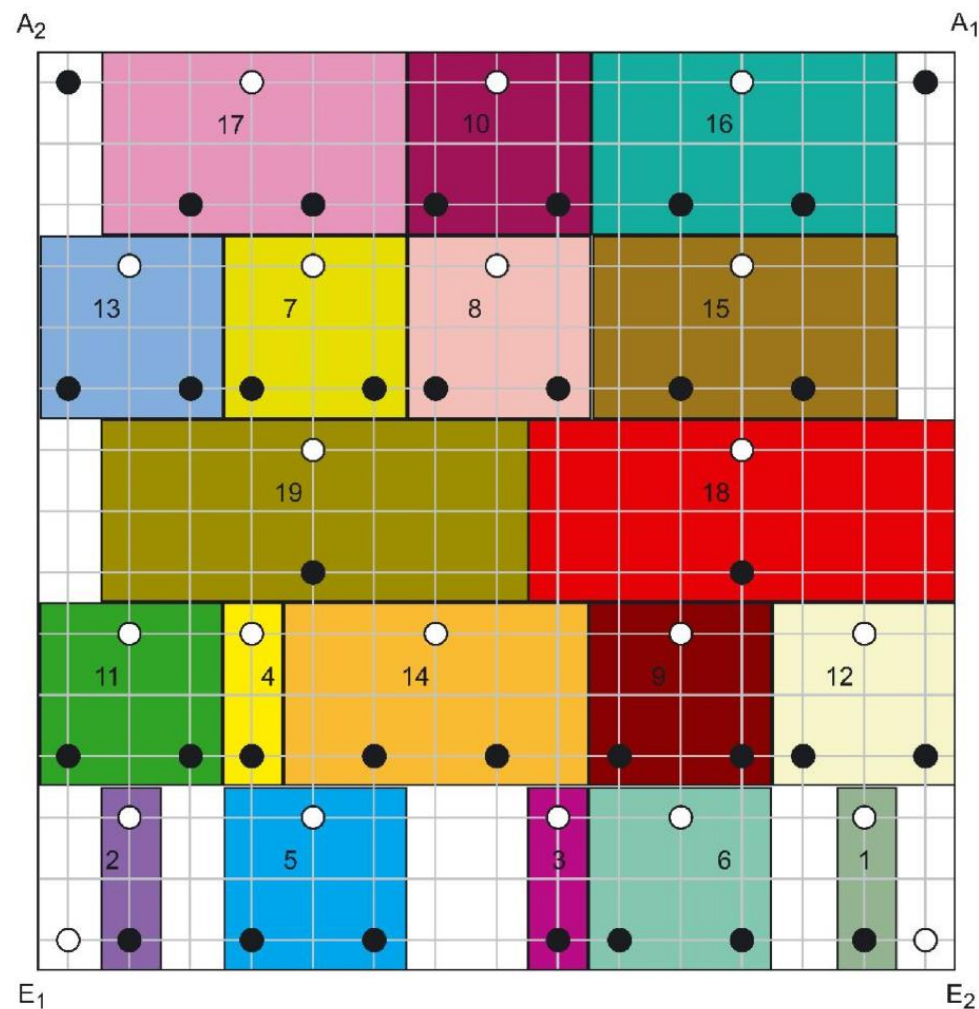
Oder - Bauteile



Latches (Z_1 , Z_2)

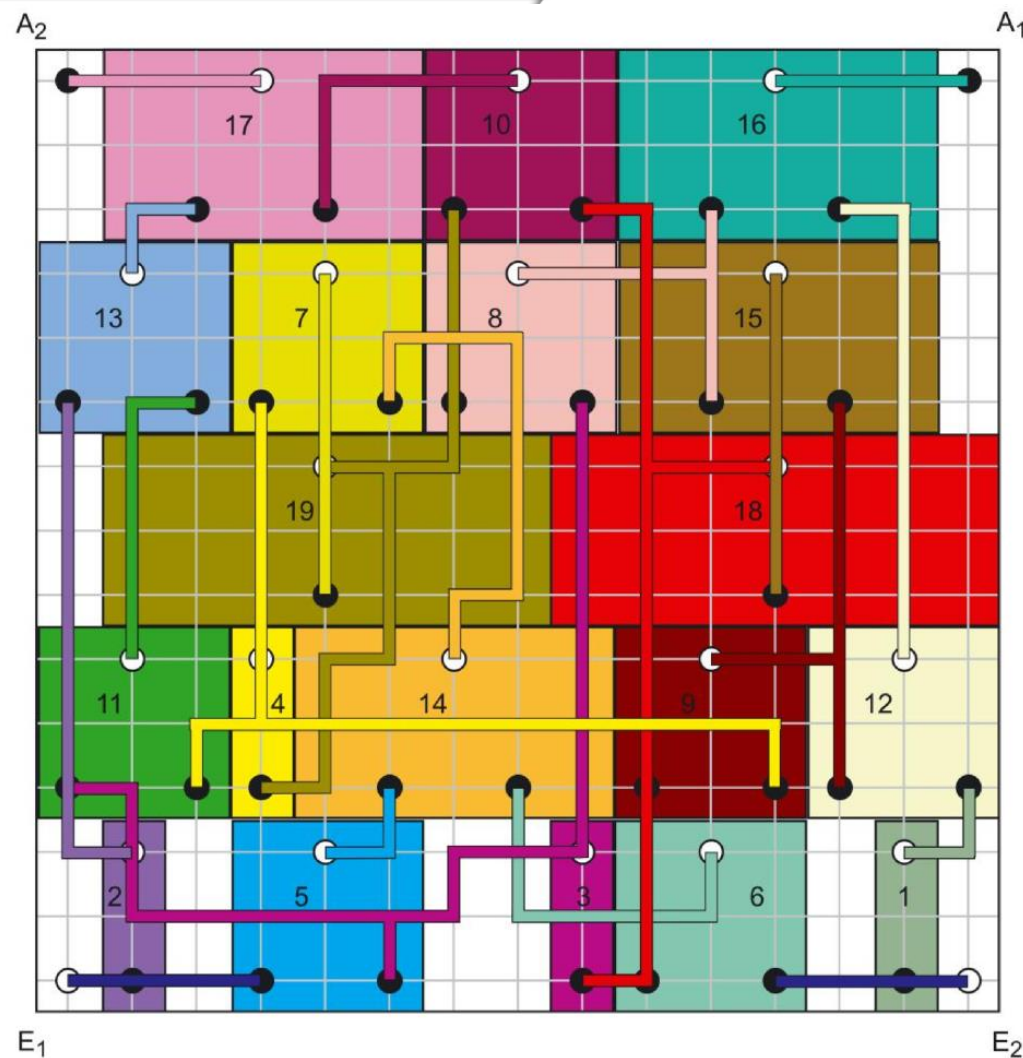
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数字芯片设计流程



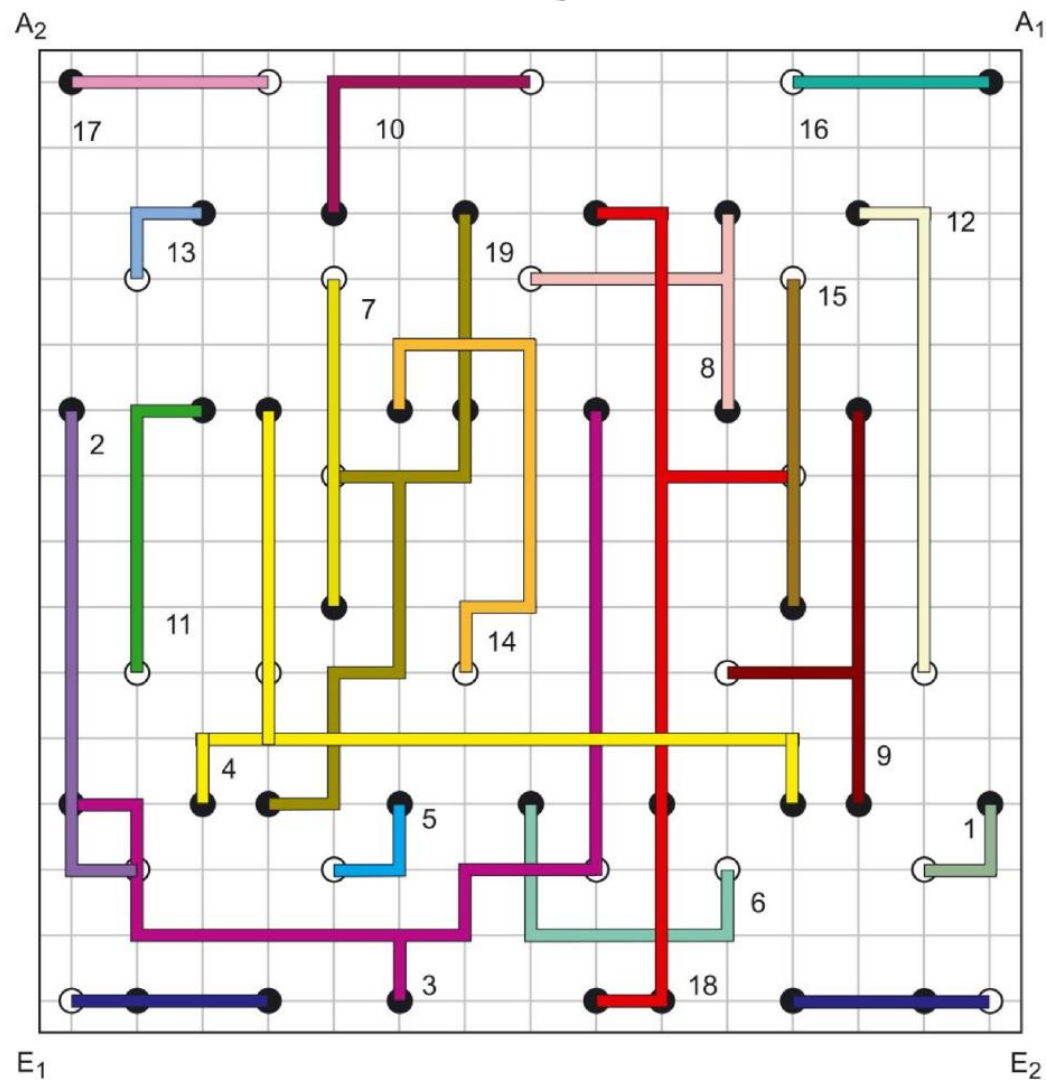
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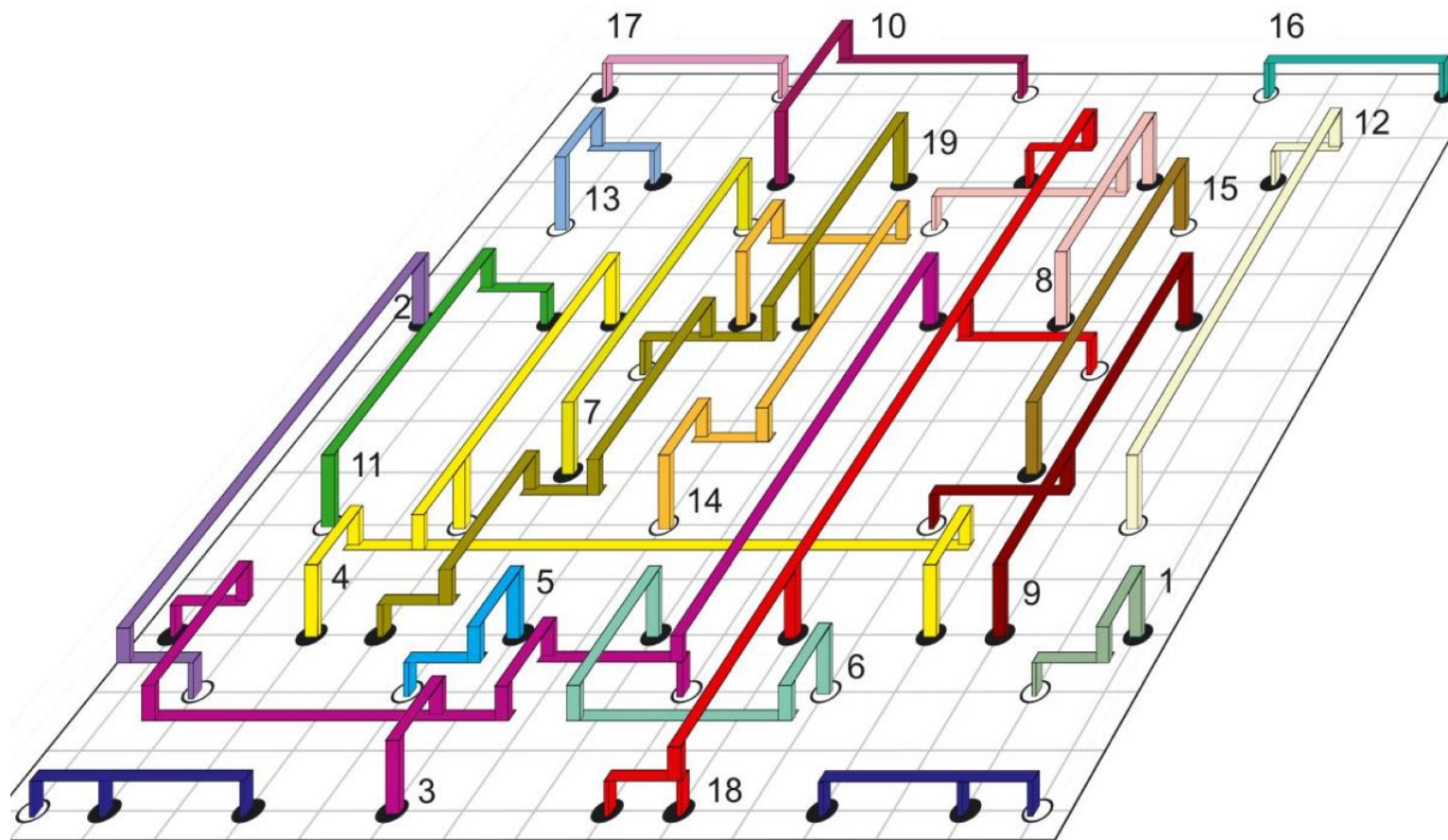
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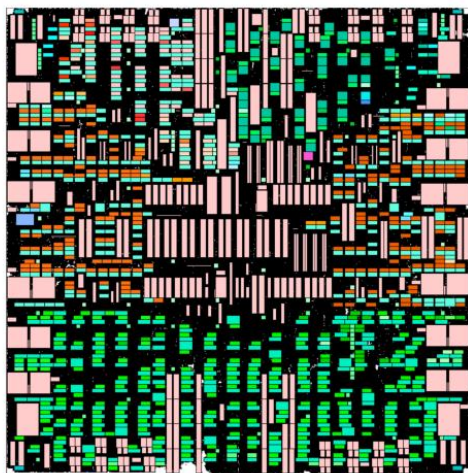
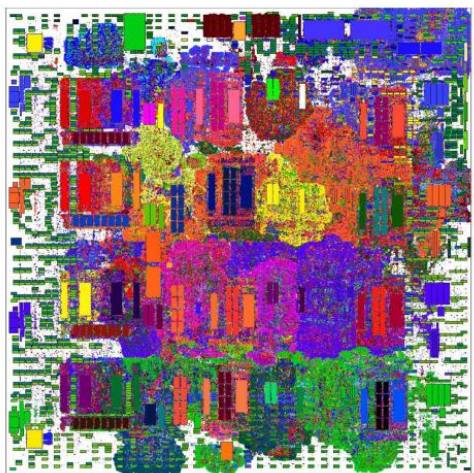
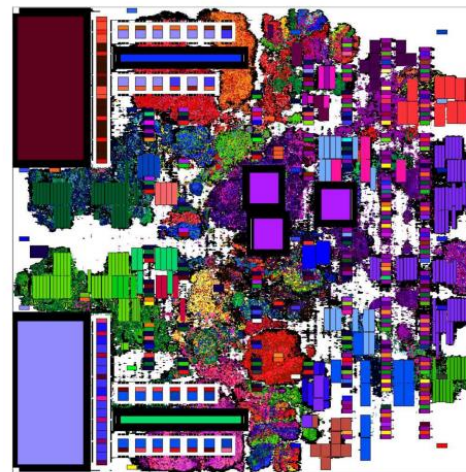
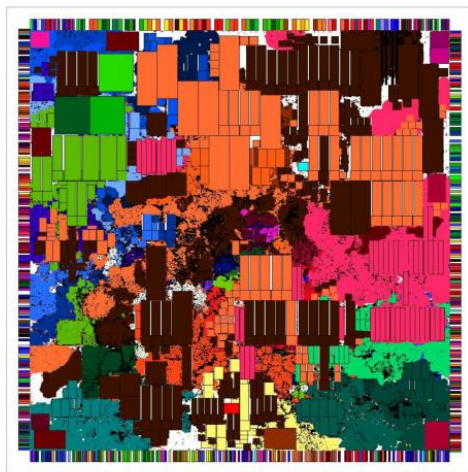
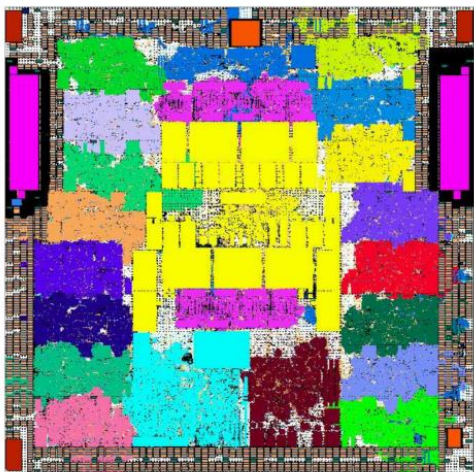
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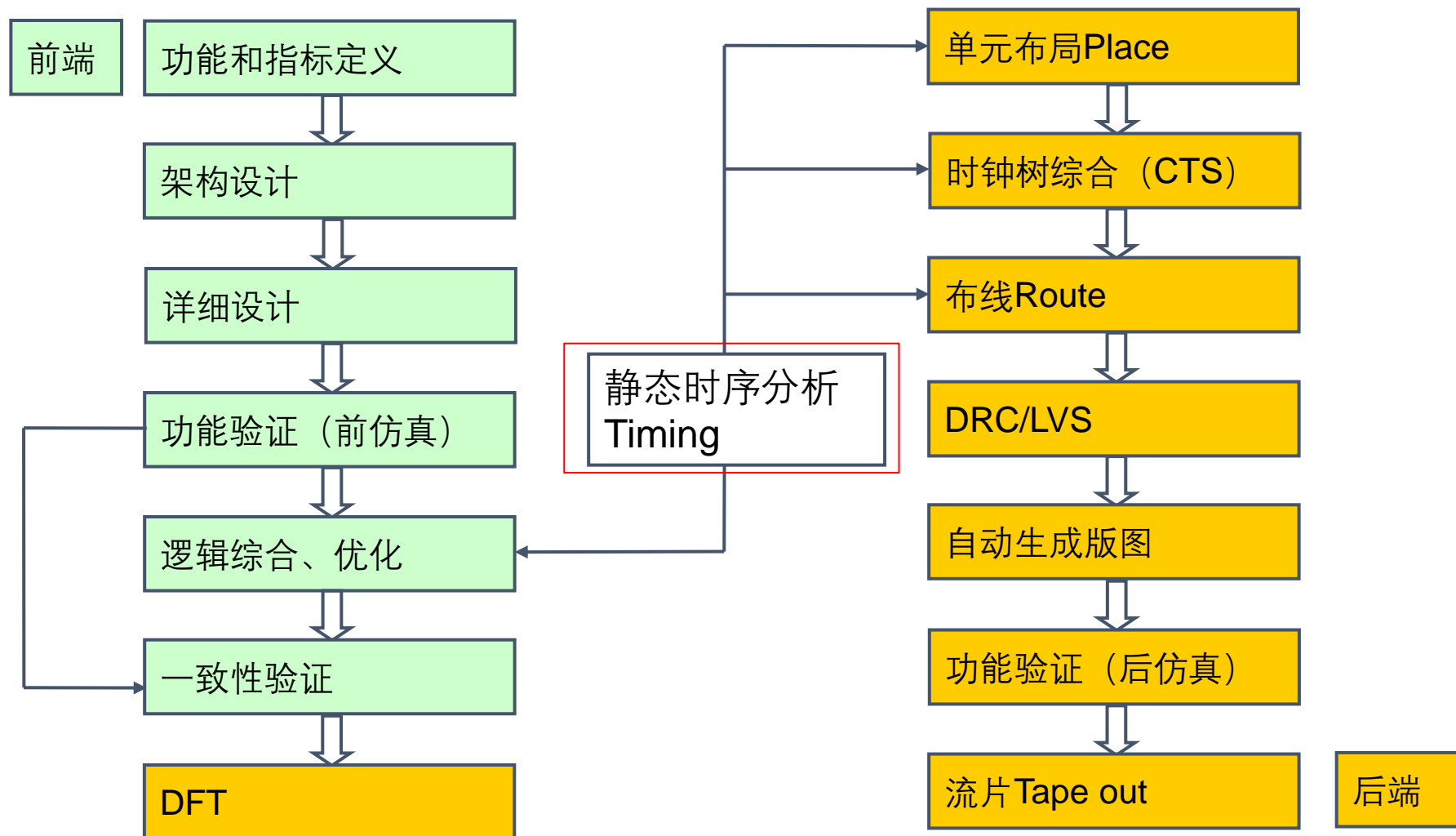
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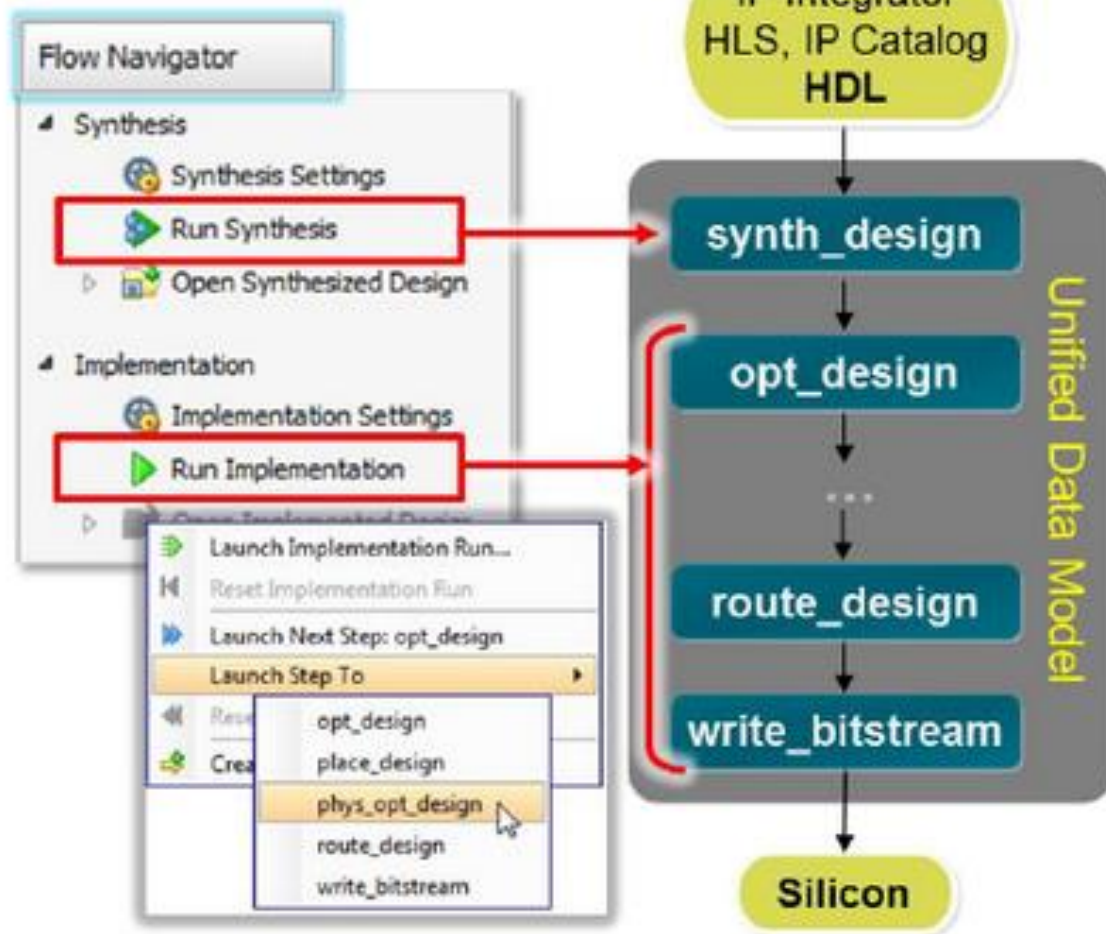
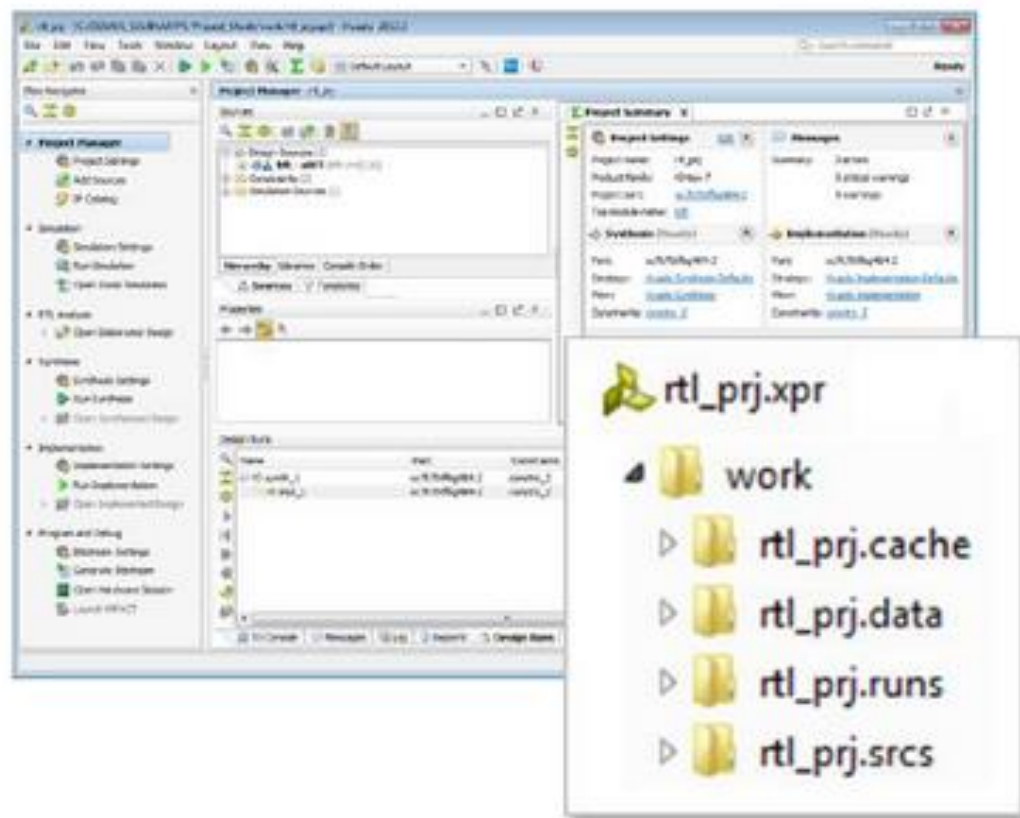


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数字芯片设计流程



FPGA设计流程

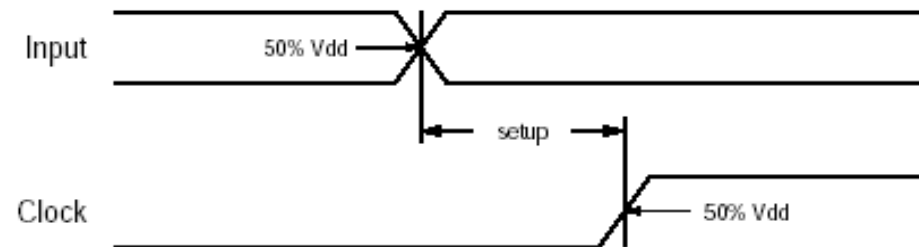
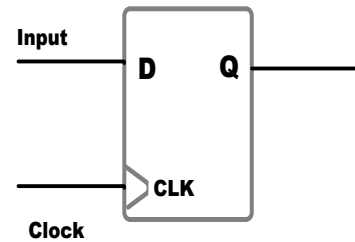




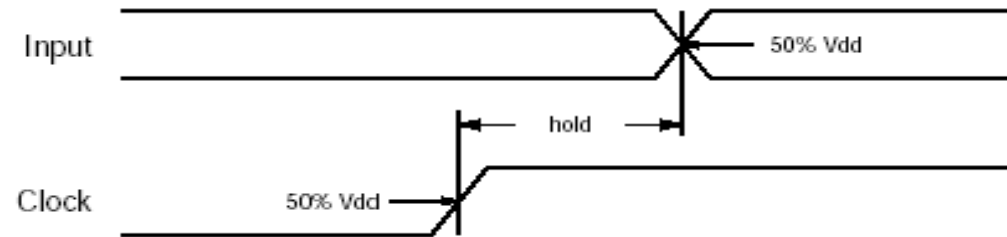
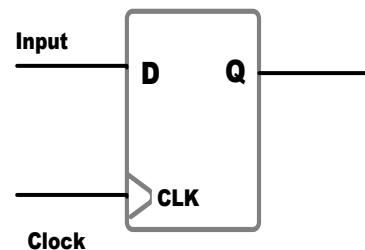
2 静态时序分析概述

静态时序分析概述

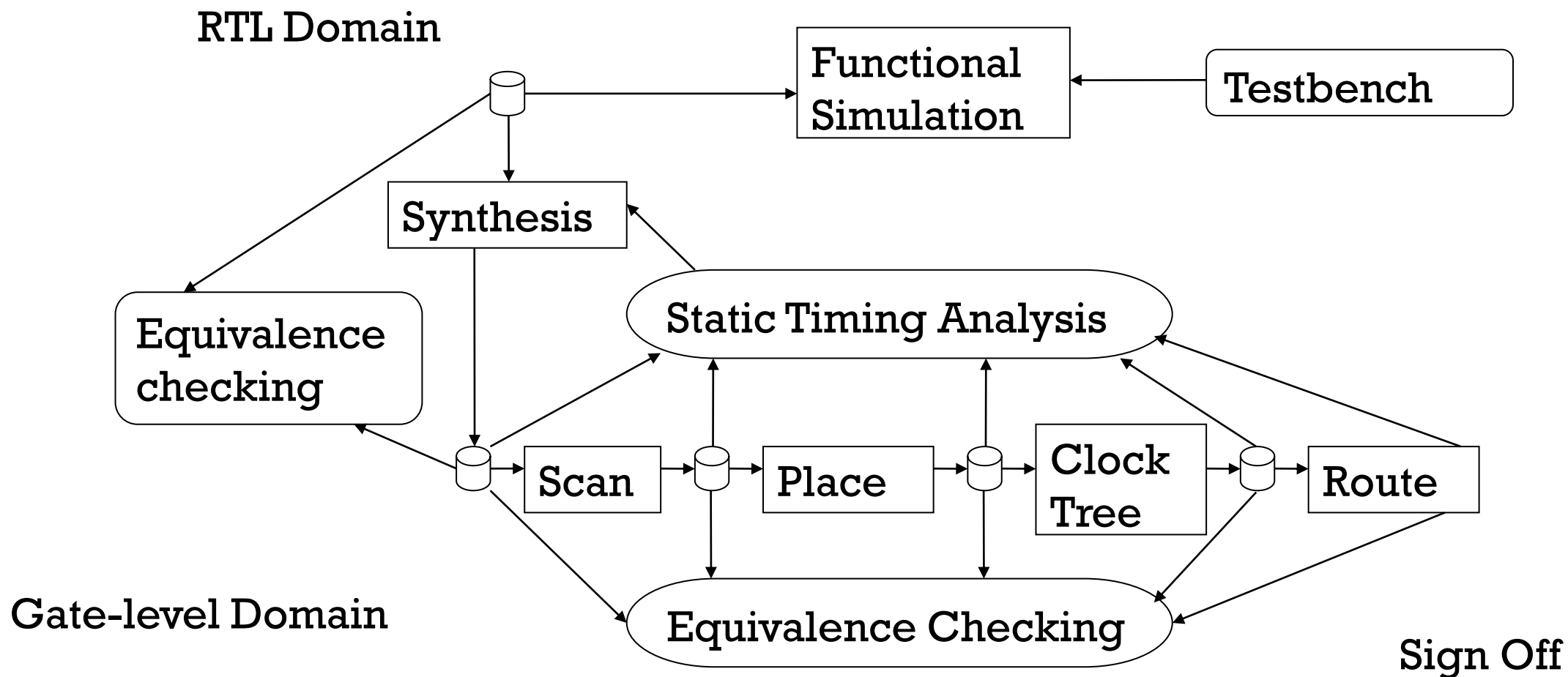
Setup Time - The length of time that data must stabilize before the clock transition.



Hold Time - The length of time that data must remain stable at the input pin after the active clock transition.



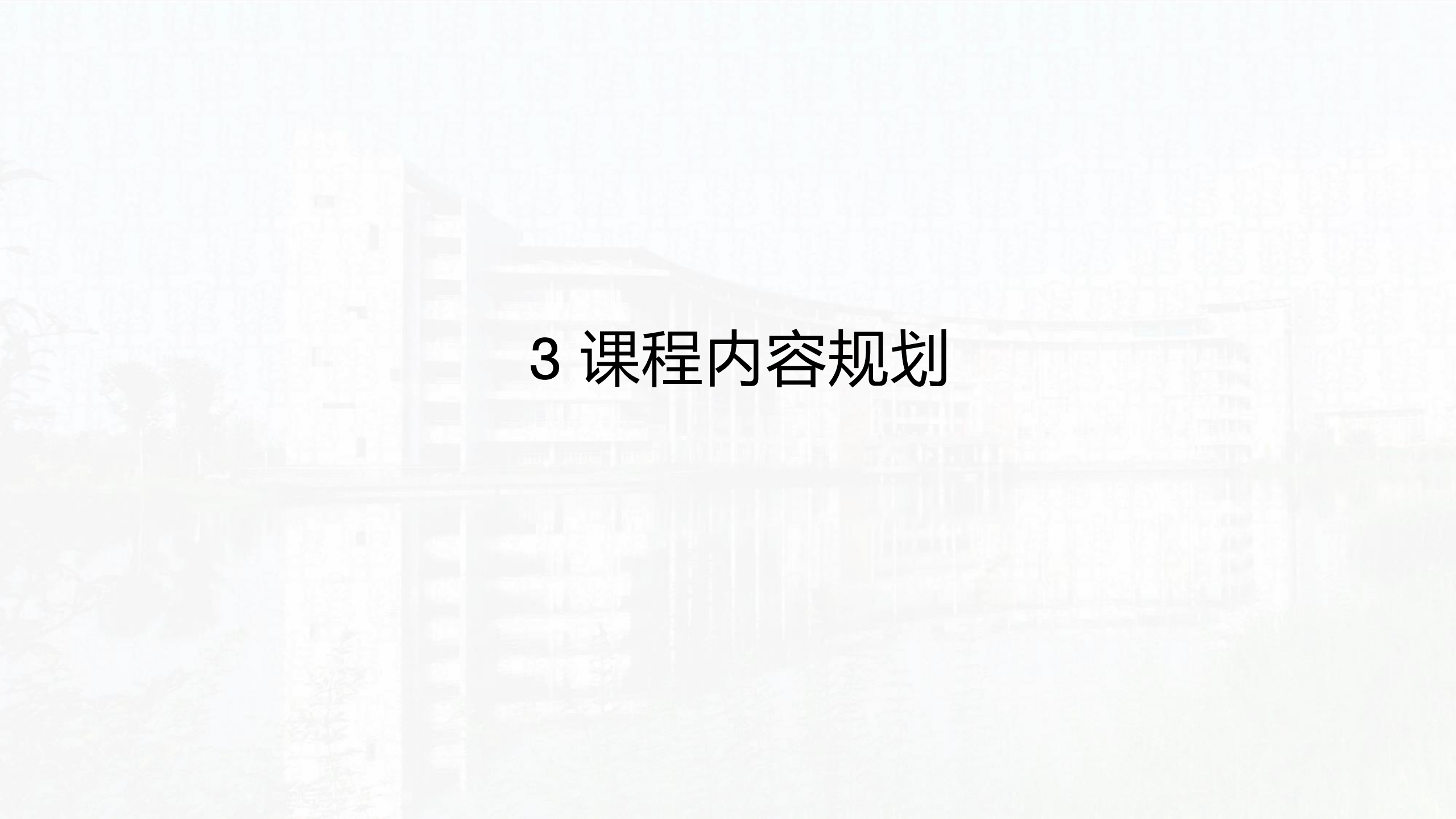
静态时序分析概述



静态时序分析概述

静态时序分析，英文全称：Static Timing Analysis，简称为STA

	Event Driven Timing simulation	STA
Vector Generation	Required	Not Required
Design Coverage	Vector dependent(limited) coverage	Vector independent exhaustive coverage
Runtime	Takes several days/weeks of CPU time	Analyzes multimillion gate design in hours
Capacity	Can run out of memory for multimillion designs	Can easily handle multimillion designs
Analysis/Debug features	No special features for timing analysis	Features such as min/mux analysis, on chip variation, dynamic loop breaking case efforts for timing analysis
Design style support	No Restrictions	Limited support for asynchronous design styles



3 课程内容规划

课程主要内容

- ①TCL语言入门、Synopsys TCL语言入门。
- ②静态时序分析基础，包括工艺库、STA环境、时序检查方法、多时钟等特殊时序分析等。
- ③SDC与习题。

TCL 全称 「 Tool Command Language 」，从这个表格中，我们可以看到TCL语言在集成电路EDA tool 控制上基本处于霸主地位。

功能	工具	语言
数字综合	DC/Genus	TCL
DFT	Tessent/Dftmax	TCL
布局布线	Innovus/ICC2	TCL
静态时序仿真	PT/Tempus	TCL
功耗分析	Redhawk/Voltus	TCL
版图工具	Calibredrv	TCL
物理验证	Calibre/PVS	SVRF/TCL
形式验证	LEC/Formality	TCL

参考书目

- ① Static Timing Analysis for Nanometer Designs: A Practical Approach. J. Bhasker, Rakesh Chadha. Springer Science Business Media, LLC 2009.
- ② 集成电路静态时序分析与建模. 刘峰, 机械工业出版社. 出版时间: 2016-07-01.
- ③ Using Tcl with Synopsys Tools. Version B-2008.09, March 2011. Synopsys.



谢谢聆听！

个人教学工作主页<https://customizablecomputinglab.github.io/>