ECE260B Winter 22

RTL design + Synthesis + PnR

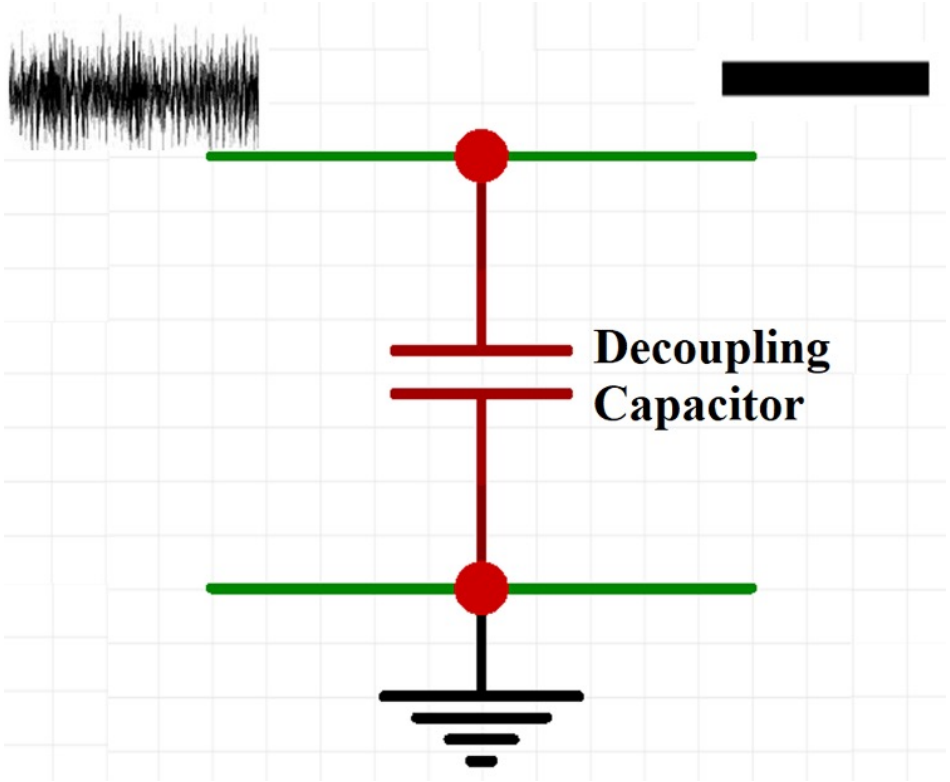
Prof. Mingu Kang

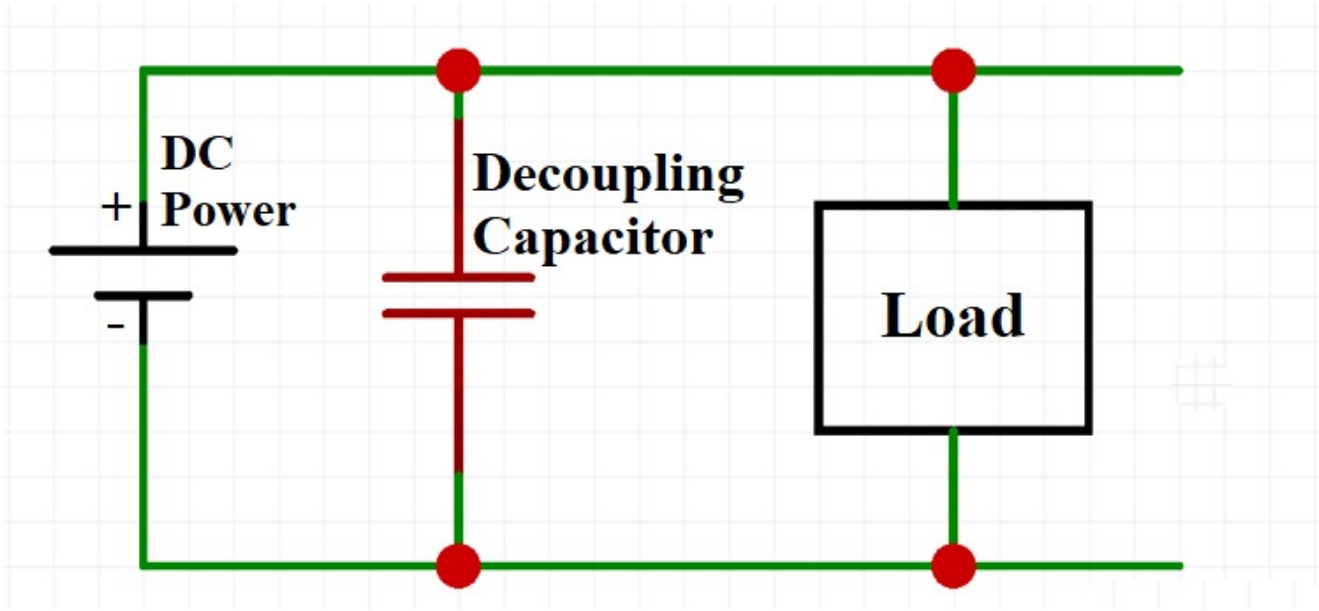
Schedule

- Midterm: Feb 22
  - In-person (except medical issue with a proof)
  - Students bring their own laptop
  - Canvas exam will be given through Quiz tab
  - 2 sheets of both-side papers (= 4 sides)
  - Sample questions will be posted soon
  - For potential technical issues, paper version will be prepared

- Project
  - Team will be formed randomly if you haven't done so
  - Will be released partially from this week
  - Related HWs will be given to help project

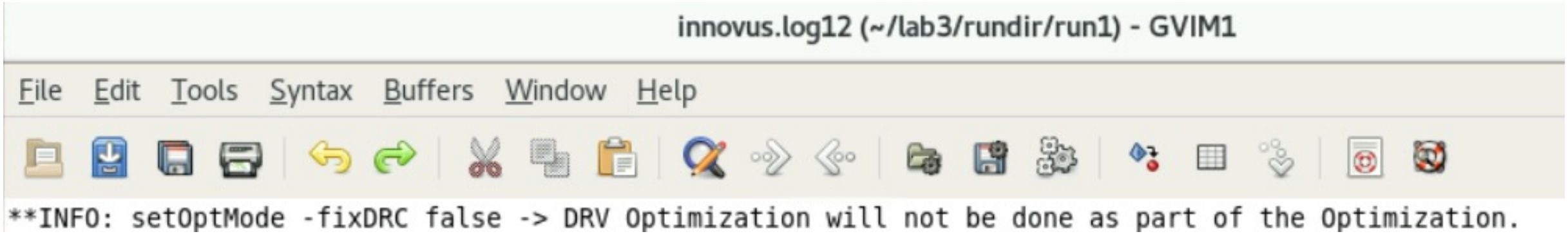
(Q&A) Decoupling Capacitor





https://components101.com/articles/decoupling-capacitor-vs-bypass-capacitors-working-and-applications

DRV vs. DRC Subtle Difference



DRC and DRV are the same ?

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

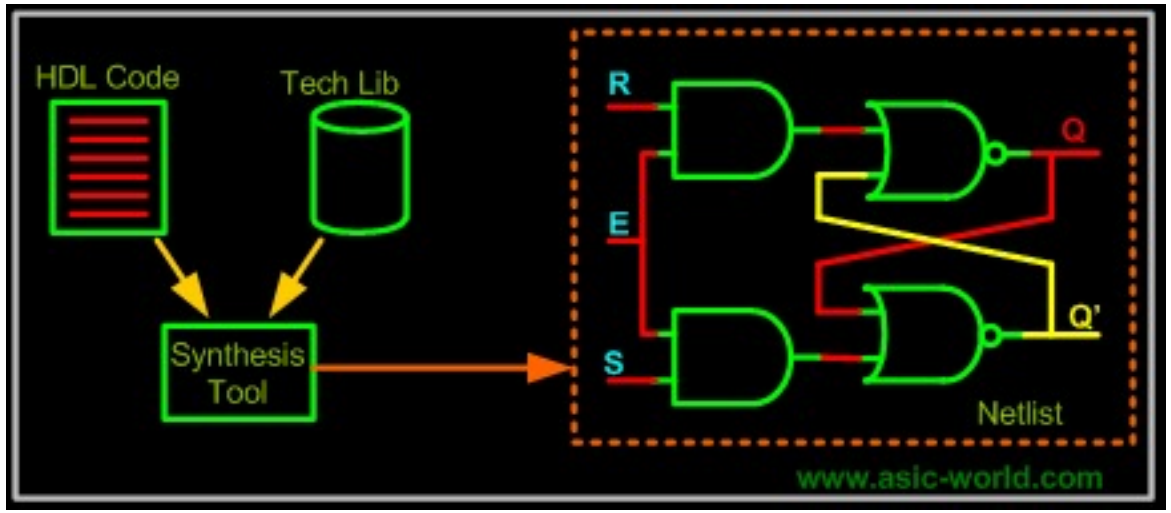
DRV: max_cap / max_tran / max_fanout / max_length …

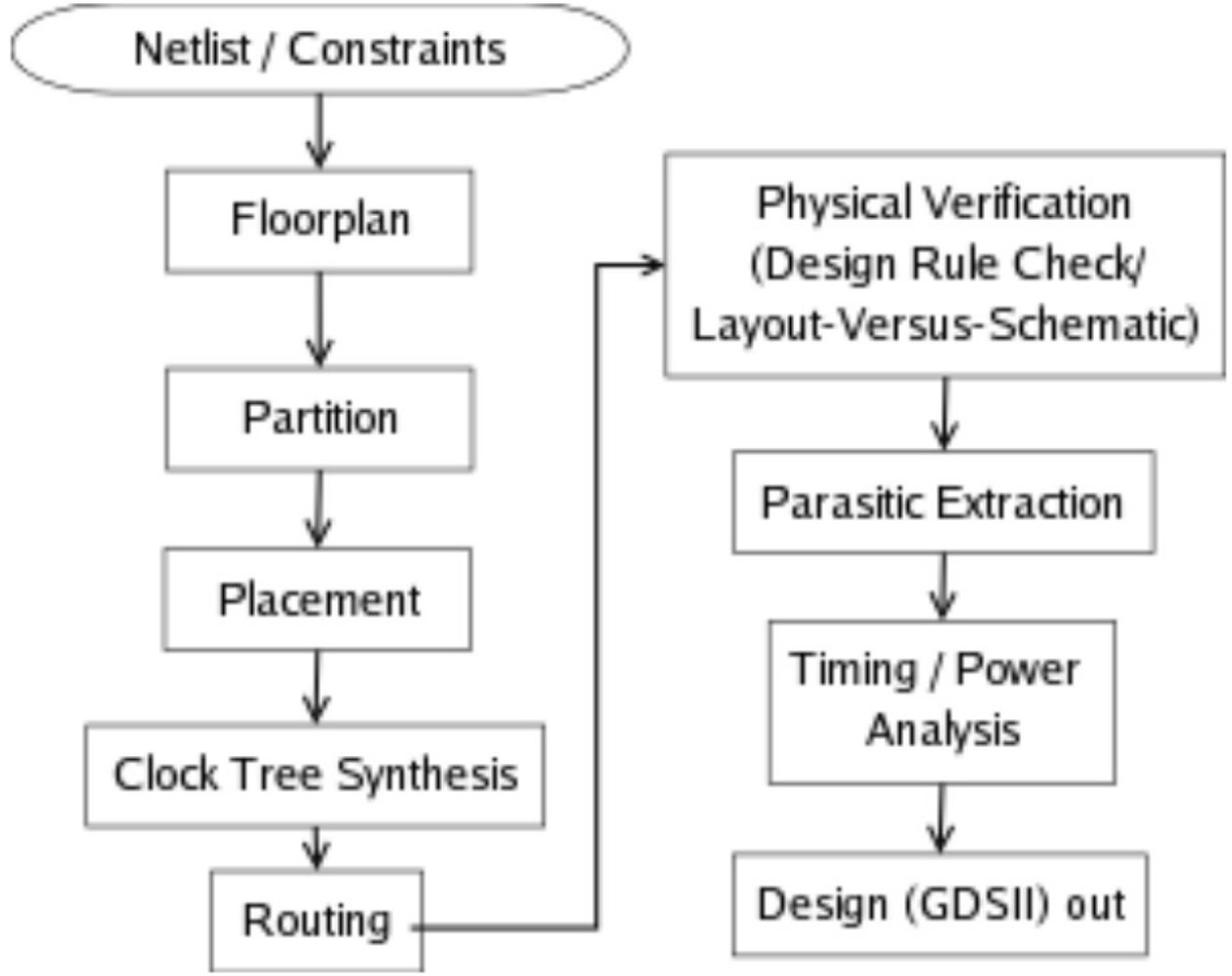
```
ECO: 5.2% of the total area was rechecked for DRC, and 6.7%
  number of violations = 9

 By Layer and Type :
                Short    SpacV   CutSpc   Totals
    M1              2        2        1        5
    M2              3        0        0        3
    M3              1        0        0        1
    Totals          6        2        1        9
```

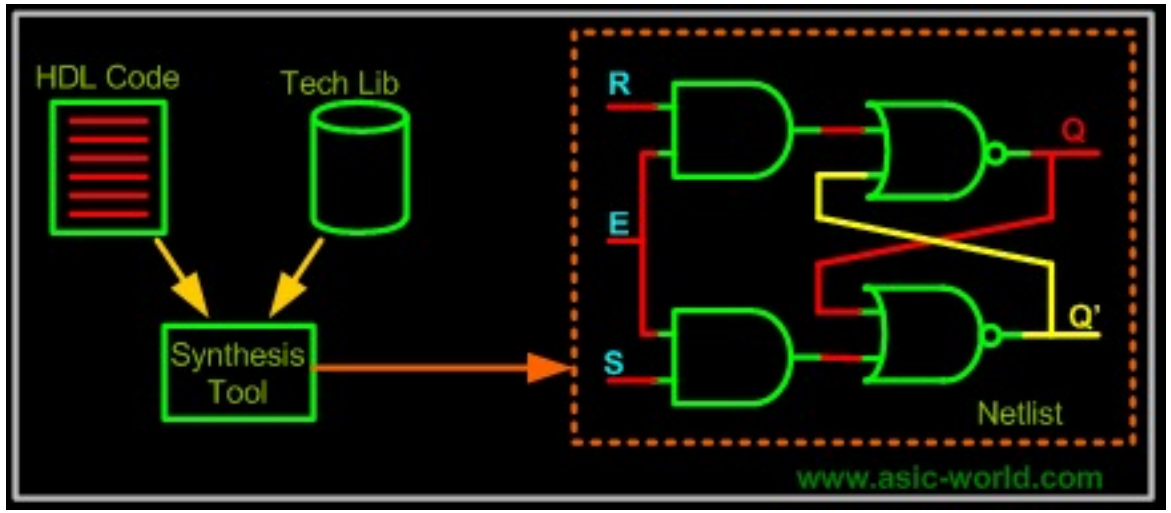
DRC: short / space / cut / ….

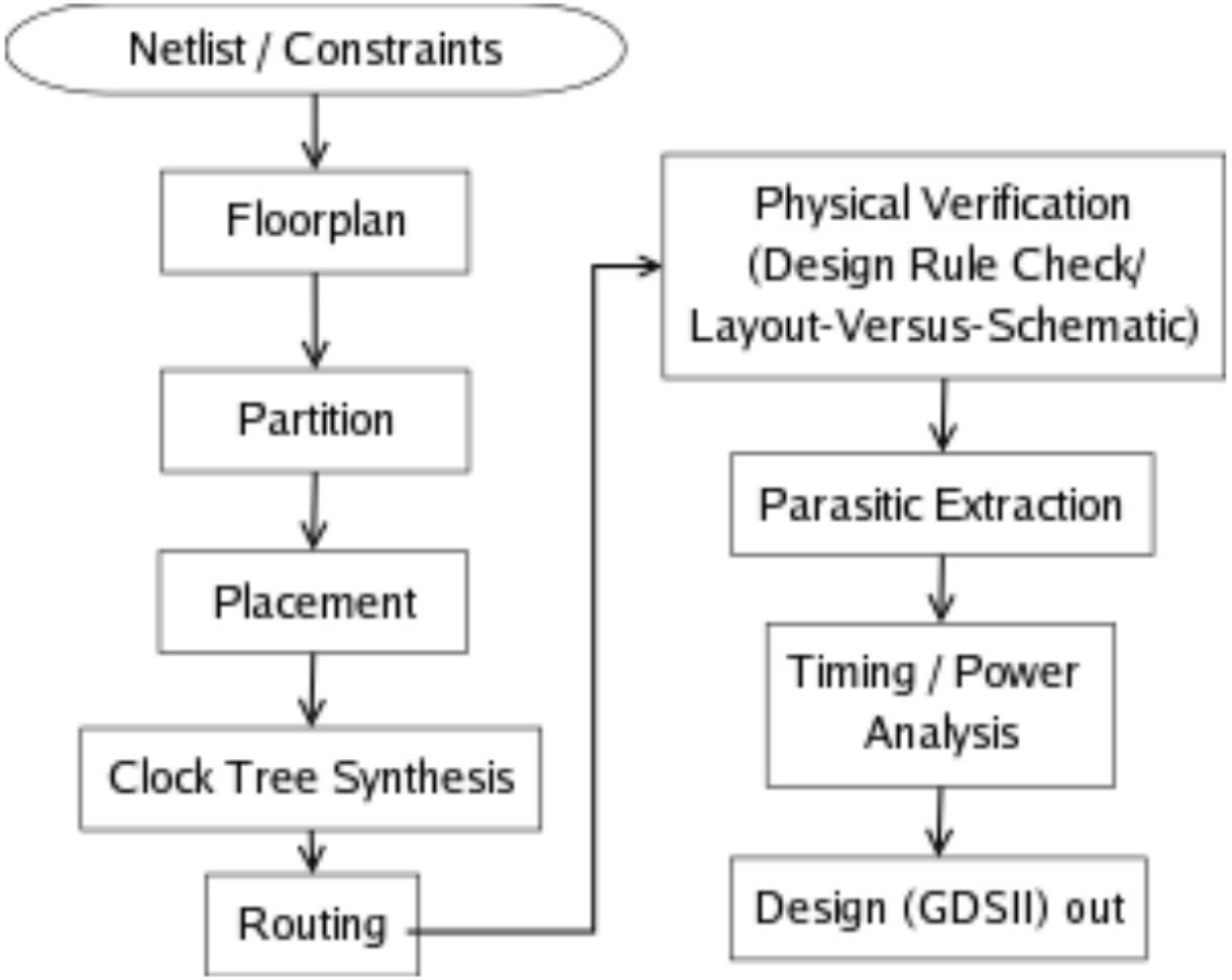
Correction


HDL Code
Tech Lib
Synthesis Tool
R
E
S
Q
Q'
Netlist
www.asic-world.com


Netlist / Constraints
Floorplan
Partition
Placement
Clock Tree Synthesis
Routing
Physical Verification (Design Rule Check/ Layout-Versus-Schematic)
Parasitic Extraction
Timing / Power Analysis
Design (GDSII) out

RTL Design + Synthesis + PnR





Directory and File Structure

1st level	2rd level	3th level
HW folder name		
	syn	constraints/ .sdc
		netlist/ .v
		(after run) log
	pnr	constraints/ .sdc
		netlist/ .out.v
		(after run) timingReports
	rtl_sim	netlist/ .pnr.v
		constraints/ .sdf

- Keep above hierarchy for uniformity
- Template script will be given based on above structure
- <name> means any variations, e.g., flatten

SDF annotated RTL simulations

SDF File Annotation

add_tb.v (~/lab4/rtl_sim) - GVIM8

```
add  add_instance (
        .clk(clk),
        .x(x),
        .y(y),
        .z(z),
        .out(out)
);

initial $sdf_annotate("add_WC.sdf", add_instance, , ,"MAXIMUM","1:1:1","FROM_MTM");

initial begin

  x_file = $fopen("x_data.txt", "r");  //activation
  y_file = $fopen("y_data.txt", "r");  //activation
  z_file = $fopen("z_data.txt", "r");  //activation


  $dumpfile("add_tb.vcd");
  $dumpvars(0,add_tb);
```

sdf file name

instance name

which corner to use

scale factor for 3 corners

- Include above line in the testbench file for simulation

SDF Contents

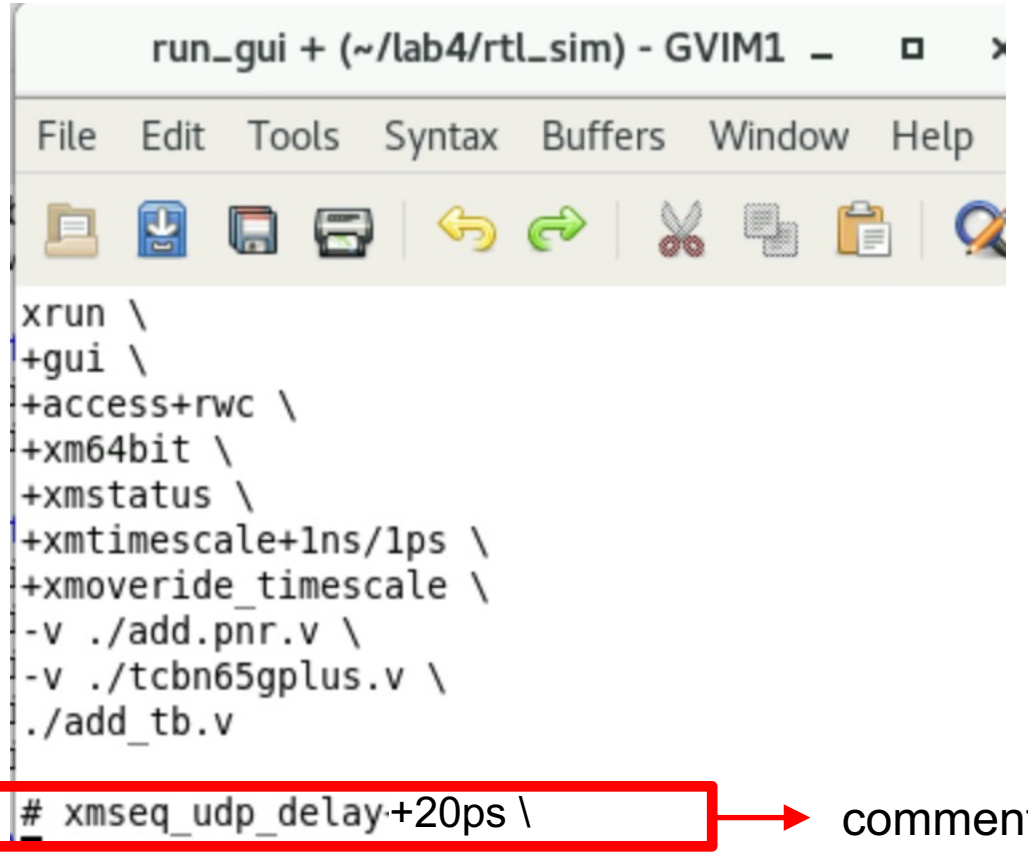
bc wc

```
(IOPATH A CO  (0.161::0.166) (0.156::0.179))
```

0 -> 1 1 -> 0

Typical delay description in SDF file

Xcelium (Ncsim) Simulation



commented out for SDF simulation

type below to run xcelium sim

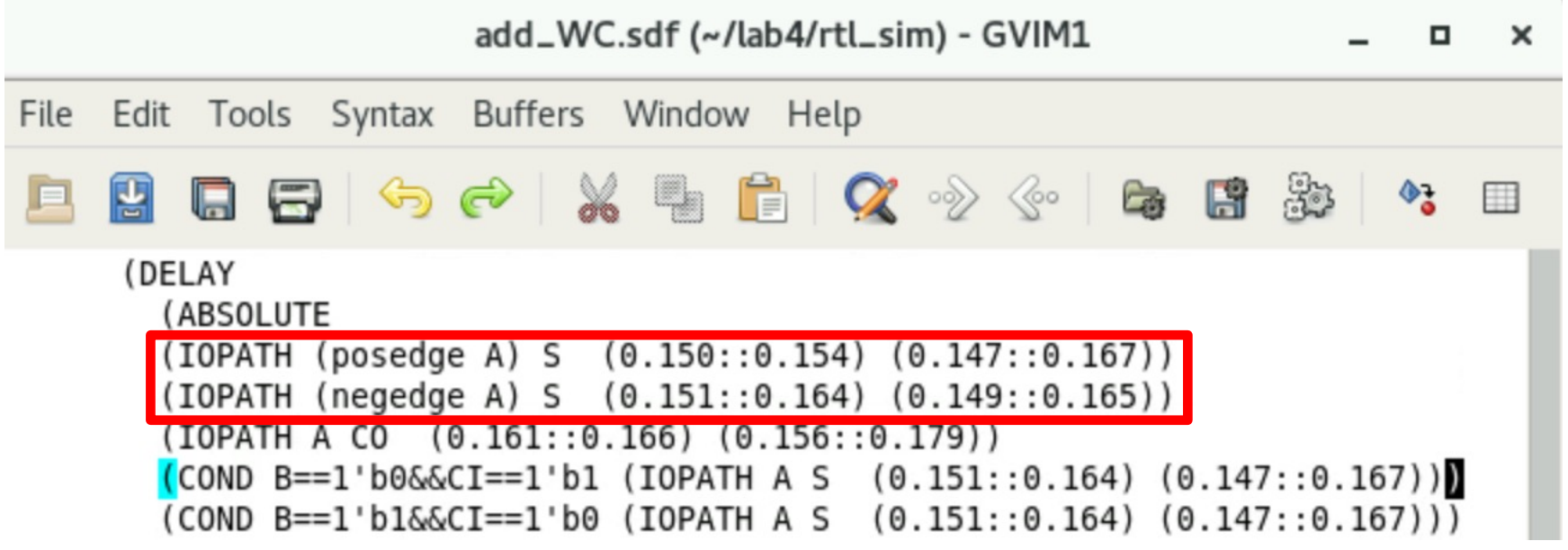
```
chmod +x run_gui
./run_gui
```

- for simulation without SDF file, include the following option: +xmseq_udp_delay+20ps

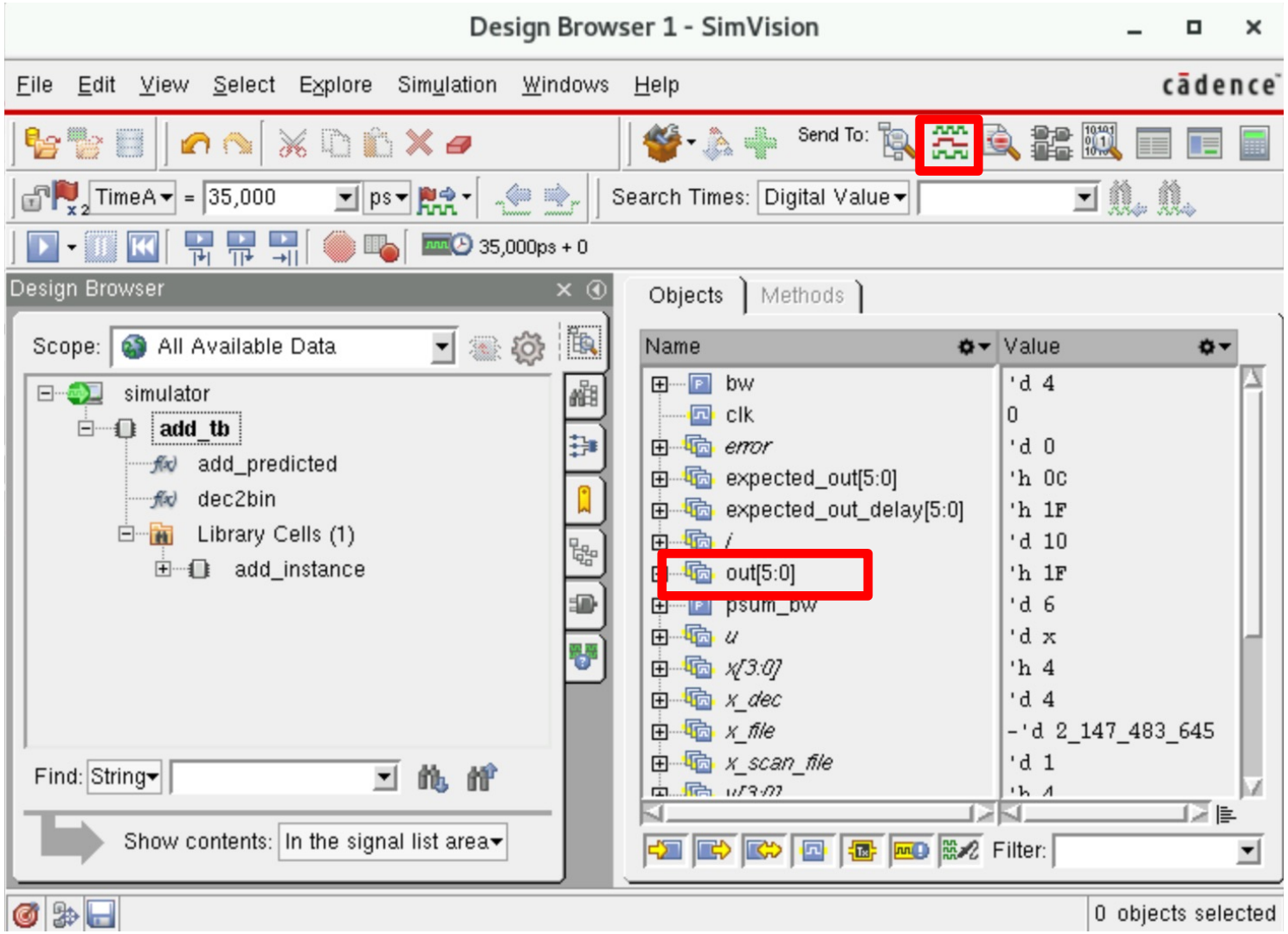
SDF Annotation Issue

```
xmelab: *W,SDFNEP: Unable to annotate to non-existent path (IOPATH (posedge A) S) of instance add_tb.add_instance.csa
3_2_instance6.U1 of module FA1D0 <./add_WC.sdf, line 301>.
xmelab: *W,SDFNEP: Unable to annotate to non-existent path (IOPATH (negedge A) S) of instance add_tb.add_instance.csa
3_2_instance6.U1 of module FA1D0 <./add_WC.sdf, line 302>.
        Annotation completed with 0 Errors and 32 Warnings
        SDF statistics:
                No. of Pathdelays = 172         No. of Disabled Pathdelays = 0        Annotated = 90.70% (156/172)
                No. of Tchecks    = 72          No. of Disabled Tchecks    = 0        Annotated = 100.00% (72/72)
                                        Total(T)           Disabled(D)      Annotated(A)          Percentage(A/(T-D))
                Path Delays                172                   0               156                    90.70
                     $width                36                   0                36                   100.00
                  $setuphold               36                   0                36                   100.00
```

Should be 100% ideally, but lots of format issue

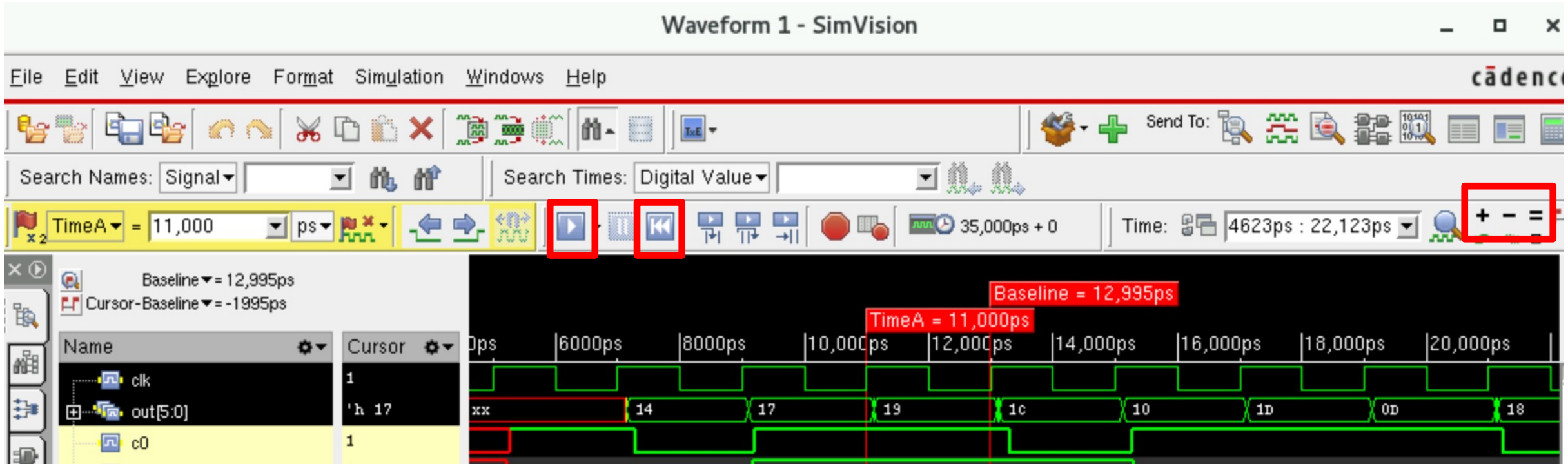


How to Use Xceilum



- select all the signals that you want to plot
- click plot icon
- Then, waveform viewer will pop-up including the signals you chose

How to Use Xceillum (similar to GTKwave)

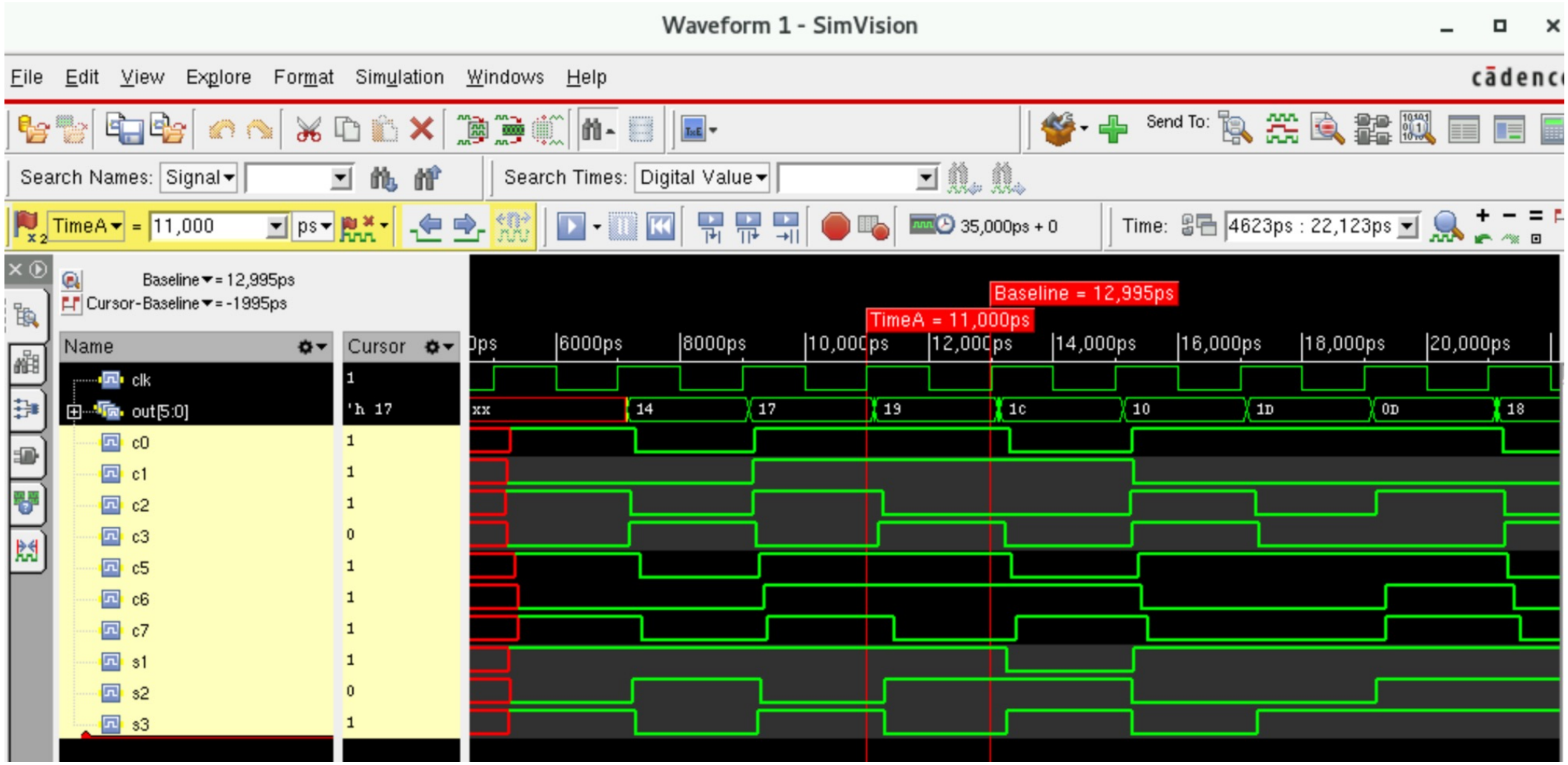


- play: run simulation
- rewind: go back before sim was executed,

e.g., could include additional signals and rerun

- + / - : zoom in / out
- mouse left button: timeA cursor moved
- mouse middle button: Baseline cursor moved
- = : zoom in between timeA and Baseline

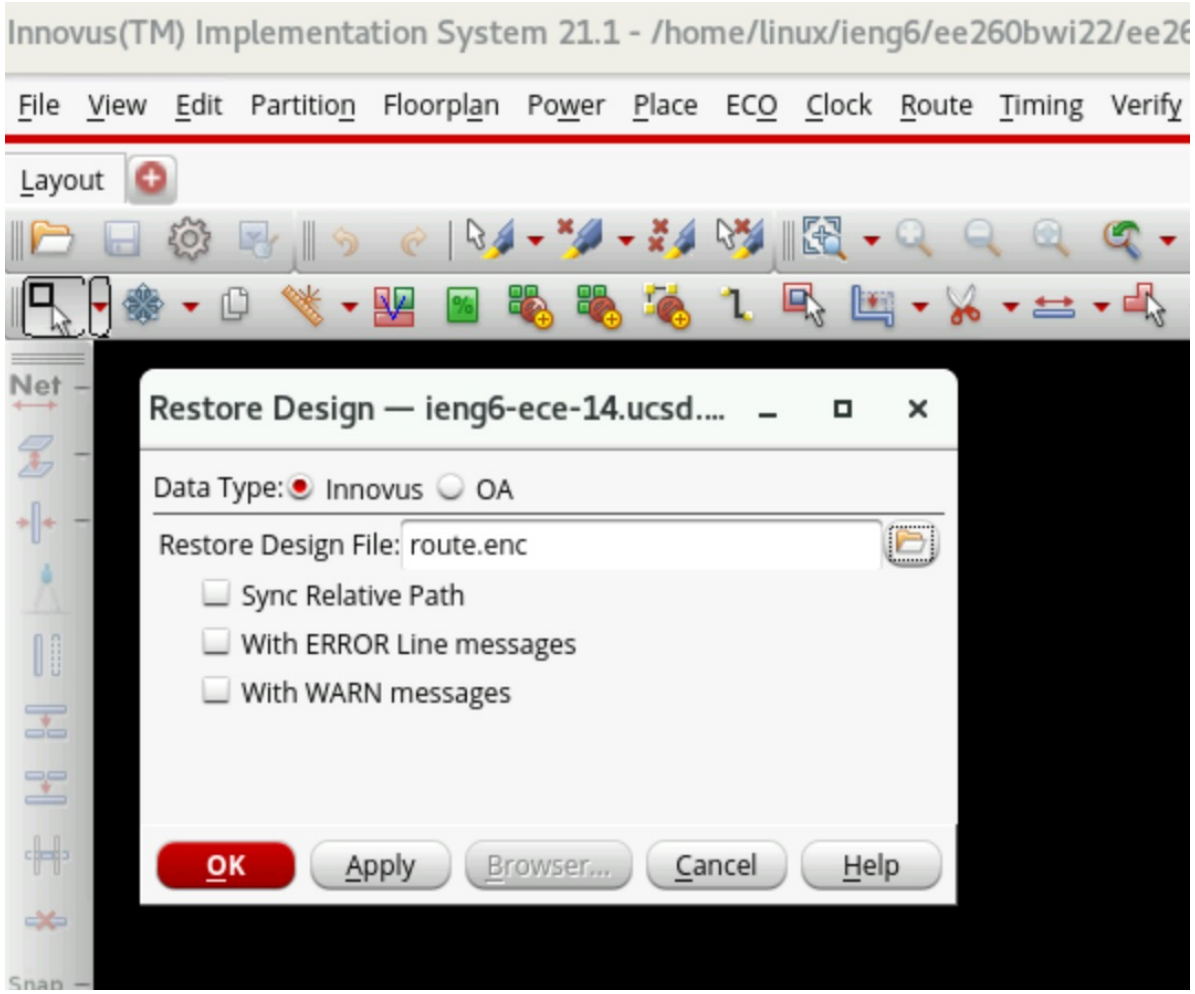
SDF Annotated Simulation Result



- Realistic delay info is shown for each signal

Power Measurement with VCD

[File]-[Restore Design] in Innovus

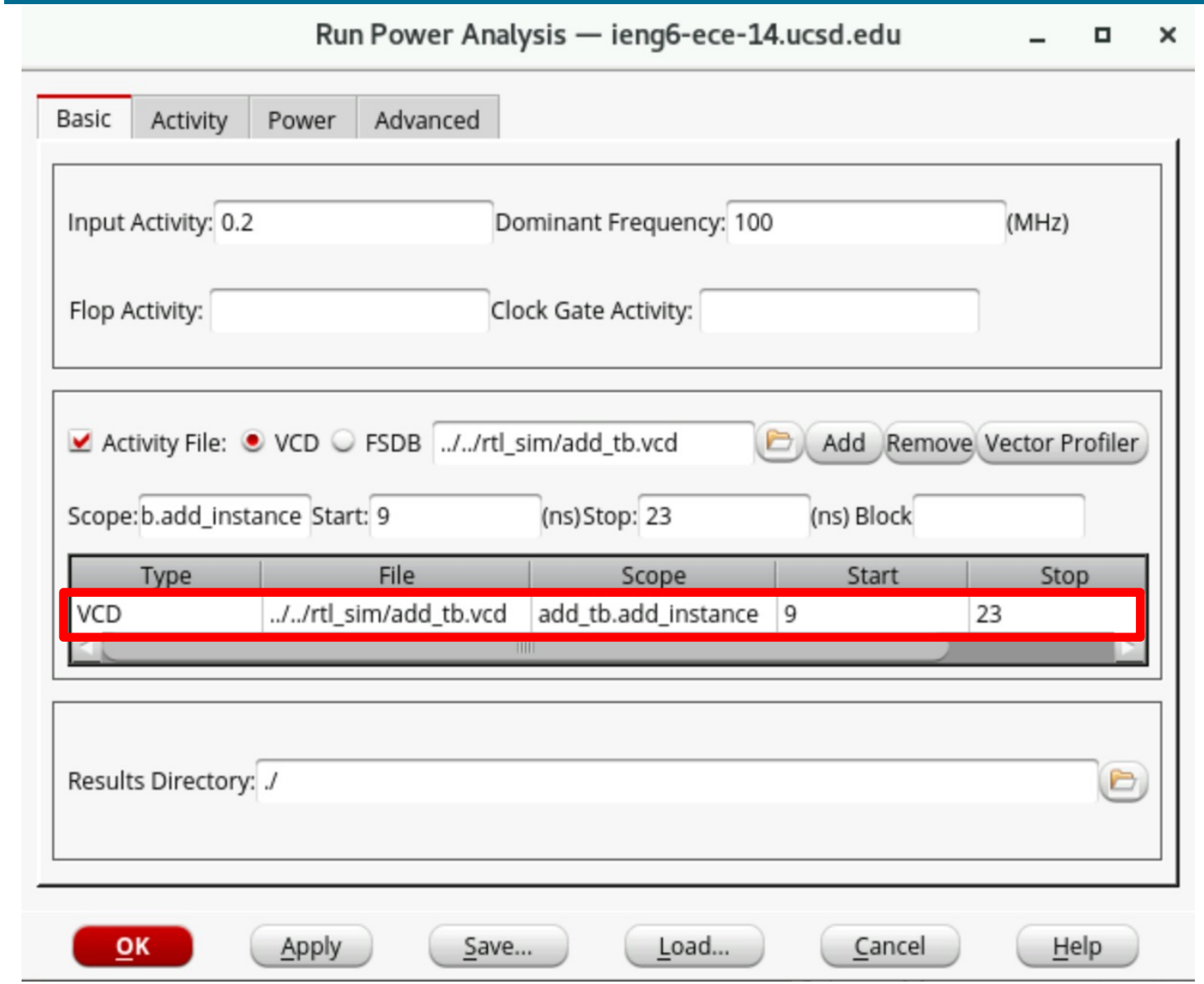


- Voltus is power-measure tool and integrated in Innovus
- Restore your design by clicking

  [File] – [Restore Design]

  e.g., route.enc file
- Click “physical view” button to see the designed blocks

Power Measure with VCD File



- Fill out vcd file name
- Fill time period to measure

  (pick multiple of complete period,

  e.g., 9-23 ns)
- Pick your scope

  e.g., add_tb.add_instance
- Click “ADD” button to see the red boxed area created

Power Measure with VCD File

successful log:

```
Activity annotation summary:
        Primary Inputs : 13/13 = 100%
          Flop outputs : 18/18 = 100%
  Memory/Macro outputs : 0/0 = 0%
      Tristate outputs : 0/0 = 0%
             Total Nets : 47/47 = 100%
```

unsuccessful log: due to view mismatch

```
** ERROR: (VOLTUS_POWR-2029): The view 'WC_VIEW' selected for power calculation
 is not active. Use report_analysis_views -type active
```

- should achieve 100% annotation from VCD file
- If view does not match, error can happen, e.g., when you save route.enc when BC_VIEW used.
- Then, you need to change view by typing as follows in the interactive window

```
setAnalysisMode -setup
set_analysis_view -setup WC_VIEW -hold WC_VIEW
```

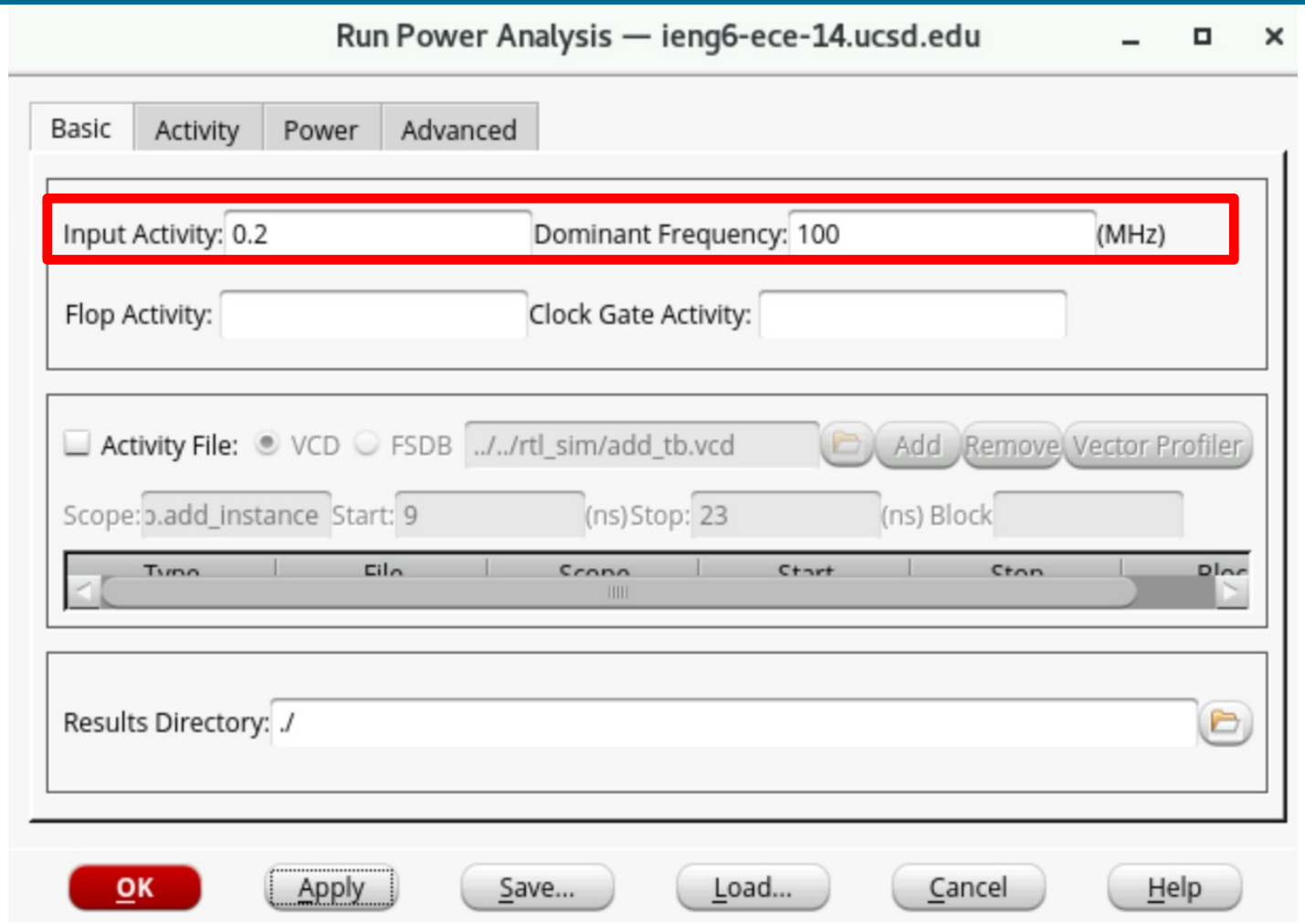
Measure Power Value with VCD File

```
Total Power
-----------------------------------------------------------------
Total Internal Power:        0.10351394            89.6188%
Total Switching Power:       0.00941049             8.1473%
Total Leakage Power:         0.00258030             2.2339%
Total Power:                 0.11550473
-----------------------------------------------------------------
```

- Measure power reported in the interactive screen, and also in log and <module name>.rpt file
- Even your vcd was generated without SDF file, you can still generate the power report with Innovus (might be less accurate)

Power Measurement without VCD

Power Measure without VCD File



- when you do not have VCD file,

  you can still generate report

- input activity and frequency should be filled out

- Though you change your freq., still sdc's freq will be used as below

```
** WARN:  (VOLTUS_POWR-1608):   Found conflicting clock definitions
for the same clock 'clk' in the SDC file.
  Retaining the last specified frequency of 833.333MHz.
```

Measured Power without VCD file

```
Total Power
-----------------------------------------------------------------------------------
Total Internal Power:         0.12639054            93.0077%
Total Switching Power:        0.00692690             5.0973%
Total Leakage Power:          0.00257508             1.8949%
Total Power:                  0.13589252
-----------------------------------------------------------------------------------
```

- measured power number is similar to the one with VCD
- Power number is proportional to input activity number

User-defined Activity

- For some signals, the activity is very low

  e.g., reset, instruction, MSB data

- each pin's activity can be defined by user in the

  interactive window as below:

```
set_switching_activity -activity 0.08 -pin y[3]
set_switching_activity -activity 0.08 -pin y[2]
...
```

add.rpt (~/lab4/rundir/run0) - GVIM4

```
User-Defined: net y[3] activity : 0
User-Defined: net y[2] activity : 0
User-Defined: net y[1] activity : 0
User-Defined: net y[0] activity : 0
User-Defined Activity : N.A.
Activity File: N.A.
Hierarchical Global Activity: N.A.
Global Activity: N.A.
Sequential Element Activity: N.A.
Primary Input Activity: 0.200000
```