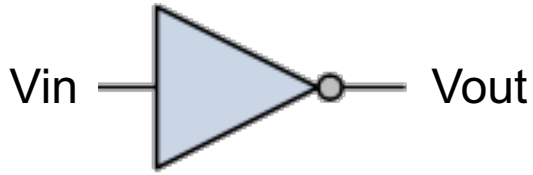
ECE260B Winter 22

Standard Cell

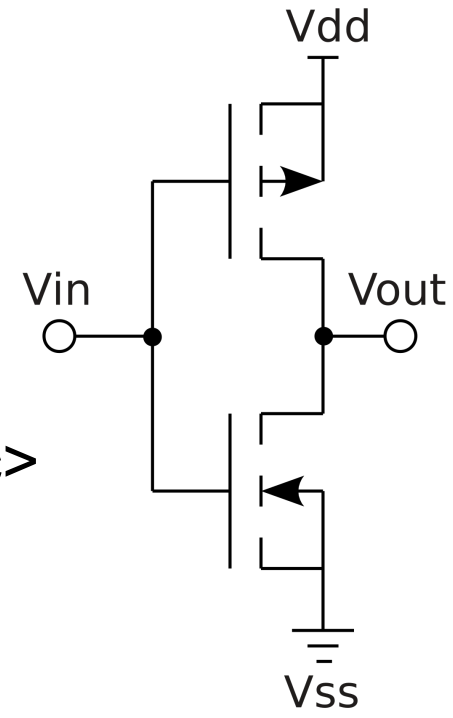
Prof. Mingu Kang

Standard Cell (STD)

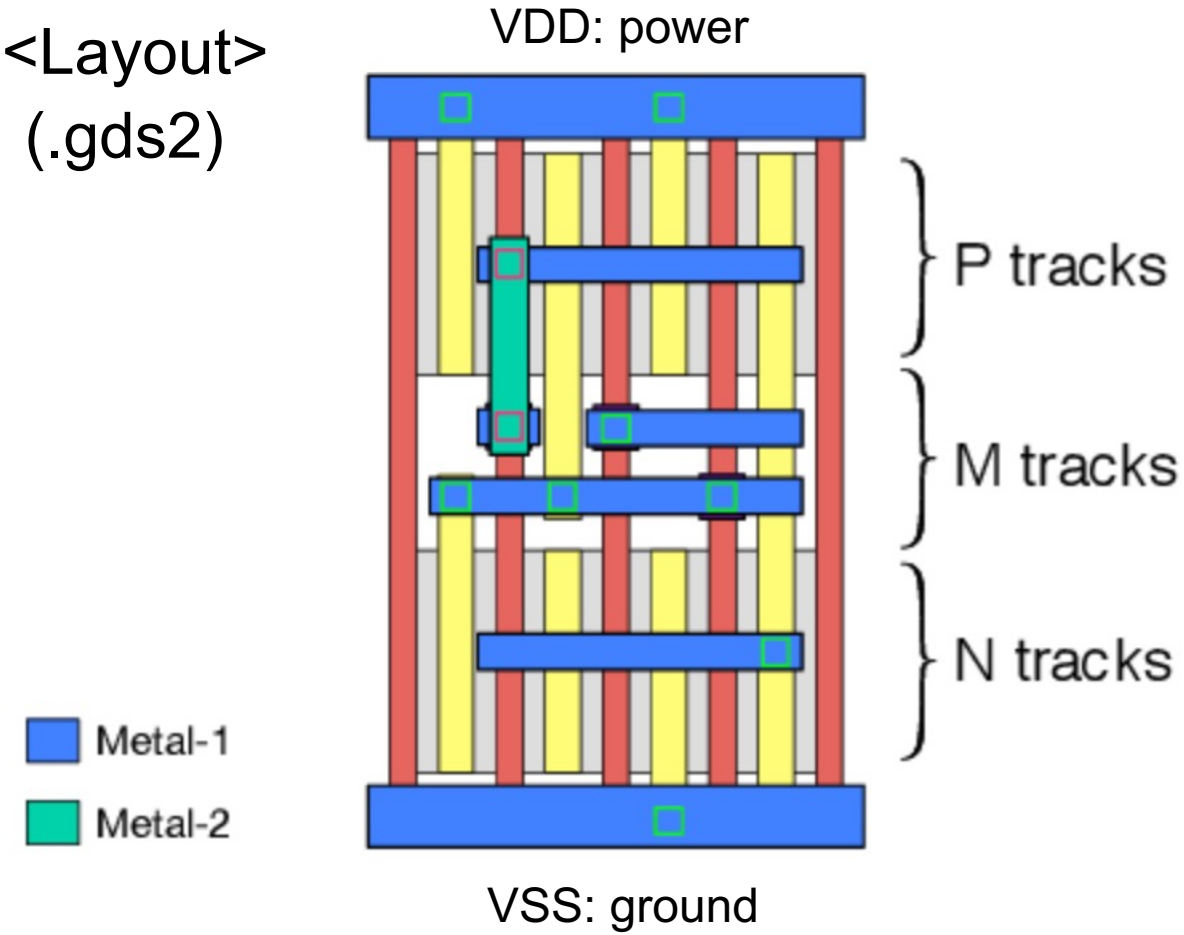
<Symbol>



<Schematic>

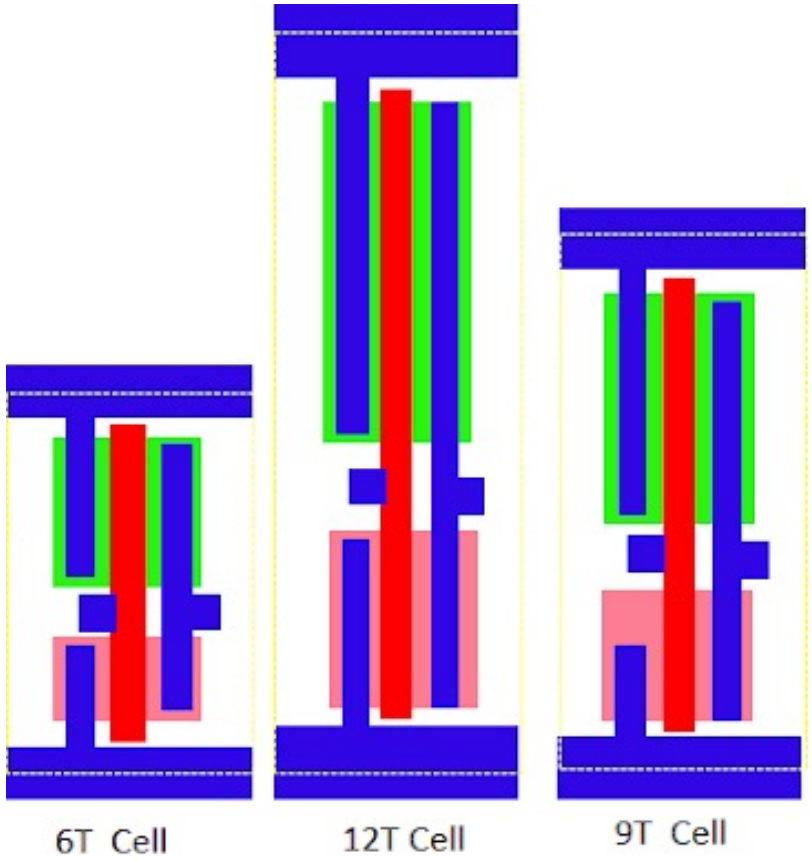


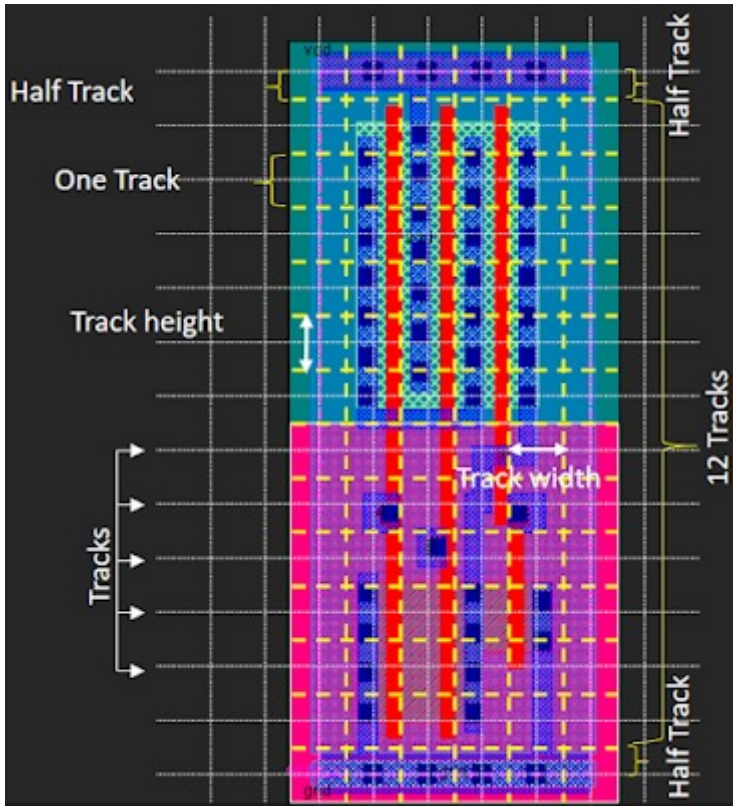
<Layout>
(.gds2)

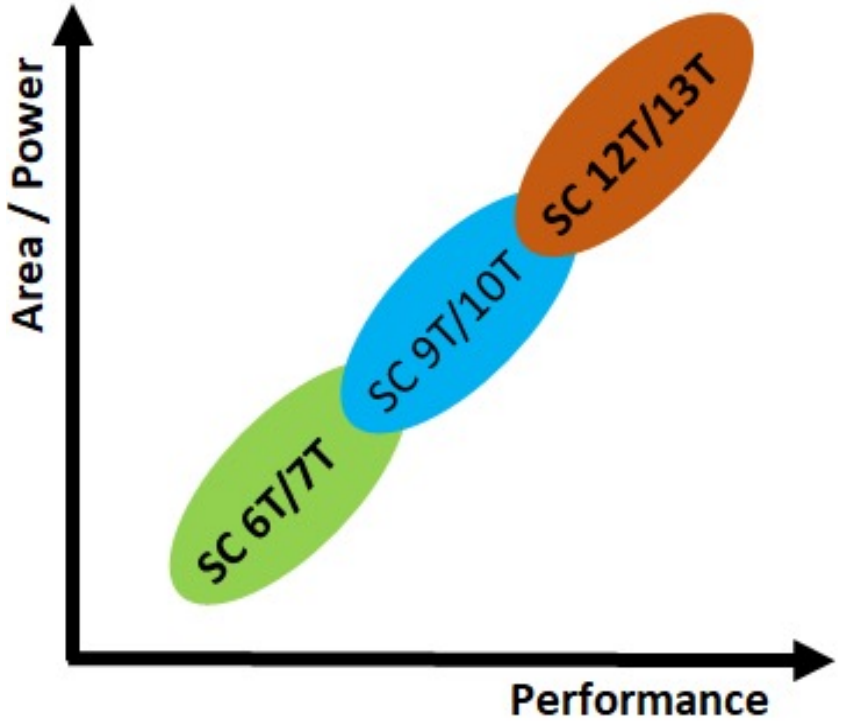


Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line, W. Ye

Standard Cell Topologies



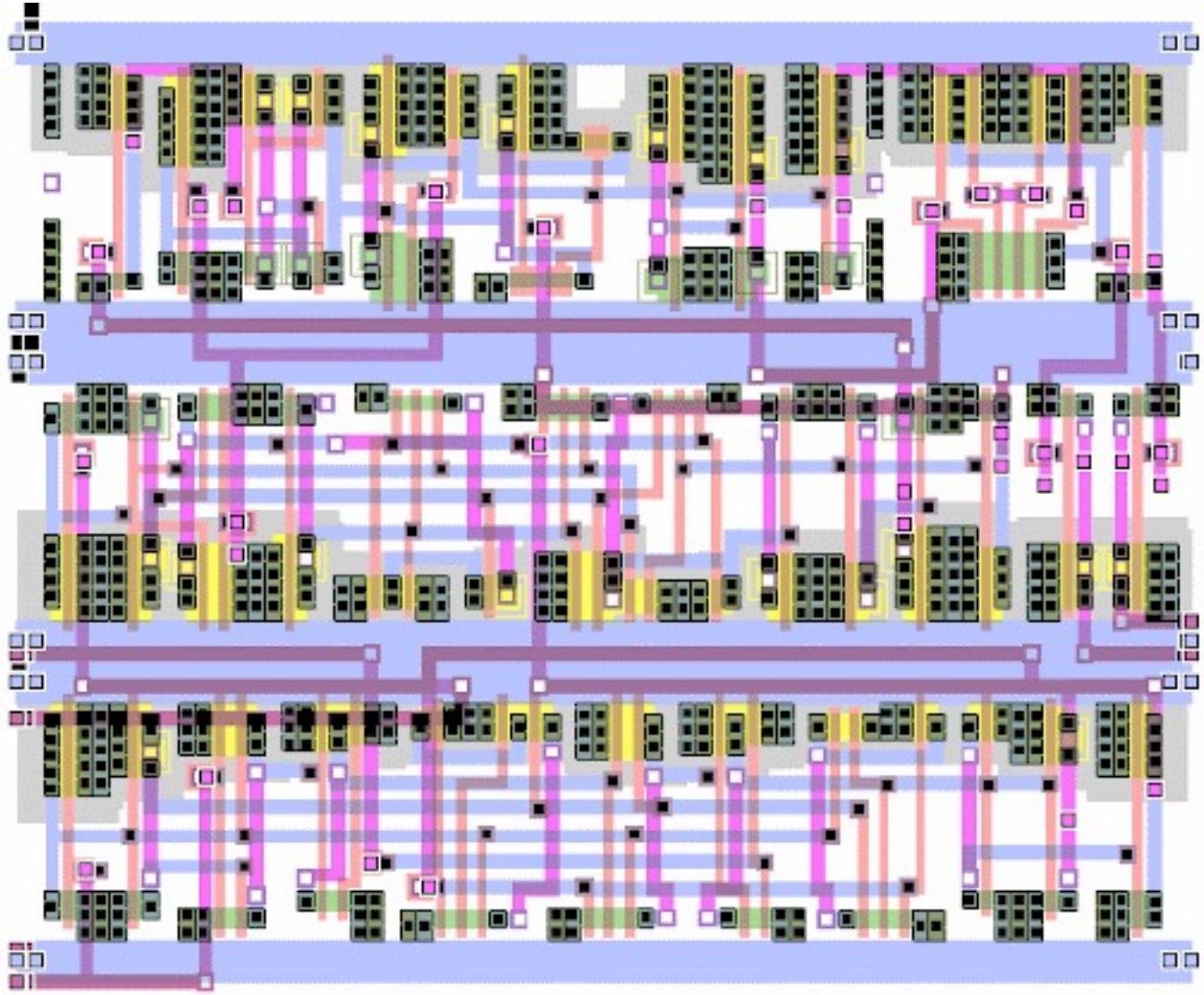




- Small track standard cells: high-density & low power consumption
- Large track standard cells: large area but having good performance

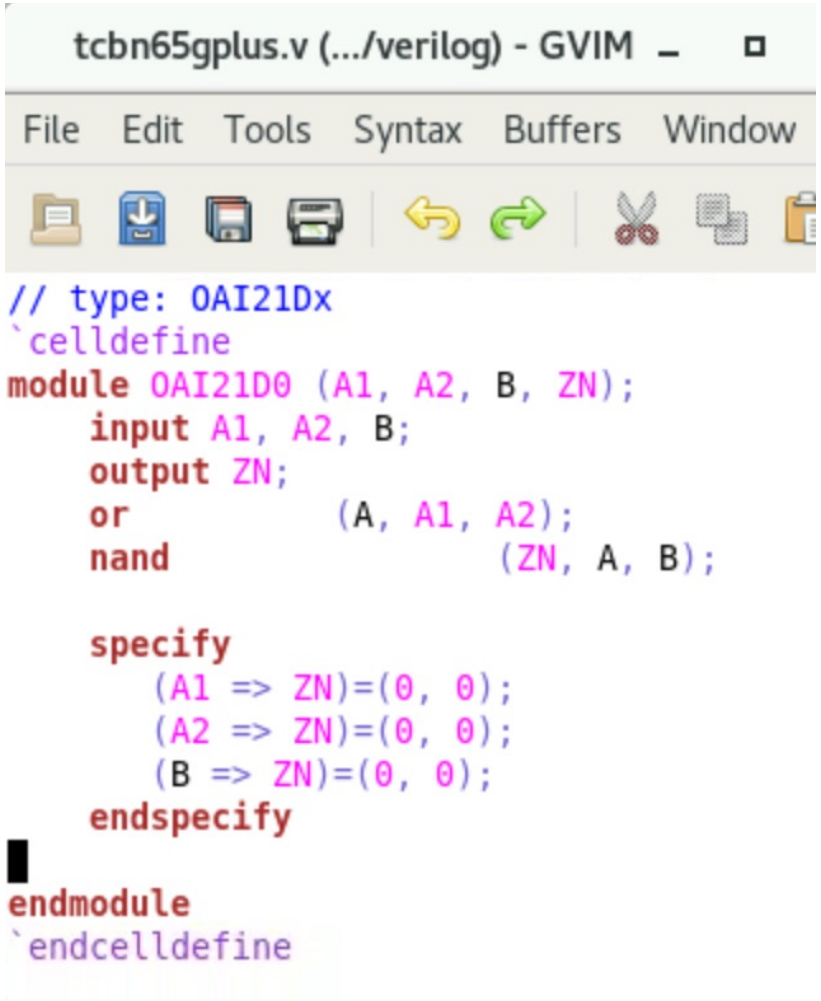
https://www.teamvlsi.com/2020/05/standard-cells.html

Logic with Multiple STD cells (Power / Ground Sharing)



http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_s00/Project/STANDARD%20CELL%20TEMPLATE%20DEFINITIONS_.htm

.v files

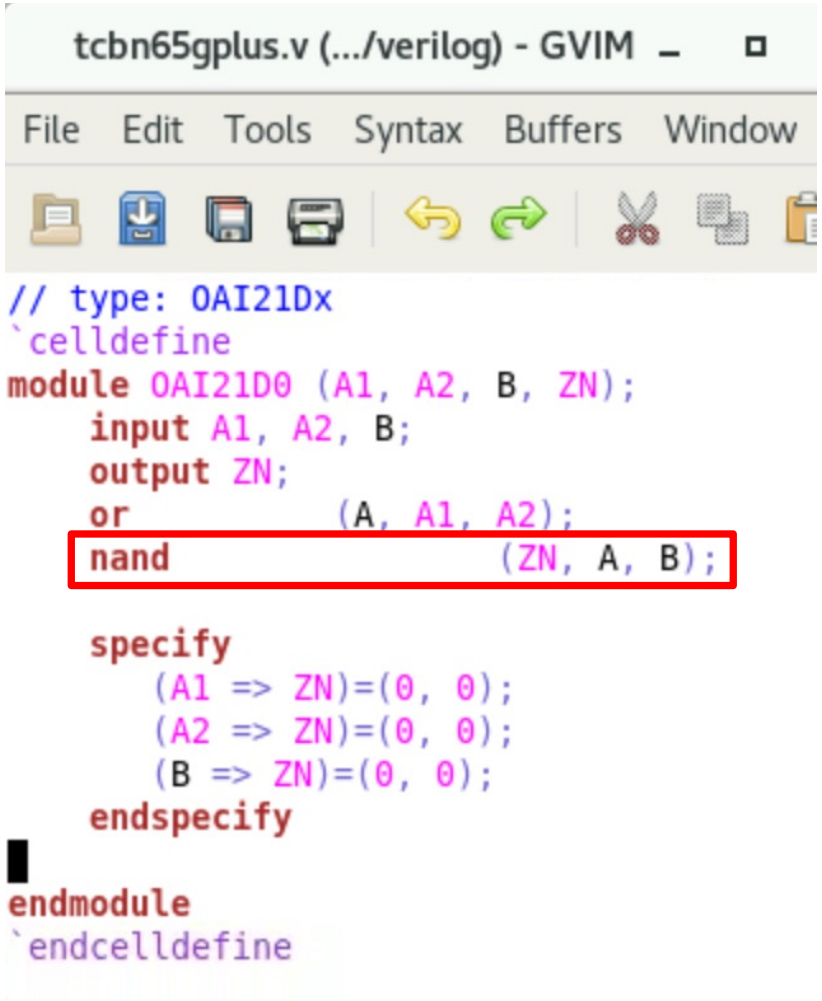


<verilog (.v)>

- behavior of each cell is described
- multiple versions for each threshold voltage
- Timing information (specify block) is 0, but

  will be overwritten by sdf (standard delay format) file

.v files



<verilog (.v)>

FYI

- OAI: OR -> And -> Inverter
- D0 / D1 / D2 … : gate size

  (sometimes, X1, X2, …)
- ZN: means inverted output
- Q: means latched (FF) output
- SI: scan chain input
- SE: scan chain enable
- specify: delay information

.lib file

tcbn65gplusbc.lib (~/PDKdata/lib) - GVIM

File Edit Tools Syntax Buffers Window Help

```
    internal_power() {
      related_pin : "A4";
      rise_power(energy_template_7x7) {
        index_1 ("0.0032, 0.0088, 0.0200, 0.0432, 0.0880, 0.1784, 0.3592");
        index_2 ("0.0038, 0.0091, 0.0196, 0.0408, 0.0830, 0.1676, 0.3367");
    values("0.0152, 0.0143, 0.0136, 0.0131, 0.0128, 0.0126, 0.0127", \
           "0.0151, 0.0143, 0.0136, 0.0131, 0.0128, 0.0126, 0.0127", \
           "0.0152, 0.0144, 0.0137, 0.0132, 0.0128, 0.0127, 0.0128", \
           "0.0156, 0.0148, 0.0141, 0.0136, 0.0132, 0.0131, 0.0132", \
           "0.0165, 0.0157, 0.0150, 0.0146, 0.0143, 0.0142, 0.0143", \
           "0.0188, 0.0178, 0.0171, 0.0167, 0.0165, 0.0164, 0.0165", \
           "0.0240, 0.0230, 0.0221, 0.0215, 0.0212, 0.0212, 0.0214");
      }
      fall_power(energy_template_7x7) {
        index_1 ("0.0032, 0.0088, 0.0200, 0.0432, 0.0880, 0.1784, 0.3592");
        index_2 ("0.0038, 0.0091, 0.0196, 0.0408, 0.0830, 0.1676, 0.3367");
    values("0.0205, 0.0191, 0.0175, 0.0158, 0.0147, 0.0143, 0.0141", \
           "0.0204, 0.0191, 0.0175, 0.0158, 0.0147, 0.0143, 0.0141", \
           "0.0207, 0.0193, 0.0176, 0.0160, 0.0148, 0.0144, 0.0142", \
           "0.0209, 0.0196, 0.0179, 0.0163, 0.0152, 0.0147, 0.0146", \
```

<power>

tcbn65gpluswc.lib (~/cs241data/libraries/lib) - GVIM1

File Edit Tools Syntax Buffers Window Help

```
    fall_capacitance : 0.0008;
  }
  pin(Z)  {
    direction : output;
    max_capacitance : 0.0842;
    function : "(A1 A2)";
    timing() {
      related_pin : "A1";
      timing_sense : positive_unate;
      cell_rise(delay_template_7x7) {
        index_1 ("0.0056, 0.0168, 0.0392, 0.0840, 0.1728, 0.3520, 0.7088");
        index_2 ("0.0009, 0.0023, 0.0049, 0.0102, 0.0208, 0.0419, 0.0842");
    values("0.0524, 0.0601, 0.0733, 0.0970, 0.1427, 0.2332, 0.4148", \
           "0.0550, 0.0627, 0.0758, 0.0995, 0.1452, 0.2357, 0.4170", \
           "0.0604, 0.0682, 0.0813, 0.1050, 0.1506, 0.2412, 0.4226", \
           "0.0720, 0.0796, 0.0927, 0.1164, 0.1621, 0.2529, 0.4343", \
           "0.0910, 0.0991, 0.1126, 0.1363, 0.1820, 0.2725, 0.4539", \
           "0.1157, 0.1249, 0.1391, 0.1634, 0.2095, 0.3001, 0.4806", \
           "0.1450, 0.1562, 0.1732, 0.1994, 0.2450, 0.3358, 0.5166");
      }
      rise_transition(delay_template_7x7) {
```

<timing>

- nominal temperature / voltage is written for each corner
- multiple corners / thresholds are provided in a separate files

.lib files for Multiple Corners of PVT

**_rvt_ff_1p1v_m40c.lib	**_hvt_ff_1p1v_m40c.lib	**_lvt_ff_1p1v_m40c.lib
**_rvt_ff_1p1v_0c.lib	**_hvt_ff_1p1v_0c.lib	**_lvt_ff_1p1v_0c.lib
**_rvt_ff_1p1v_125c.lib	**_hvt_ff_1p1v_125c.lib	**_lvt_ff_1p1v_125c.lib
**_rvt_ss_0p9v_m40c.lib	**_hvt_ss_0p9v_m40c.lib	**_lvt_ss_0p9v_m40c.lib
**_rvt_ss_0p9v_125c.lib	**_hvt_ss_0p9v_125c.lib	**_lvt_ss_0p9v_125c.lib
**_rvt_tt_1p0v_25c.lib	**_hvt_tt_1p0v_25c.lib	**_lvt_tt_1p0v_25c.lib

<Lib files for corner variations>

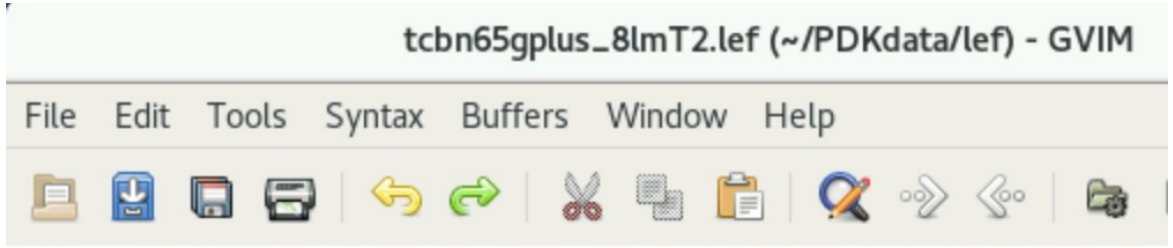
ff: nmos fast, pmos fast

ss: nmos slow, pmos slow

tt: nmos typical, pmos typical

fs: nmos fast, pmos slow

.lef file

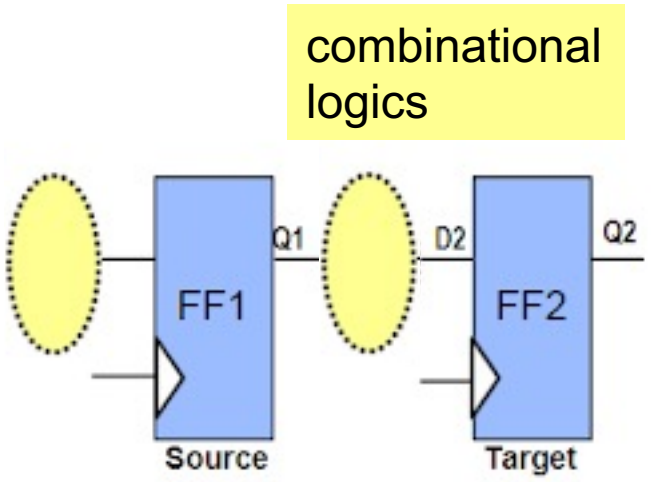


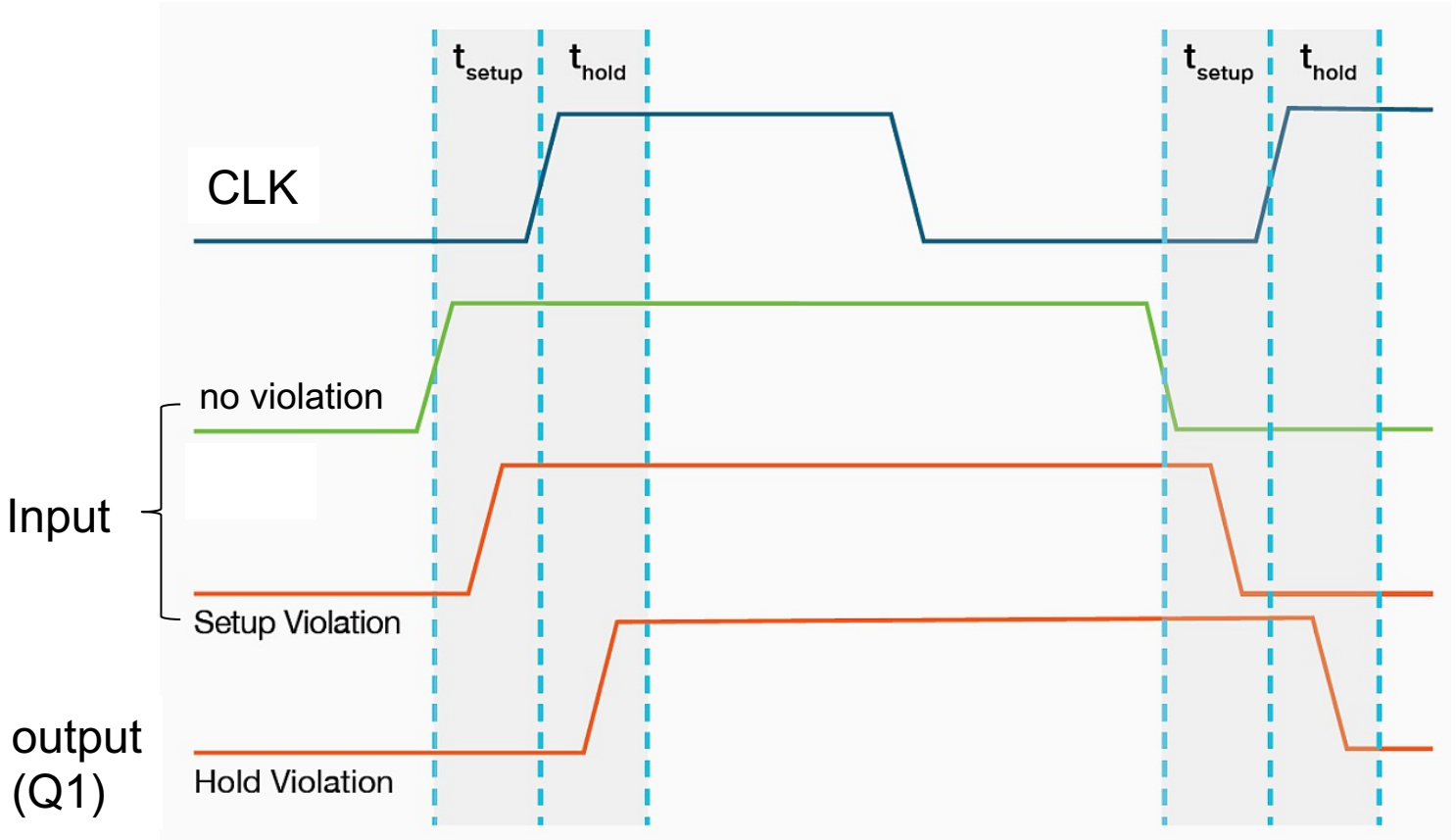

```
MACRO IOA22D4
    CLASS CORE ;
    FOREIGN IOA22D4 0.000 0.000  ;
    ORIGIN 0.000 0.000 ;
    SIZE 3.600 BY 1.800 ;
    SYMMETRY x y ;
    SITE core ;
    PIN ZN
        ANTENNADIFFAREA 0.3640 ;
        DIRECTION OUTPUT ;
        PORT
        LAYER M1 ;
        RECT  2.650 1.015 2.795 1.125 ;
        RECT  2.650 0.310 2.750 0.635 ;
        RECT  2.635 0.310 2.650 1.125 ;
        RECT  2.350 0.525 2.635 1.125 ;
        RECT  2.065 0.525 2.350 0.635 ;
        RECT  2.065 1.015 2.350 1.125 ;
        END
    END ZN
    PIN B2
        ANTENNAGATEAREA 0.0433 ;
```

- .lef file: abstract description of the location of metals and pins as a text format

- .gds2 file: full layout information including all the layers and connectinos

Why do we care multiple corners?





- Setup time violation: vulnerable in SS corner

- Hold time violation: vulnerable in FF corner

Announcement

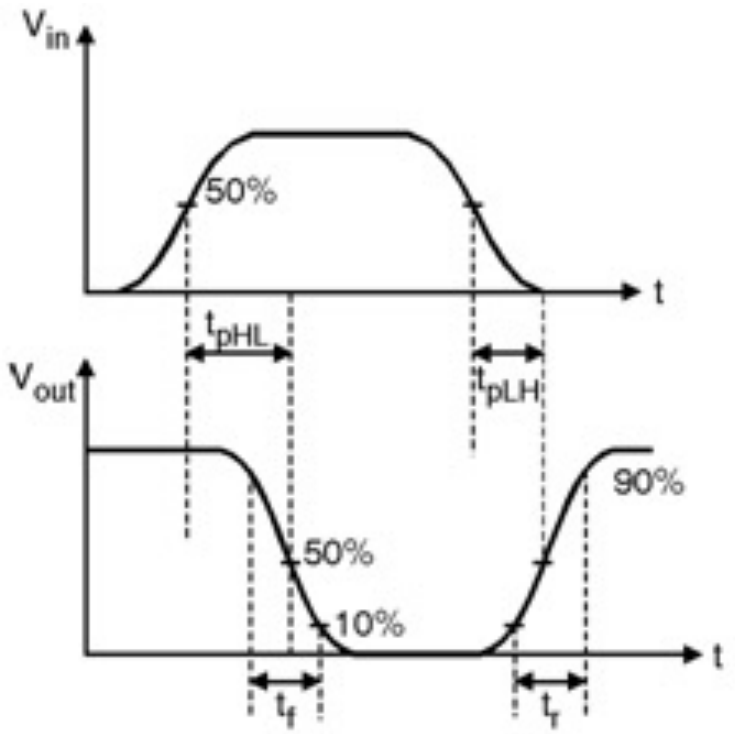
- Today was HW1 deadline, will be graded by Next Monday 9pm
- Technical questions -> Discussion tab
- Private questions -> ece260ucsd@gmail.com
- Please check previous questions in the discussion tab
- Students are encouraged to reply in the discussion tab
- Check public/PDK-group-accts-added file to find your ID

[HW2] Corner Hspice Simulations

- copy public/w2/virtuoso_sim/hspice_ff/nom/ss.include to your home folder
- Design 6 inverter chain with W90nm / L50nm (for both width / length) nmos and pmos transistors
- run corner simulations for all 3 corners (ff / nom / ss) with following temperatures in the table
- compare your 50-50% (t_{phl} and t_{plh}) delay (from input to output) to bu

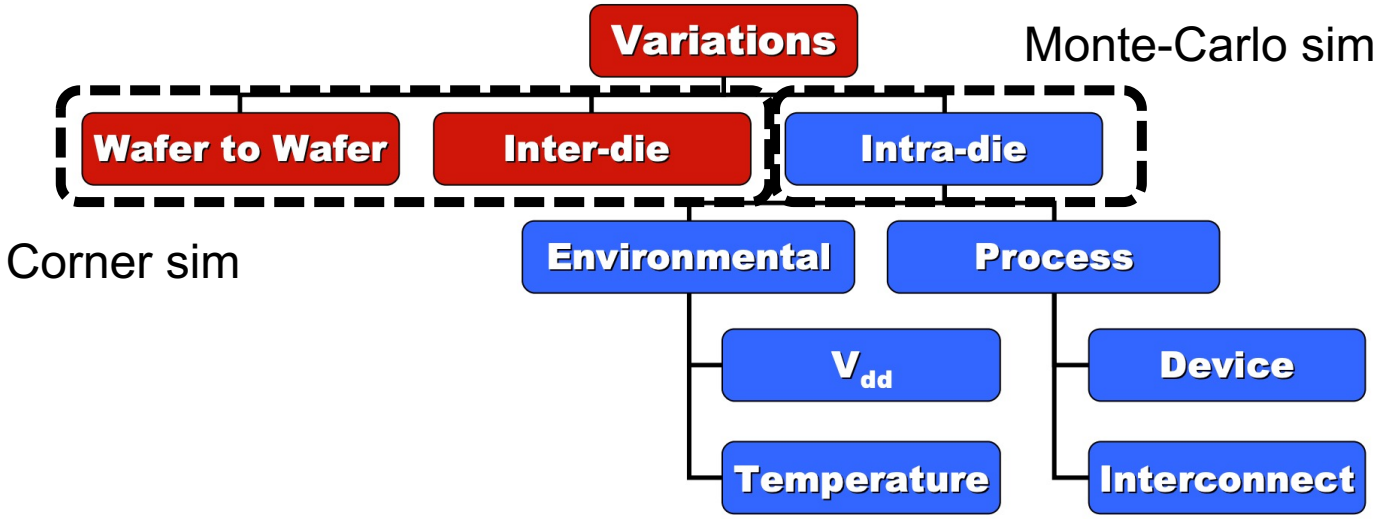
  your observation
- Vdd: 1V, slope: 100ps, use VTG transistor

	ff / 0 ℃ / 1.1V	tt / 125 ℃ / 0.9V	ss / 125 ℃ / 0.9V	Ratio of ss/ff (%)
tphl				
tplh				

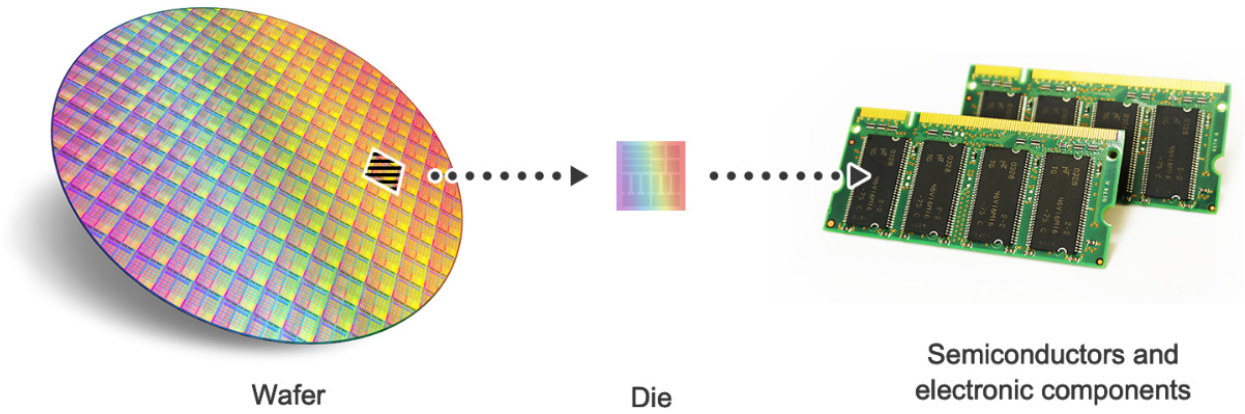


https://www.electronics-tutorial.net/Digital-CMOS-Design/Propagation-Delay/Delay-Estimation/

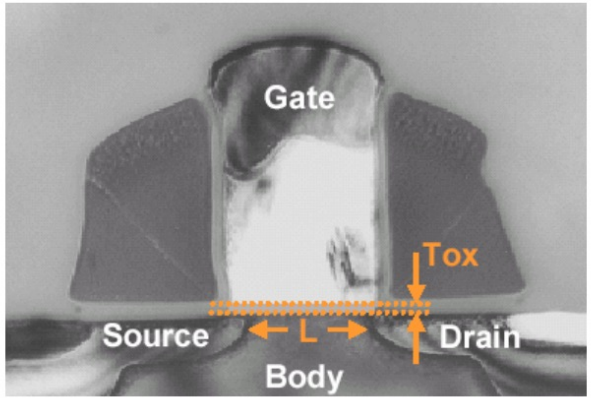
Variations



- Intra-die variations: variations within a single die
- Inter-die variations: variations across multiple dies

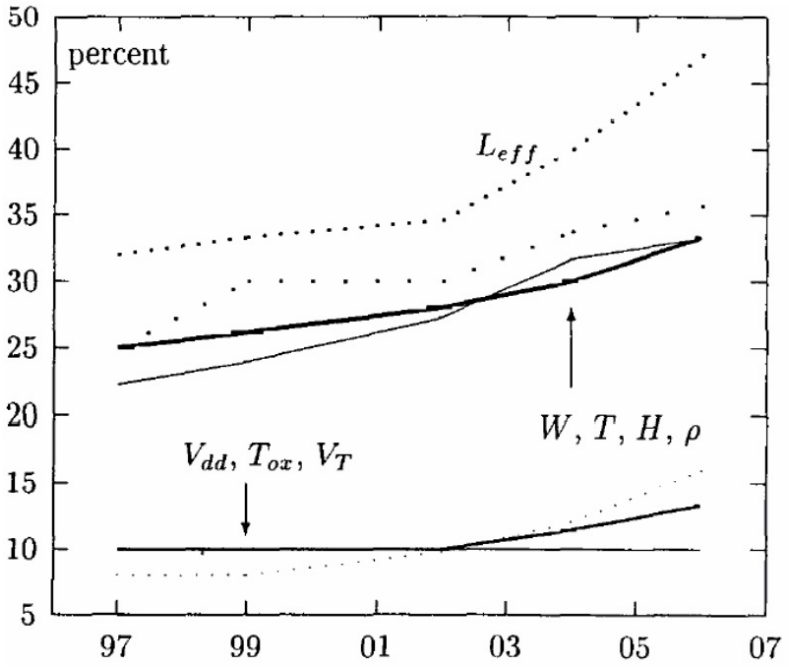


Source of Process Variations



Source of variations

- Lithography imperfection
- Random dopant fluctuation



Year	L_{eff}	T_{ox}	V_{dd}	V_t	W	H	ρ
1997	32	8	10	10	25	25	22
1999	33	8	10	10	26	33	24
2002	35	10	10	10	28	30	27
2005	40	12	10	12	30	34	32
2006	47	16	10	14	33	36	33

% variation from mean value

ISSCC00, IBM

Monte-Carlo Simulations

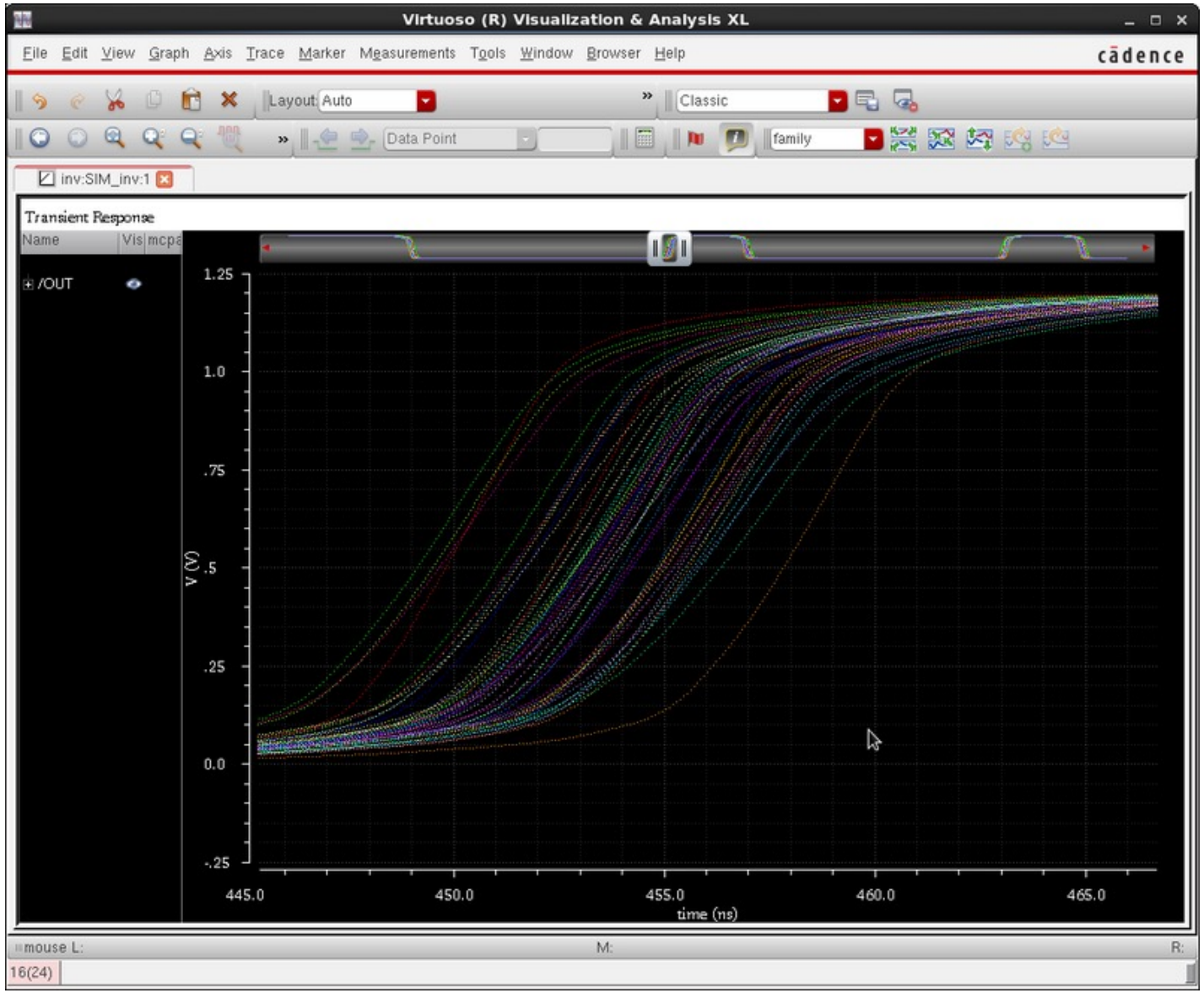
- Inject variations (usually normal variation) with mean (μ) and standard deviation (σ) for all the variables

  e.g., $v'_{th} \sim N(v_{th}, \sigma_{vth})$

- Then, observe the impact from the variations with multiple (>1000) iterations

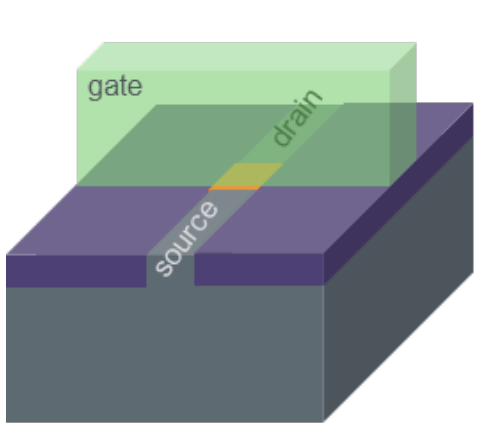
https://www.electronics-tutorial.net/Digital-CMOS-Design/Propagation-Delay/Delay-Estimation/

Monte-Carlo Simulation Results

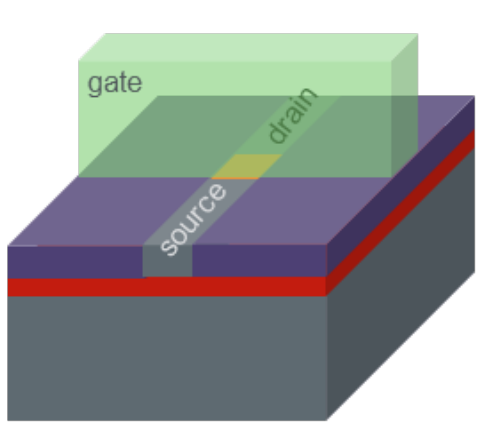


https://nano.wiki.ifi.uio.no/Cadence-Tutorial-English-cadence_6.1.6

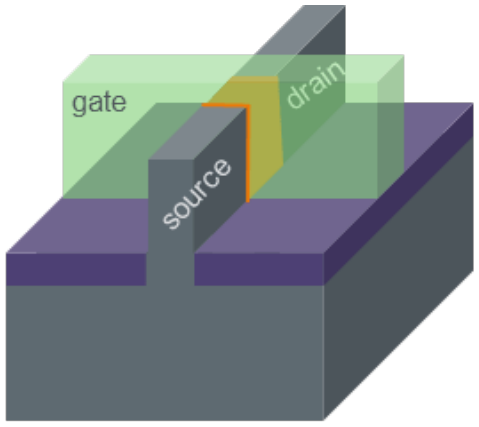
FD-SOI and finFET Technology



planar

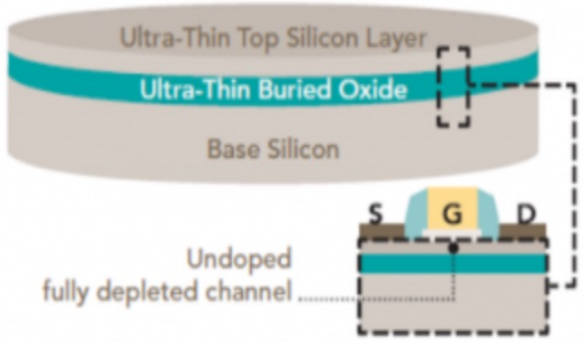


FD-SOI



finFET

Gate
High K Dielectric
Oxide
Silicon
Buried Oxide



FD-SOI architecture

$$\sigma_{\Delta VT} \propto \frac{\sqrt[4]{N_a}}{\sqrt{W \times L}}$$

N_a: dopant level

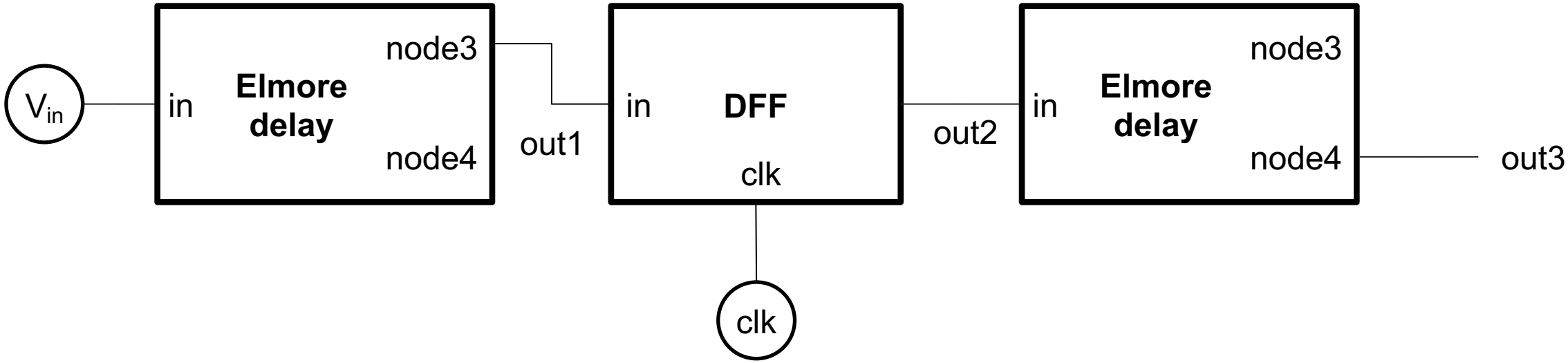
- Fully-depleted SOI
  - ultra-thin channel -> high gate controllability
  - undoped channel -> low variation
- finFET
  - 3D gate controllability
  - quantized TR width as height is fixed and width controlled by # of fins

https://semiengineering.com/the-challenges-of-process-control-on-finfets-and-fd-soi/

Bridging Analog-to-Digital Domain

See demonstration

HW: Bridging Analog-to-Digital Domain



- Build above schematic by reusing your Elmore delay block, but this time, use R=1K and C=20f everywhere
- Vin and clk are Vpulse, but Vin's period = 10ns, clk's period = 2ns (Duty cycle: 50% for both)
- Vin and clk's "Delay Time"s are 1.5ns and 1ns, respectively
- Amplitude of clk and Vin are 1V for both
- Plot Vin, clk, out1, out2, out3 from AMS simulation with duration of 20ns