

TPS22948 5.5-V, 240-mA Current Limited Load Switch with Reverse Current Blocking

1 Features

- Input operating voltage range (V_{IN}):
2.5 V to 5.5 V
- Output current limit (I_{LIMIT}):
240 mA (typical)
- Thermal shutdown (TSD)
- ON-Resistance (R_{ON}):
300 mΩ (typical)
- Slow Turn ON timing limits inrush current (typical):
 - Turn ON time (t_{ON}):
820 μs at 6.6 mV/μs
- Always-ON Reverse Current Blocking (RCB):
 - ON State activation current (I_{RCB}):
–200 mA (typical)
- Fault indication (FLT)
- Smart ON pin pull down ($R_{PD,ON}$):
 - ON V_{IH} (I_{ON}): 25 nA (maximum)
 - ON V_{IL} ($R_{PD,ON}$): 500 kΩ (typical)
- Low power consumption:
 - ON State (I_O): 50 uA (typical)
 - OFF State (I_{SD}): 0.3 uA (typical)

2 Applications

- Personal electronics
- Set top box
- HDMI output ports
- Notebook, desktop PC
- Docking stations

3 Description

The TPS22948 device is a small, single channel load switch with robust protection against fault cases with output current limiting, reverse current blocking, and thermal shutdown.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. When power is first applied, a smart pull down is used to keep the ON pin from floating until system sequencing is complete. Once the pin is deliberately driven high (>VIH), the smart pull down will be disconnected to prevent unnecessary power loss.

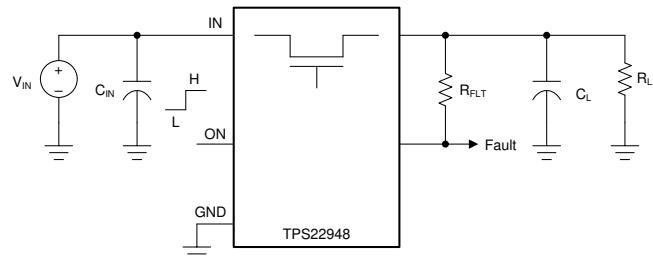
TPS22948 is available in a standard SC-70 package characterized for operation over a temperature range of -40°C to 125°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22948	SC-70 (6)	2.1 mm x 2.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

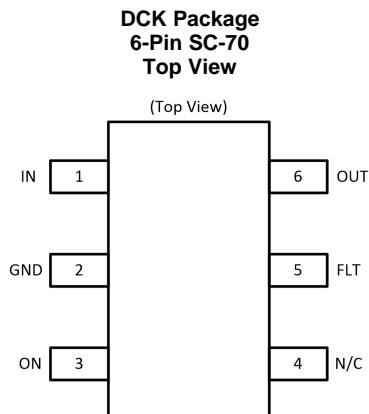
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4 Revision History

Changes from Original (March 2019) to Revision A	Page
• Changed from Advance Information to Production Data	1
• First Public Release	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input
2	GND	–	Device ground
3	ON	I	Active high switch control input. Do not leave floating.
4	N/C	–	No connect pin, leave floating or GND
5	FLT	O	Open-drain output, pulled low during thermal shutdown or reverse current-conditions.
6	OUT	O	Switch output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Maximum Input Voltage Range	-0.3	6	V
V _{OUT}	Maximum Output Voltage Range	-0.3	6	V
V _{ON}	Maximum ON Pin Voltage Range	-0.3	6	V
V _{FLT}	Maximum FLT Pin Voltage	-0.3	6	V
I _{MAX}	Maximum Output Current	Internally Limited		A
T _J	Junction temperature	Internally Limited		°C
T _{STG}	Storage temperature	-65	150	°C
T _{LEAD}	Maximum Lead Temperature (10 s soldering time)	300		°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{IN}	Input Voltage Range	2.5	5.5		V
V _{OUT}	Output Voltage Range	0	5.5		V
V _{IH}	ON Pin High Voltage Range	1	5.5		V
V _{IL}	ON Pin Low Voltage Range	0	0.35		V
I _{OUT}	Output Current Range	0	130		mA
C _{OUT} ⁽¹⁾	Output Capacitance	18			nF
T _A	Ambient temperature	-40	125		°C

- (1) The recommended output capacitance is the capacitance placed next to the output of the device that will provide optimal hard short performance across different load cable lengths.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22948	UNIT
		DCK (SC-70)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	213.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	148.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	66.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	50.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	66.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Unless otherwise noted, the characteristics in the following table applies at 5 V with a load of $C_L = 0.1 \mu\text{F}$, $R_L = 100 \Omega$. Typical Values are at 25°C.

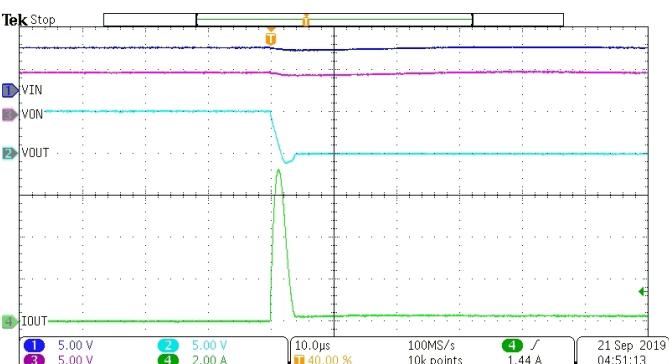
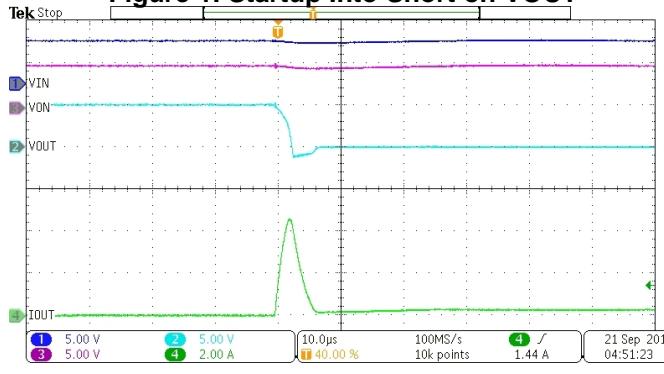
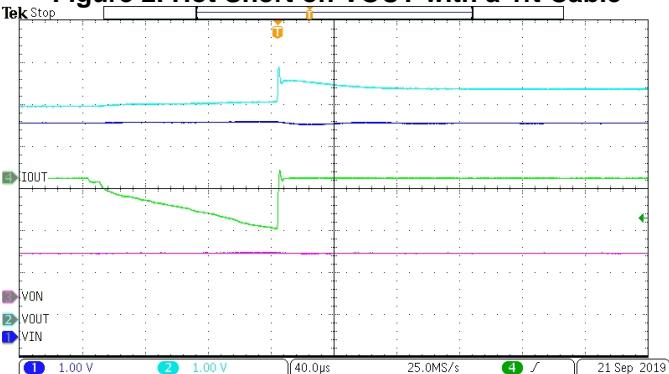
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Supply (VIN)							
I_Q, VIN	VIN Quiescent Current	$V_{ON} \geq V_{IH}$, $V_{OUT} = \text{Open}$		-40°C to 125°C	50	85	μA
I_{SD}, VIN	VIN Shutdown Current	$V_{ON} \leq V_{IL}$, $V_{OUT} = \text{GND}$		-40°C to 125°C	0.3	5	μA
ON-Resistance (RON)							
R_{ON}	ON-State Resistance	$I_{OUT} = -50 \text{ mA}$	25°C	300	350		$\text{m}\Omega$
			-40°C to 85°C	450			
			-40°C to 125°C	500			
Output Current Limit (ILIM)							
I_{LIM}	Output Current Limit		-40°C to 125°C	130	240	350	mA
t_{LIM}	Current Limit Response Time	Output hard short ($I_{OUT} > I_{LIM}$)	-40°C to 125°C	2			μs
Reverse Current Blocking (RCB)							
V_{RCB}	Activation Threshold	$V_{OUT} \text{ Rising}; V_{OUT} > V_{IN}$	-40°C to 125°C	60			mV
	Release Threshold	$V_{OUT} \text{ Falling}; V_{OUT} > V_{IN}$	-40°C to 125°C	44			mV
t_{RCB}	Response Time	$V_{OUT} = V_{IN} + 1\text{V}$	-40°C to 125°C	3			μs
I_Q, RCB	RCB Quiescent Current (VIN)	$V_{ON} \leq V_{IL}$ $V_{OUT} - V_{IN} = 1\text{V}$	$V_{ON} \leq V_{IL}$ $V_{OUT} - V_{IN} = 1\text{V}$	-40°C to 125°C	15		μA
Fault Indication (FLT)							
$V_{OL, \text{FLT}}$	Output Low Voltage	$I_{FLT} = 1 \text{ mA}$	-40°C to 125°C	0.1			V
$t_{DG, \text{FLT}}$	Fault Delay Time	$V_{ON} \geq V_{IH}$	-40°C to 125°C	10			μs
I_{FLT}	Off State Leakage	$V_{ON} \leq V_{IL}$	-40°C to 125°C	25			nA
Enable Pin (ON)							
$R_{PD, \text{ON}}$	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$	-40°C to 85°C	500			$\text{k}\Omega$
I_{ON}	ON Pin Leakage	$V_{ON} \geq V_{IH}$	-40°C to 125°C	25			nA
Thermal Shutdown (TSD)							
TSD	Thermal Shutdown	Rising	N/A	130	150	170	$^{\circ}\text{C}$
		Falling (Hysteresis)	N/A	100	120	140	$^{\circ}\text{C}$

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies at 5 V and 25°C

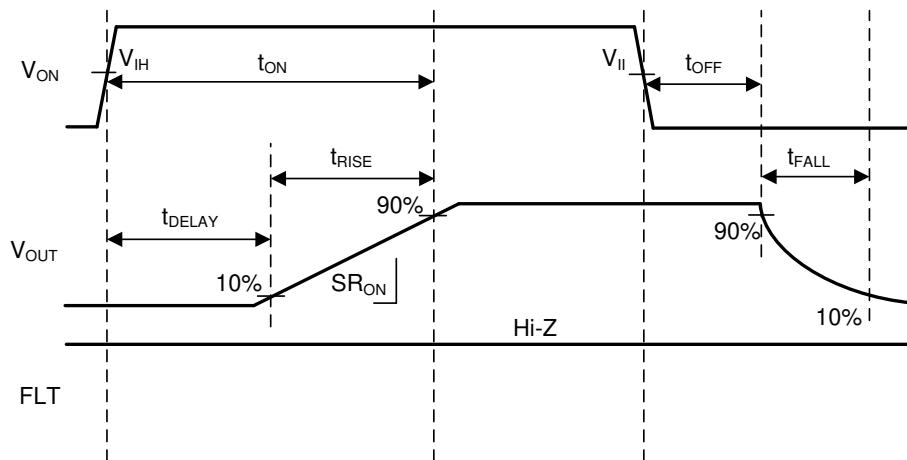
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	$C_L = 18 \text{ nF}$, $R_L = 100 \Omega$		820		μs
t_R	Output Rise Time	$C_L = 18 \text{ nF}$, $R_L = 100 \Omega$		600		μs
SR_{ON}	Turn ON Slew Rate	$C_L = 18 \text{ nF}$, $R_L = 100 \Omega$		6.6		$\text{mV}/\mu\text{s}$
t_{OFF}	Turn OFF Time	$C_L = 18 \text{ nF}$, $R_L = 100 \Omega$		15		μs
t_{FALL}	Output Fall Time	$C_L = 18 \text{ nF}$, $R_L = 100 \Omega$		6.9		μs

6.7 Typical Characteristics


 $V_{IN} = 5 \text{ V}$ $T_A = 25 \text{ }^\circ\text{C}$ $V_{OUT} = 0 \text{ V}$
Figure 1. Startup Into Short on VOUT

 $V_{IN} = 5 \text{ V}$ $T_A = 25 \text{ }^\circ\text{C}$ $C_{OUT} = 18 \text{ nF}$

 $V_{IN} = 5 \text{ V}$ $T_A = 25 \text{ }^\circ\text{C}$ $C_{OUT} = 18 \text{ nF}$
Figure 3. Hot Short on VOUT with a 3ft Cable

 $V_{IN} = 5 \text{ V}$ $T_A = 25 \text{ }^\circ\text{C}$
Figure 4. Reverse Current Blocking Behavior

7 Parameter Measurement Information

7.1 Timing Waveform Diagram


Figure 5. Timing Waveforms

8 Detailed Description

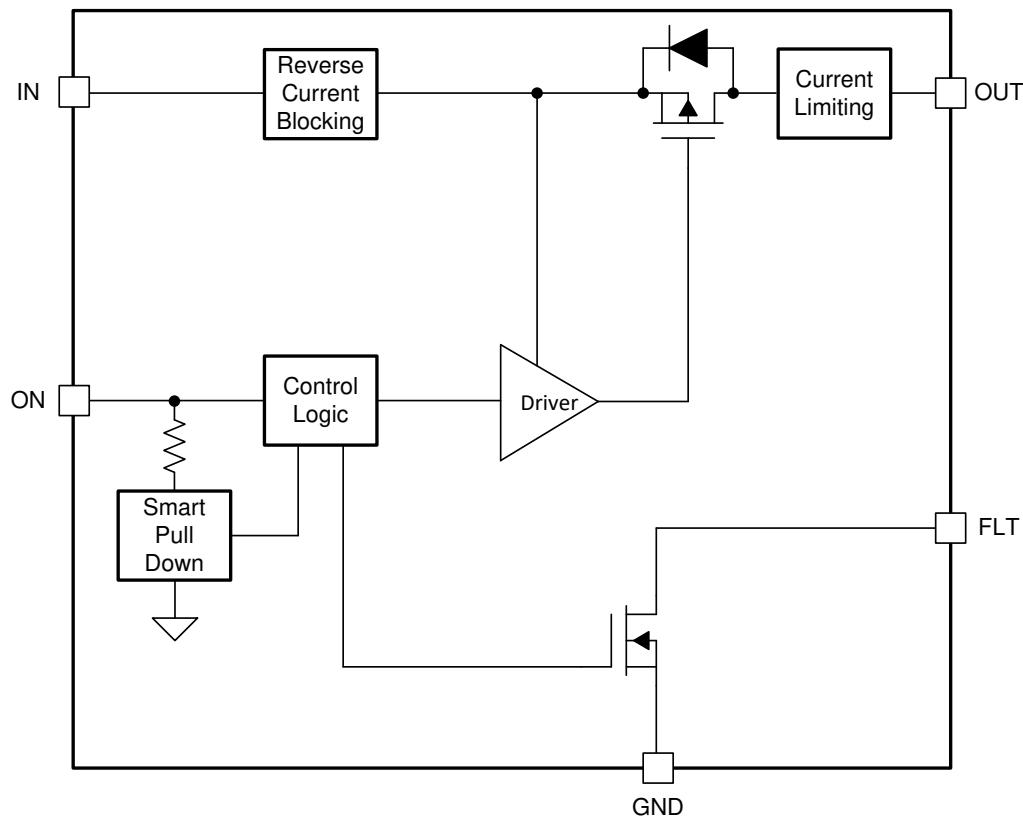
8.1 Overview

The TPS22948 device is a 5.5-V, 240-mA current limited load switch in a 6-pin SC-70 package. The 300-mΩ P-channel FET is used to switch power from input to output with minimal voltage drop across the device.

The TPS22948 device has a slow slew rate which helps reduce or eliminate power supply droop because of large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, and driver eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The TPS22948 load switch also provides protection features such as reverse current blocking, output current limiting and thermal shutdown.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to VIN, a smart pull down is used to keep the ON pin from floating until system sequencing is complete. Once the ON pin is deliberately driven high ($\geq V_{IH}$), the smart pull down is disconnected to prevent unnecessary power loss. See [Table 1](#) when the ON pin smart pull down is active.

Table 1. Smart-ON Pull Down

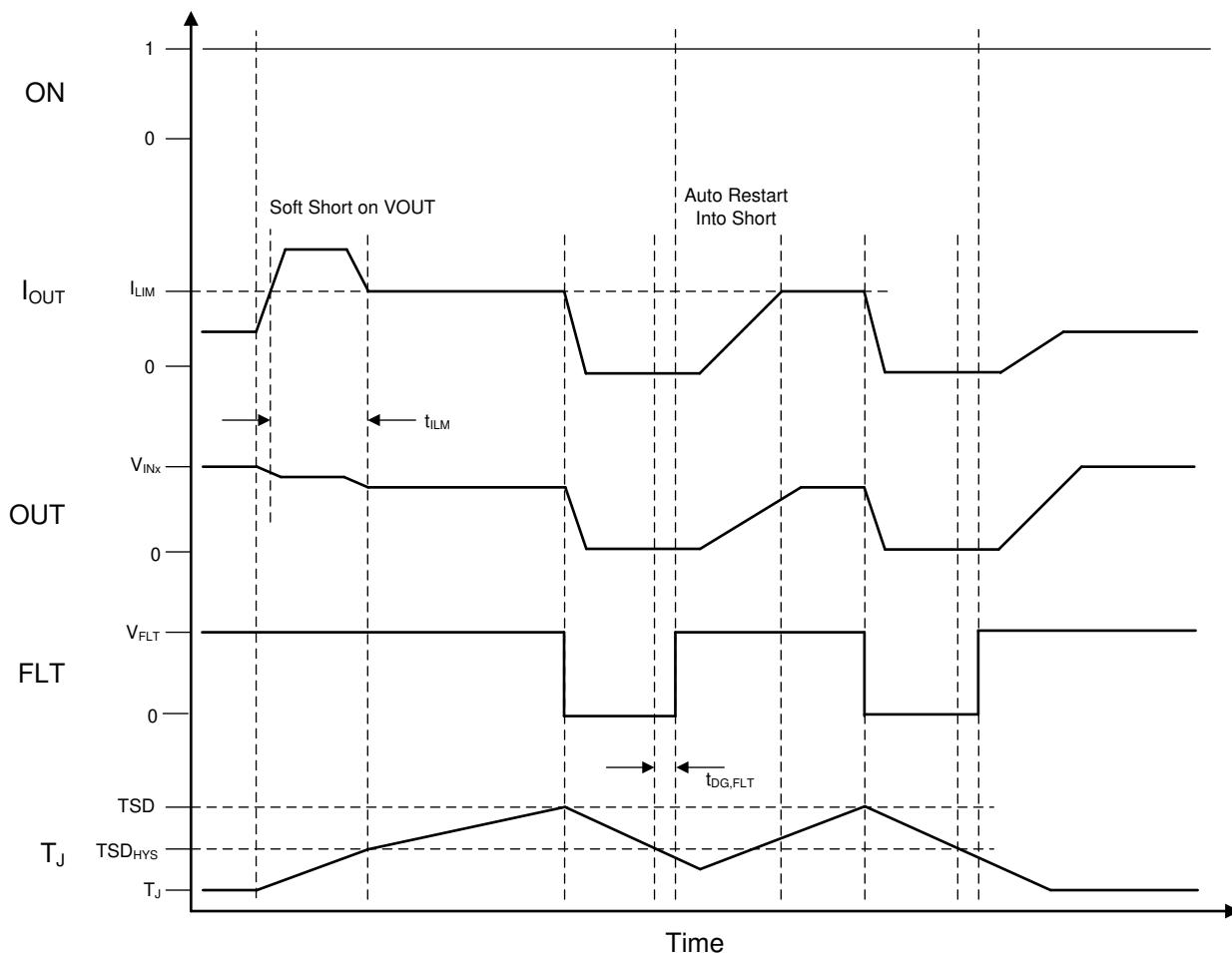
V _{ON}	Pull Down
$\leq V_{IL}$	Connected
$\geq V_{IH}$	Disconnected

8.3.2 Fault Indication (FLT)

The FLT pin is an open drain output that acts as a status indication for the device. It is pulled low during thermal shutdown or reverse-current events. The behavior of the FLT pin is shown in [Figure 6](#).

8.3.3 Current Limiting (V_{sc})

The TPS22948 responds to overcurrent conditions by limiting its output current to the ILIM level shown in [Figure 6](#).

**Figure 6. TPS22948 Current Limiting Behavior**

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present on the output and the ON pin is toggled high, turning the device on. The output voltage is held near zero potential with respect to ground and the TPS22948 ramps the output current to I_{LIM} . The TPS22948 device will limit the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and the device turns itself off. The device remains off until the junction temperature has lowered by TSD_{HYS} , and the device will turn itself back on. This will cycle until the overload condition is removed.

The second condition is when a short circuit, partial short circuit, or transient overload occurs after the device has been fully powered on. The device responds to the overcurrent condition within time t_{LIM} (see [Figure 7](#)), and before this time, the current is able to exceed I_{LIM} . In the case of a fast transient, the current-sense amplifier is overdriven and momentarily disables the internal power FET. The current-sense amplifier recovers and limits the output current to I_{LIM} . Similar to the previous case, the TPS22948 limits the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and begins thermally cycling on and off.

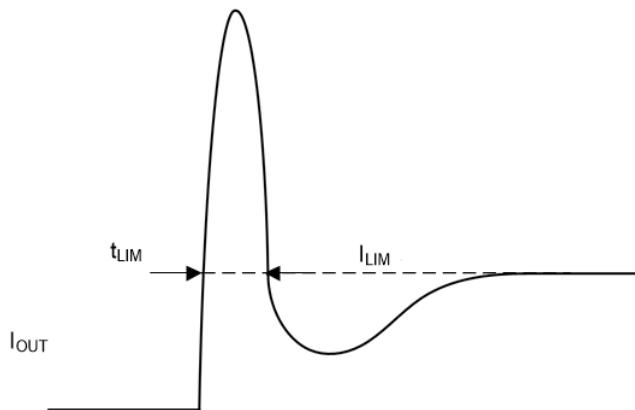


Figure 7. Transient Current Limit Waveform

8.3.4 Reverse Current Blocking (RCB)

In a scenario where the device is enabled and V_{OUT} is greater than V_{IN} , there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold is exceeded (about 200 mA), there is a delay time (t_{RCB}) before the switch turns off to stop the current flow. The switch will remain off and block reverse current as long as the reverse voltage condition exists. Once V_{OUT} has dropped below the release voltage threshold (V_{RCB}) the device will turn back on. When the ON pin is pulled low, the device will constantly block reverse current.

8.4 Device Functional Modes

[Table 2](#) describes the connection of the V_{OUT} pin depending on the state of the ON pin.

Table 2. V_{OUT} Connection

ON	TPS22919 V_{OUT}
L	Open
H	V_{IN}

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22948 device can be used to power downstream modules.

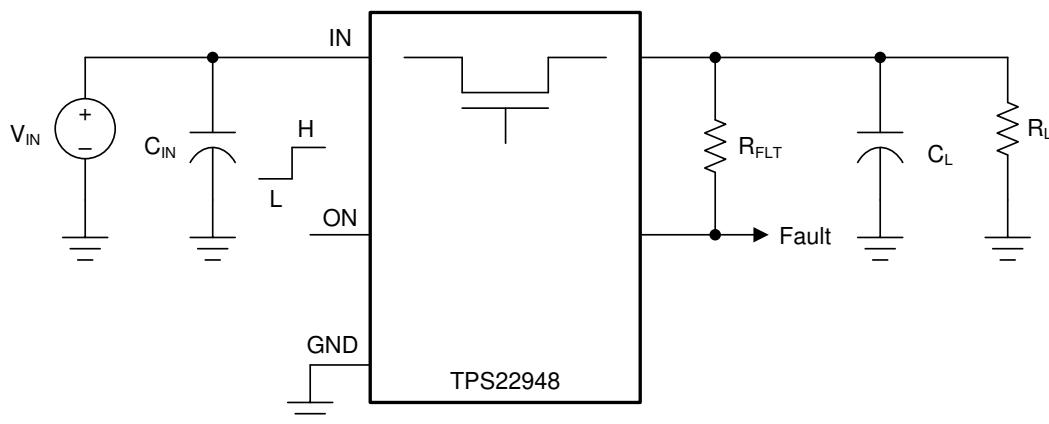


Figure 8. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in [Table 3](#) as the design parameters:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	5 V
Load Current / Resistance (R_L)	1 kΩ
Load Capacitance (C_L)	10 μF
Maximum Inrush Current (I_{INRUSH})	100 mA

Although the load capacitance is 10 μF, this is assumed to be at the end of a cable or closer to the load. An 18nF capacitance close to the output of the device is recommended for optimal performance during short circuit conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use [Equation 1](#) to find the maximum output capacitance for a given inrush current requirement.

$$C_L = I_{INRUSH} \times t_R \div (0.8 \times V_{IN})$$

where

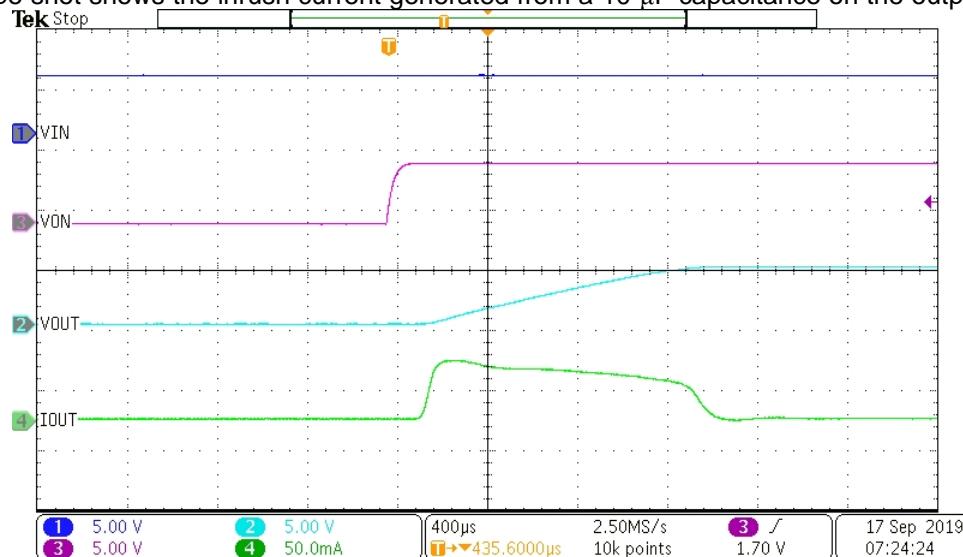
- C_L = capacitance on V_{OUT} (μF)
- I_{INRUSH} = maximum acceptable inrush current (A)
- t_R = rise time of the TPS22948 (μs)

- V_{IN} = input voltage (V) (1)

Based on [Equation 1](#), the maximum output capacitance that limits the inrush current to 100 mA is 12.5 μF . Therefore, the desired 10- μF load capacitance will not exceed the inrush current design requirement during turn on.

9.2.3 Application Curves

The below scope shot shows the inrush current generated from a 10- μF capacitance on the output.



A.

$V_{IN} = 5 \text{ V}$

$CL = 10 \mu\text{F}$

Figure 9. TPS22948 Inrush Current Control with Slow Rise Time

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 2.5 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (CIN) of 1 μ F is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input. A 18nF capacitance close to the output of the device is recommended for optimal performance during short circuit conditions.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

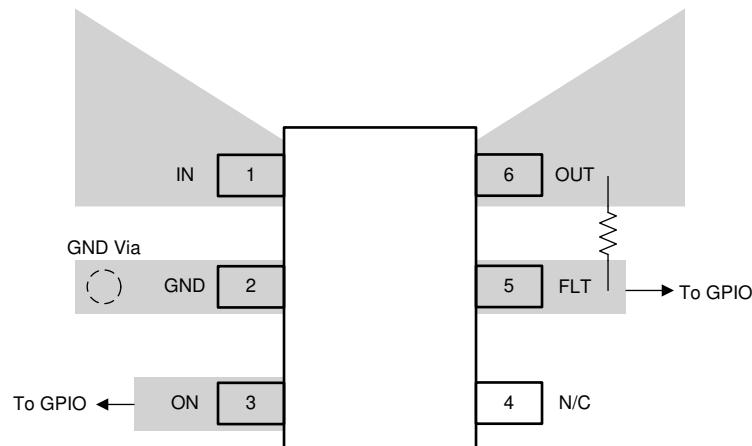


Figure 10. Recommended Board Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22948DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	1CT
TPS22948DCKR.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1CT

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

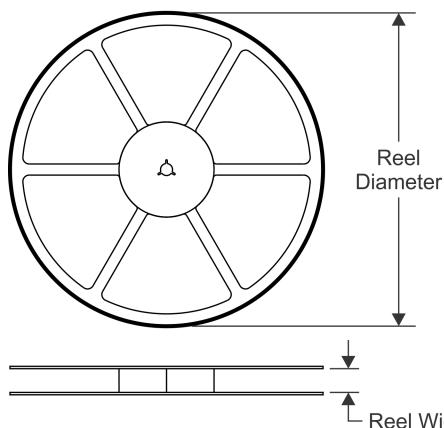
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

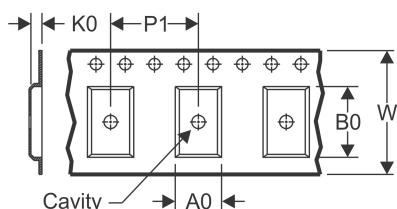
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

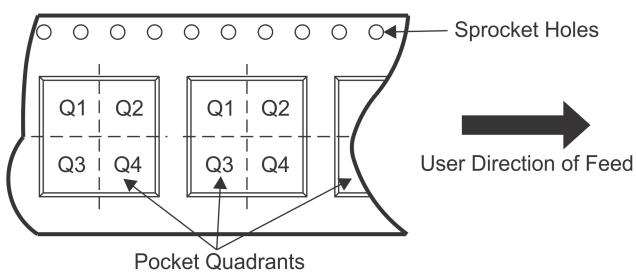


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

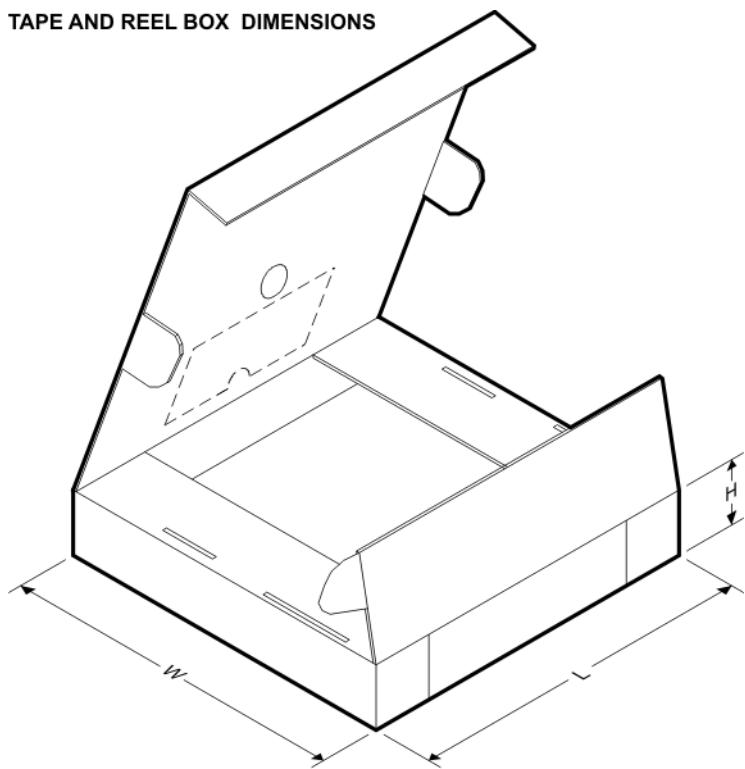
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22948DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

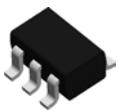


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22948DCKR	SC70	DCK	6	3000	180.0	180.0	18.0

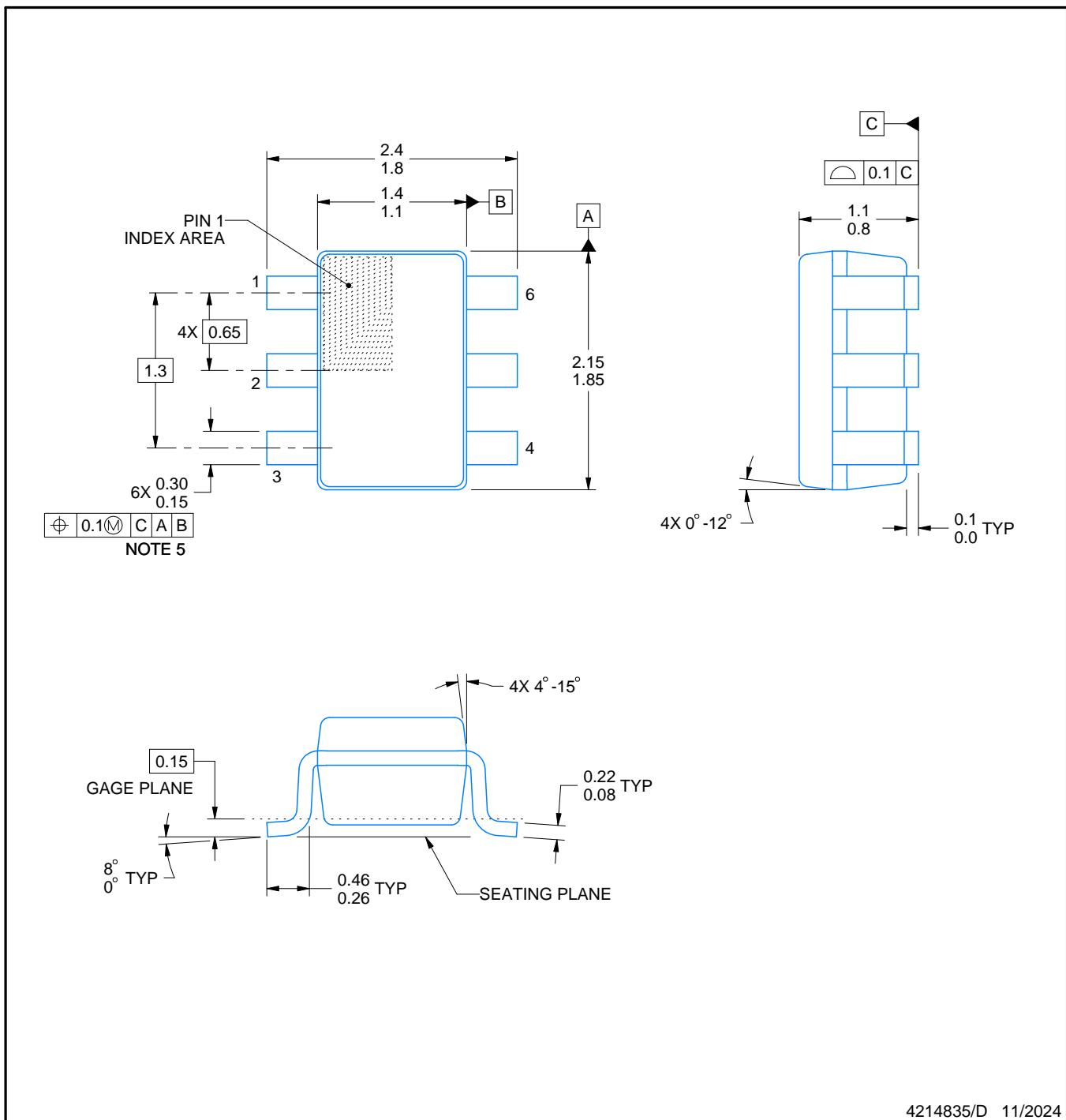
PACKAGE OUTLINE

DCK0006A



SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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NOTES:

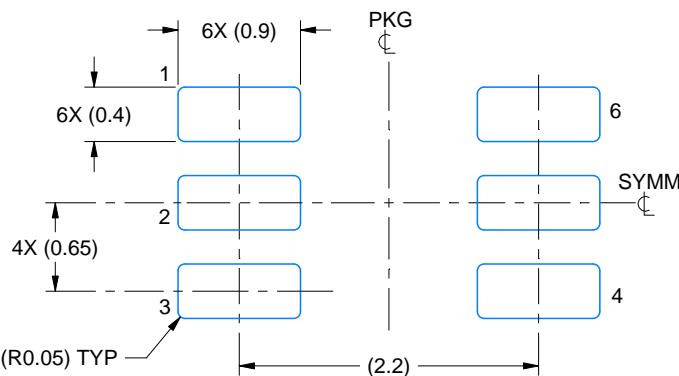
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.

EXAMPLE BOARD LAYOUT

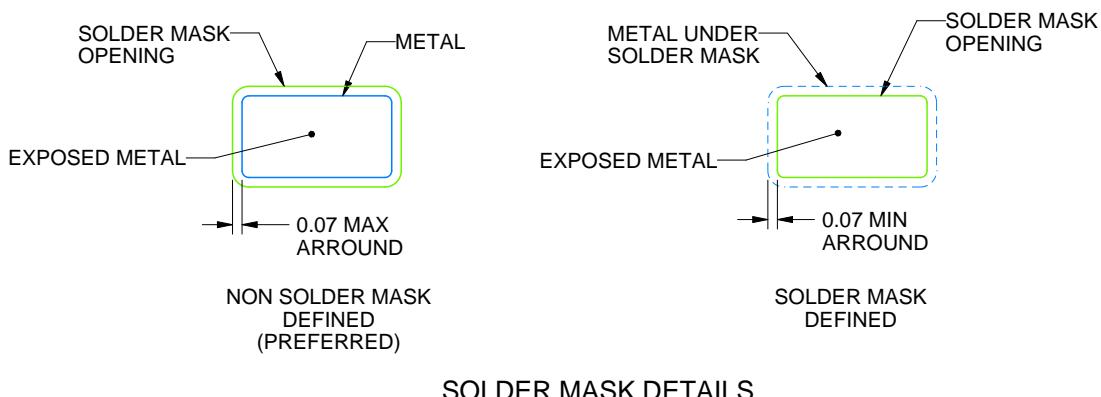
DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



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NOTES: (continued)

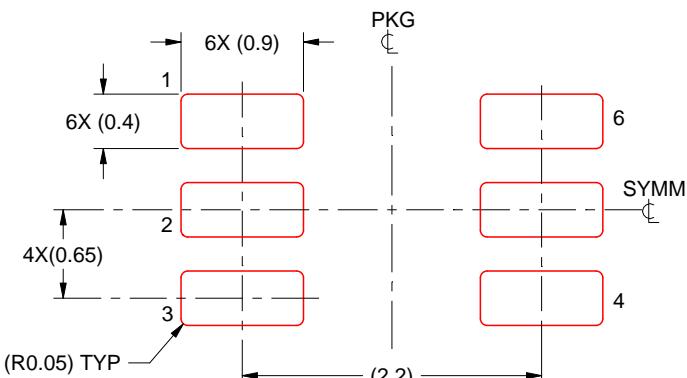
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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