

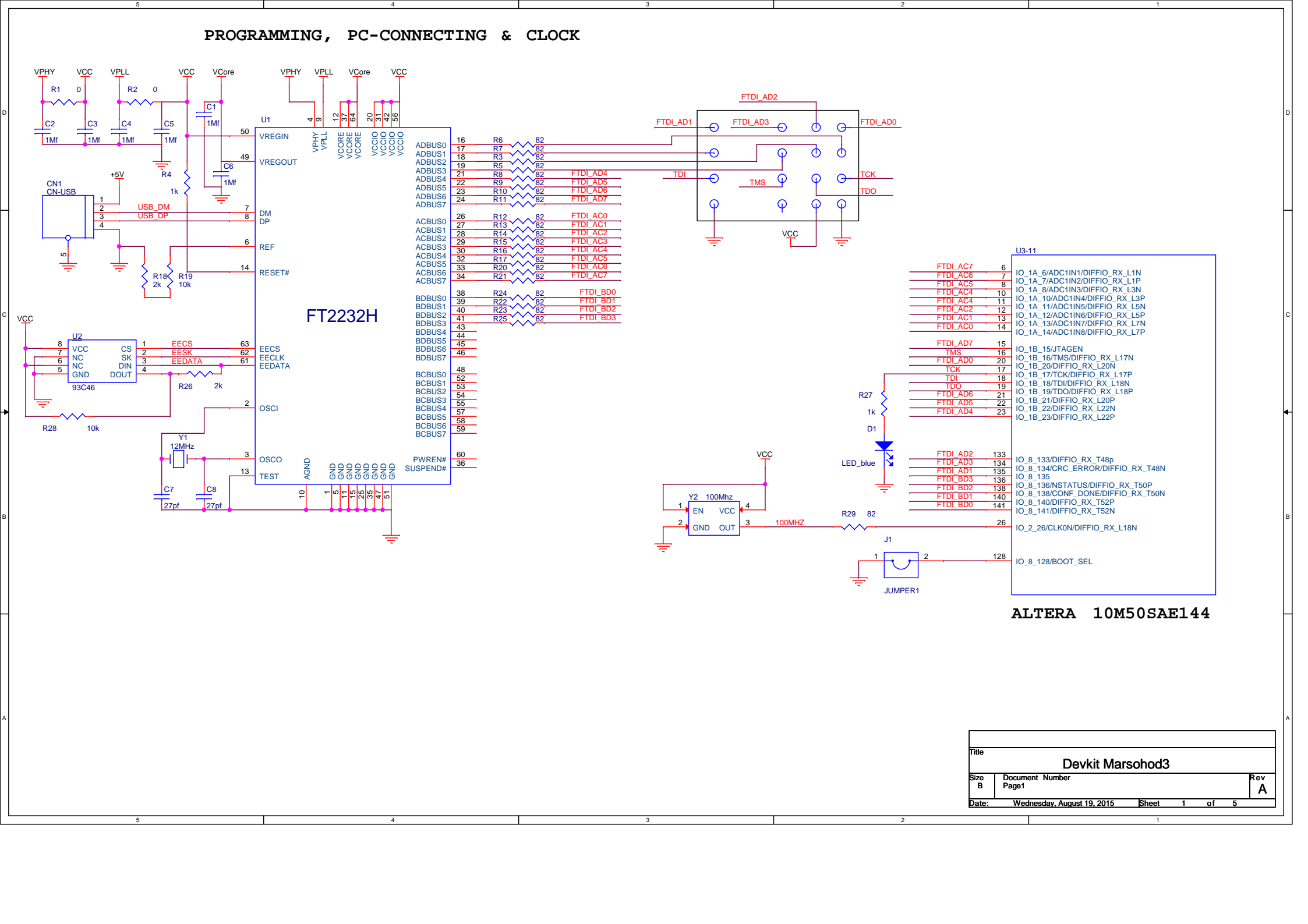
PROGRAMMING, PC-CONNECTING & CLOCK

The diagram shows the PCB layout for the FT232H module, divided into three main functional areas:

- POWER AND PROGRAMMING (Left):** Includes power supply decoupling for VPHY, VPLL, VCore, and VCC. It features a USB connector (CN1) with USB_DM and USB_DP signals, and a USB-to-UART bridge chip (U1, FT232H). The FT232H is connected to a microcontroller (U2, 93C46) via I2C (EECS, EESK, EEDATA). The microcontroller is also connected to a 12MHz oscillator (Y1) and a 100MHz oscillator (Y2).
- PC-CONNECTING (Middle):** Shows the FT232H's connection to a microcontroller (U3-11, ALTERA 10M50SAE144) via a 100MHz clock signal (Y2) and a 100MHz clock signal (Y2). The microcontroller is connected to the FT232H via a 100MHz clock signal (Y2) and a 100MHz clock signal (Y2).
- CLOCK (Right):** Shows the FT232H's connection to a microcontroller (U3-11, ALTERA 10M50SAE144) via a 100MHz clock signal (Y2) and a 100MHz clock signal (Y2).

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Pin	Signal	Pin	Signal
1	VCC	15	IO_1B_15/JTAGEN
2	GND	16	IO_1B_16/TMS/DIFFIO_RX_L17N
3	VCC	17	IO_1B_20/DIFFIO_RX_L20N
4	GND	18	IO_1B_17/TCK/DIFFIO_RX_L17P
5	VCC	19	IO_1B_18/TDI/DIFFIO_RX_L18N
6	GND	20	IO_1B_19/TDO/DIFFIO_RX_L18P
7	VCC	21	IO_1B_21/DIFFIO_RX_L20P
8	GND	22	IO_1B_22/DIFFIO_RX_L22N
9	VCC	23	IO_1B_23/DIFFIO_RX_L22P
10	GND	24	IO_1B_133/DIFFIO_RX_T48p
11	VCC	25	IO_8_134/CRC_ERROR/DIFFIO_RX_T48N
12	GND	26	IO_8_135
13	VCC	27	IO_8_136/NSTATUS/DIFFIO_RX_T50P
14	GND	28	IO_8_138/CONF_DONE/DIFFIO_RX_T50N
15	VCC	29	IO_8_140/DIFFIO_RX_T52P
16	GND	30	IO_8_141/DIFFIO_RX_T52N
17	VCC	31	IO_2_26/CLK0N/DIFFIO_RX_L18N
18	GND	32	IO_8_128/BOOT_SEL
19	VCC	33	
20	GND	34	
21	VCC	35	
22	GND	36	
23	VCC	37	
24	GND	38	
25	VCC	39	
26	GND	40	
27	VCC	41	
28	GND	42	
29	VCC	43	
30	GND	44	
31	VCC	45	
32	GND	46	
33	VCC	47	
34	GND	48	
35	VCC	49	
36	GND	50	
37	VCC	51	
38	GND	52	
39	VCC	53	
40	GND	54	
41	VCC	55	
42	GND	56	
43	VCC	57	
44	GND	58	
45	VCC	59	
46	GND	60	
47	VCC	61	
48	GND	62	
49	VCC	63	
50	GND	64	
51	VCC	65	
52	GND	66	
53	VCC	67	
54	GND	68	
55	VCC	69	
56	GND	70	
57	VCC	71	
58	GND	72	
59	VCC	73	
60	GND	74	
61	VCC	75	
62	GND	76	
63	VCC	77	
64	GND	78	
65	VCC	79	
66	GND	80	
67	VCC	81	
68	GND	82	
69	VCC	83	
70	GND	84	
71	VCC	85	
72	GND	86	
73	VCC	87	
74	GND	88	
75	VCC	89	
76	GND	90	
77	VCC	91	
78	GND	92	
79	VCC	93	
80	GND	94	
81	VCC	95	
82	GND	96	
83	VCC	97	
84	GND	98	
85	VCC	99	
86	GND	100	



PROGRAMMING, PC-CONNECTING & CLOCK

The schematic diagram illustrates the internal connections of the FT232H module. Key components and their connections include:

- Power Supply:** VPHY, VPLL, VCore, and VCC are connected to the appropriate pins of the FT232H chip (U1).
- USB Connector (CN1):** The USB connector is connected to the USB_DM and USB_DP pins of the FT232H chip.
- EEPROM (U2):** The 93C46 EEPROM is connected to the EECS, EESK, and EEDATA pins of the FT232H chip.
- Oscillator (Y2):** A 100MHz oscillator is connected to the OSCI and OSCO pins of the FT232H chip.
- FTDI Module (U3-11):** The FTDI module is connected to the FT232H chip via a series of pins (FTDI_AD0 to FTDI_AD7, FTDI_AC0 to FTDI_AC7, FTDI_BD0 to FTDI_BD3, FTDI_AD0 to FTDI_AD7, FTDI_AC0 to FTDI_AC7, FTDI_BD0 to FTDI_BD3). It also includes an LED (D1) and a jumper (J1).

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PROGRAMMING, PC-CONNECTING & CLOCK

The schematic diagram illustrates the internal connections of the FT232H module. Key components and their connections include:

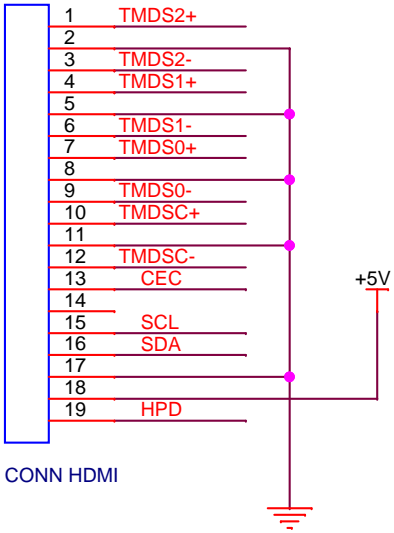
- Power Supply:** VPHY, VPLL, VCore, and VCC are connected to the appropriate pins of the FT232H chip (U1).
- USB Connector (CN1):** The USB connector is connected to the USB_DM and USB_DP pins of the FT232H chip.
- EEPROM (U2):** The 93C46 EEPROM is connected to the EECS, EESK, and EEDATA pins of the FT232H chip.
- Oscillator (Y2):** A 100MHz oscillator is connected to the OSCI and OSCO pins of the FT232H chip.
- FTDI Module (U3-11):** The FTDI module is connected to the FT232H chip via a series of pins (FTDI_AD0 to FTDI_AD7, FTDI_AC0 to FTDI_AC7, FTDI_BD0 to FTDI_BD3, FTDI_AD0 to FTDI_AD7, FTDI_AC0 to FTDI_AC7, FTDI_BD0 to FTDI_BD3). It also includes an LED (D1) and a jumper (J1).

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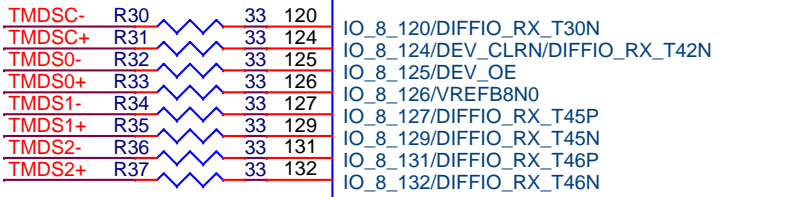
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HDMI & CONNECTORS

J2



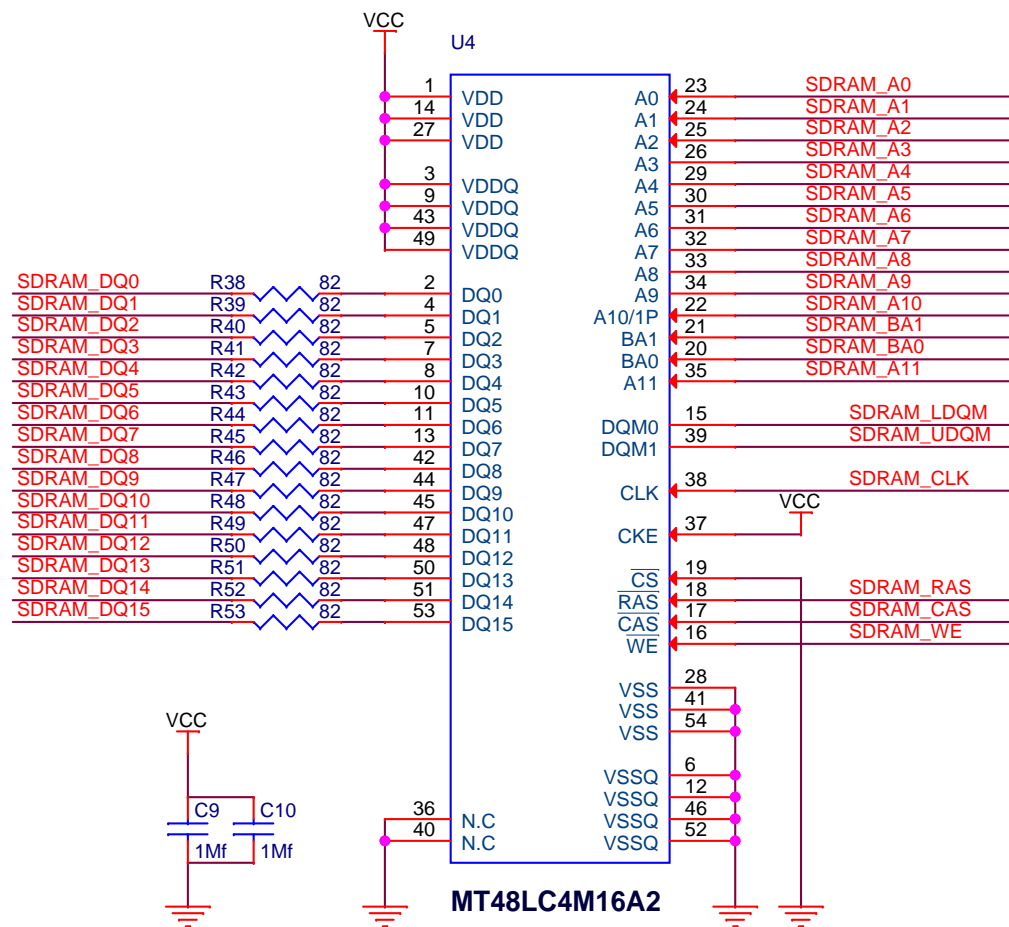
U3-9



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SDR SDRAM INTERFACE



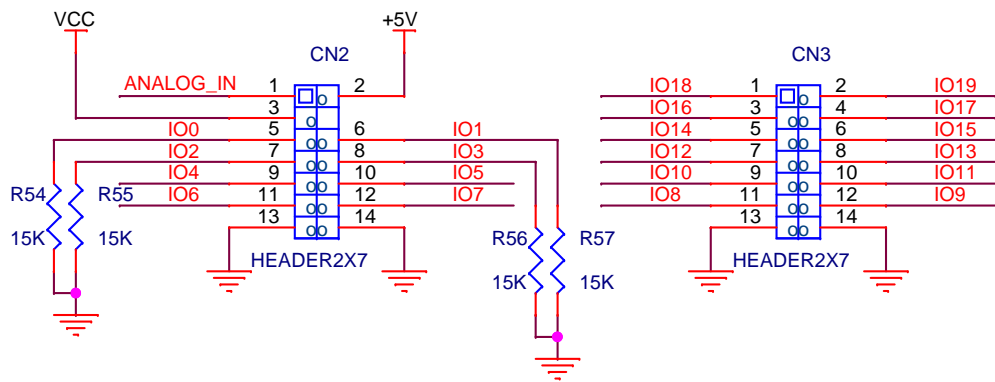
U3-4	
SDRAM_DQ15	27
SDRAM_DQ14	28
SDRAM_DQ13	29
SDRAM_DQ12	30
SDRAM_DQ11	32
SDRAM_DQ10	33
SDRAM_DQ9	38
SDRAM_DQ8	39
SDRAM_UDQM	40
SDRAM_CLK	41
SDRAM_A4	42
SDRAM_A5	43
SDRAM_A6	44
SDRAM_A7	46
SDRAM_A8	49
SDRAM_A9	50
SDRAM_A11	51
SDRAM_BA0	52
SDRAM_BA1	53
SDRAM_A10	55
SDRAM_A0	57
SDRAM_A1	58
SDRAM_A2	60
SDRAM_A3	61
SDRAM_RAS	62
SDRAM_CAS	63
SDRAM_WE	64
SDRAM_LDQM	65
SDRAM_DQ7	66
SDRAM_DQ6	69
SDRAM_DQ5	70
SDRAM_DQ4	74
SDRAM_DQ3	75
SDRAM_DQ2	76
SDRAM_DQ1	77
SDRAM_DQ0	80

IO_2_27/CLK1N/DIFFIO_RX_L36N
IO_2_28/CLK1P/DIFFIO_RX_L36P
IO_2_29/VREFB2N0
IO_2_30
IO_2_32/PLL_L_CLKOUTN/DIFFIO_RX_L59N
IO_2_33/PLL_L_CLKOUTP/DIFFIO_RX_L59P
IO_3_38/DIFFIO_TX_RX_B1N
IO_3_39/DIFFIO_TX_RX_B1P
IO_3_40/DIFFIO_TX_RX_B3N
IO_3_41/DIFFIO_TX_RX_B3P
IO_3_42/DIFFIO_TX_RX_B5N
IO_3_43/DIFFIO_TX_RX_B5P
IO_3_44/VREFB3N0
IO_3_46/DIFFIO_TX_RX_B15N
IO_3_49/DIFFIO_TX_RX_B15P
IO_3_50
IO_3_51/CLK6N/DIFFIO_TX_RX_B18N
IO_3_52/CLK6P/DIFFIO_TX_RX_B18P
IO_3_53/CLK7N/DIFFIO_TX_RX_B20N
IO_3_55/CLK7P/DIFFIO_TX_RX_B20P
IO_3_57/VREFB4N0
IO_4_58
IO_4_60/DIFFIO_TX_RX_B39N
IO_4_61/DIFFIO_TX_RX_B39P
IO_4_62
IO_4_63/DIFFIO_TX_RX_B45N
IO_4_64/DIFFIO_TX_RX_B45P
IO_4_65/DIFFIO_TX_RX_B49N
IO_4_66/DIFFIO_TX_RX_B49P
IO_4_69/DIFFIO_TX_RX_B57N
IO_4_70/DIFFIO_TX_RX_B57P
IO_5_74/DIFFIO_RX_R2P
IO_5_75/DIFFIO_RX_R2N
IO_5_76/DIFFIO_RX_R1P
IO_5_77/DIFFIO_RX_R1N
IO_5_80

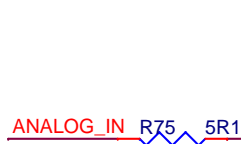
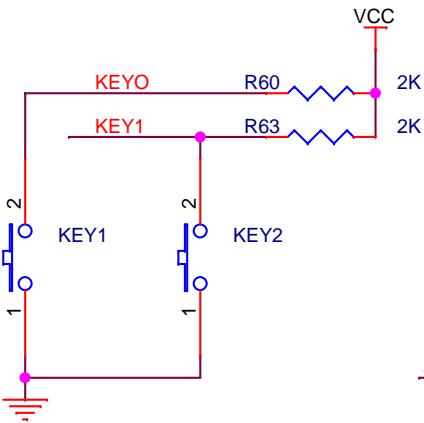
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SHIELD CONNECTOR, KEYS & LEDS

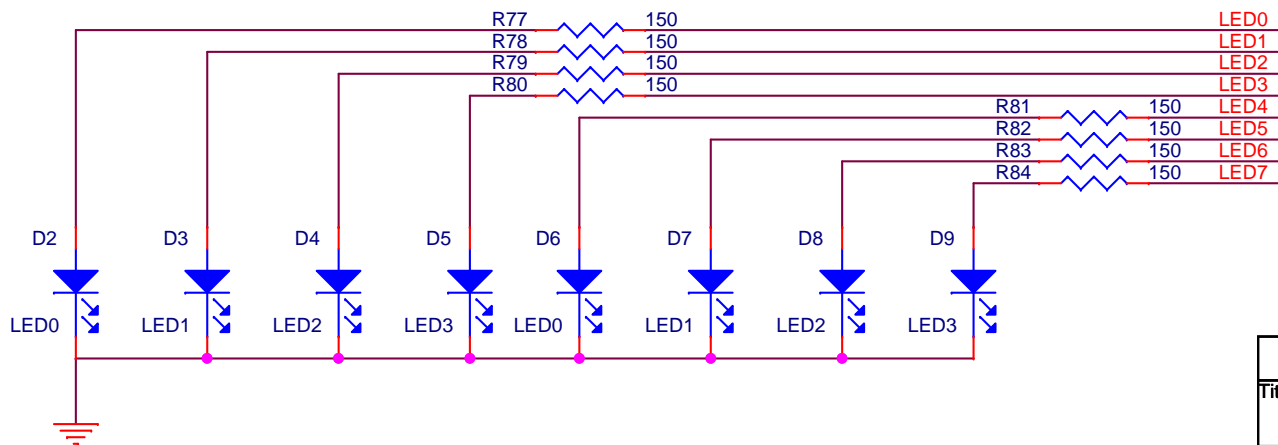


R58	82	IO0
R59	82	IO1
R61	82	IO2
R62	82	IO3
R64	82	IO4
R65	82	IO5
R66	82	IO6
R67	82	IO7
R68	82	IO8
R69	82	IO9
R70	82	IO10
R71	82	IO11
R72	82	IO12
R73	82	IO13
R74	82	IO14
R76	82	IO15



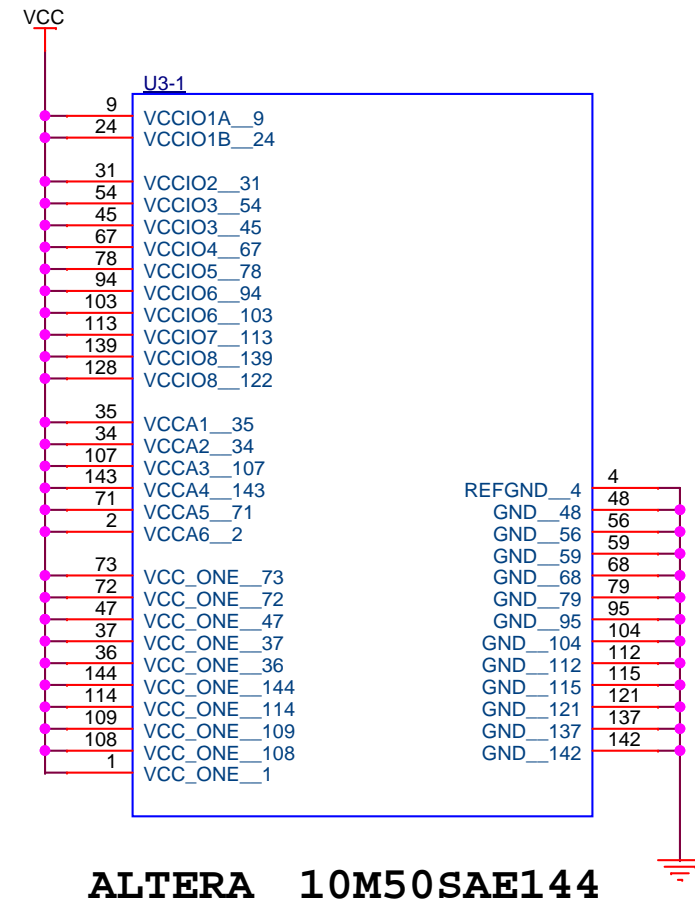
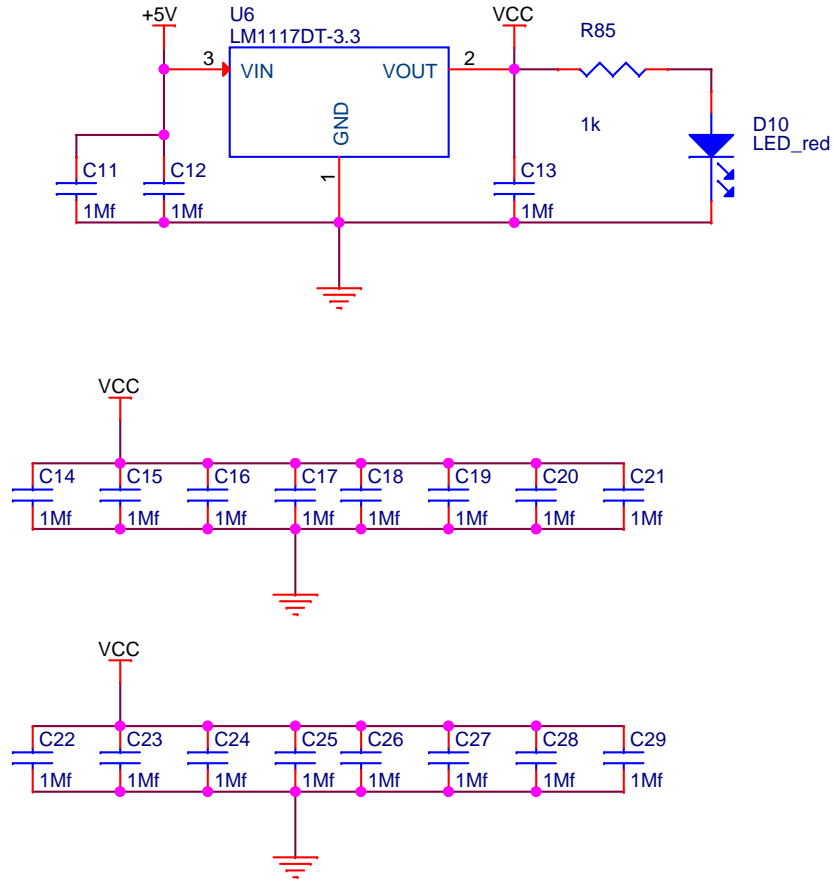
LED7	81	IO_5_81/VREFB5N0
LED6	82	IO_5_82/DIFFIO_RX_R29P
LED5	83	IO_5_83/DIFFIO_RX_R29N
LED4	84	IO_5_84/DIFFIO_RX_R33P
LED3	85	IO_5_85/DIFFIO_RX_R32P
LED2	86	IO_5_86/DIFFIO_RX_R33N
LED1	87	IO_5_87/DIFFIO_RX_R32N
LED0	88	IO_6_88/CLK2P/DIFFIO_RX_R38P
IO0	89	IO_6_89/CLK2N/DIFFIO_RX_R38N
IO1	90	IO_6_90/CLK3P/DIFFIO_RX_R40P
IO2	91	IO_6_91/CLK3N/DIFFIO_RX_R40N
IO3	92	IO_6_92/DIFFIO_RX_R42P
IO4	93	IO_6_93/DIFFIO_RX_R42N
IO5	96	IO_6_96/DPCLK3/DIFFIO_RX_R50P
IO6	97	IO_6_97/VREFB6N0
IO7	98	IO_6_98/DPCLK2/DIFFIO_RX_R50N
IO8	99	IO_6_99/DIFFIO_RX_R51P
IO9	100	IO_6_100/DIFFIO_RX_R52P
IO10	101	IO_6_101/DIFFIO_RX_R51N
IO11	102	IO_6_102/DIFFIO_RX_R52N
IO12	105	IO_6_105/DIFFIO_RX_R69P
IO13	106	IO_6_106/DIFFIO_RX_R69N
IO14	110	IO_7_110/DIFFIO_RX_T1P
IO15	111	IO_7_111/DIFFIO_RX_T1N
IO16	116	IO_7_116/VREFB7N0
IO17	117	IO_7_117/DIFFIO_RX_T20P
RESERVED	133	IO_7_133/DIFFIO_RX_T48P
IO19	119	IO_7_119/DIFFIO_RX_T30P
IO18	118	IO_7_118/DIFFIO_RX_T20N
KEY0	130	INPUT_ONLY_8_130/NCONFIG
KEY1	25	IO_2_25/CLK0N/DIFFIO_RX_L28N
ADC_VREF__5	5	
ANAIN1__3	3	

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MAX10 POWERING



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