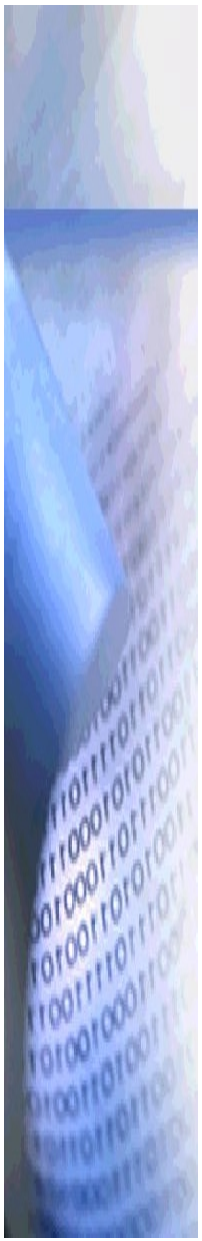


School of Electronic and Communications Engineering

Log and AntiLog Amplifiers

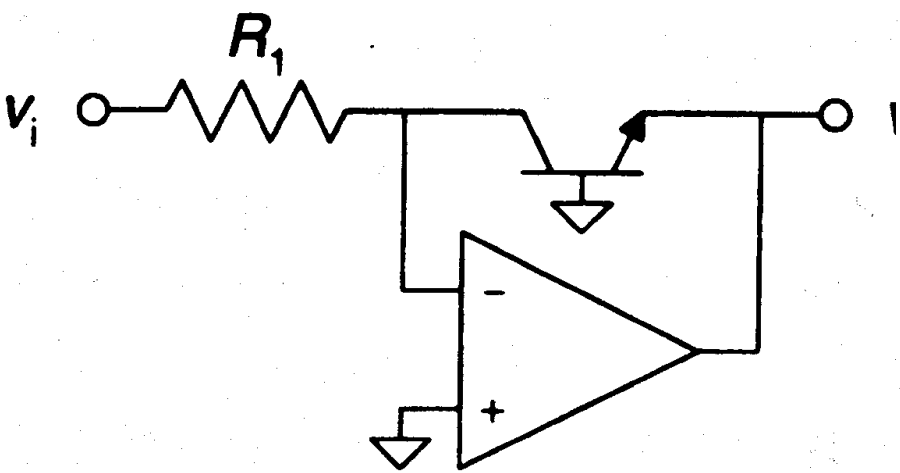
Recommended Text: Pallas-Areny, R. & Webster, J.G., Analog Signal Processing, Wiley (1999) pp. 293-321

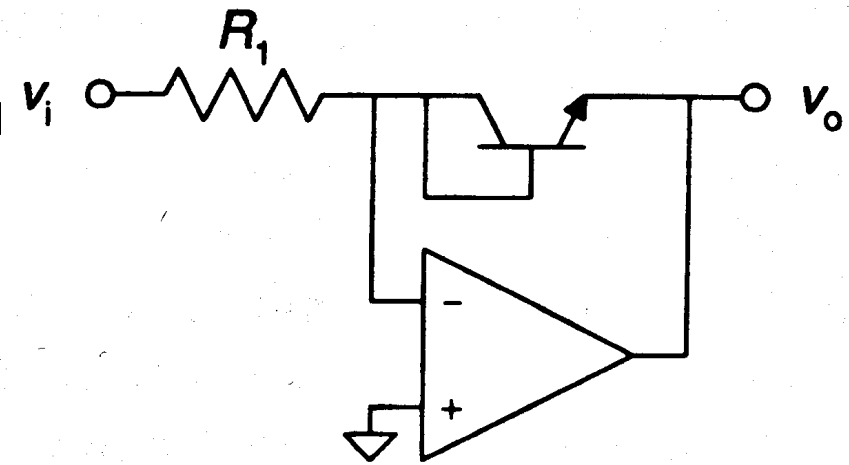
Introduction

- Log and Antilog Amplifiers are non-linear circuits in which the output voltage is proportional to the logarithm (or exponent) of the input.
- It is well known that some processes such as multiplication and division, can be performed by addition and subtraction of logs.
- They have numerous applications in electronics, such as:
  - Multiplication and division, powers and roots
  - Compression and Decompression
  - True RMS detection
  - Process control

Two basic circuits

- There are two basic circuits for logarithmic amplifiers
  - (a) transdiode and
  - (b) diode connected transistor
- Most logarithmic amplifiers are based on the inherent logarithmic relationship between the collector current, ***Ic***, and the base-emitter voltage, v_{be}, in silicon bipolar transistors.





Transdiode Log Amplifier

The input voltage is converted by *R1* into a current, which then flows through the transistor's collector modulating the base-emitter voltage according to the input voltage.

- The opamp forces the collector voltage to that at the noninverting input, 0 V
- From Ebers-Moll model the collector current is

$$I_c = I_s(e^{qVbe/kT} - 1) = I_s(e^{Vbe/V_T} - 1) \approx I_s \cdot e^{Vbe/V_T}$$

- where $\boldsymbol{I_s}$ is saturation current, $\boldsymbol{q}$ is the charge of the electron $1.6\text{x}10^{-9}$ Coulombs, $\boldsymbol{k}$ is the Boltsman's constant $1.38\text{x}10^{-23}$ Joules, $\boldsymbol{T}$ is absolute temperature, $\boldsymbol{V_T}$ is thermal voltage.
- For room temperature 300°K

$$I_c = I_s(e^{38.6Vbe} - 1) \approx I_s \cdot e^{38.6Vbe}$$

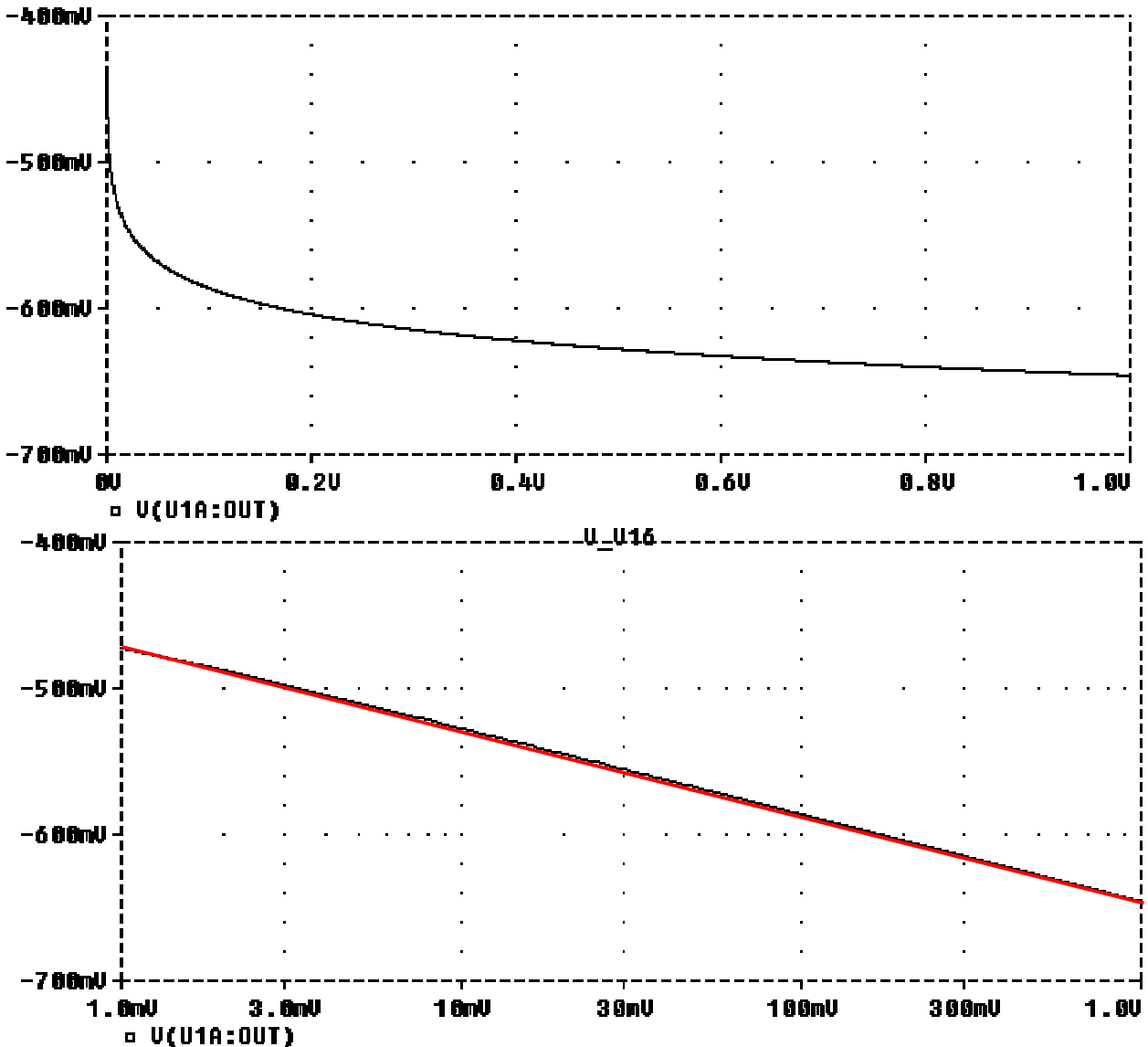
- The output voltage is therefore

$$Vout = -Vbe = -V_T \ln\left(\frac{i_C}{I_S}\right) = -\frac{V_T}{2.3}\lg\left(\frac{v_i}{R_1 I_S}\right) = \left(-0.0259 \cdot \ln\frac{Vin}{Ri \cdot Is}\right)$$

Thermal and Frequency stability

- This equation yields the desired logarithmic relationship over a wide range of currents, but is temperature-sensitive because of V_T and I_S resulting in scale-factor and offset temperature-dependent errors.
- The system bandwidth is narrower for small signals because emitter resistance increases for small currents.
- The source impedance of voltage signals applied to the circuit must be small compared to R1. Omitting R1 yields a current-input log amp.
- Using a *p-n-p* transistor changes the polarity of input signals acceptable but limits the logarithmic range because of the degraded performance *of p-n-p* transistors compared to *n-p-n* transistors

Transfer Function



IC Log Amps.

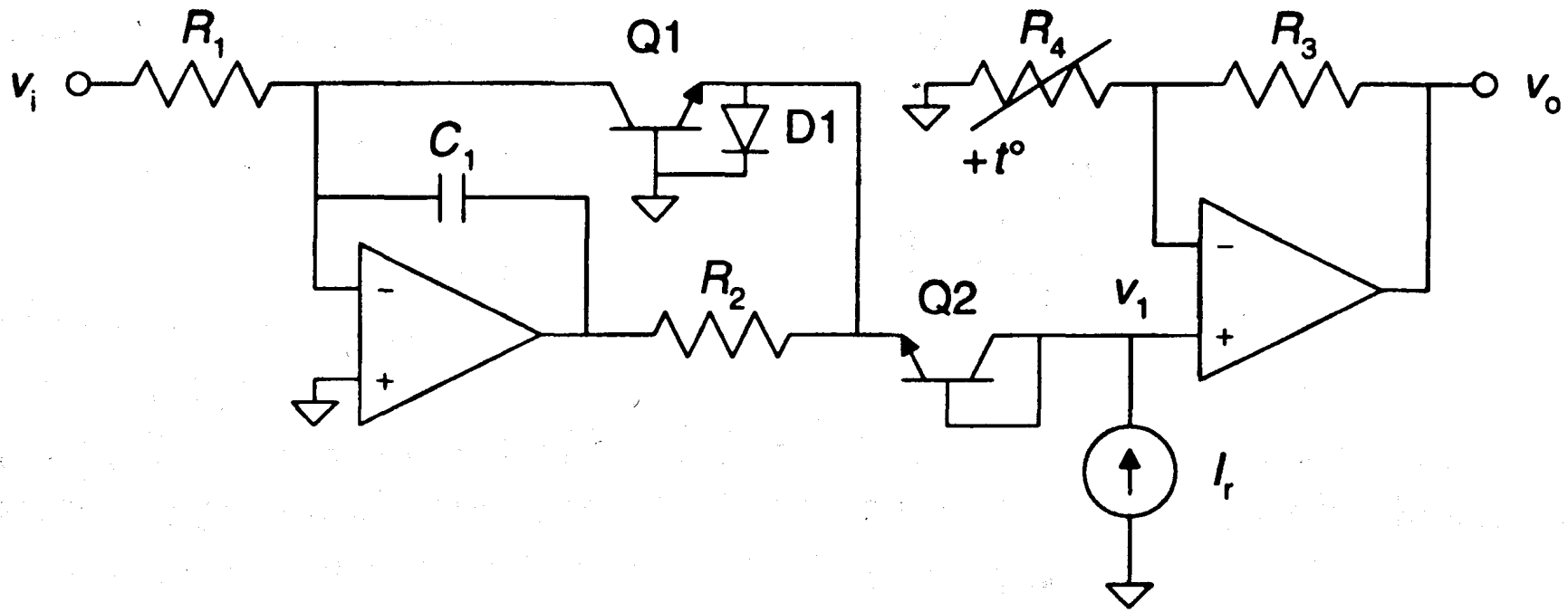
- These basic circuits needs additional components to improove the overall performance, i.e:
  - to provide base-emitter junction protection,
  - to reduce temperature effects,
  - bulk resistance error and op amp offset errors,
  - to accept bipolar input voltages or currents,
  - and to ensure frequency stability.
- Such circuit techniques are used in integrated log amps: AD640, AD641, ICL8048, LOG100, 4127.
- IC log amps may cost about ten times the components needed to build a discrete-component log amp.
- Nevertheless, achieving a 1% logarithmic conformity over almost six decades for input currents requires careful design.

Temperature Compensation

$$v_o = -V_T \ln\left(\frac{v_i}{R_1 I_S}\right)$$

- The equation for output voltage shows that the scale factor of the basic transdiode log amp depends on temperature because of V_T and
- that there is also a temperature-dependent offset because of I_S.
- Temperature compensation must correct both error sources.
- Figure (next slide) shows the use of a second, matched, transistor for offset compensation and a temperature-dependent gain for gain compensation.

Temperature Compensation



- Temperature compensation in a transdiode log amp:
- a second transistor (Q2) compensates the offset voltage and
- a temperature-sensitive resistor *(R4)* compensates the scale factor

Temperature Compensation

- For transistors Q1 & Q2 we have

$$v_{BE1} = V_T \ln\left(\frac{v_i}{R_1 I_{S1}}\right) \qquad v_{BE2} = V_T \ln\left(\frac{I_r}{I_{S2}}\right)$$

- where ***Ir*** is a reference, temperature-independent, current.
- The output voltage will be

$$v_o = v_1\left(1+\frac{R_3}{R_4}\right) = \left(v_{BE2} - v_{BE1}\right)\left(1+\frac{R_3}{R_4}\right) = V_T\left(1+\frac{R_3}{R_4}\right)\ln\left(\frac{R_1 I_r}{v_i}\frac{I_{S2}}{I_{S1}}\right)$$

- Matched transistors (***I_{S1}*** = ***I_{S2}***) will cancel offset.
- In order to compensate the gain dependence on temperature, R4 must be much smaller than *R3* and such that $d(V_T/R4)/dT = 0$.
- This requires $dR4/R4 == dV_T/V_T$ (= l/T).
- At T = 298 K, the temperature coefficient of *R4* must be 3390 x 10^{-6}K.
- ***D1*** protects the base-emitter junction from excessive reverse voltages.

Stability Considerations

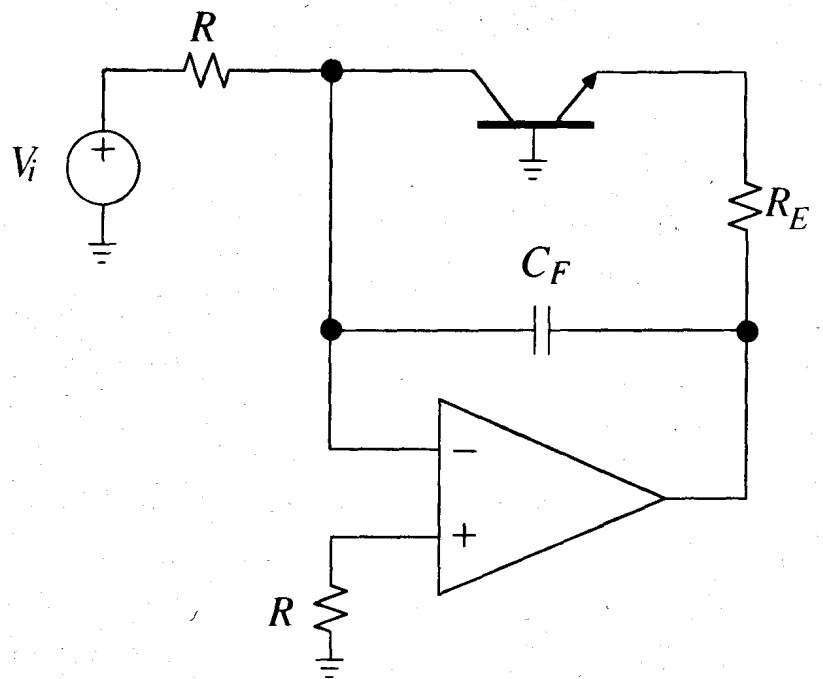
- Transdiode circuits have a notorious tendency to oscillate due to the presence of an active element in the feedback that can provide gain rather than loss.
- Consider the voltage-input transdiode. Ignoring op amp input errors, we have
- $V_n = V_i - R \cdot I_c$ and $V_o = -V_{BE}$
- The feedback factor β for a given value of V_i, is determined as

$$\beta = dV_n / dV_o = R \cdot dI_c / dV_{BE}$$

- Differentiating and using the fact that $Ic = V_i/R$, we obtain
- $$\beta = R \cdot I_c / V_T = V_i / V_T$$
- indicating that *b* can be greater than unity.
- For instance, with $\boldsymbol{V_i}$ = 10 V we have β = 10/0.026 = 400 = 52 dB, indicating that in the Bode diagram the |*1/b*| curve lies 52 dB below the 0 dB axis.
- Thus, the |*1/b*| curve intersects the \a\ curve at *fc* >> *ft*, where the phase shift due to higher-order poles is likely to render the circuit unstable; an additional source of instability is the input stray capacitance C_n

Range Considerations

- The transdiode circuit is compensated by means of an emitter resistor R_E to decrease the value of β and a feedback capacitor $\boldsymbol{C_p}$ to combat $\boldsymbol{C_n}$, as shown.
- To investigate its stability, refer to the incremental model, where the BJT has been replaced by its common-base small-signal model.



Range Considerations

- Transistor parameters r_e and r_o depend on the operating current *Ic*,

$$r_e = \alpha V_T / I_C \approx V_T / I_C \qquad r_o = V_A / I_C$$

- where V_A is called the *Early voltage* (typically ~ 100 V). C_μ is the base-collector junction capacitance. Both C_μ and *Cn* are typically ~10 pF range.

$$R1 = R \,\|\, r_o \,\|\, (r_d + R) \text{ and } R2 = r_e + R_E$$

- KCL at the summing junction yields

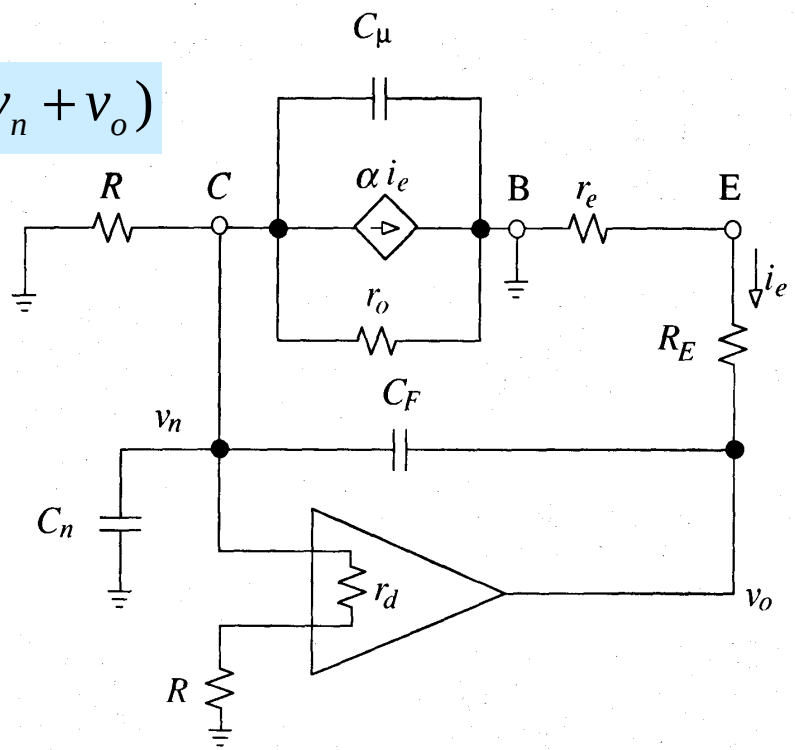
$$v_n\left(1/R1 + j\omega(C_n + C_\mu)\right) + \alpha \cdot i_e + j\omega C_F (v_n + v_o)$$

- Eliminating i_e and rearranging yields

$$v_n \frac{1 + j\omega R1C1}{R1} = v_o \frac{1 + j\omega R2C_F}{R2}$$

- where $\boldsymbol{i_e = -v_o/R2}$ and $\boldsymbol{C1 = C_n + C_\mu + C_F}$

$$\frac{1}{\beta} = \frac{v_o}{v_n}\frac{R2}{R1}\frac{1 + j\omega R2C_F}{1 + j\omega R1C1}$$



Range Considerations

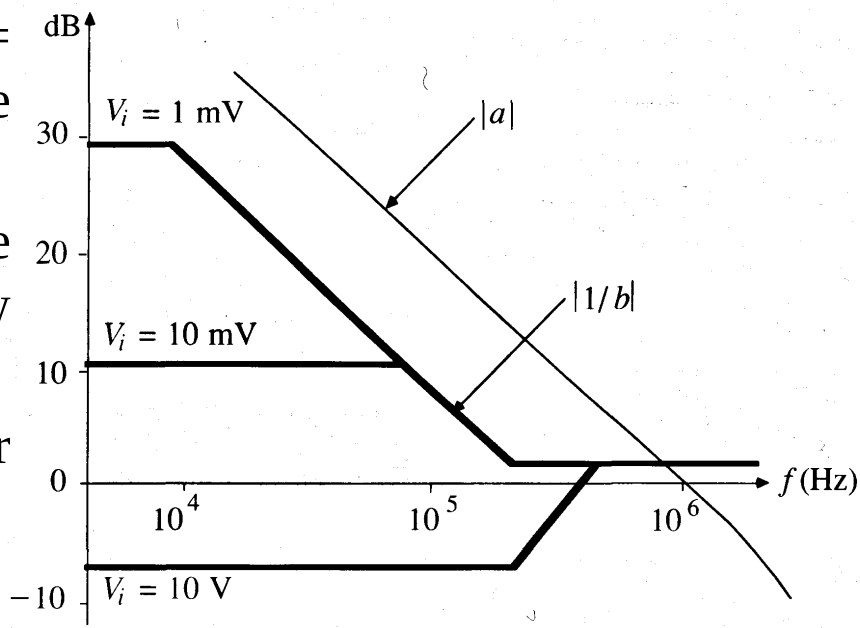
$$\frac{1}{\beta} = \frac{v_o}{v_n} = \frac{R2}{R1} \cdot \frac{1 + j(f / f_z)}{1 + j(f / f_p)} \quad \text{where} \quad f_z = \frac{1}{2\pi R1 C1} \quad \text{and} \quad f_z = \frac{1}{2\pi R1 C_F}$$

- The | *1/b*| curve has a low-frequency asymptote at *R2/R1*, a high-frequency asymptote at *C1/*C_F, and two breakpoints at *f=fz* and *f= fp*.
- While *C1/*C_F and *fz* are constant, *R2/R1* and *fp* depend on the operating current I_C. As such, they can vary over a wide range of values.

The hardest condition is when *Ic* = *Ic*(max), since this minimizes the value of *R2/R1* while maximizing that of *fp*,.

As a rule of thumb, R_E is chosen to make R2(min)/*R1* ~ 0.5 for a reasonably low value of |β|max,

C_F is chosen to make *fp(max)* ~ 0.5 *fc* for reasonable phase margin.

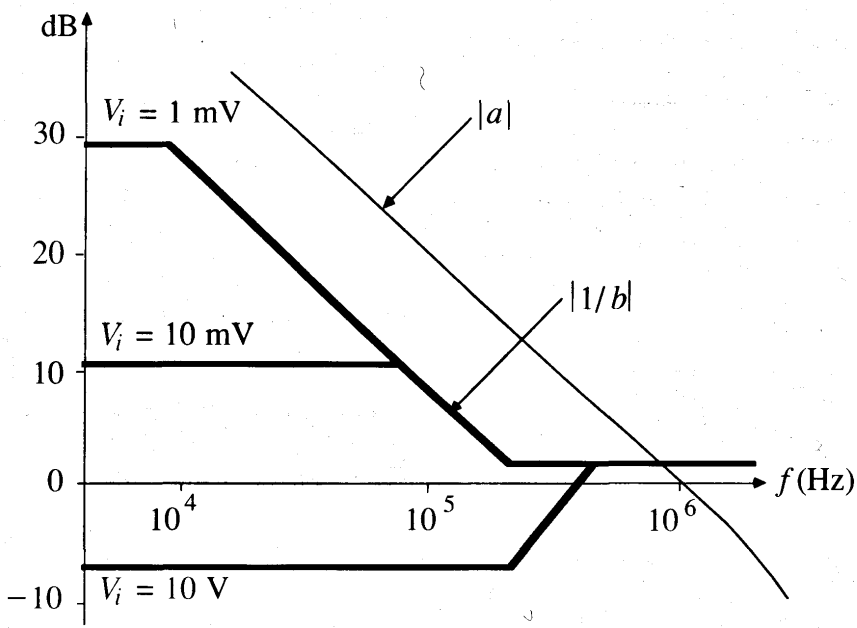


Frequency stability

- As the input level is decreased, we witness an increasing dominance of *fp* , which slows down the dynamics of the circuit.
- Since at sufficiently low current levels $r_e >> R_E$, we have $fp = 1/(2\pi r_e C_F)$
- The corresponding time constant is $\tau = r_e C_F = (V_T/I_C)C_F = (V_T/V_i)RC_F$ indicating that τ is inversely proportional to the input level, as expected.
- For instance, with *Ic* = 1 nA and *Cp* = 100 pF, we have $\tau = (26 \times 10^{-3}/10^{-9}) \times 100 \times 10^{-12} = 2.6$ ms.

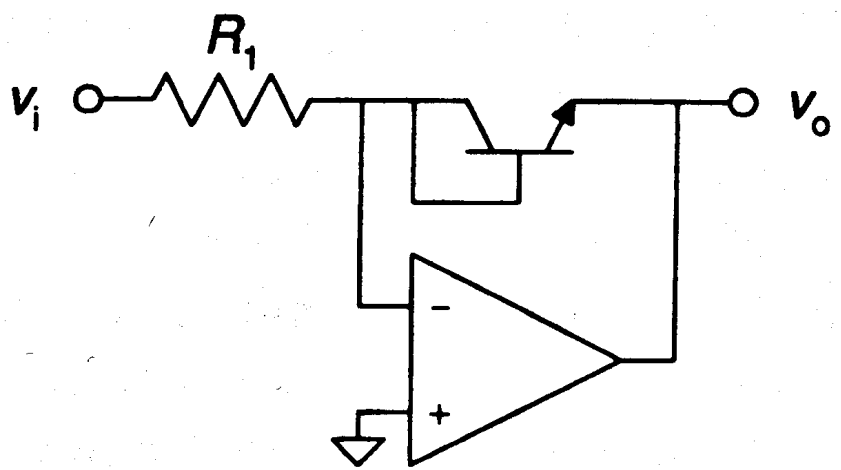
It takes 4.6 τ for an exponential transition to come within 1 percent of its final value, therefore our circuit will take about 12 ms to stabilize to within 1 percent.

his limitation must be kept in mind when operating near the low end of the dynamic range.



Diode-connected Log Amp

- In the second circuit a BJT connected as a diode to achieve the logarithmic characteristic.
- The analysis is the same as above for the transdiode connection, but the logarithmic range is limited to four or five decades because the base current adds to the collector current.
- On the pro side,
  - the circuit polarity can be easily changed by reversing the transistor,
  - the stability improves, and
  - the response is faster.

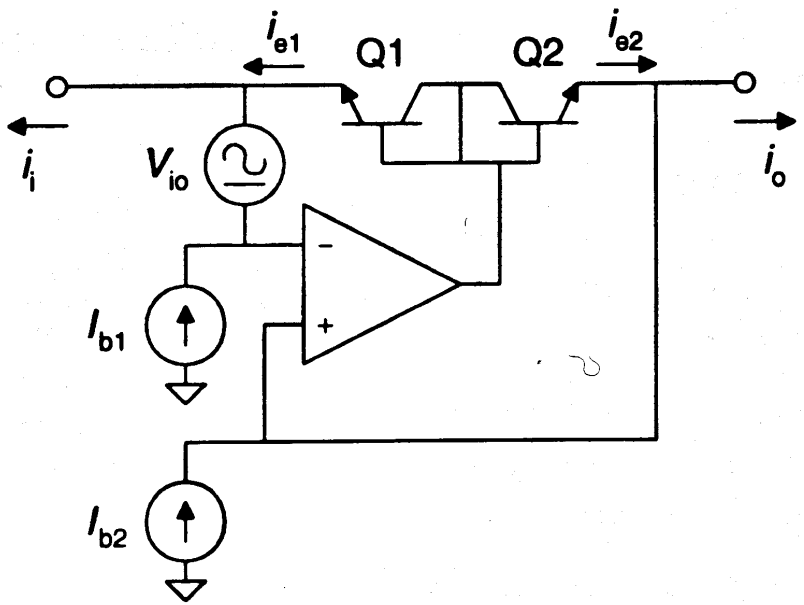


Input Current Inversion

- The basic log amp in only accepts positive input voltages or currents.
- Negative voltages or currents can be first rectified and then applied to the log amp, but this adds the errors from the rectifier.
- Alternatively, the log amp can be preceded by a precision current inverter.
- The current inverter in Figure below uses two matched *n-p-n* transistors and a precision op amp to achieve accurate current inversion.
- The collector-base voltage in both Ql and Q2 is 0 V, so that the Ebers-Moll model for BJT transistors leads to

$$\left.\begin{aligned} i_{e1} &= I_{ES1}(e^{v_{BE1}/V_T} - 1) \\ i_{e2} &= I_{ES2}(e^{v_{BE2}/V_T} - 1) \end{aligned}\right\}$$

where I_{ES1} and I_{ES2} are the respective emitter saturation currents of ***Ql*** and ***Q2.***



Input Current Inversion

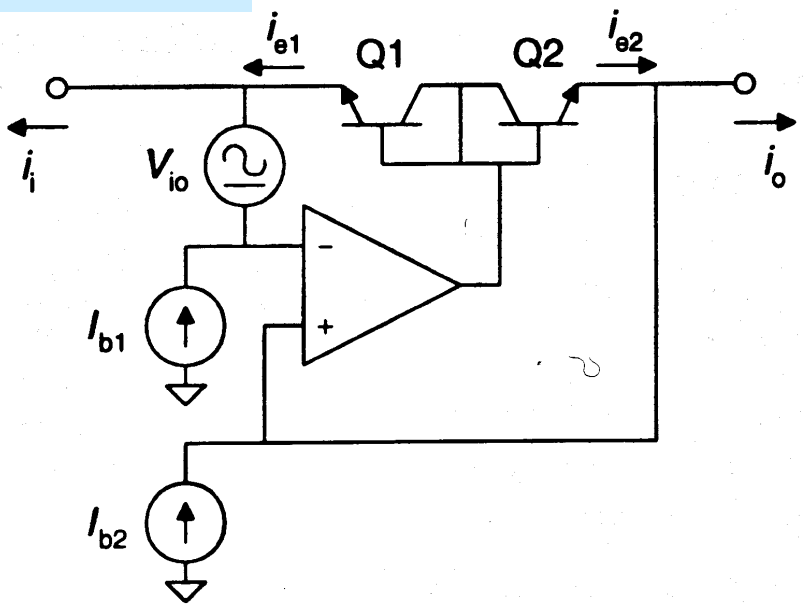
- From circuit inspection, assuming an op amp with infinite open-loop gain but finite input currents and offset voltage,

$$\left.\begin{aligned} i_{e1} &= i_i + I_{b1} \\ i_{e2} &= i_o + I_{b2} \\ v_{BE2} &= v_{BE1} + V_{io} \end{aligned}\right\}$$

Solving for the output current in terms of the input current yields

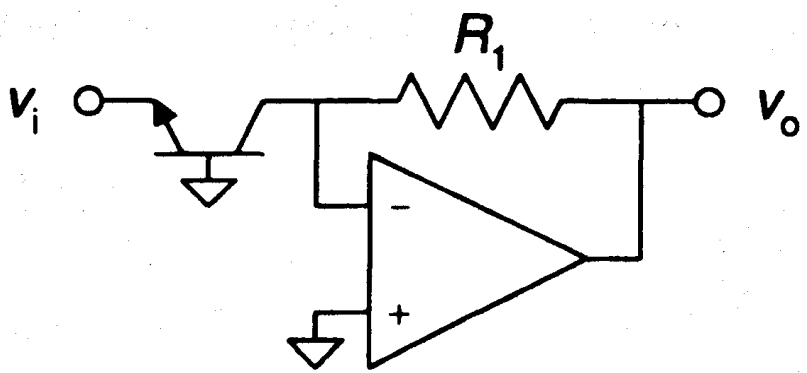
$$i_o = i_i \frac{I_{ES2}}{I_{ES1}} e^{V_{io}/V_T} + I_{ES2}\left(1 + \frac{I_{b1}}{I_{ES1}}\right) e^{V_{io}/V_T} - I_{ES2} - I_{b2}$$

- which shows that, in order to have small gain and offset errors, the offset voltage must be small compared to V_T,
- the op amp offset current must be small compared to the input current,
- and Ql and Q2 must be matched.

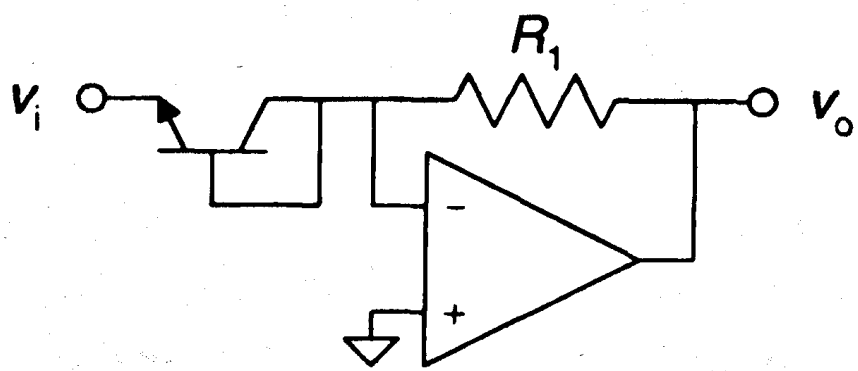


Exponential (Antilog) Amplifiers

- An exponential or antilogarithmic amplifier (antilog amp), performs the function inverse to that of log amps:
- its output voltage is proportional to a base (10, *e)* elevated to the ratio between two voltages.
- Antilog amps are used together with log amps to perform analog computation.
- Similar to Log Apms there are two basic circuits for logarithmic amplifiers
  - (a) transdiode and
  - (b) diode connected transistor



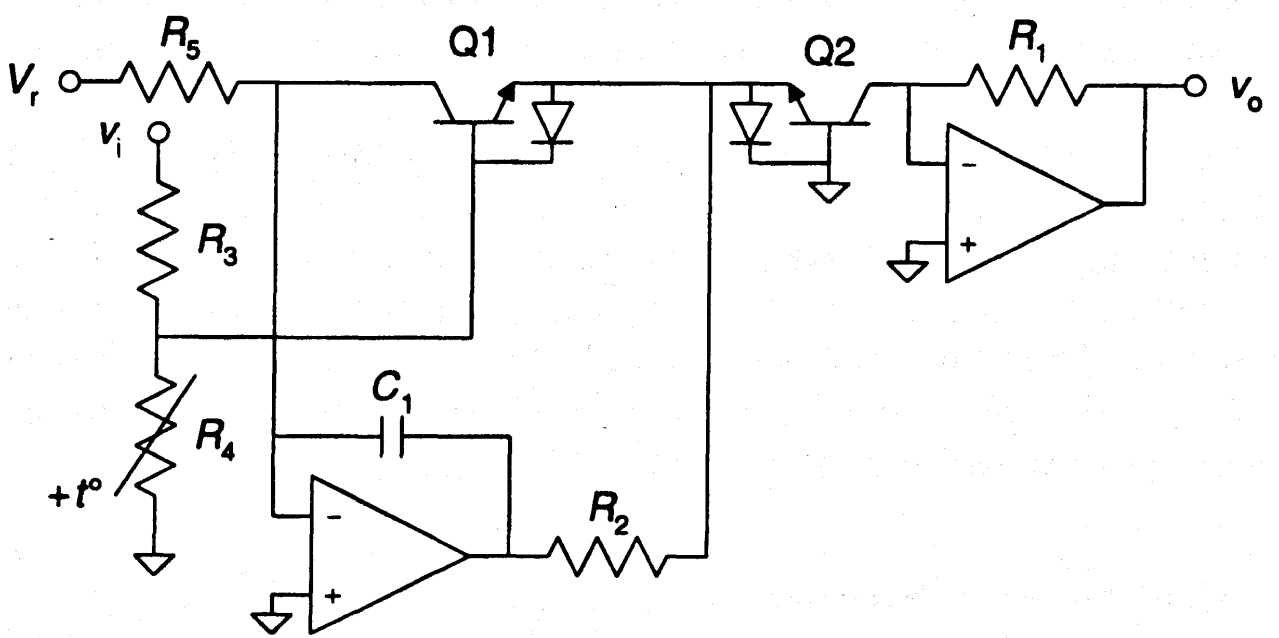
(a)



(b)

Antilog Amplifier

- Interchanging the position of resistor and transistor in a log amp yields a basic antilog amp.
- The base-collector voltage is kept at 0 V, so that collector current is given by
- $$i_c \approx I_s \cdot \exp(v_{BE} / V_T)$$
- and for negative input voltages we have: $v_o = i_C R_1 = I_S R_1 \exp(-v_i / V_T)$
- There is again a double temperature dependence because of $\boldsymbol{I_S}$ and $\boldsymbol{V_T}$.
- Temperature compensation can be achieved by the same technique shown for log amps.



Temperature Compensation

- The input voltage is applied to a voltage divider that includes a temperature sensor. If *R3* » *R4*, v_{BC1} ~ 0V and applying $I_c = I_s(\exp(v_{BE}/V_T)-1)$ to Ql yields

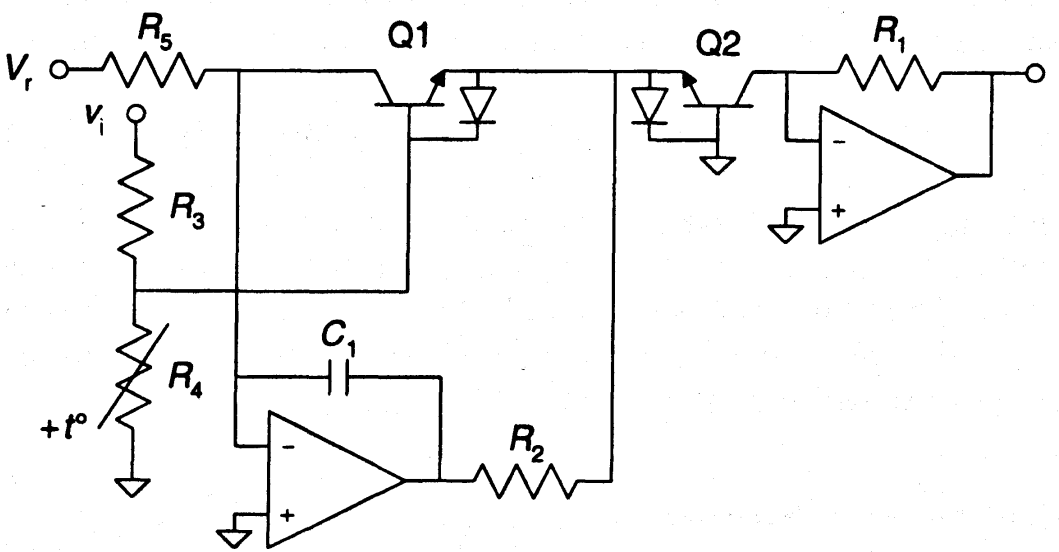
$$i_{c1} \approx I_{s1}\exp(v_{BE}/V_T) = V_r/R5$$

- where *Vr* is a reference voltage and we have assumed $V_{BE1} >> V_T$ (25 mV).
- In **Q2** V_{BC2} = 0V and hence : $i_{c2} \approx I_{s2}\exp(v_{BE2}/V_T) = V_o/R5$ Also:

$$v_i \frac{R4}{R4+R3} = v_{BE1} - v_{BE2}$$

- Substituting v_{BE1} and v_{BE2}, and solving for v_o,
- if Ql and Q2 are matched yields

$$v_o \approx V_r \frac{R1}{R5}\exp\left(-\frac{v_i}{V_T}\frac{R4}{R3+R4}\right)$$



Therefore, if the temperature coefficient of R4 is such that *dR4/R4* == dV_T/V_T = l/T the voltage divider will compensate for the temperature dependence of V_T. At *T* = 298 K, the temperature coefficient of *R4* must be 3390 x 10^{-6}K.

Log-Antilog

- Log and antilog amp circuits include the same elements but arranged in different feedback configurations.
- Some integrated log amps have uncommitted elements allowing us to implement antilog amps.
- Some **IC** (like ICL8049) are a committed only antilog amp.
- Some so-called *multifunction converters* (AD538, LH0094, 4302) include op amps and transistors to simultaneously implement log and antilog functions, or functions derived thereof, such as
  - multiplication,
  - division,
  - raising to a power,
  - or taking a root

Basic Multiplier

- Multipliers are based on the fundamental logarithmic relationship that states that the product of two terms equals the sum of the logarithms of each term.
- This relationship is shown in the following formula:

$$\ln(a \times b) = \ln a + \ln b$$

- This formula shows that two signal voltages are effectively multiplied if the logarithms of the signal voltages are added.

Multiplication Stages

- The multiplication procedure take three steps:

1. 1. To get the logarithm of a signal voltage use a Log amplifier.

$$V_1^* = \ln(V_1) \quad \text{and} \quad V_2^* = \ln(V_2)$$

2. 2. By summing the outputs of two log amplifiers, you get the logarithm of the product of the two original input voltages.

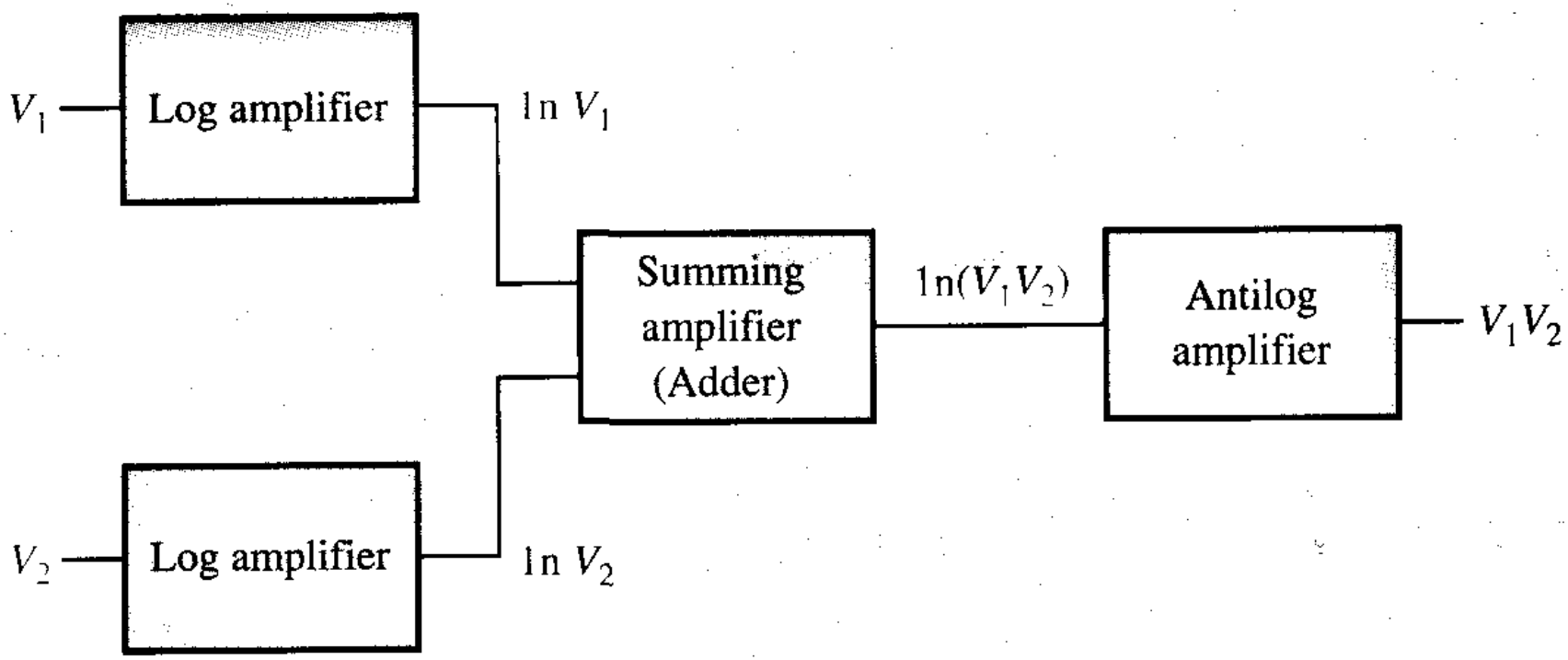
$$V_O^* = V_2^* + V_2^* = \ln(V_1) + \ln(V_2) = \ln(V_1 \cdot V_2)$$

3. 3. Then, by taking the antilogarithm, you get the product of the two input voltages as indicated in the following equations:

$$V_O = \exp(V_O^*) = \exp[\ln(V_1 \cdot V_2)] = V_1 \cdot V_2$$

block diagram of an analog multiplier

- The block diagram shows how the functions are connected to multiply two input voltages.
- Constant terms are omitted for simplicity.



Basic Multiplier Circuitry

- The outputs of the log amplifier are stated as follows:

$$V_{out(\log 1)} = -K_1 \cdot \ln\left(\frac{V_{in1}}{K_2}\right)$$

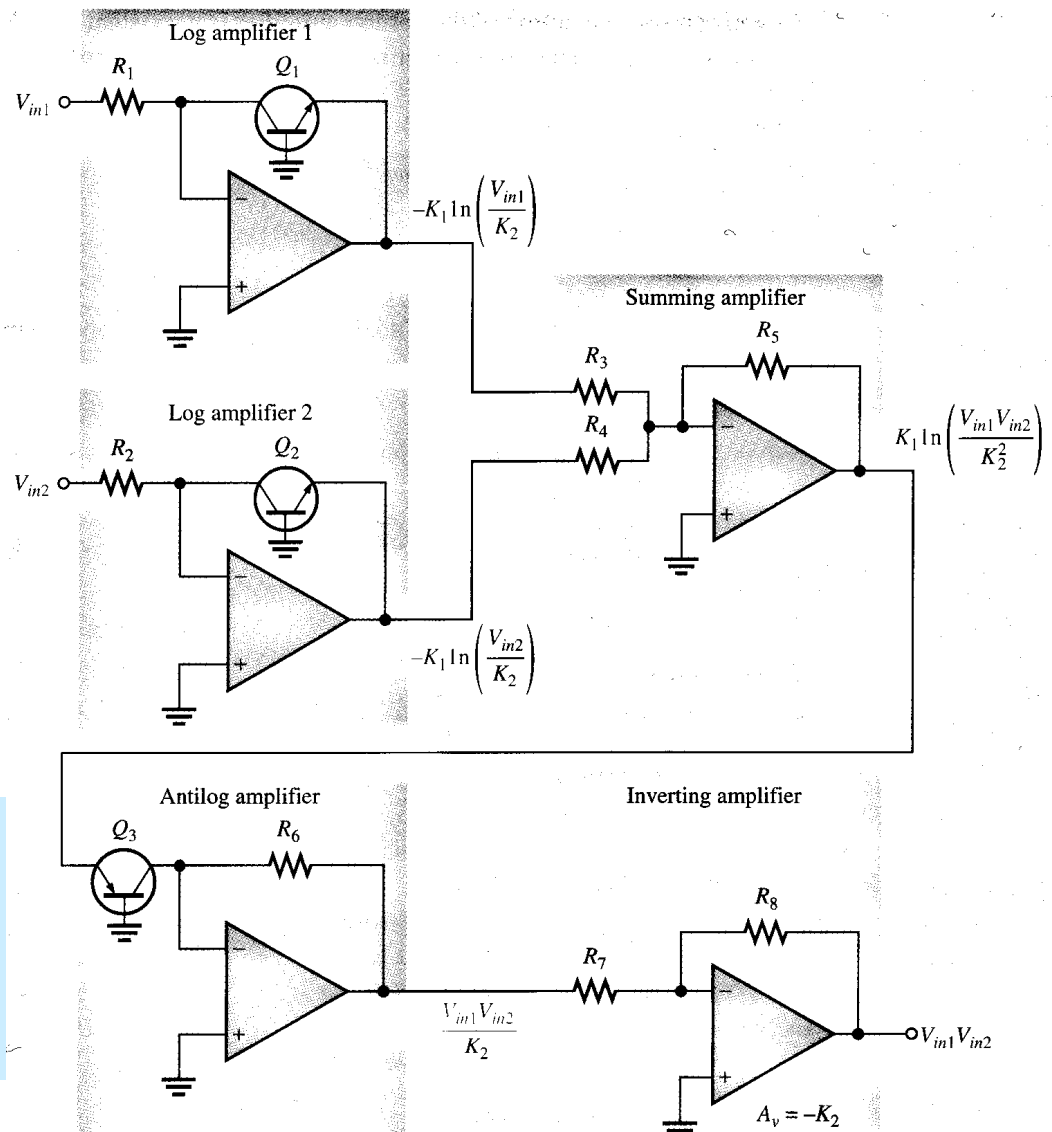
$$V_{out(\log 2)} = -K_1 \cdot \ln\left(\frac{V_{in2}}{K_2}\right)$$

where K_1 = 0.025 V, $K_2 = R \cdot I_{ebo}$ and $R = R1 = R2 = R6$.

The two output voltages from the log amplifiers are added and inverted by the unity-gain summing amplifier to produce the following result:

$$V_{out(sum)} = K_1 \cdot \ln\left[\ln\left(\frac{V_{in1}}{K_2}\right) + \ln\left(\frac{V_{in2}}{K_2}\right)\right] =$$

$$= K_1 \cdot \ln\left(\frac{V_{in1} \cdot V_{in2}}{K_2^2}\right)$$



- This expression is then applied to the antilog amplifier; the expression for the multiplier output voltage is as follows:

$$V_{out(\exp)} = -K_2 \cdot \exp\left(\frac{V_{out(sum)}}{K_1}\right) = -K_2 \cdot \exp\left[\frac{1}{K_1} K_1 \cdot \ln\left(\frac{V_{in1} \cdot V_{in2}}{K_2^2}\right)\right] =$$

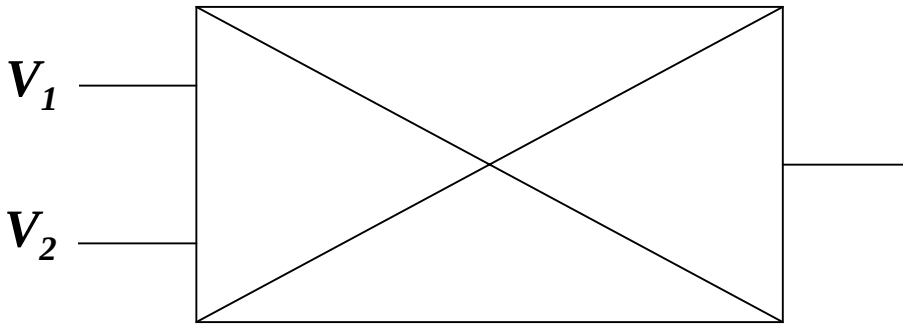
$$= -K_2\left(\frac{V_{in1} \cdot V_{in2}}{K_2^2}\right) = -\frac{V_{in1} \cdot V_{in2}}{K_2}$$

- The output of the antilog (exp) amplifier is a constant (*1/K2*) times the *product* of the input voltages.
- The final output is developed by an inverting amplifier with a voltage gain of *—K2*.

$$Vout = -K_2\left(-\frac{V_{in1} \cdot V_{in2}}{K_2}\right) = V_{in1} \cdot V_{in2}$$

Four-Quadrant Multipliers

- Four-Quadrant Multiplier is a device with two inputs and one output.



$$V_{out} = k \cdot V_1 \cdot V_2$$

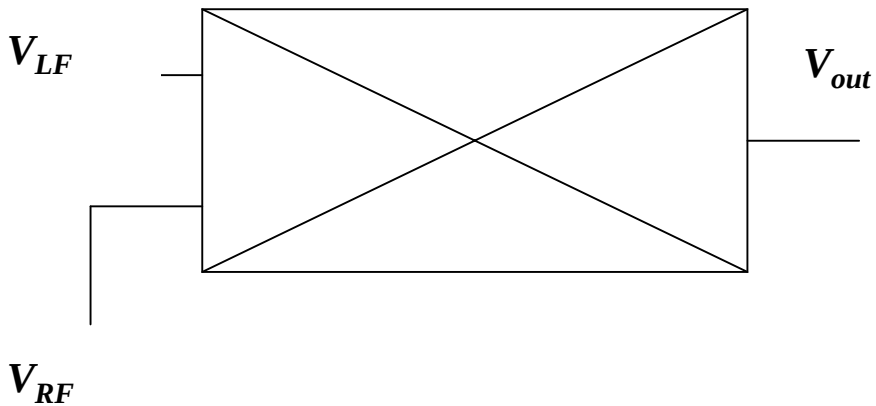
- Typically k = 0.1 to reduce the possibility of output overload.
- It is called four-quadrant since inputs and output can be positive or negative.
- An example device is Motorola MC1494, powered by ± 15 V power supply

Multiplier Applications

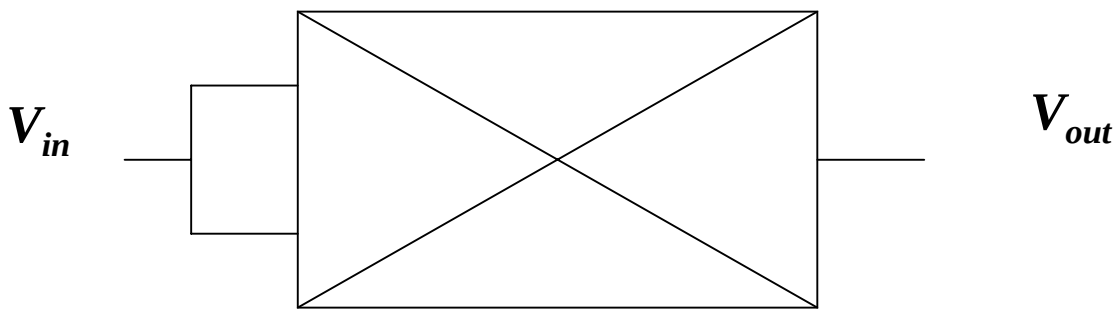
- Alongside the multiplication Multipliers have many uses such as:
  - Squaring
  - Dividing
  - Modulation / demodulation
  - Frequency and amplitude modulation
  - Automatic gain control

Amplitude Modulation & Squaring

- Amplitude Modulation

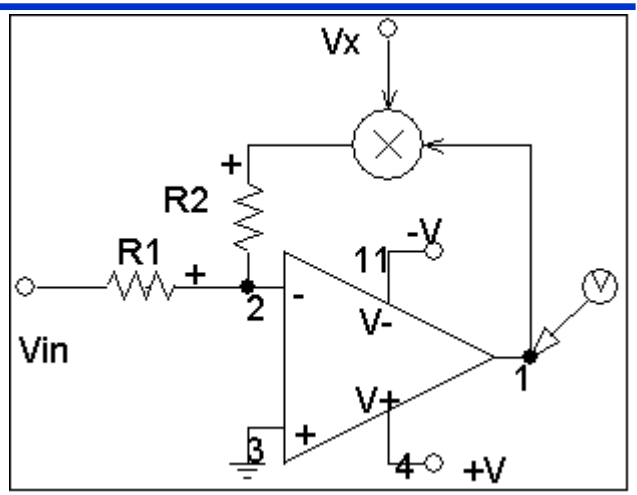


- Squaring circuit



Divider

- Divider $Vm = K \cdot Vx \cdot Vout$



$$i_1 = \frac{Vin}{R1} \qquad i_2 = \frac{Vm}{R2}$$

$$Vin = -Vm = -K \cdot Vx \cdot Vout$$

$$Vout = \frac{Vm}{K \cdot Vx} = -\frac{Vin}{K \cdot Vx}$$

- Square root: If $Vx = Vout$

$$Vout = -\frac{Vin}{K \cdot Vout}$$

$$Vout = \sqrt{\frac{-Vin}{K}}$$