Table 2-10: CA80C85B Extended Instruction Set

Name	Opcodes	Flags	Cycles	States	Description
ARHL	00010000 Addressing: Register	CY	2	7	**Arithmetic Shift of H and L to the Right:** The contents of registers H and L are shifted right one bit is shifted into the carry bit. The result is saved in registers H and L. H7=H7; Hn-1=Hn; L7=H0; Ln-1=Ln; CY=L0
DSUB	00001000 Addressing: Register	Z, S, P, CY,	3	10	**Double Subtraction:** The contents of registers B and Care subtracted from the contents of registers H and L. The result is saved in registers H and L. (H) (L)=(H) (L) - (B) (C)
JNUI	11011101 low-order address high-order address Addressing: Immediate	none	2 or 3	7 or 10	**Jump on NOT UI Flag:** Control is transferred to the instruction address specified in bytes 2 and 3 of the current instruction. The result is saved in registers H and L. (H) (L)=(H) (L) - (B) (C)
JUI	11111101 low-order address high-order address Addressing: Immediate	none	2 or 3	7 or 10	**Jump on UI Flag:** Control is transferred to the instruction address specified in bytes 2 and 3 of the current instruction. if the Unsigned Indicator Flag (UI) is set. Otherwise control continues sequentially. (H) (L)=(H) (L) - (B) (C)
LDHI	00101000 data Addressing: Immediate Register	none	3	10	**Load D and E with L Plus Immediate Byte:** The immediate byte is added to the contents of registers H and L, and the result is saved in registers D and E. (D) (E) = (H) (L) + (byte 2)
LDSI	00111000 data Addressing: Immediate Register	none	3	10	**Load D and E with SP Plus Immediate Byte:** The 2 bytes of register SP are added to the immediate byte, and the result is saved in registers D and E. (D) (E) = (SPH) (SPL) + (byte 2)
LHLX	11101101 data Addressing: Register Indirect	none	3	10	**Load H and L Indirect Through D and E:** The contents of the memory location given by registers D and E are moved to register L. The contents of the next location are moved to register H L=((D) (E)); H=((D)(E) + 1)
RDEL	00011000 Addressing: Register	CY, V	3	10	**Rotate D and E Left Through Carry:** The contents of the registers D and E are rotated one bit left through the carry flag. The low-order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high-order bit Dn+1=Dn; D0; E7; CY=D7; En+1=En; E0=CY
RSTV	11001011 Addressing: Register Indirect	none	1 or 3	6 or 12	**Restart on Overflow:** If overflow flag V is set, then the actions below are performed. Otherwise, control continues sequentially. If (V): SP - 1=PCH; SP - 2=PCL; SP=SP - 2; PC=40HEX
SHLX	11011001 Addressing:	none	3	10	**Store H and L Indirect Through D and E:** The contents of register L are moved to the memory location given by registers D and E. The contents of register H are