AN ULTRA LOW POWER FAULT TOLERANT SRAM DESIGN IN 90NM CMOS

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ABSTRACT

To mitigate the single-event effect, improve the stability and also maintain the low power characteristic of sub-threshold SRAM, a Dual Interlocked Storage Cell (DICE) based SRAM cell in 90nm CMOS technology was proposed to eliminate the drawback of conventional DICE cell during read operation. In order to make the proposed SRAM cell work under different power supply voltages from $0.3V$ to $0.6V$, an improved replica sense scheme is applied to produce a reference control signal, with which the optimal read time could be achieved. In this paper, a 256×8bytes SRAM core was simulated and the operating frequency at $V_{DD} = 0.3V$ is up to $4.7MHz$ with power dissipation $6.0\mu W$, while it is $45.5MHz$ at $V_{DD} = 0.6V$ dissipating $140\mu W$. The layout of SRAM core was also done in 90nm CMOS technology.

Index Terms— SRAM, sub-threshold, Dual Interlocked cell (DICE), fault tolerance, Single Event Upset (SEU)

I. INTRODUCTION

With the increment of mobile, biomedical and space applications these years, there is an aggressive demand to reduce power consumption and improve the reliability of an LSI, while the speed and area are the secondary considerations. Subthreshold operation is an efficient way to achieve this, and there has been some research reported [1]. As a main part of LSI, ultra low power memory design is challenging and should be kept in mind for circuit designers. For biomedical and space applications, not only low power of the SRAM is required, high stability and immunity to Single Event Upsets (SEU) are also critical in terms of safety. In some cases, we even have to sacrifice some power to achieve high stability.

Both the read and write stability of conventional 6T SRAM cell degrades with the aggressively scaled supply voltage V_{DD} [2]. When supply voltage $V_{DD} = 0.3V$, the average SNM of 6T cell is only $32.5mV$, which will lead to unaffordable SRAM storage error. Several sub-threshold cells have been proposed to replace 6T cell under subthreshold voltage [3–6]. The main idea of these cell designs is to decouple read and write operation, which can significantly improve Static Noise Margin (SNM) of SRAM. For example, the average SNM of the 10T cell in[6] increases to $98.0mV$ with $0.3V$ supply voltage, approximately three times of that for 6T cell. However, when it comes to high reliability and fault tolerant applications, a radiation harden design is necessary, such as Dual Interlocked Storage Cell which is insensitive to radiation induced single event upsets[7]. Nonetheless, conventional DICE cell could only eliminate single effect in hold state, not in read operation. Therefore, to avoid SEUs during read operation of DICE cell, decoupled scheme is applied here. The following section presents the DICE based sub-threshold SRAM cell design. Section 3 presents an improved replica technique for sense clock generating, which is according to the worst case of discharging the bit lines. Finally, the simulation results and layout of this SRAM core are given in section 4 and 5 respectively.

II. SRAM CELL DESIGN BASED ON DICE STRUCTURE

As a Radiation Harden by Design (RHBD) memory cell design, DICE cell provides SEU immunity and is a good choice in sub-threshold memory circuits[8]. There are four nodes redundantly storing the data as two pairs of complementary values. Figure 1 shows a conventional DICE cell with 0101 stored in node X_0, X_1, X_2, X_3 respectively.

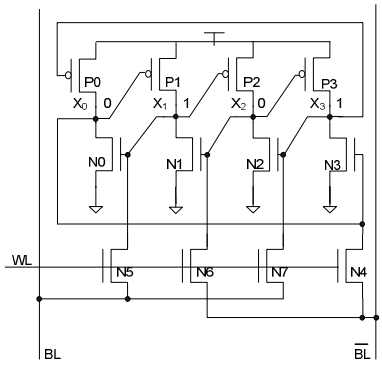
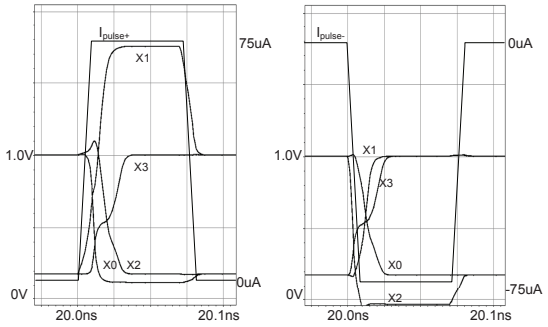


Fig. 1. Conventional DICE cell

During the hold state of DICE cell, neither a negative upset pulse nor a positive one could affect the logic state stored in the cell, which shows the immunity of DICE cell to radiation-induced upsets. However, during read operation, this immunity will not exist due to the turned-on access transistors and the precharged bit lines. When the bit lines are both precharged to V_{DD}, the turned-on access transistors will drive the storage nodes. If an upset pulse occurs during

the read operation, the logic state will be flipped, shown in Figure 2.



(a) Negative pulse at node X_2 (b) Positive pulse at node X_3

Fig. 2. Simulation waveforms for upsets in DICE cell

In Figure 2(a), logic state 1010 was stored in node X_0, X_1, X_2, X_3 before a positive current upset pulse occurred in node X_1. Here, a $700pS$ wide current pulse with magnitude of $75uA$ was applied to simulate a single event. Since it was read operation, N4-7 were all on. During the current pulse, node X_1 would be charged to "1", duo to which, negative transient of node X_0 was induced since N0 and N4 were both sinking X_0. Furthermore, both N3 and P3 were off when node X_0 was "0", so the current of the access transistor N7 would drive node X_3 to "1". Once X_3 was "1", N2 was on, which would sink node X_2 to "0". Finally, all the nodes were flipped, i.e. the immunity of SEU in storage nodes is destroyed during read operation. The key difference between hold state and read operation is whether there is driving current in access transistor N7 to flip node X_3. Figure 2(b) shows a negative current upset pulse at node X_2. The logic state is also flipped with this pulse. In order to keep the immunity of SEUs during read operation, the decoupled scheme is introduced to high reliable DICE cell design, shown in Figure 3.

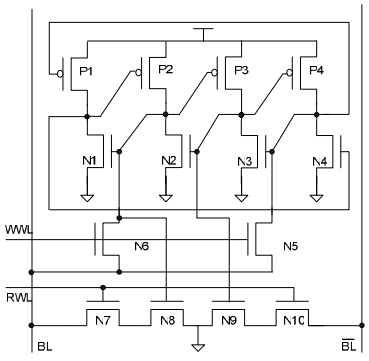


Fig. 3. Proposed DICE based cell

In this proposed fault tolerant cell, N_{1-4} and P_{1-4} form the DICE structure. And N_{7-10} are added for read operation so that there is no access transistor driving the nodes of cell during read operations, and the cell is also immune to SEUs. Instead of using four transistors for write operation, we use only N_5 and N_6 in this cell. The reduced two transistors could save some static power, and word line driving capability is also decreased. Here, There are two word lines, one is Read Word Line (RWL) for read operation, and the other is Write Word line (WWL) for write operation. Since only two transistors are used for write operation, boost voltage of WWL is necessary when "1" is written to the cell. In this design the boost voltage V_{boost} is $0.3V$ higher than V_{DD}, i.e. $V_{boost} = V_{DD}+0.3V$. Although the read and write operations become more complicated and an additional boost circuit is needed, this cell is still valuable and promising in high reliable applications.

III. REPLICA TECHNIQUE FOR READ OPERATION CONTROL

In sub-threshold operation, transistors will not go into saturation region, which implies that the gain and speed of an analog amplifier is too limited for a voltage-mode sense amplifier to be implemented and used for SRAM designs. Also, in low power SRAM designs, for the sake of saving power, clocked current-mode sense amplifiers are preferred. Therefore, the Differential Latch Type (DLT) sense amplifier is applied in this design[9], which, however, brings the problem of how to generate the sense clock. In many previous work, inverter chain is often applied to match the delay of data path. However, with the supply voltage varying from $0.3V$ to $0.6V$, inverter chain could not always track and match the data path delay very well. A self-timed sense scheme based on replica technique is proposed in [10], in which dummy cells are used to drive the dummy bitline to get sense clock. This method is able to generate the proper sense clock in super-threshold operations, however, needs to be improved when it comes to sub-threshold operation and standby leakage current is carefully considered.

In terms of leakage current, the worst case of reading a cell is that all other cells in the same column have different value of the accessed cell. In this case, the current of the accessed cell I_R will discharge the BL while the total leakage current of unaccessed cells in this column I_L will discharge $\overline{BL}$ simultaneously. In sub-threshold SRAM, when each column has a large number of cells, the ratio I_R/I_L will be decreased significantly, which could result in increased time delay to get sufficient voltage swing between BL and $\overline{BL}$. In order to sense this swing correctly, the sense clock should be generated according to the largest time delay. Therefore, in our design, two different types of dummy cells are proposed for dummy column—Dummy Active Cell (DAC) and Dummy Sleeping Cell (DSC), which are shown in Figure 4(a) and (b) respectively. DAC is the proposed

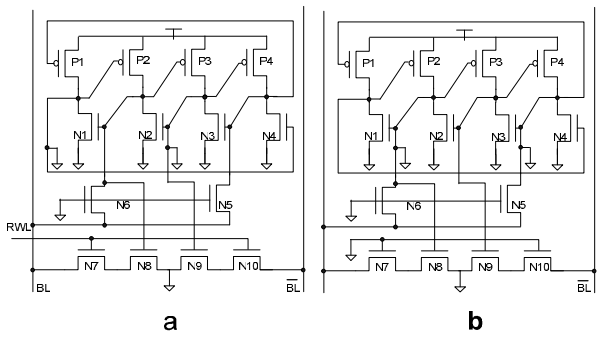


Fig. 4. (a) dummy active cell, (b) dummy sleeping cell

cell with two nodes and WWL connected to V_{SS} so that it always stores a "0" with no write operation, shown in Figure 4(a). DSC is the proposed cell with the other two nodes and both wordlines connected to V_{SS}. DSC always stores an "1" and has no read and write operations. The dummy column consists of 2 DACs and 254 DSCs, which matches the worst case of read operation.

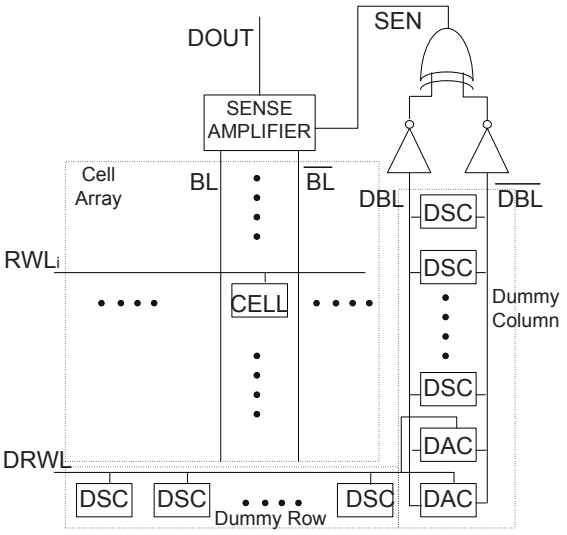


Fig. 5. self-timed sense scheme

Figure 5 shows the self-timed sense scheme. During read operation, RWL_i and Dummy RWL $DRWL$ go high simultaneously. The storage cell in cell array is accessed by RWL_i while the two DACs in dummy column are accessed by $DRWL$ to discharge DBL. When DBL is discharged to low and $\overline{DBL}$ remains high, the output of the EXOR gate, i.e. the sense clock, will go to high to activate the sense amplifier. In this scheme, a DAC drives the same current as the accessed cell, and two DACs will drive 2 times of current on DBL. Therefore, the falling transient of DBL will be sped up, and the voltage swing between accessed BL and $\overline{BL}$ is about 10% of V_{DD}, which is large enough for sensing.

In this self-timed scheme, no delay element is needed and hence there is no inverter chain. The scheme based on the worst case could eliminate the negative effect of standby leakage current and gain high reliability.

IV. SIMULATION RESULTS

Simulation of a 256×64-bit SRAM core was performed in 90nm technology under typical condition (25^oC). Here, the parasitic capacitance of WLs and BLs was not taken into account. Figure 6 shows the simulation waveforms of read operation with the power supply $V_{DD} = 0.3V$. Bit-line voltage swing is only approximately 10% of V_{DD}, which could save bit-lines discharging power while provide enough swing for sensing. The read time in Figure 6 is $0.212\mu S$. The replica sense scheme can keep the optimal read time when supply voltage varies. In Table 1, with the supply voltage of $0.3V$, $0.4V$, $0.5V$ and $0.6V$, read and write access time, maximum operating frequency and power dissipation comparisons are given. From Table 1, we can find that this SRAM consumes very low power while the speed is enough for many low speed applications.

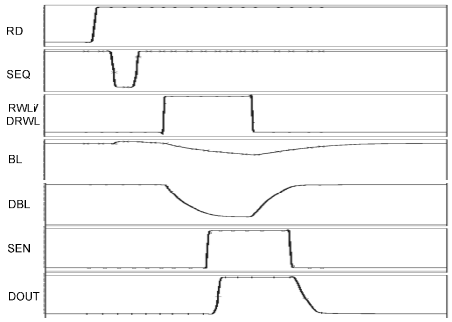


Fig. 6. Read operation Waveform

Table I. Simulation results with different power supplies

V_{DD} $[V]$	Write Time $[\mu S]$	Read Time $[\mu S]$	F_{MAX} $[MHz]$	power $[\mu W]$
0.3	0.141	0.212	4.7	6.0
0.4	0.042	0.056	17.8	27.9
0.5	0.027	0.029	34.5	76.7
0.6	0.019	0.022	45.5	140.0

In sub-threshold circuit design, especially for memory design, standby leakage power takes a major part of the total power dissipation. Table 2 shows the standby leakage current of the conventional 6T cell, conventional DICE cell and the cell proposed in this paper with the power supply voltage of $0.3V$.

From Table 2, we can find that the proposed DICE cell has slightly more leakage current than conventional DICE cell which is about two times of that for 6T cell. This slightly increased leakage current will lead to a little more

Table II. Standby leakage comparison of three cells

	6T	DICE	proposed
$I_{leakage}$	117pA	239pA	275pA

power dissipation which, however, is worthwhile in term of reliability.

V. LAYOUT

The layout of a 256×8 bytes SRAM core was done in $90nm$ CMOS technology. The proposed DICE based cell has 14 transistors, which is relatively more than that of 6T and 10T cells. Therefore, the area is larger. The area of a single DICE based cell is $3.9\mu M \times 3.4\mu M$. Figure 7 shows the layout of the SRAM core, including cell array, sense amplifiers, row and column decoders, and dummy column and row. The total size of this SRAM core is $500\mu M \times 515\mu M$.

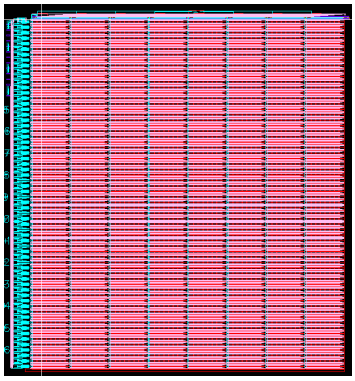


Fig. 7. Layout of SRAM core

VI. CONCLUSION

In this paper, an improved DICE based SRAM cell with high reliability is proposed. The proposed 14-Transistor SRAM cell has significant improvement of stability compared to previous cell designs. And this cell has immunity to single event upset during read operation, though the cell area and power dissipation are relatively larger compared to conventional cells working at subthreshold voltage. The replica technique used in sense control makes this SRAM core be able to work under variable power supply voltages and achieve the optimal speed. Although the standby leakage current is a little bit more than conventional DICE cell, it is still promising in many high reliable low power applications, such as space, biomedical and military applications, since this proposed cell is aimed at working at subthreshold voltage, where the standby leakage current is instinctually much lower than that working at standard supply voltage.

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