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Basic Memory Elements Using DICE Cells for Fault-Tolerant 28 nm CMOS RAM

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Abstract—A CMOS DICE (Dual Interlocked Storage Cell) cell consists of two transistor groups whose layout on the crystal increases the cell's stability against the impact of single nuclear particles. A fault of the cell's state does not take place if the particle impacts transistors of one group only. The topological layouts of basic memory elements with a different relative position of two transistor groups of 28 nm CMOS DICE cells were designed and analyzed. Different cell layouts with a distance between the sensitive pairs of transistors of two groups of 1, 2, and 3 μm and a set of basic memory elements for designing memory arrays of static RAM with increased stability with respect to state faults due to the particle track charge separation between two transistor groups of the cell were proposed. The area of the DICE cells is larger by a factor of 2.1–2.5 than that of six-transistor cells with transistors of the same size.

Keywords: memory cell, RAM, simulation, single nuclear particle, charge sharing, layout

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1. INTRODUCTION

The basis of static CMOS RAM with increased tolerance to the single-event impact of nuclear particles is the DICE (Dual Interlocked Storage Cell) cell [1]. Memory cells and DICE flip-flops designed by scaling the topology [2, 3] of design rules from 0.18 μm to 32 nm have lost their advantages with respect to common *D* flip-flops and 6T CMOS memory cells, as regards the soft error rate (SER) and critical charge [4–6], as the node rules were reduced. For commercial 32–40 nm CMOS technologies the advantage of single-event impact is not more than 30–50% for single neutrons with an energy higher than 10 MeV [2, 3], while additional area and consumed power expenses are required.

The soft error rate of CMOS flip-flops with a hardened circuit design to single-event nuclear particle impact can be reduced [7–10] by increasing the space between the sensitive nodes. The larger the distance between the sensitive nodes of a device in the active silicon layer the lower the probability of multiple impact and fault.

A 0.18 μm bulk-standard CMOS static RAM [9] based on DICE cells was manufactured with different distances between the drains of transistor pairs reverse biased for storing "0" (distance $D_{\text{“0”}} = 0.9$ μm) and "1" (distance $D_{\text{“1”}} = 2.5$ μm). The soft error rate of "1" states in such a CMOS RAM affected by 1 GeV protons was smaller by a factor of 15 ($D_{\text{“1”}} = 2.5$ μm) than that of "0" states ($D_{\text{“0”}} = 0.9$ μm).

The dependence of SER upon the single-event impact of nuclear particles (neutrons and protons) for RAM storage cells and *D* flip-flops with 28–65 nm CMOS on the distance between the sensitive nodes of CMOS storage cells and flip–flops was experimentally established in [7, 8]. A distance of 1 μm between the sensitive nodes of storage cells and DICE flip-flops reduces SER by a factor of 100 [8] compared to the case when this distance is equal to 100...300 nm, which is typical for 28 nm CMOS *D* flip-flops and DICE cells. If the distance between nodes is increased to 3 μm SER is additionally reduced by a factor of 10.

No such generalization for heavy ions is available yet; however, by analyzing the data on the impact of heavy ion beams at different angles to the crystal surface of the device, the distance between sensitive nodes subject to multiple faults can be estimated. Thus, in the case of a 90 nm standard CMOS DICE flip-flop fault due to the action of copper ion ^{63}Cu with an energy of 945 MeV and LET = 17 MeV cm^2/mg for a trajectory inclination angle of 80° [6] and a thickness of the active silicon layer of 0.4 μm the track length in the active layer is not shorter than 2.3 μm. For smaller design rules the thickness of the active layer (epitaxial or implanted) is smaller, and therefore, it is also

smaller for the area in which ionization under the impact of a single ion takes place.

The simulation of effects of the single-event impact on 90 nm 6T CMOS RAM cells demonstrated [11] that for carbon ions with an energy of 131 MeV SER probability decreases by a factor of 100 for a distance of 0.7 μm from the ion's hitting point to the center of the inverse biased drain *pn* junction of the CMOS transistor, and by a factor of 10^3 for a distance of 1.0 μm. For argon ions with an energy of 372 MeV SER is reduced by a factor of 100 for a distance of 1.6 μm and by a factor of 10^3 for a distance of 2 μm.

If the distance between sensitive nodes of a cell (element) increases, alternative methods for designing the topology of such an element are required in order to avoid the inefficient use of the crystal area. The problem of increasing noise immunity is solved using topological methods. The experimental studies of 28 nm CMOS DICE flip-flops with transistors situated along a straight line [12] demonstrated quite a low SER for neutron, proton, and heavy ion irradiation in all azimuthal directions of the particle tracks except that of the topological position of DICE cell transistors.

Another approach to increasing the noise immunity of DICE cells was substantiated in [13–15] by the fact that transistors of a DICE cell can be united in two groups in such a way that a particle impact on one of them does not result in the error of the cell's logical state. The noise stability of such a cell can be increased by spacing these two transistor groups on the crystal.

2. TAKING INTO ACCOUNT SPECIFIC FEATURES OF DICE CELLS IN TOPOLOGY DESIGN

Figure 1 shows the schematic of a DICE cell. For increasing noise immunity to the single-event impact of nuclear particles DICE cells should be designed in the form of two transistor groups [13–15] spatially separated on the crystal. They, in turn, can be grouped into basic memory elements as matrices of alternating transistor groups.

Each of the two groups of a DICE cell contains two *N*MOS and two *P*MOS transistors of the memory cell flip-flop; in one logical state of the cell one pair of *N*MOS and *P*MOS transistors in each group are closed, and in the other state the other pairs of *N*MOS and *P*MOS transistors are closed. Within one group a single-event impact on a pair of transistors in the closed state does not result in the upset of the cell's flip-flop. The cell's state fails only if the closed transistors of two different groups are affected; that is why these transistor groups should be spatially separated in order to reduce the critical effect of the particle track charge.

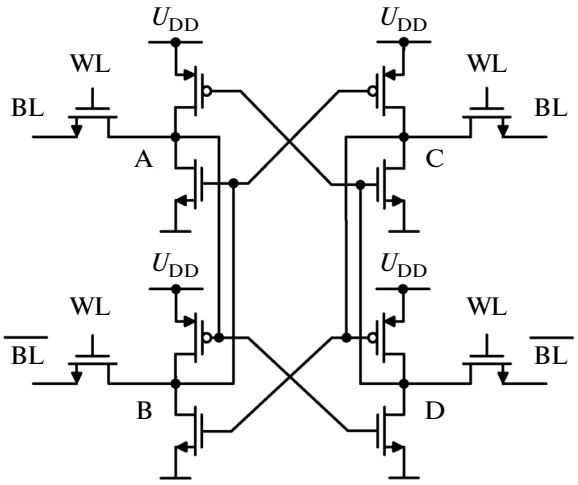

Fig. 1. DICE cell circuit.

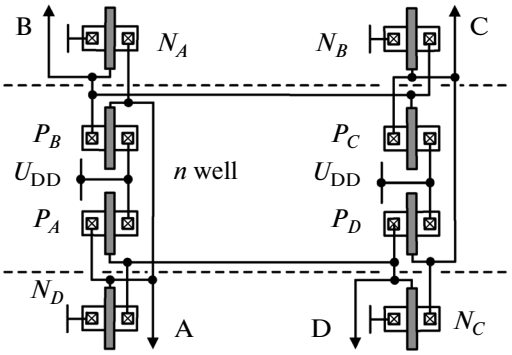

Fig. 2. DICE cell flip-flop layout for column transistor groups.

3. BASIC MEMORY ELEMENTS FOR 28 nm CMOS RAM MEMORY ARRAYS

Three versions of the basic memory elements using 28 nm CMOS DICE cells for 32 × 64 memory array are presented.

The objective of developing basic memory elements is to provide the maximum distance between the sensitive areas of two transistor groups of DICE cells in the minimum memory array area. Memory arrays have guard rings for eliminating the thyristor effect. For reducing the area occupied by the rings the number of *n*-wells was minimized by placing a large number of PMOS transistors in *n*-wells. The polysilicon lines are unidirectional.

A. Different Relative Positions of Two Transistor Groups of a DICE Cell in Basic Memory Elements

The flip-flop of a DICE cell consists of two transistor groups, four transistors each. Figure 2 shows the layout of the flip-flop of a DICE cell for two column

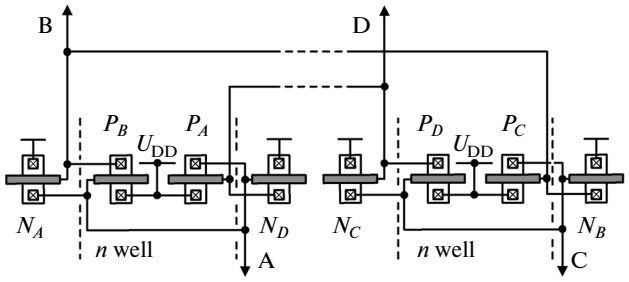

Fig. 3. DICE cell flip-flop layout for line transistor groups.

N_A							N_B						
P_B							P_C						
P_A							P_D						
N_D							N_C						

Fig. 4. *N*MOS and *P*MOS transistor matrix for eight DICE cells of 8 × 1 basic element 1DICE.

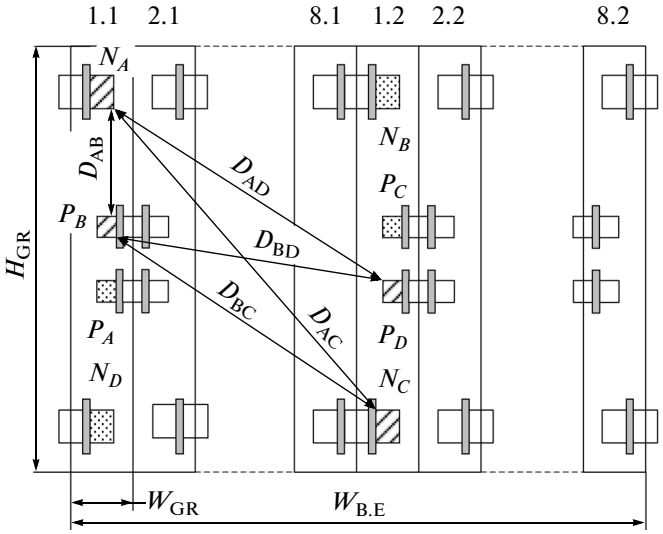

Fig. 5. Cell transistor topology in basic memory element 1DICE containing eight DICE cells.

transistor groups, and Fig. 3 shows it for two line groups of cell transistors.

The basic memory element is formed from similar repeated transistor groups. Transistor groups can be repeated both in the horizontal and vertical directions, forming a matrix of *similar transistor groups with similar transistor connections*. Each DICE cell can be formed by a two-wire connection of two transistor groups situated along a row or column of the basic memory element matrix.

The requirement of 28 nm CMOS technology to the periodicity of polysilicon lines results in the discrete width of the basic memory element. In order to eliminate area losses upon joining basic elements their width should be multiples of the half-period of the polysilicon lines, which comes to 65 nm for a transistor channel length of 30 nm. The main contribution to the memory array area is made by metallization of the connection lines.

The basic memory element capacity $m_A \times m_D$ is determined by the number of its address lines m_A and data lines m_D for connecting with memory array buses. Particular values of m_A and m_D for basic elements are determined by the specific features of minimization of the metallization area in basic elements with a different relative position of the transistor groups.

B. Basic 1DICE Memory Element with a Capacity of 8 × 1

Sixteen columns of the matrix of the basic 1DICE memory element with a capacity of $m_A \times m_D = 8 \times 1$ (see Fig. 4) are repeated in the horizontal direction. Such an alternation of columns of eight memory cells provides a distance between two groups of each of the eight cells equal to the width of seven transistor groups. The position of two transistor groups of one memory cell in the matrix in Fig. 4 corresponds to the parallel position of two groups (see Fig. 2). Figure 4 shows the position of the *P*MOS and *N*MOS transistors in two groups (columns) of the first DICE cell only in the basic memory element of eight cells. On the whole, the first half of the columns contain eight first transistor groups of eight memory cells, then eight columns of the second eight transistor groups. Two transistor groups of one memory cell are connected by only two wires. Thus, eight memory cells have 16 connection lines.

Figure 5 shows the topology of the basic 1DICE memory element; in this figure, the columns are denoted by two numbers, the first one is the cell number, and the second one is the number of the transistor group of a given cell. The distance between sensitive pairs of *pn* transitions' drain-substrate of the transistors which are situated in the case of inverse biasing in one of the logical states of a DICE cell are denoted in Fig. 5 as D_{AC}, D_{AD}, D_{BD}, D_{BC}, and D_{AB}. In the other logical state the same distances are between the drains of other pairs of the closed transistors.

In the basic 1DICE element the width of one transistor group (column) $W_{GR} = 0.26$ μm. The metallization area in the basic element exceeds the total area of the columns of eight memory cells; that is why the width of the basic 1DICE element is increased by the column width in order to place all metallization lines. For the channel width of the *N*MOS transistor $W_N =$ 350 nm and that of the *P*MOS transistor $W_P = 160$ nm the area of the corresponding memory array 32 × 64 1DICE is $S_{M.A} = 3075$ μm (see Table 1).

Hereinafter, the following notation is used for basic memory elements and memory arrays: for example, in 2DICE1 the first number denotes the number of the

Table 1. Parameters of basic DICE memory elements and 28 nm CMOS DICE RAM 32 × 64 bit memory arrays

Basic element	0DICE	1DICE	2DICE1	2DICE2	3DICE
Memory array	0DICE	1DICE	2DICE1	2DICE2	3DICE
Design rule	28 nm	28 nm	28 nm	28 nm	28 nm
W_N, nm	350	350	170	350	340
W_P, nm	160	160	115	160	230
Group area $H_{GR} \times W_{GR}$, μm^2	2.63 × 0.26	2.63 × 0.26	2.06 × 0.325	2.51 × 0.325	2.06 × 0.52
S_{GR}, μm^2	0.6838	0.6838	0.6695	0.8157	1.0712
S_{CELL}, μm^2	1.3676	1.3676	1.339	1.6314	2.1424
Number of cells in basic element	1	8	8	8	4
Capacity of basic element $m_A \times m_D$	1 × 1	8 × 1	2 × 4	2 × 4	1 × 4
$S_{B.E}$, μm^2	1.37	11.63	10.712	13.13	10.712
$H_{B.E} \times W_{B.E}$, μm^2	2.63 × 0.52	2.63 × 4.42	4.12 × 2.6	5.05 × 2.6	8.24 × 1.3
D_{AB}, μm	0.59	0.59	0.59	0.59	0.59
D_{AC}, μm	1.67	2.79	1.89	2.16	3.95
D_{AD}, μm	0.92	2.44	2.66	3.10	4.71
D_{BC}, μm	0.92	2.44	1.18	1.40	3.24
D_{BD}, μm	0.26	2.27	1.94	2.35	4
D_{MIN}, μm	0.26	2.27	1.18	1.40	3.24
$S_{M.A}$, μm^2	2800	3075	2769	3406	5518
$H_{M.A} \times W_{M.A}$, μm^2	168.32×16.64	168.32 × 18.27	65.92 × 42.41	80.32 × 42.41	131.84 × 41.86
t_{DEL}, ps	91	80	130	93	100
$t_{1.0}$, ps	129	123	260	160	155
P_{ACTIVE} (writing), μW	286	287	213	294	535
P_{ACTIVE} (reading), μW	27.3	29.8	15.2	26.2	40.8
Transistor matrix	Fig. 4	Fig. 4	Fig. 6	Fig. 6	Fig. 7

basic element, and the second number, the variant of this basic element. The notation 0DICE is used for the basic element consisting of only one DICE cell.

Table 1 gives the parameters of basic memory elements and variants of memory arrays of 32 × 64 bit RAM. These parameters are given here: W_N is the channel width of *N*MOS transistors, W_P is the channel width of *P*MOS transistors, H_{GR} and W_{GR} are the height and width of a transistor group of a memory cell, S_{GR} is the area of one transistor group, S_{CELL} is the area of a memory cell, $H_{B.E}$ and $W_{B.E}$ are the height and width of the basic memory element, $S_{B.E}$ is the area of the basic memory element, $H_{M.A}$ and $W_{M.A}$ are the height and width of the memory array, $S_{M.A}$ is the area of the memory array, t_{DEL} is the delay time of a memory cell signal in the memory array, $t_{1.0}$ is the transition time of the memory array from logical 1 to logical 0, and P_{ACTIVE} (writing) and P_{ACTIVE} (reading) are the average active powers of the memory array in the writing and reading modes, respectively. The data were obtained by simulation using topp_tt models of nch_mac and pch_mac transistors at a temperature of 25°C and a supply voltage of 0.9 V. The transistor channel length is 30 nm. In Table 1 D_{AB} is the distance between the rows of the *N*MOS and *P*MOS transistors of one group whose joint fault does not result in a cell error; D_{AC}, D_{AD}, and D_{BD}, D_{BC} are the distances between the drains of the closed transistors of two groups whose joint fault may result in the DICE cell

N_A	DICE cell 2	DICE cell 3	DICE cell 4	DICE cell 5	DICE cell 6	DICE cell 7	DICE cell 8
P_B							
P_A							
N_D							
N_C							
P_D							
P_C							
N_B							

Fig. 6. Matrix of *N*MOS and *P*MOS transistors of eight DICE cells, one memory cell in each column of the basic element 2DICE with a capacity of 2 × 4.

$\boldsymbol{N_A}$	$\boldsymbol{N_A}$
$\boldsymbol{P_B}$	$\boldsymbol{P_B}$
$\boldsymbol{P_A}$	$\boldsymbol{P_A}$
$\boldsymbol{N_D}$	$\boldsymbol{N_D}$
N_A	N_A
P_B	P_B
P_A	P_A
N_D	N_D
$\boldsymbol{N_C}$	$\boldsymbol{N_C}$
$\boldsymbol{P_D}$	$\boldsymbol{P_D}$
$\boldsymbol{P_C}$	$\boldsymbol{P_C}$
$\boldsymbol{N_B}$	$\boldsymbol{N_B}$
N_C	N_C
P_D	P_D
P_C	P_C
N_B	N_B

Fig. 7. Matrix of *N*MOS and *P*MOS transistors of four DICE cells, two memory cells in each column of the basic element 3DICE with a capacity of 1 × 4.

upset; and D_{MIN} is the minimum distance between the closed transistors of two transistor groups of one memory cell.

C. Basic 2DICE Memory Element with a Capacity of 2 × 4

The capacity of a basic 2DICE memory element (see Fig. 6) is $m_A \times m_D = 2 \times 4$. The DICE cell in the basic 2DICE memory element consists of two groups of transistors whose relative position in the vertical direction is shown in Fig. 3. Figure 6 shows the layout of eight memory cells of a basic 2DICE element. Transistors of one DICE cell occupy one column of the matrix in such a way that the upper part of the column in Fig. 6 is the first transistor group of the memory cell (four transistors), and the lower part of the column is the second transistor group of the same memory cell (four transistors). The two transistor groups of one memory cell are connected by two wires.

The area of the first variant of the 2DICE1 memory array (see Table 1) made from 2DICE1 basic elements is $S_{M.A} = 2769$ μm^2. The transistor's packing density is slightly smaller than that of the 1DICE memory array. For the second variant of the 2DICE2 memory array with increased channel width for *N*MOS and *P*MOS transistors $W_N = 350$ nm and $W_P = 160$ nm (see Table 1) the memory array area $S_{M.A} = 3406$ μm^2, which is 10% higher than that of 1DICE.

D. Basic 3DICE memory Element with a Capacity of 1 × 4

Figure 7 shows the layout of four memory cells in the basic 3DICE element (with vertical alternation of groups of DICE cells in the columns of the basic element matrix). The element capacity is $m_A \times m_D = 1 \times 4$. Groups of transistors in the cell are situated according to Fig. 3. One column is occupied by the *N*MOS and *P*MOS transistors of the two DICE cells in such a way that the upper half of the matrix column (see Fig. 7) contains two first transistor groups (four transistors each) of the first (shown in bold type) and second cells, and the lower half of the matrix column contains two second transistor groups (four transistors each) of the first (shown in bold type) and second cells. The first and second transistor groups of each memory cell are connected by two buses. One column of two DICE cells has four connection lines.

The basic 3DICE memory element (see Fig. 7) uses the vertical alternation of transistor groups of two memory cells in the column matrix, which results in a larger number of connection lines compared to the 2DICE element and larger metallization area. For placing metallization lines the column width is increased to 0.52 μm, which is larger by a factor of two than the column width of the basic element 1DICE.

The transistor channel width of the basic element 3DICE $W_N = 340$ nm and $W_P = 230$ nm. Transistors of sensitive pairs are situated in different wells. The metallization area of the basic 3DICE element is 20% larger than the area occupied by the transistors and rings. For placing power supply and grounding lines in the third metallization layer the width of the basic memory element is increased by two periods of the polysilicon grid and amounts to 1.3 μm. The area of the 3DICE memory array is $S_{M.A} = 5518$ μm^2, which has smaller than the transistor packing density in the 1DICE and 2DICE2 units by a factor of 1.8 and 1.6, respectively.

Figure 8 shows the diagrams for comparing the parameters of different layouts of basic memory elements and memory arrays designed for the 28 nm CMOS standard. The dependences are ordered by the

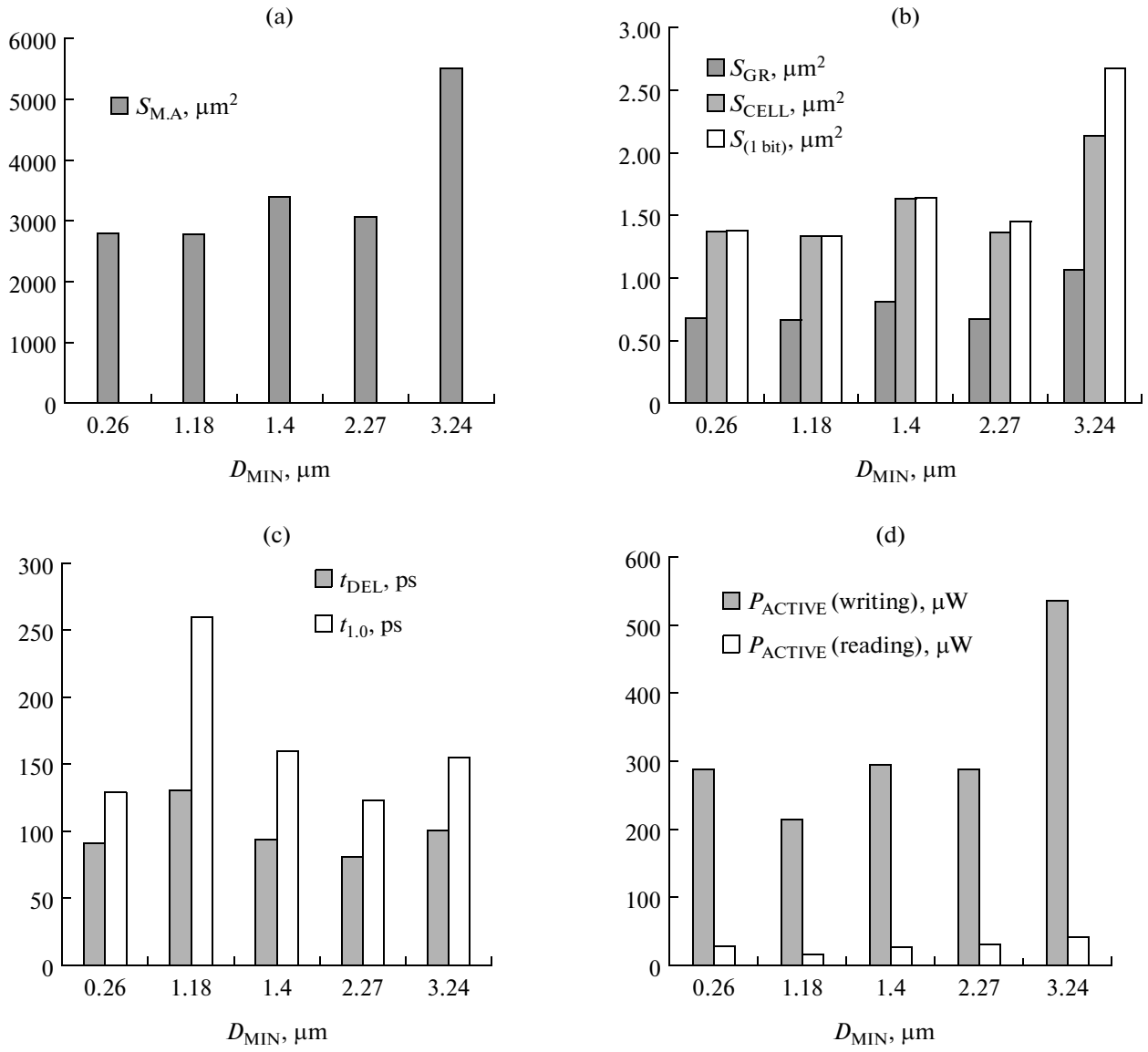

Fig. 8. Parameters of basic memory elements and 28 nm CMOS memory arrays RAM 32 × 64 bit as functions of the minimum distance D_{MIN} between drains of closed transistors in DICE cell: (a) memory array areas; (b) group and cell areas and areas per 1 bit; (c) switching delays; and (d) active power.

minimum distance D_{MIN} between the closed transistors of two different transistor groups of one memory cell. The diagrams in Fig. 8 include the parameters of the basic elements and memory arrays based on four variants of DICE cells with the following distances between the drain areas of transistors of different groups for a memory cell of the corresponding basic element: 1DICE (D_{MIN} = 2.27 μm), 2DICE1 (D_{MIN} = 1.18 μm), 2DICE2 (D_{MIN} = 1.4 μm), and 3DICE (D_{MIN} = 3.24 μm) (see Table 1).

The variant 0DICE with D_{MIN} = 0.26 μm was designed from two neighboring transistor groups without alternation with other groups (groups 8.1 and 1.2 in Fig. 5). The element 0DICE is used for comparison and is just one DICE cell with practically conventional topology and two closely situated transistor lines. The difference is the line (column) composition, which is not transistors differing by the type of conductivity (one line *N*MOS transistors and the second line *P*MOS transistors), but two transistor groups, according to Fig. 2. The parameters of the element 0DICE and the corresponding memory array are given in Table 1 and the minimum distance between closed transistors of two groups is 0.26 μm.

4. BASIC MEMORY ELEMENTS FOR 65 nm CMOS RAM MEMORY ARRAYS

Three designs of basic memory elements using 65 nm CMOS DICE cells [15] for 32 × 64 memory

Table 2. Parameters of basic elements and 65 nm CMOS RAM 32 × 64 bit memory arrays

Basic element	65-1	65-2	65-3
Memory array	65-1	65-2	65-3
Design rule	65 nm	65 nm	65 nm
W_N, nm	280	400	600
W_P, nm	180	180	180
$I_{C.NMOS}$, μA	216	307	461
$I_{C.PMOS}$, μA	67	67	67
Group area $H_{GR} \times W_{GR}$, μm^2	3.59 × 0.62	3.83 × 0.62	4.23 × 0.62
S_{GR}, μm^2	2.23	2.37	2.62
S_{CELL}, μm^2	4.46	4.74	5.24
Number of cells in basic element	4	4	4
Capacity of basic element $m_A \times m_D$	4 × 1	4 × 1	4 × 1
$H_{B.E} \times W_{B.E}$, μm^2	3.59 × 4.96	3.83 × 4.96	4.23 × 4.96
$S_{B.E}$, μm^2	17.8	19.0	21.0
D_{AB}, μm	0.95	0.95	0.95
D_{AC}, μm	3.41	3.41	3.41
D_{AD}, μm	2.64	2.64	2.64
D_{BC}, μm	2.76	2.76	2.76
D_{BD}, μm	2.32	2.32	2.32
D_{MIN}, μm	2.32	2.32	2.32
$S_{M.A}$, μm^2	9117	9727	10742
$H_{M.A} \times W_{M.A}$, μm^2	28.72 × 317.44	30.64 × 317.44	33.84 × 317.44
t_{DEL}, ps	110	100	80
$t_{1.0}$, ps	230	180	150
P_{ACTIVE} (writing), μW	52.2	58.5	75.8
P_{ACTIVE} (reading), μW	17.3	23.6	35.7
Transistor matrix	Fig. 4	Fig. 4	Fig. 4

arrays are presented for comparison. Table 2 gives the basic parameters of these elements. Figure 9 shows the diagrams for comparing the parameters of different basic memory elements (denoted as 65-1, 65-2, 65-3 in Table 2) and 65 CMOS memory arrays (see parameters in Table 2). The diagrams in Fig. 9 include the parameters of the 28 nm 1DICE element (denoted by 28-1) for comparison (see parameters in Table 1).

The 65 nm basic element and 28 nm element denoted by 28-1 shown in Fig. 9 are designed using column transistor group alternation (see Figs. 2 and 5), according to the transistor matrix shown in Fig. 4. They are characterized by practically equal minimum distances between the drains of closed transistors $D_{MIN\ 65\ nm} = 2.32$ μm and $D_{MIN\ 28\ nm} = 2.27$ μm. The difference is that basic elements 65-1, 65-2, and 65-3 with an unequal channel width of *N*MOS transistors (see Table 2) contain four 65 nm memory cells per element, while element 28-1 contains eight 28 nm cells.

Elements 65-3 (with maximum *N*MOS transistor currents, see Table 2) and 28-1 (see element 1DICE in Table 1) possess the smallest and practically equal delays t_{DEL} and $t_{1.0}$. The memory array using 65-3 elements has a maximum area among 65 nm units; unlike it, the 28 nm memory array using 28-1 elements has an area smaller by a factor of 3.5.

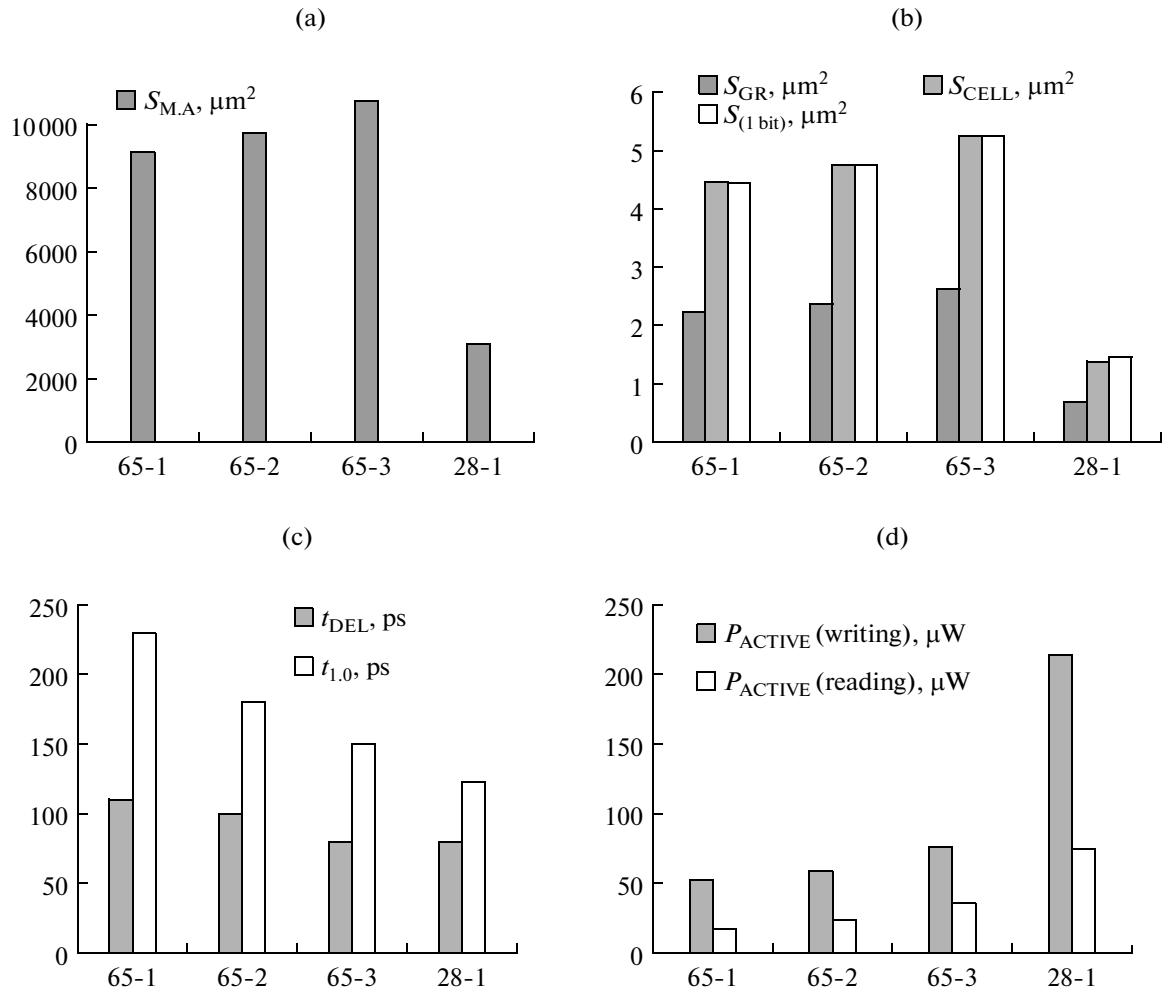

Fig. 9. Parameters of basic memory elements and 65 nm CMOS memory arrays RAM 32 × 64 bit with column transistor groups of DICE cells and the distances $D_{MIN\ 65\ nm} = 2.32$ nm and $D_{MIN\ 28\ nm} = 2.27$ nm: (a) memory array areas; (b) group and cell areas and areas per 1 bit; (c) switching delays; and (d) active power.

5. SIX-TRANSISTOR 28 nm CMOS MEMORY CELLS AND MEMORY ARRAYS

A DICE cell flip-flop is schematically shown in Fig. 10; in this figure, two transistor groups, four transistors each, and two connection lines between them are shown. These two transistor groups are the groups spatially separated from each other in different DICE cell topologies in order to increase noise immunity. If the two connection lines between two groups (see Fig. 10) are broken and these groups are connected pair-wise, we obtain two *D* flip-flops which are the basis of conventional static 6T CMOS memory cells. Taking into account that each flip-flop node of a DICE cell is connected to a transistor of the sampling (see Fig. 1), each transistor group of the DICE cell after closing the corresponding connections forms a 6T memory cell.

Figure 11 shows two variants of the relative position of two groups of flip-flop *N*MOS and *P*MOS transistors of one DICE cell forming basic elements of two CMOS 6T memory cells. Figure 11a shows two groups of flip-flop *N*MOS and *P*MOS transistors of two DICE cells containing four columns, two transistors each, which form a basic element with the capacity

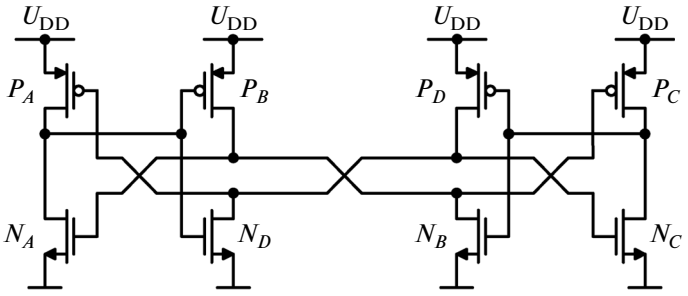

Fig. 10. DICE cell flip-flop circuit.

(a)

P_A	P_B	P_D	P_C
N_A	N_D	N_B	N_C

(b)

N_A	N_B
P_B	P_C
P_A	P_D
N_D	N_C

Fig. 11. Position of *N*MOS and *P*MOS transistors of two 6T memory cells in basic elements: (a) two columns per cell in 2 × 1 basic element; (b) in two groups (columns) of 1 × 2 basic element.

$m_A \times m_D = 2 \times 1$. The first two columns form one 6T cell, and the second two columns, the second 6T cell.

Two layouts of 6T cells with the relative transistor position shown in Fig. 11a are designed for minimizing the cell area: 6T-1 (*N*MOS channel width W_N = 170 nm) and 6T-2 (W_N = 350 nm); the parameters of these cells are given in Table 3. Figure 11b shows a layout of two groups (columns) of *N*MOS and *P*MOS transistors of a one DICE cell forming the basic element of two CMOS 6T cells with the capacity $m_A \times m_D = 1 \times 2$ consisting of two columns, four transistors each.

Table 3 gives the parameters of 6T CMOS memory cells: 6T-1 and 6T-2, with the transistors situated according to Fig. 11a and minimized areas, and 1D-1, 1D-2, and 2D-2 formed by the transistors of one group of 1DICE, 2DICE1, and 2DICE2 cells according to Fig. 11b.

The absence of connection lines between the columns in the basic element of the two 6T memory cells results in the lower metallization area; therefore, the basic element is not added by columns not containing transistors. For identical columns of the DICE cell of the basic DICE element and one 6T memory cell the transistor's packing density for a memory array based on 6T cells is the same as the transistor's packing density for DICE cells with the same size of the group of four transistors.

The time parameters of the 6T memory cell 2D-1 based on DICE group transistors with W_N = 170 nm are the same (with a difference of 13–16%) as those of

Table 3. Parameters of basic 6T memory elements and 28 nm CMOS RAM 32 × 64 bit memory arrays

Basic element	6T-1	6T-2	1D-1	2D-1	2D-2
Memory array	6T-1	6T-2	1D-1	2D-1	2D-2
Design rule	28 nm	28 nm	28 nm	28 nm	28 nmn
W_N, nm	170	350	350	170	350
W_P, nm	115	160	160	115	160
Group area $H_{GR} \times W_{GR}$, μm^2	1.015 × 0.52	1.24 × 0.52	2.63 × 0.26	2.06 × 0.325	2.51 × 0.325
S_{GR}, μm^2	0.5278	0.6448	0.6838	0.6695	0.8157
S_{CELL}, μm^2	0.5278	0.6448	0.6838	0.6695	0.8157
Number of cells in basic element	2	2	2	2	2
Capacity of basic element $m_A \times m_D$	2 × 1	2 × 1	1 × 2	1 × 2	1 × 2
$S_{B.E}$, μm^2	1.0556	1.2896	1.368	1.339	1.630
$H_{B.E} \times W_{B.E}$, μm^2	1.015 × 1.04	1.24 × 1.04	2.63 × 0.52	2.06 × 0.65	2.51 × 0.65
$S_{M.A}$, μm^2	1081	1321	1400	1371	1670
$H_{M.A} \times W_{M.A}$, μm^2	64.96 × 16.64	79.36 × 16.64	84.16 × 16.64	65.92 × 20.8	80.32 × 20.8
t_{DEL}, ps	101	76	75	117	94
$t_{1.0}$, ps	216	133	127	243	168
P_{ACTIVE} (writing), μW	97.2	110.4	135	106.7	150.7
P_{ACTIVE} (reading), μW	7.4	10.8	12.5	9.2	13.5

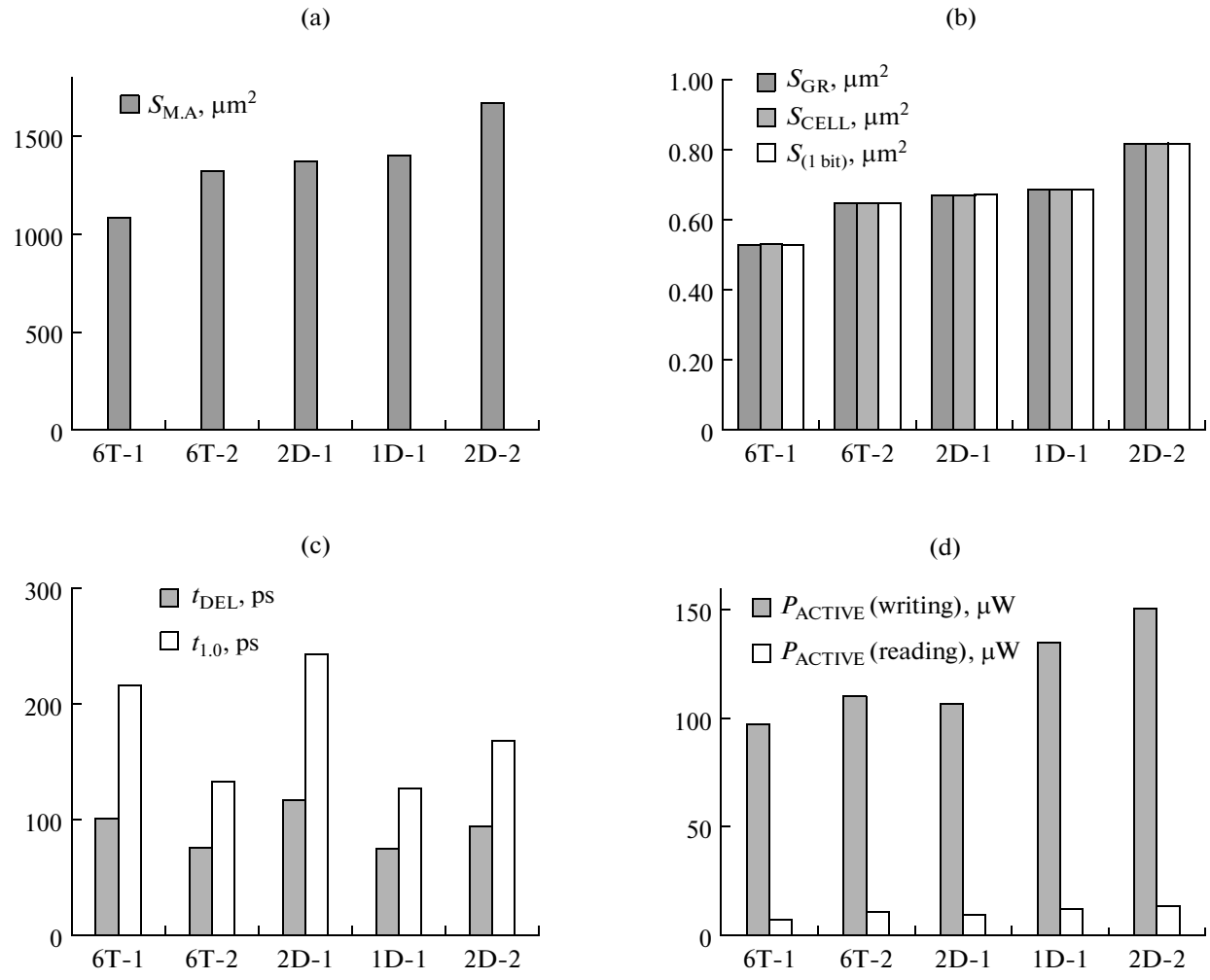

Fig. 12. Parameters of 6T memory cells and 6T 28 nm CMOS memory arrays RAM 32 × 64 bit: (a) memory array areas; (b) group and cell areas and areas per 1 bit; (c) switching delays; and (d) active power.

the 6T-1 cell, while the area of the 2D-1 cell is larger by 27%; the time parameters of the 6T memory cells 1D-1 and 2D-2 based on transistors of the DICE group with $W_N = 350$ nm are practically the same (with a difference less than 16%) as those of the 6T-2 cell, while the area of the 2D-1 cell is larger by 8%, and that of 2D-2 cell, by 28%.

Figure 12 shows the diagrams for comparing the parameters of the 28 nm CMOS 6T memory cells and the memory arrays (the parameters are given in Table 3). The diagrams in Fig. 12 show the parameters for 6T cells 6T-1 and 6T-2 with minimized areas with respect to one transistor group of the DICE cell. The parameters of three variants of the 6T memory cells based on the transistor group of the DICE cells are also shown. These cells are denoted as follows: 1D-1 is the memory cell based on a transistor group of DICE cell; while 2D-1 and 2D-2 are based on the transistor group of 2DICE1 and 2DICE2 cells.

6. COMPARISON OF THE PARAMETERS OF MEMORY CELLS, BASIC ELEMENTS, AND RAM MEMORY ARRAYS

Comparison of DICE Cell Memory Arrays

The areas of memory arrays of the same capacity change proportional to the areas of memory cells used in these arrays. The smallest area among DICE memory arrays (for a channel width of *N*MOS transistors $W_N = 350$ nm) is that of 1DICE (see Table 1). The minimum distance between the sensitive areas of transistors of the two groups of 1DICE cell is 2.27 μm, which is larger by a factor of 1.6 than that of 2DICE2 (1.4 μm), and the delay times of the signal propagation t_{DEL} and transition from state 1 to state 0 are smaller than those of the 1DICE unit. The 3DICE memory array ($W_N = 340$ nm), possessing the largest area, has also maximum distances of 3.24–4.7 μm between the sensitive areas of the two groups.

Thus, the 1DICE memory array has the maximum switching rate, minimum area, and sufficiently large distance $D_{MIN} = 2.27$ μm between sensitive areas. The 3DICE memory array ($W_N = 340$ nm) has the maximum area, lower switching rate, and maximum distances between sensitive areas of transistors, the characteristic distance $D_{MIN} = 3.24$ μm. The advantage of the 2DICE1 memory array is the smaller area (channel width of *N*MOS transistors $W_N = 170$ nm), while its switching rate is worse, and the distances between the sensitive areas of transistor pairs are smaller and the characteristic distance $D_{MIN} = 1.18$ μm.

Comparison of DICE and 6T Cells and the Memory Arrays Based on Them

The memory arrays 1DICE, 2DICE2, and arrays with 6T-2 cells based on transistors with the same size $W_N = 350$ nm and $W_P = 160$ nm have practically the same signal propagation delays in the range of 75–95 ps, while the area of 1DICE cells is larger by a factor of 2.12 and that of 2DICE2 cells is larger by a factor of 2.54 than that of 6T-2 cell with a minimum area of 0.645 μm^2. The corresponding memory array based on 1DICE cells has an area larger by a factor of 2.34, and that based on 2DICE2, by a factor of 2.58, than the area of the memory array based on 6T-2 cells.

The areas of basic memory elements and their constituent DICE cells (see Table 1) are limited by the minimum areas of the metallization layer of the element connections. These areas correspond to the maximum transistor size (channel width) given in Table 1. The reduction of the transistor size does not result in the reduction of the basic element area, and if the size is increased, as compared to the values given in Table 1, the areas of the DICE cells and the basic memory element also increase.

The time parameters of 6T memory cells 1D-1, 2D-1, and 2D-2 designed using the same transistor groups as the DICE cell are the same (within 5%) as the values of t_{DEL} and $t_{1.0}$ for the DICE cell.

The minimum distance between closed transistors for a 28 nm DICE flip-flop with LEAP linear transistor layout [12] is $D_{MIN} = 0.855$ μm for the same transistor size as that of 2DICE1 (in which $D_{MIN} = 1.18$ μm), and $D_{MIN} = 0.90$ μm for the same transistor size as that of 2DICE2 (in which $D_{MIN} = 1.4$ μm). The DICE cells with transistors separated into two groups and the linear topology considered above yield D_{MIN} that is better by 38–55%.

CONCLUSIONS

The layouts of basic memory elements with the different relative position of two transistor groups of 28 nm CMOS DICE cells were designed and the parameters of these layouts were analyzed. The minimum distances between the sensitive areas of transistors of the two groups of DICE cells in the basic memory elements of memory arrays amount to 2.27 μm (element 1DICE), 1.18 μm (element 2DICE1), and 3.24 μm (element 3DICE). The areas of DICE cells are larger by a factor of 2.1–2.5 than those of 6T cells with transistors of the same size.

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