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Evaluation of the temperature influence on SEU vulnerability of DICE and 6T-SRAM cells

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***Abstract*—In this paper, we evaluate the temperature influence on the vulnerability to single event upsets (SEU) of 6-transistor static random access memory (6T-SRAM) cells and dual interlocked storage cells (DICE). The critical charge (Q_{crit}, minimum charge capable of generating an SEU) is evaluated for 65nm, 45nm, 32nm and 22nm bulk CMOS technologies and temperatures between -50°C and 150°C. A double exponential signal is used to model the current pulse generated by ionizing particles. SPICE simulations have shown that Q_{crit} is sensibly reduced by the rise of temperature. Q_{crit} variations of up to 88.4% and 99.9% have been calculated for 6T-SRAM and DICE cells, respectively.**

Keywords—Reliability; SRAM; DICE; SEU; temperature; critical charge

I. INTRODUCTION

Static random-access memories (SRAM) are widely used in integrated circuit (IC) design due to their speed and compatibility with standard logic process. Technology scaling brought important SRAM cell size reductions and enabled the implementation of systems on a chip with larger cache memories. Unfortunately, the SRAM cell area and supply voltage need to be kept as low as possible in order to limit the leakage power consumption and improve the integration density. This cannot be done without affecting the SRAM vulnerability to hard and soft errors (SE).

A major cause of SE in SRAM cells, also known as single event upsets (SEU), is the ionizing radiation. The interaction of an ionizing particle with the semiconductor substrate can generate sufficient electrical charge to flip the logic state of an SRAM cell and produce an SEU. The minimum collected electrical charge that may result in an SEU is called critical charge (Q_{crit}) [1].

Special SRAM cell designs were proposed to increase Q_{crit} and, implicitly, improve the resilience to radiation induced SEU [2][3][4]. As compared to a conventional 6 transistors (6T) SRAM cell, the dual interlocked storage cell (DICE) relies on a double number of transistors and a special wiring with which a cell node cannot control more than one of the transistors that drive another cell node [2]. As a result, the state of a sensitive node can be regenerated once it has been flipped by a radiation-induced charge.

In this paper, SPICE simulations are used to assess the impact of the storage temperature on Q_{crit} of conventional 6T-SRAM and DICE designs for 65nm, 45nm, 32nm and 22nm technology nodes. This is an extension of other works devoted to the temperature impact on the soft error rate of conventional 6T-SRAM cells [5][6][7][8]. It is shown that Q_{crit} is sensibly reduced by the increase of the temperature and the considered SRAM designs become more vulnerable to SEU. Q_{crit} reductions of up to 88.4% and 99.9% have been estimated for 6T-SRAM and DICE cells, respectively.

The rest of the paper is organized as follows. Section II details the design of 6T-SRAM and DICE cells. Simulation setup and results are presented in sections III and IV. An analysis of the obtained results is given Section V. Conclusions are summarized in section VI and section VII details the future work.

II. 6T-SRAM CELLS AND DICE DESIGNS

In this section, we briefly describe the structures of the standard 6T-SRAM and the DICE cells. Their function and basic parameters are also introduced. For the purpose of the paper, these two structures have been implemented in a SPICE simulator as detailed below in the paper.

A. 6T-SRAM cells

The standard 6T-SRAM cell consists of a couple of cross-connected inverters and two NMOS access transistors, as depicted in the scheme of Fig. 1. In the scheme, four resistors are included in the two-inverters coupled-structure to simulate the internal resistance on VDD and GROUND nodes. Similarly, two capacitances are connected to the NMOS access transistors and represent bit lines (BIT and BITB) equivalent capacitances. The pair of inverters enables the storage of either logic '1' or logic '0', a single bit that is set through the voltage

difference forced on the bit lines couple, BIT and BITB, during the write access. The word line signal (WORD in the scheme) drives the two access transistors (NMOS Access 1 and NMOS Access 2) enabling the charge transfer between the cell nodes Q and QB, and BIT and BITB during write and read access cycles.

Our study analyzes the response of the cell to ionizing particles during retention mode. For this purpose, we chose to simulate the storage of logic '1': node Q is at '1' (VDD) and node QB at '0' (0V). We could have done it for logic '0' with similar results due to cell symmetry. WORD is at '0' (GROUND), forcing the access transistors OFF state (no access: retention mode). BIT and BITB are connected to VDD, which is the value commonly forced by the pre-charge circuit during retention mode.

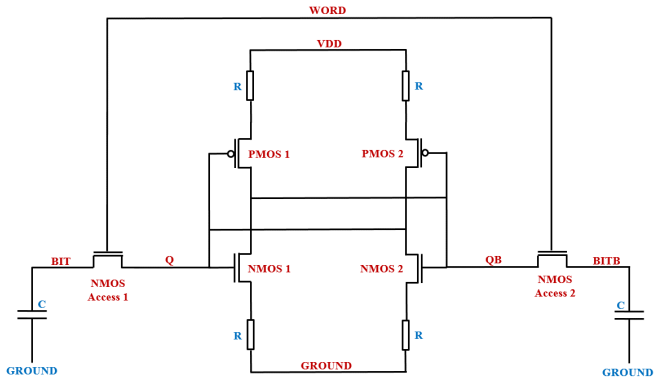

Fig. 1. Schematic of the 6T-SRAM cell used in simulations

The dimensioning of transistors is an important matter in 6T-SRAM cell design, since its stability and resilience to noise largely depends on it. The final dimensions of the transistors, especially in the two-inverter loop, is a trade-off among several requirements:

- The need of integration, which pushes in the direction of employing the minimum size allowed by the technology node;
- The need to ensure nominal symmetry, with equal strength of stored logic '1' and logic '0';
- Enhancement of resilience to electromagnetic interference (noise, particle impact, etc.);
- The cell must be sufficiently strong to be accessed during read operation without destroying its contents;
- The cell must not be too much strong in order to allow the changing of the stored value during write operation.

For our simulations, we followed these requirements to design 6T-SRAM cells with several technology nodes: 65nm, 45nm, 32nm and 22nm. SPICE models for bulk CMOS transistors from the predictive technology models (PTM) have been used in our simulations [9]. The supply voltages for the different technologies correspond to the PTM transistors predicted values [10]. They are depicted in Table. I.

TABLE I. SUPPLY VOLATGES FOR 6T-SRAM CELLS SIMULATIONS

Technology node (nm)	65	45	32	22
Supply voltage (V)	1	1	0.9	0.8

For each designed cell, the static noise margin (SNM) has been calculated in a large range of temperatures (from -50°C to +150°C). In retention mode, SNM is the maximum value of noise that can be tolerated by the cell without flipping the stored value [11][12].The SNM can be calculated through the *butterfly curve*, which is obtained by drawing the voltage transfer characteristics of the pair of inverters and mirroring one of them. SNM is the side length of the maximum square that can be fitted in both loops of the *butterfly curve* (Fig. 2). As we chose the same dimensions of NMOS and PMOS transistors in both inverters, the *butterfly curve* is symmetric and the maximum squares fitting in both loops are identical.

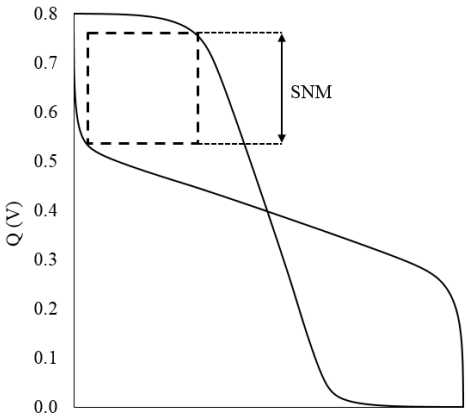

Fig. 2. *Butterfly curve* and SNM calculation for a 6T-SRAM cell

B. *DICE storage cell*

The DICE cell is used as storage CMOS cell with the feature of high resilience to upsets [3]. Its design is based on redundancy and feedback allowing the restoring of data in the case of a particle strike.

The redundancy introduced in the design provides a source of uncorrupted data after single-event strikes, since the uncorrupted section delivers the correct state restoring the feedback to recover the state of the affected node. This hardening feature of DICE cell is not dependent on optimal transistor sizing [3]. The DICE design has four nodes (X1, X2, X3 and X4, Fig. 3) that are set (for data storage) as two pairs of complementary logic states. During write/read operations, the complementary pairs are simultaneously accessed through four NMOS access transistors (N5-N6-N7-N8).

As for the standard 6Tcell, in this study, we implemented the DICE cell in 65nm, 45nm, 32nm and 22nm technology nodes for SPICE simulations using bulk CMOS transistors from the predictive technology models (PTM). The same supply voltages as for 6T-SRAM cells have been used for the DICE simulations. Since, as said above, DICE cell resilience performance is not dependent on optimal transistor sizing, we

used similar transistors sizes as in 6T-SRAM cells for the same technology nodes, in order to make a fair comparison between the two cells.

Differently from the 6T cell, we did not produce any butterfly plots or SNM calculations for the DICE cell in this paper.

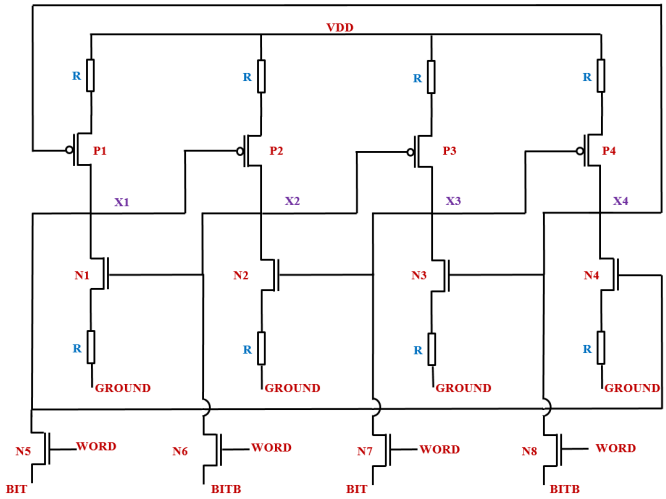

Fig. 3. Schematic of the DICE used in simulations

III. Simulation Setup

In both 6T-SRAM and DICE cells, the nodes connected to the drain of a NMOS or PMOS transistor in OFF state are sensitive to particle strikes. A particle strike results in a current pulse across the junction of such a transistor and the collected charge can flip the value of the cell. The amount of collected charge depends on the shape and duration of the current pulse produced by the particle strike.

In order to simulate the effect of a particle strike, a current source is added in parallel to the considered OFF-NMOS or OFF-PMOS transistor. Here, we chose to apply the current source on the OFF-NMOS transistors for both 6T-SRAM and DICE cells [5]. One common expression used to model the transient current generated by the SEU is the double exponential law that considers the drift and diffusion mechanisms in material [13][14][15]:

$$I(t) = \frac{Q}{t_f - t_r} \mathrm{x} \left(e^{-\frac{t}{t_f}} - e^{-\frac{t}{t_r}}\right) \quad (1)$$

where Q is the charge collected by the transistor drain and produced by the particle strike, t_f is the decay time of the current pulse and t_r is an initial time constant for particle track establishment. Q is the integral over time of the current pulse. The minimal Q that is able to flip a cell is referred to as critical charge Q_{crit}.

In our study, we chose fixed initial values for time constants t_f and t_r and also for the maximum current I_{max} that the current peak reaches during the transient. As explained in [13] and [17] and as we chose to have a decay time 50 times higher than the rise time ($t_f = 50\, t_r$), equation (1) can be written as follows:

$$I(t) = \alpha\, I_{max} \left(e^{-\frac{t}{t_f}} - e^{-\frac{50\,t}{t_f}}\right) \quad (2)$$

with α being a known constant resulting from the proportionality ratio existing between t_f and t_r.

As fixed initial values, we chose t_r to be equal to 10ps, t_f to be equal to 500ps and I_{max} to be equal to 100µA. These time constants and the current amplitude have been chosen in agreement with the values found in bibliography[14][15]. In fact, diffusion models and transient current pulses induced by ionizing particles have been studied to fix the initial chosen values of I_{max}, t_r and t_f for our simulations [13][17].

In order to evaluate Q_{crit} for the considered technology nodes and temperature range, the current pulse is modulated via a proportionality constant k that affects the time constants and the maximum amplitude as expressed in equation (3).

$$I(t) = \alpha\, k\, I_{max} \left(e^{-\frac{t}{k\,t_f}} - e^{-\frac{50\,t}{k\,t_f}}\right) \quad (3)$$

Consequently, the current pulse keeps the same shape as for the initial conditions but the induced charge is dependent on the constant k. The higher the value of k, the wider is the current pulse and consequently the corresponding maximum amplitude and induced electrical charge is higher. Fig. 4 depicts examples of applied current pulses.

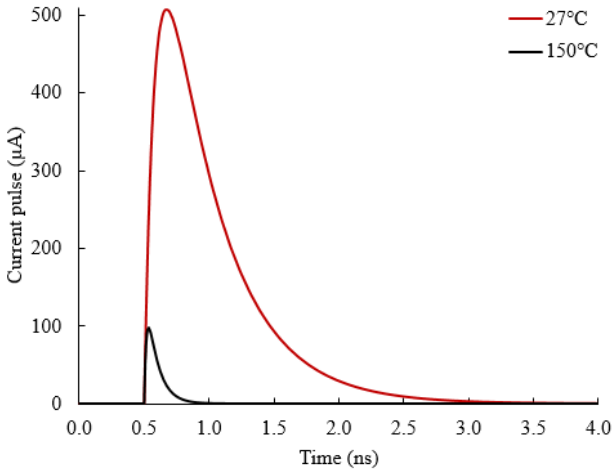

Fig. 4. Example of minimal current pulses able to flip a 32nm DICE

The calculation of Q_{crit} has been made for 6T-SRAM and DICE cells implemented in 65nm, 45nm, 32nm and 22nm technology nodes and storage temperatures between -50°C and 150°C.

IV. Results

A first set of simulations has been performed only on the 6T-SRAM cell, for the calculation of the SNM. For this purpose, the *butterfly curves* have been drawn by initially setting the cell node Q at '1' and the node QB at '0'. A voltage source simulates the effect of noise on nodes Q and QB alternatively. *Butterfly curves* are obtained by drawing Q

versus QB and QB versus Q simultaneously. SNM has been than calculated for the different technology nodes and temperatures, as shown in Table. II.

TABLE II. SNM EVOLUTION WITH TEMPERATURE FOR 6T-SRAM CELLS

Technology node	Temperature (°C)			
	-50	***27***	***90***	***150***
65nm	0.344	0.314	0.295	0.279
45nm	0.328	0.296	0.276	0.258
32nm	0.281	0.251	0.231	0.214
22nm	0.224	0.182	0.156	0.137

Concerning the study of Q_{crit}, of 6T-SRAM cells, the results are summarized by the graph in Fig. 5, which gives the evolution of the critical charge versus temperature for the considered technology nodes. Similarly, Fig. 6 summarizes Q_{crit} evolution for the DICE.

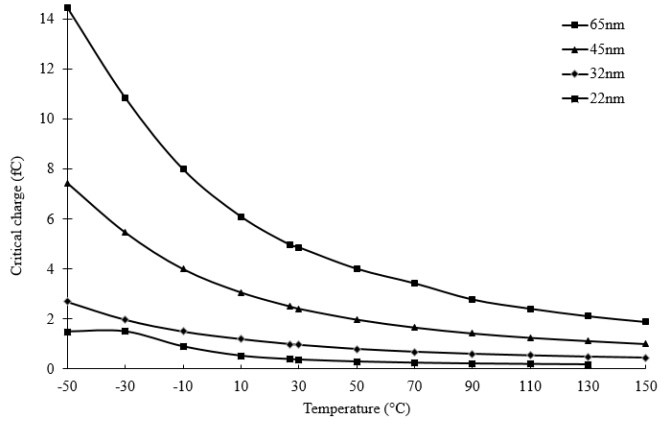

Fig. 5. Critical charge evolution with temperature for 6T-SRAM cells

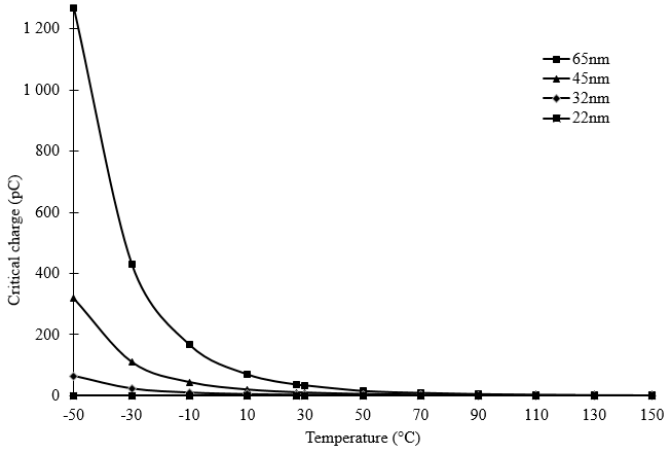

Fig. 6. Critical charge evolution with temperature for DICE cell

V. RESULTS ANALYSIS

A. 6T-SRAM cells

For the 6T-SRAM cell, Q_{crit} monotonically decreases with the increase of temperature and with the reduction of the technology node. The obtained results are consistent with the degradation some electrical parameters with increasing temperature. For example, the drain current of the transistors in ON state decreases with the temperature and it may be overcame by weaker current pulses in the OFF-state transistors that drive the same node. Concerning the technology node, using smaller transistor and wiring sizes reduces the value of critical charge, since the equivalent capacitances of the sensitive nodes are reduced.

Fig. 7 shows the ratio of Q_{crit} at -50°C, 90°C and 150°C with respect to Q_{crit} at 27°C. The maximum ratio is obtained at the minimum considered temperature for all technology nodes. Over the whole temperature range, Q_{crit} is increased by up to 88.4% as compared to its minimal value at 150°C.

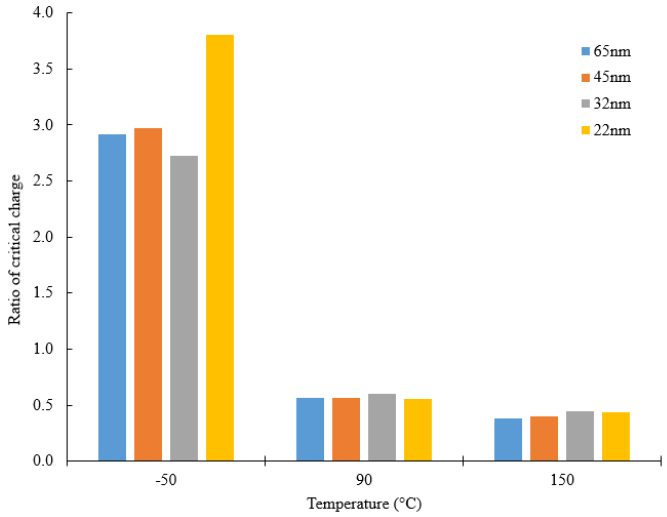

Fig. 7. Critical charge ratio compared to 27°C for 6T-SRAM cell

B. DICE cell

As for 6T-SRAM cells, Q_{crit} of DICE cells monotonically decreases with the temperature and technology node. Fig. 8 shows the ratio of Q_{crit} at -50°C, -10°C and 10°C with respect to Q_{crit} at 27°C. The maximum Q_{crit} is obtained at the minimum considered temperature and could reach 99.9% as compared to its minimal value at 150°C.

The order of magnitude of Q_{crit} for the different temperatures and technology nodes is consistent with the fact that DICE is more resilient to SEU than standard 6T-SRAM cells. For the considered temperature range, Q_{crit} of 6T-SRAM is between 0.17fC and 14.5fC while Q_{crit} of DICE is between 9.6fC and 1270pC. For the 65nm node at -50°C, the maximum Q_{crit} ratio between DICE and 6T-SRAM cells reaches a maximal value equal to 8.7×10^4. It is worth noting that Q_{crit} of the 22nm DICE cell at 130°C and 150°C has the same order of magnitude as Q_{crit} of the 6T-SRAM cell at -30°C and -50°C.

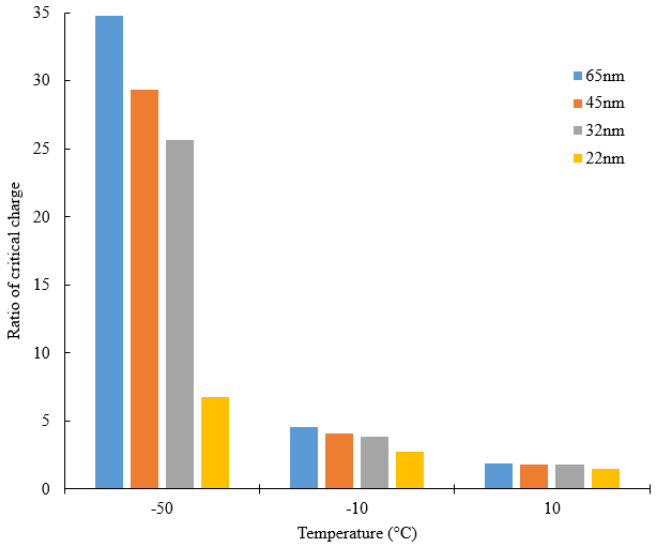

Fig. 8. Critical charge variations compared to 27°C for DICE

VI. Conclusion

In this paper, the influence of temperature along with the technology scaling on SEU vulnerability has been studied for standard 6T-SRAM and DICE cells. SPICE simulations for bulk CMOS 65nm, 45nm, 32nm and 22nm technology nodes for both types of cells allowed comparing the values of critical charge (Q_{crit}) for SEU triggering over a temperature range between -50°C and 150°C.

In the case of a 6T-SRAM cell, SNM calculation has been carried out to ensure the good dimensioning of the design. A double exponential model has been retained for the simulation of the current induced by ionizing particle strikes. Simulations showed that Q_{crit} is sensibly reduced by the rise of temperature and monotonically decreases with technology scaling. Over the whole temperature range, Q_{crit} variations of up to 88.4% and 99.9% have been simulated for 6T-SRAM and DICE cells, respectively.

VII. Future Work

This study will be complemented by the use of more accurate models for transient currents, e.g. on the base of Monte Carlo simulations. The consideration of a realistic population of ionizing particles, in order to extract the exact values of time constants t_r and t_f and maximum current I_{max} is therefore planned. Future work will also consider different operation conditions as supply voltage noise and process variations and their effect on critical charge values for the considered range of temperatures and technology nodes.

References

[1] R. Naseer, Y. Boulghassoul, J. Draper, S. DasGupta, and A. Witulski, "Critical charge characterization for soft error rate modeling in 90nm SRAM," IEEE Int. Symp. on Circuits and Systems, 2007, pp. 1879–1882

[2] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," IEEE Transactions on Nuclear Science, Dec-1996.

[3] M. Haghi and J. Draper, "The 90 nm Double-DICE storage element to reduce Single-Event upsets," IEEE International Midwest Symposium on Circuits and Systems, 2009, pp. 463–466.

[4] A. Maru, H. Shindou, T. Ebihara, A. Makihara, T. Hirao, and S. Kuboyama, "DICE-Based Flip-Flop With SET Pulse Discriminator on a 90 nm Bulk CMOS Process," IEEE Transactions on Nuclear Science, Dec. 2010.

[5] G. Tsiligiannis, I.E. Vatajelu, L. Dilillo, A. Bosio, S. Pravossoudovitch and A. Todri,, "SRAM soft error rate evaluation under atmospheric neutron radiation and PVT variations," IEEE 19th International On-Line Testing Symposium, 2013, pp. 145–150.

[6] D. Truyen, J. Boch, B. Sagnes, N. Renaud, E. Leduc and S. Arnal, "Temperature Effect on Heavy-Ion Induced Parasitic Current on SRAM by Device Simulation: Effect on SEU Sensitivity," IEEE Transactions on Nuclear Science, vol. 54, no. 4, pp. 1025–1029, Aug. 2007.

[7] E. Boufouss, J. Alvarado, and D. Flandre, "Compact modeling of the high temperature effect on the single event transient current generated by heavy ions in SOI 6T-SRAM," Addit. Pap. Present., vol. 2010, no. HITEC, pp. 77–82, 2010.

[8] G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, and A. Todri-Sanial, "Temperature impact on the neutron SER of a commercial 90nm SRAM," IEEE Nuclear and Space Radiation Effects Conference, 2013.

[9] "PTM - Latest models." [Online]. Available: http://ptm.asu.edu/latest.html.

[10] Y. Cao, "Predictive Technology Model of Conventional CMOS Devices," in Predictive Technology Model for Robust Nanoelectronic Design, Boston, MA: Springer US, 2011, pp. 7–23.

[11] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," IEEE J. Solid-State Circuits, vol. 22, no. 5, pp. 748–754, 1987.

[12] E.I Vatajelu, G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, and S. Pravossoudovitch, "On the correlation between Static Noise Margin and Soft Error Rate evaluated for a 40nm SRAM cell," IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2013.

[13] F. Wrobel, L. Dilillo, A. D. Touboul, V. Pouget, and F. Saigne, "Determining Realistic Parameters for the Double Exponential Law that Models Transient Current Pulses," IEEE Transactions on Nuclear Science, vol. 61, no. 4, pp. 1813–1818, Aug. 2014.

[14] B. Gill, M. Nicolaidis, F. Wolff, C. Papachristou, and S. Garverick, "An efficient BICS design for SEUs detection and correction in semiconductor memories," Proceedings of the conference on Design, Automation and Test in Europe-Volume 1, 2005, pp. 592–597.

[15] E. Dupont, M. Nicolaidis, and P. Rohr, "Embedded robustness IPs for transient-error-free ICs," IEEE Design & Test of Computers, 2002.

[16] T. Heijmen, D. Giot, and P. Roche, "Factors that impact the critical charge of memory elements," IEEE International On-Line Testing Symposium, 2006, p. 6–pp.

[17] F. Wrobel, L. Dilillo, A. D. Touboul, and F. Saigné, "Comparison of the transient current shapes obtained with the diffusion model and the double exponential law - Impact on the SER," IEEE Radiation and Its Effects on Components and Systems (RADECS), 2013, pp. 1–4.