

1、(10)

1-bit comparator – logic expression , draw the circuit and complete the time diagram

A	B	$F_{A<B}$	$F_{A=B}$	$F_{A>B}$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

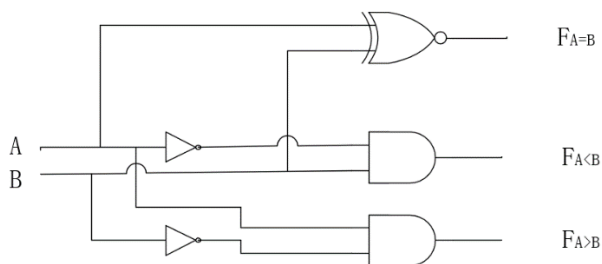
Expression:

$$F_{A=B} = \overline{A \oplus B}$$

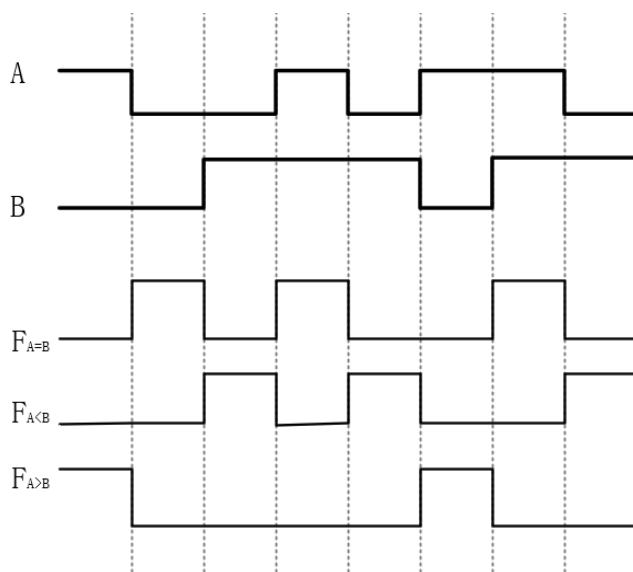
$$F_{A<B} = \overline{A} B$$

$$F_{A>B} = A \overline{B}$$

Circuit: (4p)



Time diagram: (6p)



2、 reduce the expression  $F(x, y, z, w) = \sum m(2, 4, 6, 8, 13, 14, 15) + \sum d(0, 7, 9, 10)$   
(6p)

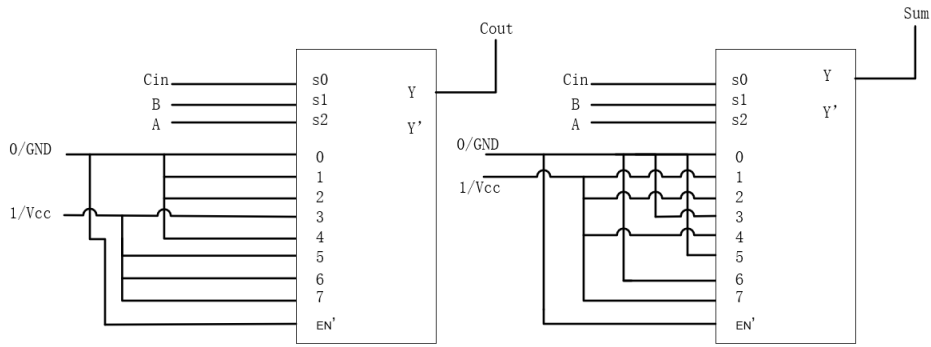
xy \ zw	00	01	11	10
00	d	1		1
01			1	d
11		d	1	
10	1	1	1	d

$$F = \bar{y}\bar{w} + \bar{x}\bar{w} + yz + x\bar{z}w \quad (4p)$$

3、 (15p) truth table of 1-bit full adder & implement it using 1-of-8 multiplexer

(8p)

A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



(7p)

4、  $f(a, b, c) = b\bar{c} + a\bar{b} + abc$

1)(10p) SOP and POS

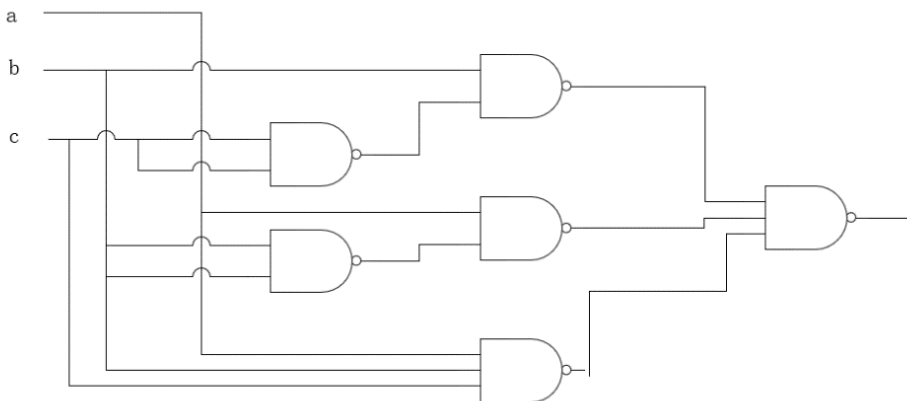
$$\Sigma m(2, 4, 5, 6, 7) = \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b}c + \bar{a}b\bar{c} + \bar{a}bc + abc \quad (5p)$$

$$\prod M(0, 1, 3) = (a + b + c)(a + b + \bar{c})(a + \bar{b} + \bar{c}) \quad (5p)$$

2) (10p)nand gates

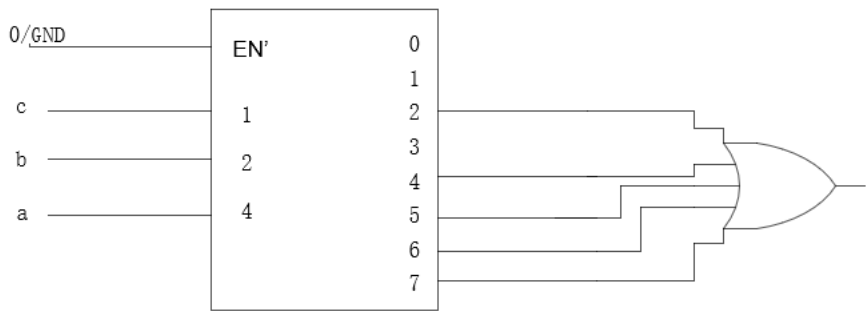
$$f(a, b, c) = \overline{\bar{b}\bar{c}} \cdot \overline{a\bar{b}} \cdot \overline{abc} \quad (5p)$$

(或者是  $\overline{\bar{a} \cdot \bar{b}\bar{c}}$  )



(5p)

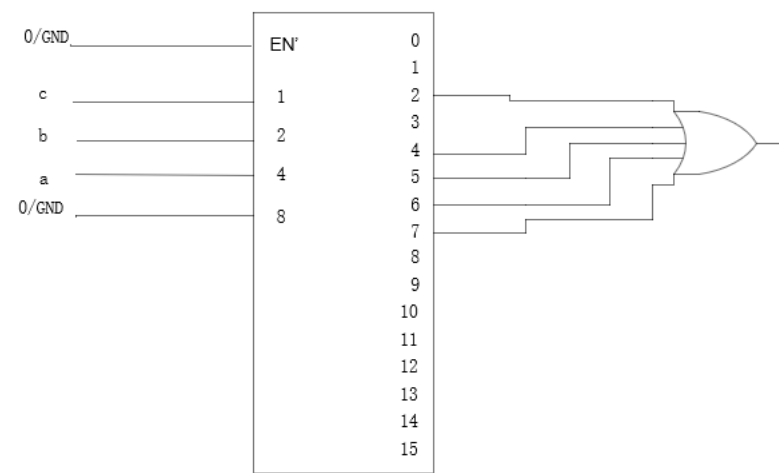
3) (15p) 3-line-to-8-line decoder



(使能信号可以是 CS1,CS2,CS3 的形式 (取 1, 0, 0) 等, 输出也可以采用低有效输出, 使用与门连接 0, 1, 3, 或者采用与非门连接 2, 4, 5, 6, 7)

4)(15p) 1-of-16 decoder (4-to-16 decoder)

与上一小问类似, 可以将最高位连接 1, 此时采用输出位 8-15, 若是低有效输出采用与门或者与非门连接, 或者将最高位接 0, 此时采用输出位 0-7, 高有效输出时采用或门, 低有效输出时与上面类似)



5)(15p)1-of-4 multiplexer

(4p)

ab \ c	00	01	11	10
0	0	1	1	1
1	0	0	1	1

降维(4p)

a \ b	0	1
0	0	1
1	C'	1

选择一个数据输入端作为信号输入，S1 连接 a,S0 连接 b,D0 接地，D1 接 c',D2 和 D3 接 Vcc (7p)

