四川大学平时测验试题（2018~2019 - 1）

学号： 姓名：

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1. A modulus-13 counter has 13 states requiring \_ \_ flip-flops. A modulus-13 ring counter requiring \_\_ \_\_\_ flip-flops.

2. Assume the clock for a 3-bit binary counter is 16MHz. The output frequency of the third stage (Q2) is ( )

a. 2MHz b. 128MHz c. 5.33MHz d. 48MHz

3. An asynchronous counter differs from a synchronous counter in ( ).

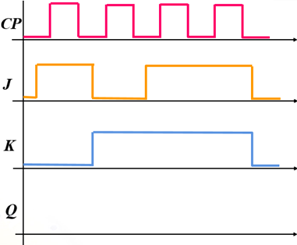
a. the number of states in its sequence. b. the method of clocking.

c. the type of flip-flops used. d. the value of the modulus.

4. A 4-bit binary up/down counters is in the binary state of 0111. The next state in the DOWN mode is

5. List the true tables and the characteristic equations of SR flip-flop, JK flip-flop and D flip-flop

6. In the figure for this problem, complete the timing diagram for a positive edge triggered J-Kflip-flop.



7. Given the logic diagram and CP for this problem, complete the Q0, Q1 and Q2 waveforms.

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8. Design a counter to produce the following binary sequence with J-K flip-flops: 1, 4, 3, 5, 7, 6, 2, 1,...

9. Construct a Mealy state diagram that will detect a serial input sequence of 01010