IBM z16
Performance, Stories, Facts, Evolution, and Good to Know

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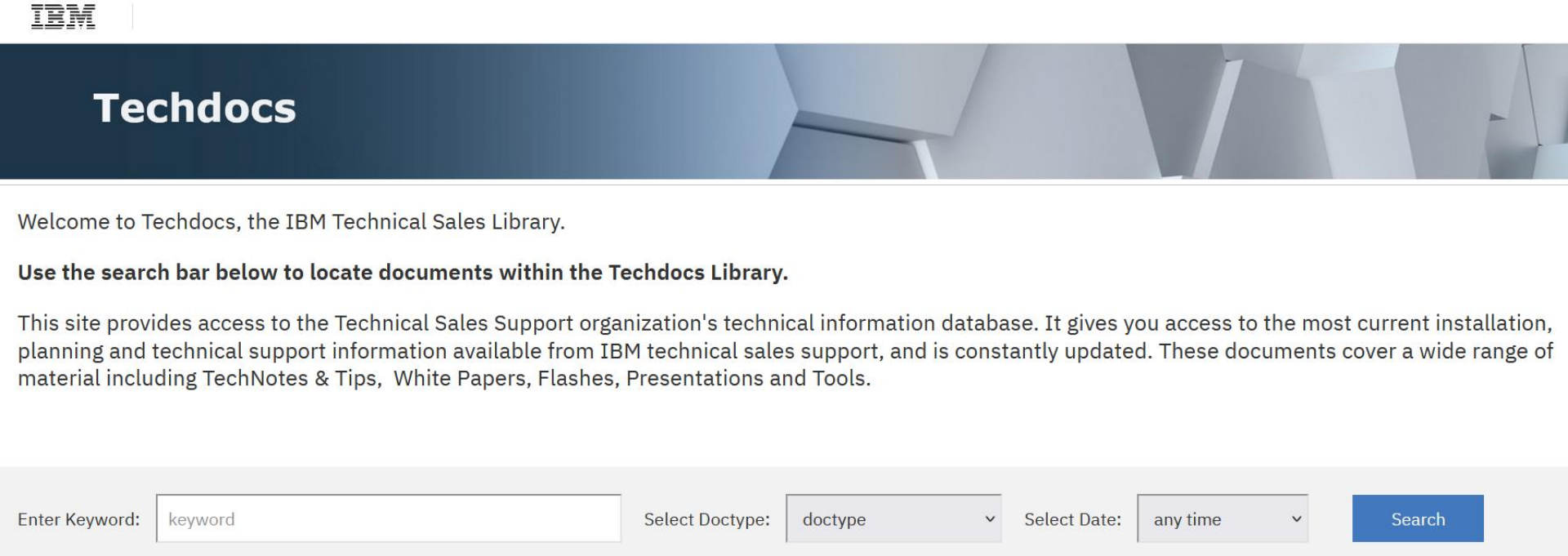
Agenda

- IBM z16™ Processor Information
  - Hardware Overview
  - Cache Topology / CPU MF Updates
  - New Flex Capacity and SRB Offerings
- IBM zPCR Tool Information
  - Large Partition support
  - HiperDispatch and Topology support
- CPACF and AIU Measurements
  - SMF 30 Count Information
  - AIU CPU MF / SMF 113 Usage information

Techdocs Updates

- https://www.ibm.com/support/pages/ibm-techdocs-technical-sales-library



IBM z16 – Built to Build the Future of Business

Up to 200 Cores

7nm technology, 5.2GHz, 1.5x Cache

11% per core performance improvement

17% total system capacity growth

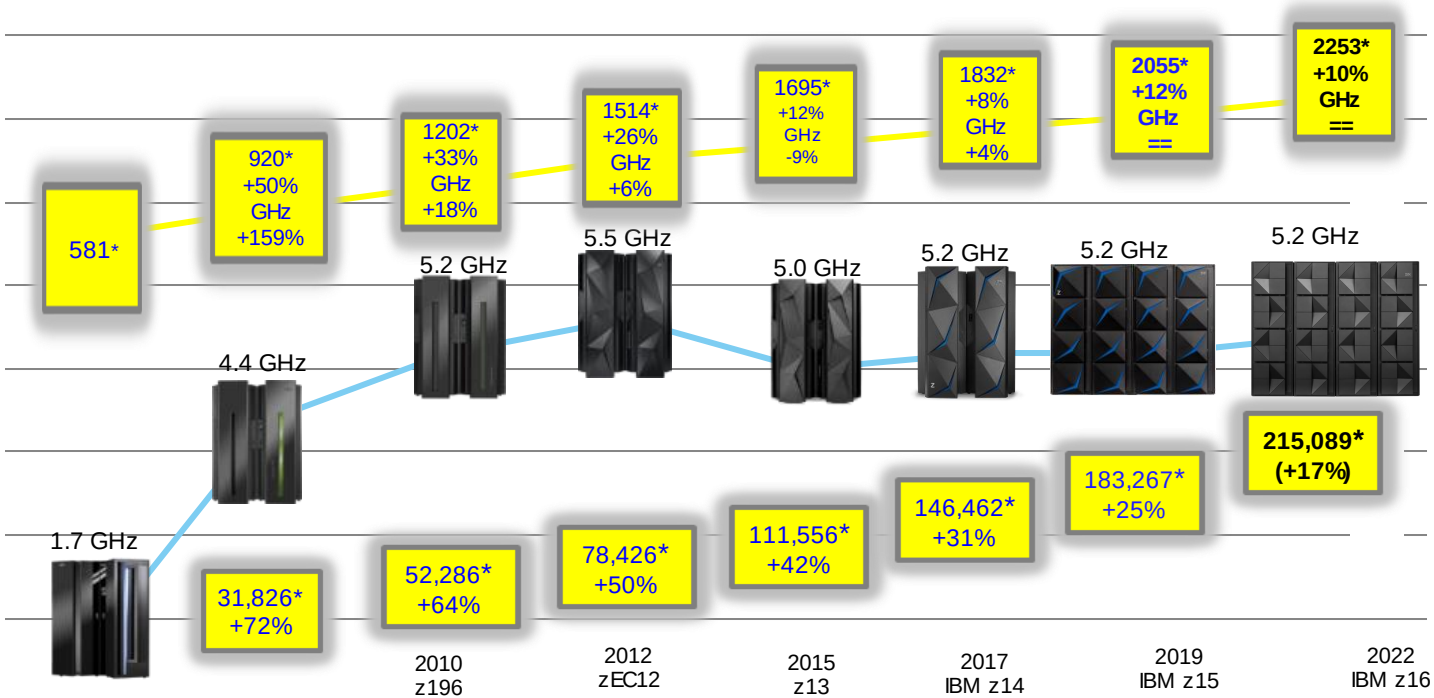
25% more processor capacity per drawer

Up to 40TB memory

1 to 4 19-inch frames

Up to 25 billion encrypted transactions per day [1]

IBM z16 Continues the CMOS Mainframe Heritage



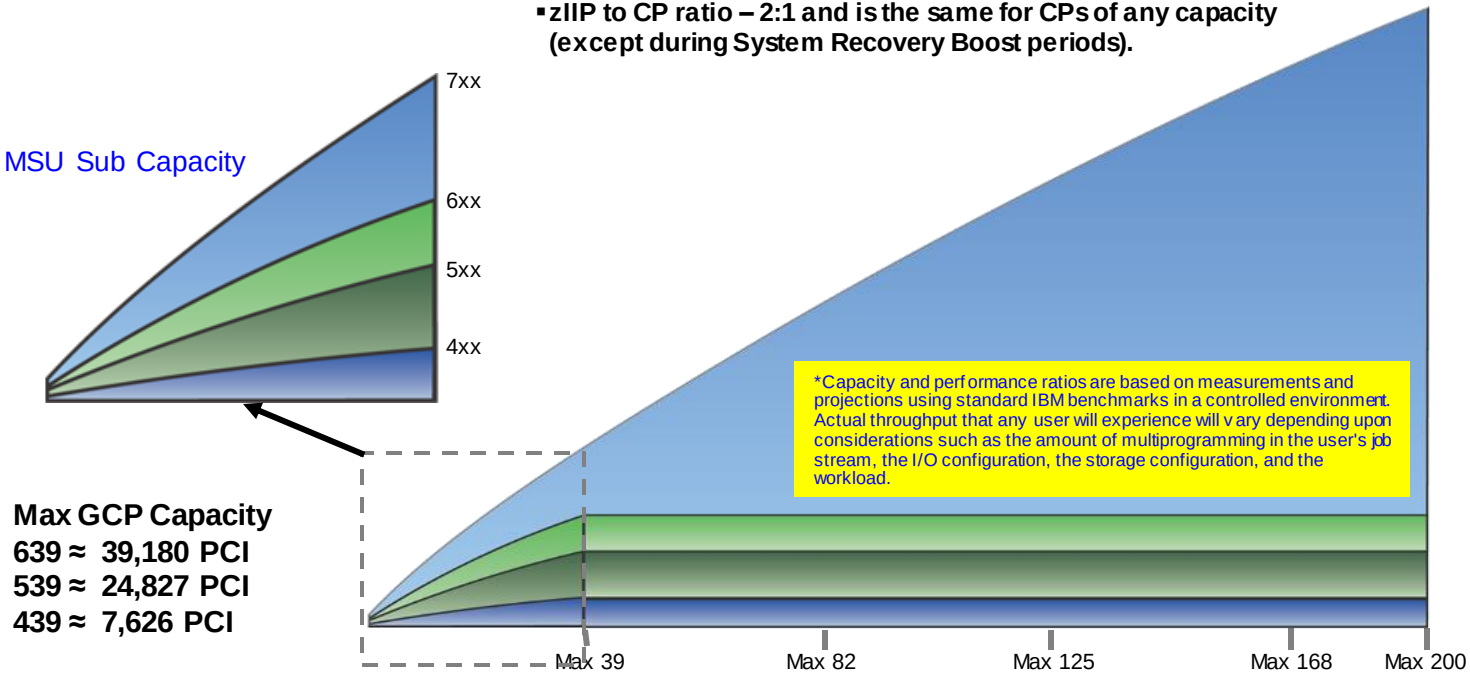
* PCI Tables are NOT adequate for making comparisons of IBM Z processors. Additional capacity planning required

** Number of PU cores for customer use

IBM z16 Full and Sub-Capacity CP Offerings

CP Capacity – Relative to Full Capacity Uni
701 = 100% ≈ 2,253 PCI
601 ≈ 66% ≈ 1,496 PCI
501 ≈ 41% ≈ 937 PCI
401 ≈ 12% ≈ 280 PCI

- **Subcapacity CPs, up to 39 may be ordered (317 total capacity levels). If more CPs are ordered, all must be full 7xx capacity.**
- **All CPs on an IBM z16 CPC must be the same capacity (except during Recovery Boost periods).**
- **All specialty engines are full capacity.**
- **zIIP to CP ratio – 2:1 and is the same for CPs of any capacity (except during System Recovery Boost periods).**



z16 Sub Capacity Ratios

- The IBM z16 Sub capacity models have different ratios than earlier models
- 6xx and 5xx models are closer in capacity to the 7xx model
  - More use cases for sub-capacity models

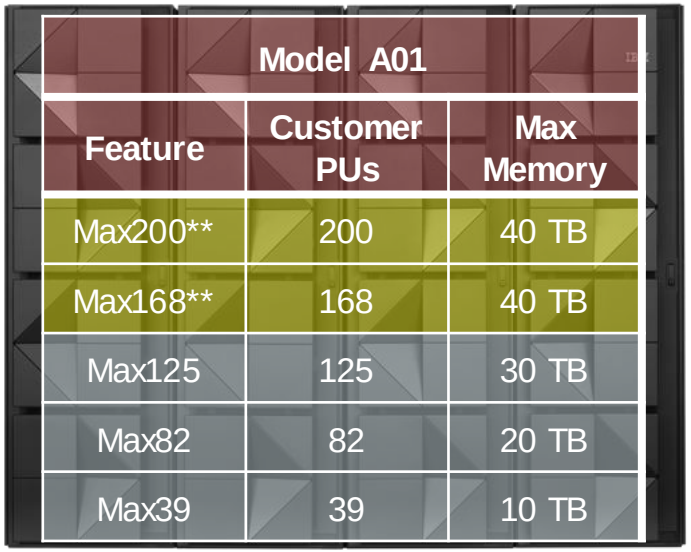
Capacity Ratios Relative to 7xx within family			
	z15		z16
401	0.13		0.12
501	0.38		0.41
601	0.56		0.66
701	1.00		1.00

z15 to z16 Sub Cap*	
z15 7xx to z16 6xx	0.73

*at equal n-way

IBM z16 At a Glance

IBM z16



Model A01		
Feature	**Customer PUs**	**Max Memory**
Max200**	200	40 TB
Max168**	168	40 TB
Max125	125	30 TB
Max82	82	20 TB
Max39	39	10 TB

** - NOTES: Max168 and Max200 are factory build only (no CPC Drawers field upgrades)

- Machine Type: **3931**
- One Model – **A01**
  - One, two, three, or four 19” Frames (A, B, C, IBM Z)
- Five features
- Max39, Max82, Max125, Max168** and Max200**
- Processor Units (PUs)
  - 48 (57 for Max200) PU cores per CPC drawer
  - Up to 24 standard SAPs per system (up to 8 optional additional SAPs)
  - 2 spares designated per system
    - 85 LPARs
  - Sub-capacity available for up to 39 CPs
- Memory
  - 6 x 2 x 8 channel Reed Solomon RAIM Memory design
  - System Minimum of 512 GB
  - Up to 10 TB per drawer
  - Up to 40 TB for System and up to 32 TB per LPAR (OS dependent)
  - Virtual Flash Memory
- I/O
  - Up to 48 PCIe+ Gen3 Fanouts -- 2 port @16GBps each and Integrated Coupling Adapters 2 port @ 8 GBps per system

Processor Unit (Core) Locations: Customer, SAP, IFP and Spare

IBM z16		1st Drawer				2nd Drawer				3rd Drawer				4th Drawer			
Feature	Cust PUs	Cust PUs	SAP	IFP	Spare	Cust PUs	SAP	IFP	Spare	Cust PUs	SAP	IFP	Spare	Cust PUs	SAP	IFP	Spare
Max200	200	47	6	2	2	51	6	0	0	51	6	0	0	51	6	0	0
Max168	168	39	5	2	2	43	5	0	0	43	5	0	0	43	5	0	0
Max125	125	39	5	2	2	43	5	0	0	43	5	0	0				
Max82	82	39	5	2	2	43	5	0	0								
Max39	39	39	5	2	2												

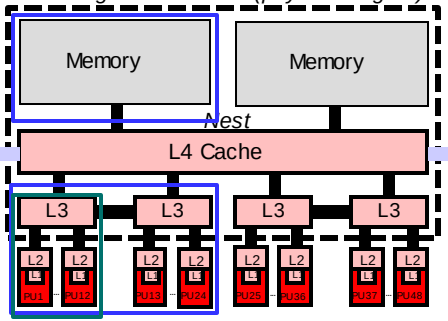
- PUs can be purchased as CPs, IFLs, Unassigned IFLs, zIIPs, ICFs or Additional SAPs
  - zIIP to CP purchase ratio is 2:1
  - Additional SAPs + Permanent SAPs may not exceed 32
  - Any un-configured PU can act as an additional Spare PU
  - CPs and zIIPs initial placement in 1st drawer working up
  - IFLs and ICFs initial placement in highest order drawer working down
- Upgrades available from any lower feature to any higher any models
  - Achieved via Concurrent Drawer Add from Max39 to Max125
  - Upgrade to Max168 and Max200 from any other feature not supported. Max168 and Max200 are factory built only.

z16 vs z15 Hardware and Topology Comparison

z15 CPU 5.2 GHz
Caches L1 private 128k i, 128k d / core
L2 private 4 MB i, 4 MB d / core
L3 shared 256 MB / CP chip
L4 shared 960 MB / drawer

Topology
- 12 cores + 1 L3 / CP chip
- 2 CP chips / cluster
- 2 clusters + 1 L4 (48 engines) / drawer
- 5 drawers / CEC
- Drawer interconnect: NUMA star

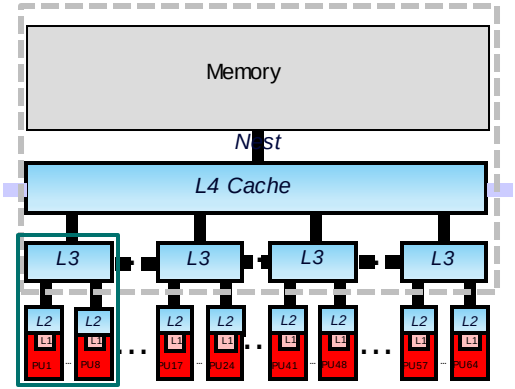
z15 Single Drawer View (physical+logical)



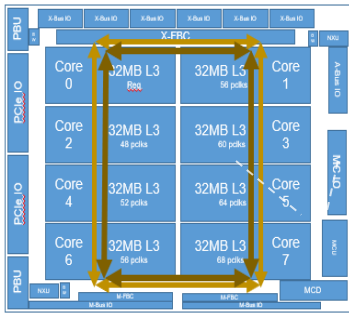
z16 CPU 5.2 GHz
Caches L1 private 128k i, 128k d / core
L2 *private* 32 MB unified / core
virtual victim L3 up to 7x32 = 224 MB / CP chip
virtual victim L4 up to 8x32x7 = 1.75 GB / drawer

Topology
- 8 (core + L3)s / CP chip
- 2 CP chips / DCM
- 4 DCMs (64 engines) / drawer
- 4 drawers / CEC
- Drawer interconnect: NUMA star

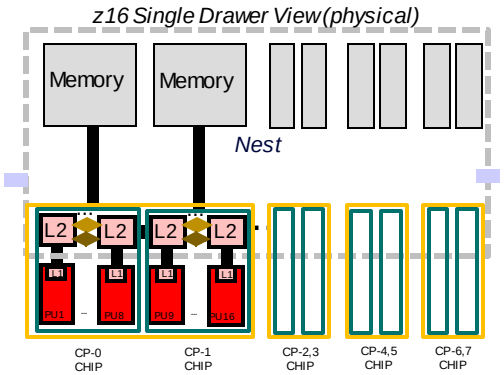
z16 Single Drawer View (logical)



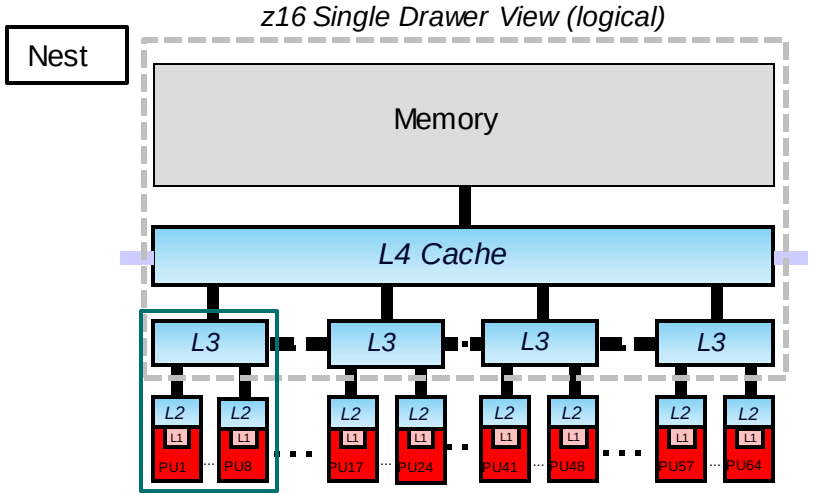
z16 Single CP Chip View (physical)



z16 Single Drawer View (physical)



CPU MF Instrumentation – SMF 113 Records



SMF 113 records introduced with the
IBM System z10 server on February 26, 2008.
The IBM Best Practice based on z10 lessons learned is to enable the
SMF 113 records with **CTR=ALL**
on ALL z/OS LPARs

Looking for z16 Migration "Volunteers" SMF data

- Want to validate / refine Workload selection metrics

Looking for "Volunteers"

(3 days, 24 hours/day, SMF 70s, 71s, 72s, 99 subtype 14s,113s per LPAR)

Before z14 / z15" and "After z16"

Production partitions preferred

If interested send note to **stephanie.deluca@ibm.com**

No deliverable will be returned

Benefit: Opportunity to ensure your data is used to influence analysis

- Implementation Instructions
  - https://www.ibm.com/support/pages/cpu-mf-2022-update-and-wsc-experiences

CPU MF SIIS Information

- CPU MF can be used to help identify potential SIIS timeframes
  - Based on % of certain I Writes / D Writes sourced
  - LPAR view, identifies when it happens, not who is causing it
    - Identify the program(s) running in the time period, e.g. via zBNA Top Programs
    - Use a hot spot analyzer to find the issue
    - Remediate the source code to correct the issue
- White paper - http://www.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/WP102806

Processor	SIIS Indicator %	Description
zEC12 / zBC12	E130 / B4 * 100%	D Writes sourced with L2 intervention / D Writes
z13 / z13s	E163 / B2 * 100%	I Writes sourced with L3 intervention / I Writes
z14 / ZR1	E164 / B2 * 100%	I Writes sourced with L3 intervention / I Writes
z15	E164 / B2 * 100%	I Writes sourced with L3 intervention / I Writes
z16	E170 / B2 * 100%	I Writes sourced with L2 intervention / I Writes

IBM Z Flexible Capacity for Cyber Resiliency

On demand, automatable transfer of capacity between IBM z16 machines

Greater Flexibility

Dynamically shift production capacity cross sites between IBM z16 machines

Flexibility and elasticity for DR test, planned maintenance, proactive outage avoidance and actual DR scenarios

Works in conjunction with other temporary record types, e.g., On/Off Capacity On Demand, Tailor Fit Pricing for Hardware, etc.

Complete Customer Control

Remotely transfer capacity – no on-site personnel (IBM or customer) required after initial set up

Flexible duration of capacity transfer, up to 1 year

Fully automated using solutions such as GDPS

Improved Compliance for Disaster Recovery

Simplify compliance and improve confidence DR scenarios including test

Closer mapping between test and production scenarios

No need for CBU records using this solution

System Recovery Boost Options – z16 Enhancements

1	**Customer-Identified Middleware Region start/restart Boost (5 minute boost)** Boost the z/OS system on which an STC middleware instance is being started/restarted
2	**SVC Dump Boost (2 minute boost)** Boost System on which an SVC Dump is being taken CHNGDUMP, DISPLAY DUMP,INFO and DISPLAY DUMP,OPTIONS enhancements
3	**Hyperswap configuration Load Boost (2 minute boost)** Boost load/re-load processing for making changes to z/OS Hyperswap policy/configuration

- The new boost use cases share the existing recovery process boost time pool of 30 minutes per LPAR per day (in aggregate) with the earlier z15 use cases

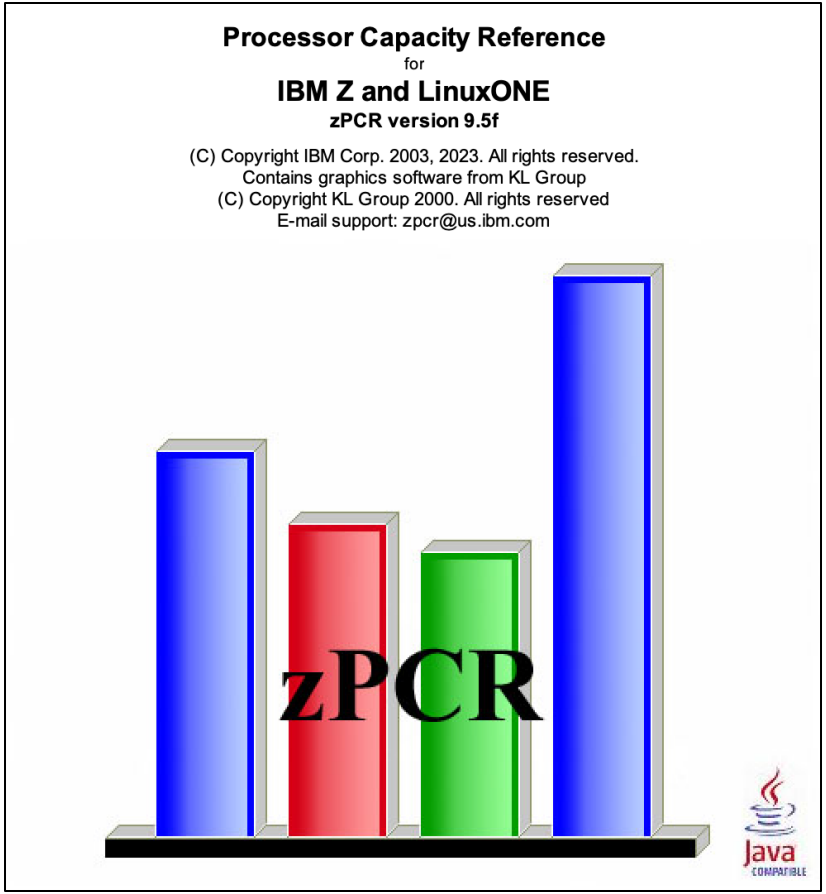
zPCR Support for z16

IBM Clients

- Obtain zPCR at: http://www.ibm.com/support/pages/node/6354029
- Obtain zBNA at: https://www.ibm.com/support/pages/node/6354321

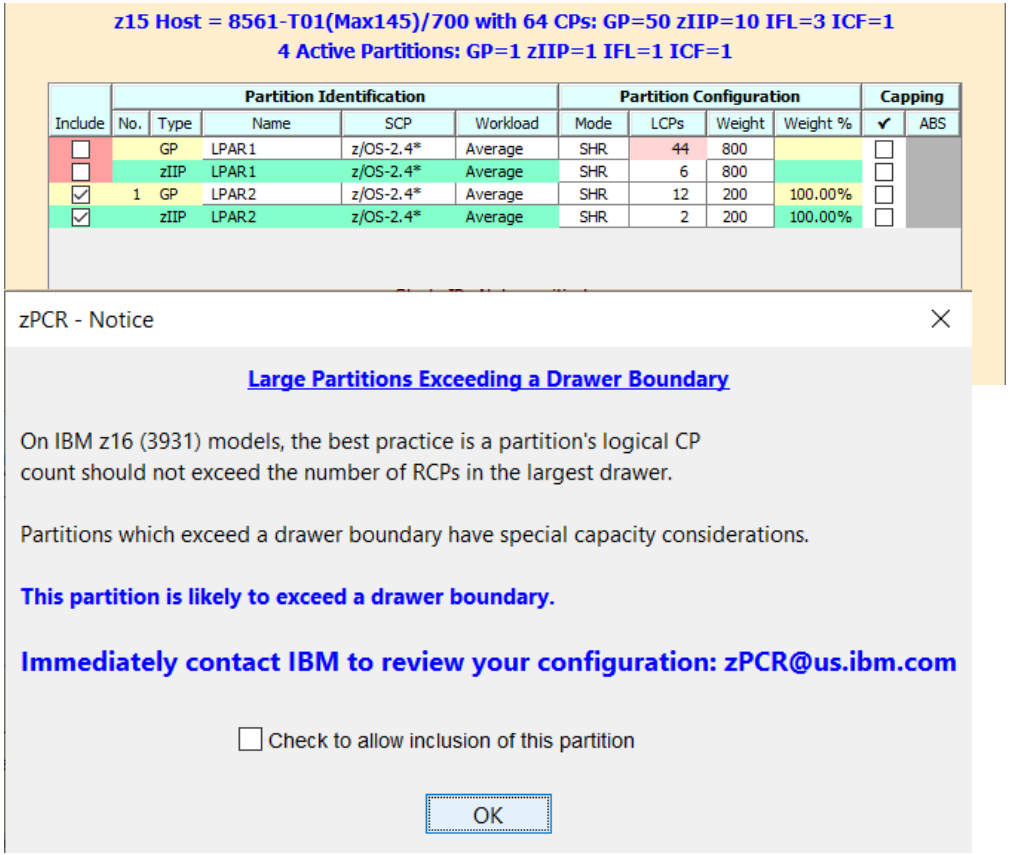
IBM Authorized Business Partners

- Site is being migrated to IBM Partner Plus
- Until available, contact cpstools@us.ibm.com for download and support



zPCR Large Partition Support

- There can be negative impacts on a partition's performance when CPs are in different drawers
  - PR/SM will attempt to put all VH and VM CPs for a partition on the same drawer
- zPCR will warn you when LCPs defined are larger than a drawer



Value of Adding One LPAR

Configuration change modeled:

1. Running two 38-way LPARs with 13 zIIPs changed to
2. Running 2 LPARs with 28-way LPAR with 8 zIIPs and 1 20-way LPAR with 9 zIIPs

Value of Parallel Sysplex with True Data Sharing

LPAR Host Capacity Comparison Report

Capacity by Partition Type

More LPAR Config: Cloned from Base Config

Capacity basis: 2094-701 @ 593.00 MIPS for a shared single-partition configuration

Capacity for z/OS on z10 and later processors is represented with HiperDispatch turned ON

Partition Type	#1 Base Config 8561-T01(Max145)/700: GP=75 zIIP=25					#2 More LPAR Config 8561-T01(Max145)/700: GP=75 zIIP=25					Capacity Net Change	
	# of LPs	Usable RCPs	Active LCPs	SHR LCP:RCP	Full Capacity	# of LPs	Usable RCPs	Active LCPs	SHR LCP:RCP	Full Capacity	MIPS	% Delta
GP	2	75	76	1.013	77,432	3	75	76	1.013	92,775	+15,343	+19.8%
zAAP	0	0	0			0	0	0				
zIIP	2	25	26	1.040	24,889	3	25	25	1.000	29,885	+4,996	+20.1%
IFL	0	0	0			0	0	0				
ICF	0	0	0			0	0	0				
Total	4	100	102		102,321	6	100	101		122,660	+20,339	+19.9%

Comparison Report by Partition: Minimum Capacity | Maximum Capacity

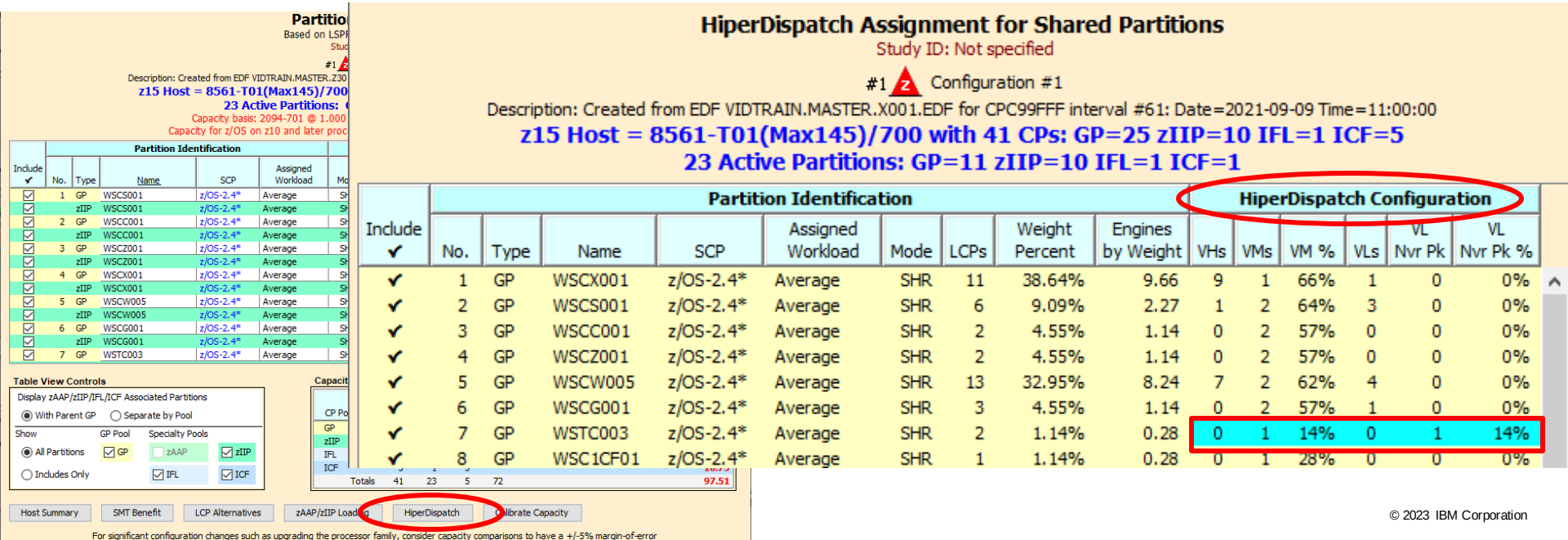
Show capacity as: (•) Full CPC ( ) Single-CP

Consider Margin-of-Error

For significant configuration changes such as upgrading the processor family, consider capacity comparisons to have a +/-5% margin-of-error

zPCR HiperDispatch Window

- Dynamically shows VH/VM/VL CPs for each partition based on weights of all partitions
- Small partitions with share of < 1 CP but with 2 or more CPs will have 1 VM and 1 VL never parked, noted in the tool



HiperDispatch Assignment for Shared Partitions

Study ID: Not specified

#1 Configuration #1

Description: Created from EDF VIDTRAIN.MASTER.X001.EDF for CPC99FFF interval #61: Date=2021-09-09 Time=11:00:00

z15 Host = 8561-T01(Max145)/700 with 41 CPs: GP=25 zIIP=10 IFL=1 ICF=5

23 Active Partitions: GP=11 zIIP=10 IFL=1 ICF=1

Include ✓	Partition Identification								HiperDispatch Configuration					
	No.	Type	Name	SCP	Assigned Workload	Mode	LCPs	Weight Percent	Engines by Weight	VHs	VMs	VM %	VLs	VL Nvr Pk	VL Nvr Pk %
✓	1	GP	WSCX001	z/OS-2.4*	Average	SHR	11	38.64%	9.66	9	1	66%	1	0	0%
✓	2	GP	WSCS001	z/OS-2.4*	Average	SHR	6	9.09%	2.27	1	2	64%	3	0	0%
✓	3	GP	WSCC001	z/OS-2.4*	Average	SHR	2	4.55%	1.14	0	2	57%	0	0	0%
✓	4	GP	WSCZ001	z/OS-2.4*	Average	SHR	2	4.55%	1.14	0	2	57%	0	0	0%
✓	5	GP	WSCW005	z/OS-2.4*	Average	SHR	13	32.95%	8.24	7	2	62%	4	0	0%
✓	6	GP	WSCG001	z/OS-2.4*	Average	SHR	3	4.55%	1.14	0	2	57%	1	0	0%
✓	7	GP	WSTC003	z/OS-2.4*	Average	SHR	2	1.14%	0.28	0	1	14%	0	1	14%
✓	8	GP	WSC1CF01	z/OS-2.4*	Average	SHR	1	1.14%	0.28	0	1	28%	0	0	0%

New z16 Processor Topology Support

- Beneficial to know where logical CPs are for each partition
  - –New support in z16 puts information in RMF 70 records
    - Get data from all LPAR types
    - Written every interval, with change indicator
  - –On z15 and earlier processors can only get information via HMC (z14 and later), LPAR dump or SMF 99(14) records
    - https://www.ibm.com/support/pages/system/files/inline-files/IBM_Z-_Accessing_the_LPAR_Resource_Assignment_Task.pdf
- Support
  - –z/OS new Data Gatherer functionality is delivered with APAR OA62064
    - PTFs are available for z/OS V2.5, V2.4, and V2.3.
  - –z/VM support is provided via APARs for z/VM 7.1 and z/VM 7.2
    - Built into base of z/VM 7.3

zPCR NEW Topology Window

- Takes advantage of new data in RMF 70 record
- Latest Versions of CPSTools extract required
  - –z/OS
    - https://www.ibm.com/support/pages/zos-data-extraction-program-cp3kextr-zpcr-and-zbna
  - –z/VM
    - https://www.ibm.com/support/pages/cp3kvmxt-vm-extract-utility-zcp3000-and-zpcr-capacity-planning-support-tools
- Accessed via the Partition Detail Window
  - – Shows current, not updated with configuration changes

Topology

Study ID: Not specified

#1 Configuration #1

Description: Created from EDF z16 Example.edf for CPC5D6D8 interval #4: Date=2022-01-14 Time=12:15:00

z16 Host = 3931-A01(Max168)/700 with 168 CPs: GP=82 zIIP=2 IFL=82 ICF=2

17 Active Partitions: GP=8 zIIP=1 IFL=6 ICF=2

Note: Topology configuration changed during the measurement interval.

ID			Drawer 1							Drawer 2						Drawer 3				Drawer 4				
			DCM 1		DCM 2		DCM 3		DCM 4	DCM 1		DCM 2		DCM 1	DCM 2	DCM 3		DCM 4		DCM 1		DCM 2		DC
No.	Name	Type	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1	Chip 2	Chip 1
1	AST1	GP					(1)L	(4)H (2)M (1)L																
2	ACPX2	GP	(4)H (2)M	(8)L	(4)L	(2)L																		
	ACPX2	IFL																(7)H (1)M	(2)H (4)L	(1)M (2)L	(2)L			
	ACPX2	ICF																						
3	ACT1	GP			(4)H (2)M (2)L	(2)L																		

IBM z16 ...
CPACF Usage Tracking

Deliver a new hardware managed counter set to track crypto algorithms, bit lengths and key security (e.g., AES 256 encrypted).

Provides evidence for:

- Compliance (i.e., which crypto is used)
- Performance (i.e., frequency of crypto use)
- Configuration (i.e., proof of change)

For z/OS, the counters could be:

- Synchronized with the SMF recording interval
- Stored in new triplet section of existing SMF Type 30 records
- Configured system wide (i.e., IEASYSxx)

Available to all IBM Z operating systems

New and/or enhanced audit logs containing CPACF counter values

Correlated with the workload that invoked the CPACF function (e.g. PCI workload)

Enhanced SMF Type 30 Records

- Include new crypto counter sections that contain counters for CPACF cryptographic instructions utilized by a job in a given period. These sections are produced only for those instructions that are used.
- These counters are correlated with z/OS jobs and users for the determination of the algorithms, bit lengths, and key security utilized by a given workload.
- This data can aid in compliance, performance, and configuration.
- Support
- For z/OS - APAR OA61511 and OA61395 to gather data in SMF 30 records
- PTFs are available for z/OS V2.5 and V2.4

SMF 30 Crypto Example

- z16 simple IFASMFDP step
  - Encrypting output data set
  - Results in CPACF Counts for algorithms

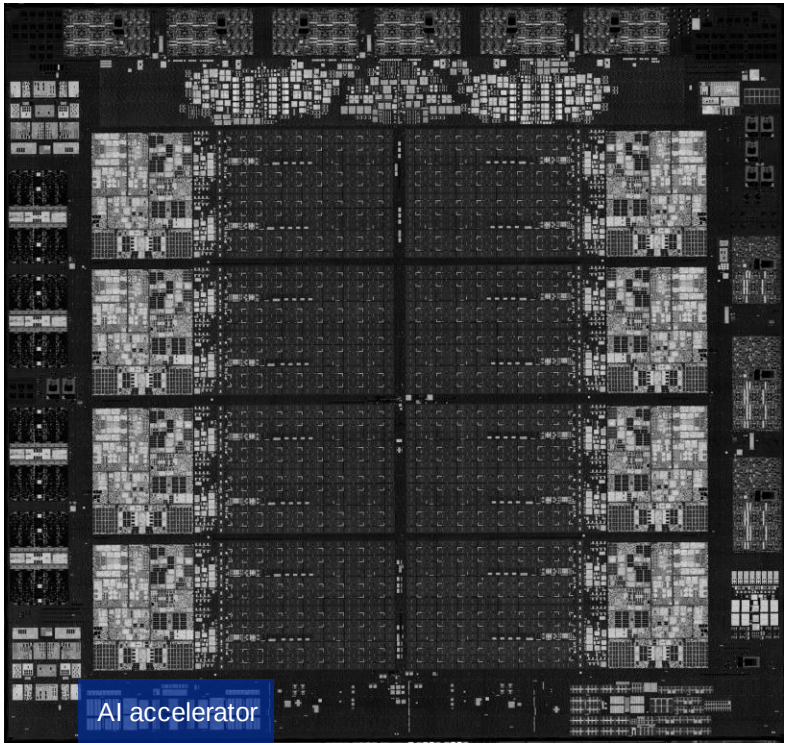
```
//STEP8    EXEC PGM=IFASMFDP
//*
//* CREATES EF ENCRYPTED DATA SET PHYSICAL SEQ DATA SET
-  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  1 Line(s
//*
//INDD1    DD  DSN=JPBURG.WSCSYSD.SMF.SYSD.SEP1417.T03,DI
-  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  4 Line(s
//OUTDD1   DD  DSN=JPBURG.WSCSYSD.SMF.SYSD.T03.EFEN2,DISP
-  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -_ 1 Line(s
//           DATACLAS=DSENCS,
//           STORCLAS=ATSCTS,
//           DSKEYLBL='SAMPLE.SECRET.AES256.KEY001',
```

```
Subtype Record 4
SMF ID SYSD Work Type JES2 Ho Min Sec 091237  Year Mon Day 20220415
Usage Offset 0 Length 76 Number 0
zEDC Offset 1375 Length 64 Number 0
z16 Crypto Offset 1525 Length 10 Number 2  Num Sections in Addl Records 0  Yes Crypto Counters
Crypto Counters - Entry Id:  16 Count Value: 73395 Description: KM-XTS-Encrypted-AES-256 function ending w cc=0
Crypto Counters - Entry Id:  118 Count Value: 24477 Description: PCC-Compute-XTS-Parameter-Using-Encrypted-,
             AES-256 function ending with CC=0
z16 NNPI (AI) Offset 1519 Length 10 Number 0  Num Sections in Addl Records 0   No AIU Counters
TYP   PFlags   RV  4    96   05
Job Step Program JPBURGE8 STEP8    IFASMFDP
EXCPs 49001 SSCHs 17205
CPU Time and SRB Time in Seconds 0.18   0.13
Highest task % and Program Name 0 IEFIIC
Tot, TCB, SRB and I/O Ser Units 34333 17177 12252 4904
Total Instructions 689240763  Instruction Flags (0 is normal) = 0
TCB and SRB Time in Microseconds 183579.1875   130943.25  CPI  2.372
```

IBM z16 Integrated Accelerator for AI

Centralized On-chip accelerator shared by all cores

- Very low and consistent inference latency
- Compute capacity for utilization at scale
- Variety of AI models ranging from traditional ML to RNNs and CNNs
- Security – provide enterprise-grade memory virtualization and protection
- Extensibility with future firmware and hardware updates

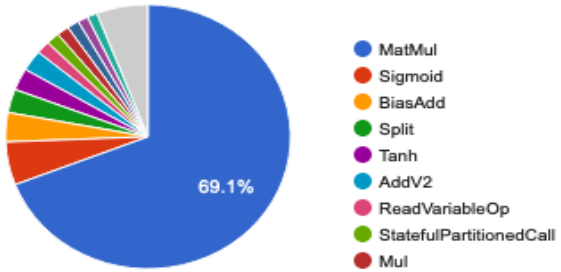


*CPU MF must be enabled to see performance metrics

AI Accelerator

- More than just matrix multiplication!

- AI Functions/Macros abstracted via NNPA instruction
  - Elementwise, Activation
  - Normalization, Pooling
  - Matrix-multiplication
  - Convolution
  - Conv+Scale+Activate
  - MatMul+Compare/Activate
  - RNN activation



RNN model

Function group	#	Function support in GA1
Elementwise ops	0x10	NNPA_EL_ADD
	0x11	NNPA_EL_SUB
	0x12	NNPA_EL_MUL
	0x13	NNPA_EL_DIV
	0x14	NNPA_EL_MIN
	0x15	NNPA_EL_MAX
Activation ops	0x20	NNPA_LOG
	0x21	NNPA_EXP
	0x31	NNPA_RELU
	0x32	NNPA_TANH
	0x33	NNPA_SIGMOID
Norm op.	0x34	NNPA_SOFTMAX
	0x40	NNPA_BATCHNORM
Pooling	0x50	NNPA_AVGPOOL2D
	0x51	NNPA_MAXPOOL2D
Systolic ops	0x70	NNPA_CONVOLUTION
	0x71	NNPA_MATMUL_OP
	0x72	NNPA_MATMUL_OP_BCAST23
RNN	0x60	NNPA_LSTMACT
	0x61	NNPA_GRUACT
	0x00	NNPA_QAF

SMF 30 AIU Neural Network Processing Assist (NNPA) Entry IDs

- 27 NNPA Entry Ids
  - Which NNPA functions and how many occurrences in an address space?
  - Tensor attributes

    6 Entry IDs, 22-27
  - See:

    SYS1.MACLIB(IFASMFCN)

Counter number	Processor activity counted
1	NNPA-ADD function ending with CC=0
2	NNPA-SUB function ending with CC=0
3	NNPA-MUL function ending with CC=0
4	NNPA-DIV function ending with CC=0
5	NNPA-MIN function ending with CC=0
6	NNPA-MAX function ending with CC=0
7	NNPA-LOG function ending with CC=0
8	NNPA-EXP function ending with CC=0
9	Reserved for IBM use
10	NNPA-RELU function ending with CC=0
11	NNPA-TANH function ending with CC=0
12	NNPA-SIGMOID function ending with CC=0
13	NNPA-SOFTMAX function ending with CC=0
14	NNPA-BATCHNORM function ending with CC=0
15	NNPA-MAXPOOL2D function ending with CC=0
16	NNPA-AVGPOOL2D function ending with CC=0
17	NNPA-LSTMACT function ending with CC=0
18	NNPA-GRUACT function ending with CC=0
19	NNPA-CONVOLUTION function ending with CC=0
20	NNPA-MATMUL-OP function ending with CC=0
21	NNPA-MATMUL-OP-BCAST23 function ending with CC=0
22	NNPA function with conditions as described in “Common Oper
23	NNPA function with conditions as described in “Common Oper
24	NNPA function with conditions as described in “Common Oper
25	NNPA function with conditions as described in “Common Oper
26	NNPA function with conditions as described in “Common Oper
27	NNPA function with conditions as described in “Common Oper

SMF 30 AIU NNPA Example

- z16 AIU NNPA Example 1
  - Including Tensor

```
Subtype Record 4
SMF ID S01  Work Type OMVS Ho Min Sec 143016  Year Mon Day 20220302
Usage Offset 0 Length 76 Number 0
zEDC Offset 1279 Length 64 Number 0
z16 Crypto Offset 1519 Length 10 Number 0  Num Sections in Addl Records 0  No Crypto Counters
z16 NNPI (AI) Offset 1525 Length 10 Number 5  Num Sections in Addl Records 0   Yes AIU Counters
AIU Counters - Entry Id:  16 Count Value: 14 Description: NNPA - AvgPool2D
AIU Counters - Entry Id:  22 Count Value: 10 Description: NNPA - Tensor Small bat
AIU Counters - Entry Id:  25 Count Value: 3 Description: NNPA - Tensor 1 Mb frame suitable
AIU Counters - Entry Id:  26 Count Value: 11 Description: NNPA - Tensor 2 Gb frame suitable
AIU Counters - Entry Id:  27 Count Value: 220 Description: NNPA - Tensor AIU data area access exception
TYP   PFlags   RV  4    96   05
Job Step Program TESTFLR1 *OMVSEX  BPXPRECP
EXCPs 6827 SSCHs 112
CPU Time and SRB Time in Seconds 12.92   0
```

z16 SMF 30 Considerations for Crypto and AIU NNPA Support

- The counts represent a delta value for each interval – WSC requirement
  - Can determine accesses / load in interval and correlate to other performance metrics
  - Provides basis for performance analysis
    - What is CPU impact when utilizing encryption algorithm?
    - Which address space is using (or not using) what algorithm / function?
- SMF 30 Support for AIU NNPA instruction
  - Expect to see SMF30 NNPA data for WMLz and Db2 address spaces
  - SMF 30 Counts are not available for zCX applications

z16 CPU MF

- z16 CPU MF Published Implementation and Formulas
  - https://www.ibm.com/support/pages/cpu-mf-2022-update-and-wsc-experiences

Updated

- All extended counters are documented in IBM publication SA23-2261-07
  - Contains info for all processors from z10 and later
  - https://www.ibm.com/support/pages/cpu-measurement-facility-extended-counters-definition-z10-z196z114-zec12zbc12-z13z13s-z14-z15-and-z16
- AIU Counters of special note:
  - Counter 267 – Increments by one for every NUERAL NETWORK PROCESSING ASSIST instruction executed
  - Counter 268 – Increments by one for every NUERAL NETWORK PROCESSING ASSIST instruction executed that ended in Condition Codes 0, 1 or 2
  - Counter 269 – Cycles CPU spent obtaining access to IBM Z Integrated Accelerator for AI
  - Counter 270 – Cycles CPU is using IBM Z Integrated Accelerator for AI

z16 WSC AIU Metrics

New

- Formulas still under development – intent is to publish
- AIU Metrics
  - In addition to address space SMF 30 AIU IDs and counts, CPU MF can be utilized
  - CPU MF has thread level if running in SMT2
- Load information (How Much?)
  - LPARCPU equivalents, is absolute load, where 100 = 1 “Engine”
    - **AIUCPU** – Total AIU CPU (calculated)

      WAIUCPU – Waiting for access to AIU

      Maximum is logical processors * CF * 100

      If zIIPs running SMT2 scale by Capacity Factor (CF), 1 for GCPs

      CAIUCPU – Executing on AIU

      Maximum is 100 for a Chip (up to 8 cores driving 1 AIU accelerator)
- Rate of delivery information (CPI)
  - Cycles per instruction metric for AIU
    - **AIUCPI –** AIU Executing Cycles per completed instruction

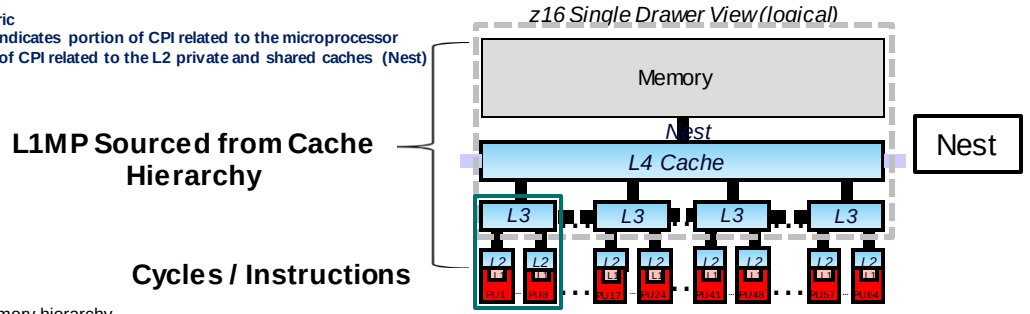
Sample z16 CPU MF Metrics

CPI — **Work Load Mix** — **CPI Micro Proc** — **CPI L2 & 'Nest'** — **How Often? 100% of L1 Misses** — **How Far?** — **How Much?** — **LSPR Workload Match**

Hour	CPI	Prb State	Instr Cmplx CPI	Finite CPI	SCPL1M	L1MP	L2P	L3P	L4LP	L4RP	MEMP	Rel Nest Intensity	LPARCPU	Eff GHz	Machine Type	LSPR Wkld
18.50	2.09	33.46	1.19	0.90	22	4.1	96.6	0.9	2.1	0.0	0.4	0.23	6.3	5.2	Z16	LOW

Finite CPI
Important Metric for LPAR Controls

CPI – Cycles per Instruction – A rate of delivery metric
- EICPI – Estimated Instruction Complexity CPI – Indicates portion of CPI related to the microprocessor
- EFCPI - Estimated Finite CPI – Indicates portion of CPI related to the L2 private and shared caches (Nest)



Workload Characterization
L1 Sourcing from cache/memory hierarchy

CPU MF – Fraud Detection AIU Test

- CPU MF by pool / logical
  - SMT2 thread level for each logical
- **AIUCPI**
  - AIU Exec Cycles per completed instruction
- **AIUCPU –** Total AIU CPU
- **WAIUCPU –** Waiting for access to AIU
  - Maximum is logical processors * 100
  - zIIPs SMT scale by capacity factor
- **CAIUCPU –** Executing on AIU
  - Maximum is 100 for a Chip

6 zIIPs 2 Threads each

SYSID	DAY	HOUR	CPU NUM RMF	Thread	Z16 CPI	POOL	CPID	LPARCPU	Z16 EICPI	Z16 EFCPI	L1MP	Z16 SCPL1M	AIUCPI	AIUCPU	WAIUCPU	CAIUCPU
P53	7	21.33	18	0	5.57	6	48	91.90	4.18	1.39	3.96	35	47,026.98	56.07	41.92	14.14
P53	7	21.33	18	1	5.65	6	49	89.40	4.26	1.39	4.00	35	47,784.31	55.11	41.50	13.61
P53	7	21.33	19	0	5.62	6	50	88.90	4.24	1.38	3.98	35	47,553.72	54.93	41.43	13.50
P53	7	21.33	19	1	5.63	6	51	88.80	4.25	1.38	3.99	35	47,565.40	54.82	41.34	13.48
P53	7	21.33	1A	0	8.50	6	52	58.90	7.22	1.29	3.60	36	41,213.35	45.70	38.49	7.21
P53	7	21.33	1A	1	9.91	6	53	53.20	8.50	1.41	3.83	37	42,081.49	41.85	35.72	6.13
P53	7	21.33	1B	0	10.96	6	54	46.20	9.53	1.43	3.73	38	41,377.42	37.60	32.64	4.96
P53	7	21.33	1B	1	12.03	6	55	42.70	10.52	1.51	3.83	39	41,567.97	34.91	30.50	4.40
P53	7	21.33	1C	0	12.93	6	56	36.60	11.39	1.54	3.73	41	41,106.93	30.46	26.91	3.54
P53	7	21.33	1C	1	13.80	6	57	33.90	12.20	1.61	3.80	42	41,680.38	28.14	24.91	3.22
P53	7	21.33	1D	0	13.33	6	58	29.20	11.79	1.54	3.52	44	41,204.98	24.35	21.70	2.66
P53	7	21.33	1D	1	14.40	6	59	27.00	12.77	1.64	3.67	45	41,324.69	22.46	20.03	2.43
															Total ==>	89.28

Q: Given 6 zIIPs resided on a Chip, how busy is the AIU Accelerator?

A: Sum of CAIUCPU / 100 * 100% = 89.28%

IBM WSC Tech Bytes Conference

- IBM Virtual Conference held Oct/Nov 2022
- In depth information in many IBM Z areas
- Can still register and listen to all recorded sessions
- Key Presentations:
  - How to Measure Those New z16 Capabilities
  - IBM z16 Technical Overview
  - z/OS Hot Topics
  - Unleash the Power of IBM Performance Reporting
- Other presentations specific to Cloud, Db2, CICS, IMS, etc.
- Presentations available for download
  https://www.ibm.com/support/pages/wsc-tech-bytes-conference-proceedings

z/End

Q & A / discussion

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