

嵌入式 SOC 第三次实验

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实验内容

本次实验将通过高层次综合的方法，在 Zynq 的 PL 中实现一个 kNN 算法的加速单元。

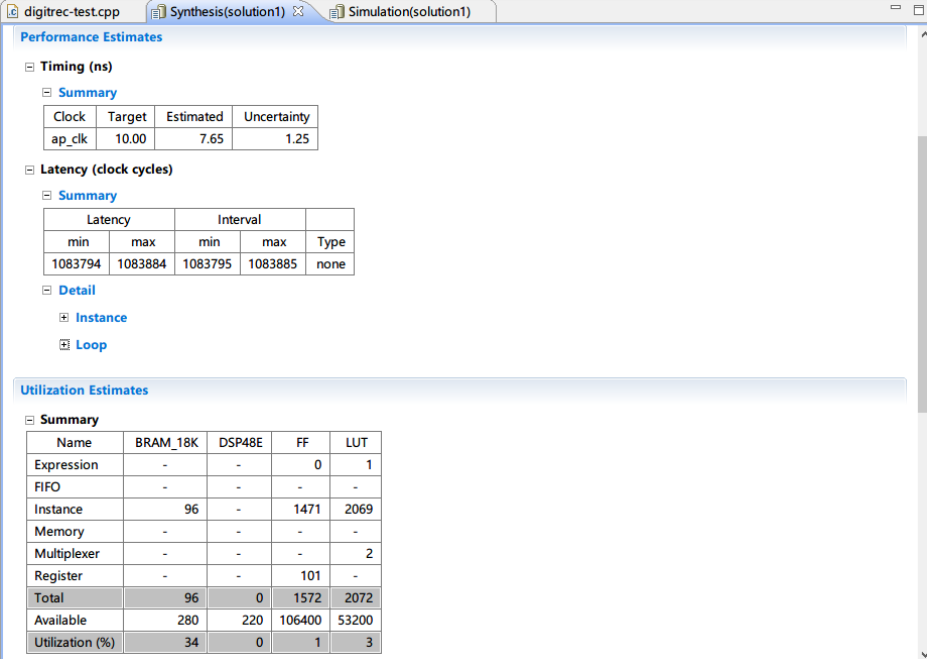
实验结果

算法执行结果

```
root@localhost:~/hw3# make
Compiling & executing digitrec on local host ...
g++ digitrec.cpp host.cpp -o host.o
./host.o
Number of test instances = 180
Overall Error Rate = 4.44444%
digitrec FPGA : 1 calls; 1951.431 msecs total time
root@localhost:~/hw3# make
Compiling & executing digitrec on local host ...
g++ digitrec.cpp host.cpp -o host.o
./host.o
Number of test instances = 180
Overall Error Rate = 4.44444%
digitrec FPGA : 1 calls; 1957.261 msecs total time
```

时间平均为 1954ms，错误率为 4.44%。相较于软件方法（3417.179ms 错误率 4.44%），速度有了明显提高，提升了 42.8%。

HLS 的结果



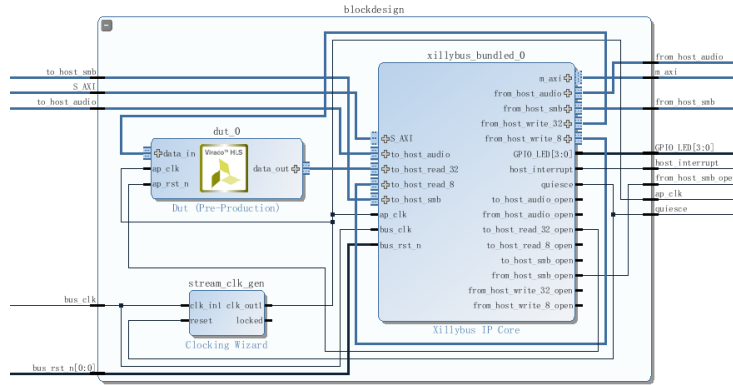
The screenshot displays the Xilinx IDE interface with two tabs: 'Synthesis(solution1)' and 'Simulation(solution1)'. The 'Performance Estimates' window is open, showing timing and latency data. Below it, the 'Utilization Estimates' window is also open, showing resource usage.

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	7.65	1.25

Latency		Interval		Type
min	max	min	max	
1083794	1083884	1083795	1083885	none

Name	BRAM_18K	DSP48E	FF	LUT
Expression	-	-	0	1
FIFO	-	-	-	-
Instance	96	-	1471	2069
Memory	-	-	-	-
Multiplexer	-	-	-	2
Register	-	-	101	-
Total	96	0	1572	2072
Available	280	220	106400	53200
Utilization (%)	34	0	1	3

插入 IP 核的位置和连线



优化情况

我们进行了循环展开的优化，对时间开销最严重的 `knn_vote` 函数进行了并行化操作，并手动指定了变量长度。

算法优化后执行情况

```
root@localhost:~# cd ./hw3/
root@localhost:~# make
make: Warning: File 'Makefile' has modification time 578 s in the future
Compiling & executing digitrec on local host ...
g++ digitrec.cpp host.cpp -o host.o
./host.o
Number of test instances = 180
Overall Error Rate = 4.44444%
digitrec FPGA      :      1 calls; 134.072 msecs total time
make: warning: Clock skew detected. Your build may be incomplete.
```

资源占用情况

digitrec.cpp

Synthesis(solution1)

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	9.66	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
72196	72286	72197	72287	none

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
Expression	-	-	0	1
FIFO	-	-	-	-
Instance	57	-	1818	2083
Memory	-	-	-	-
Multiplexer	-	-	-	2
Register	-	-	101	-
Total	57	0	1919	2086
Available	280	220	106400	53200
Utilization (%)	20	0	1	3

可以看到有了近 15 倍的加速