## UNSW Mechatronics Laboratory L220 PC104 I/O Address Map

Control pointer   Digital Output Low Byte   Bits (0 to 7)   Bits (0 to 7)   Digital Output Low Byte   Bits (0 to 7)   Bits (0		101041/074	aareee map	J. C.
Base Address MSI-404 - 4 channel 32 bit Quadrature Counter	Address	I/O Card		Comments
Channel O Least Significant Byte (read last)   Channel 1 Reset   Channel 0: 8 way SIL		Read Operation	Write Operation	
Channel O Least Significant Byte (read last)   Channel 1 Reset   Channel 0: 8 way SIL 201h   Channel 0 2nd L S byte (read scroon)   Channel 2 Reset   Socket via 4 pair 202h   Channel 0 2nd MS Byte (read scroon)   Channel 2 Reset   Screened Cable to 1   Channel 2 Channel 0 2nd MS Byte (read scroon)   Channel 2 Reset   Channel 1 Channel 2 Channel 1 Least Significant Byte (read list)   Channel 3 Reset   Channel 1 Least Significant Byte (read list)   Channel 4 Reset   Channel 1 Least Significant Byte (read list)   Channel 5 Reset   Channel 1 Znd MS Byte (read second)   Channel 7 Most Significant Byte (read list)   Channel 7 Reset   Channel 1 Znd MS Byte (read second)   Channel 2 Znd Spte (read second)   Channel 2 Znd Spte (read second)   Channel 2 Znd Spte (read second)   Channel 2 Znd MS Byte (read second)   Channel 3 Least Significant Byte (read first)   Channel 3 Least Significant Byte (read list)   Channel 3 Most Significant Byte (read first)   MUX scan   Channel 3 Most Significant Byte (read first)   Digital Output Low Byte   MUX scan   MUX scan   Channel 8 range control   Ribbon Cable   C	200h	Base Address MSI-404 - 4	•	unter
Channel O and LS Byte (read third)   Channel 1 Reset   Screened Cable to		The state of the s	And the Control of th	
Channel 2 2nd MS Byte (read second) Channel 3 Reset Channel 0 Most Significant Byte (read first) Channel 3 Reset Channel 1 Least Significant Byte (read list) Channel 3 Reset Channel 1 Znd LS Byte (read third) Channel 1 Znd LS Byte (read third) Channel 1 Znd LS Byte (read third) Channel 1 Znd LS Byte (read second) Channel 1 Most Significant Byte (read first) Channel 1 Znd LS Byte (read second) Channel 2 Znd MS Byte (read second) Channel 3 Znd LS Byte (read third) Channel 3 Znd LS Byte (read second) Channel 3 Znd LS Byte (read second) Channel 3 Most Significant Byte (read first) Channel 3 Znd LS Byte (read second) Channel 3 Znd LS Byte (read second) Channel 3 Most Significant Byte (read first) Channel 3 Znd LS Byte (read second) Channel 3 Most Significant Byte (read first) Channel 3 Znd LS Byte (read second) Channel 3 Most Significant Byte (read first) Channel 3 Most Significant Byte (read first)  Base Address PCM-3718HG - 12 bit Programmable Gain A/D and Digital I/O  Base Address PCM-3718HG - 12 bit Programmable Gain A/D and Digital I/O  Base Address PCM-3718HG - 12 bit Programmable Gain A/D and Digital I/O  But a digital Duby nibble & channel  A/D ligh byte A/D ligh byte A/D ligh byte A/D ligh byte A/D Status Register  Digital Input Low Byte (bits 0 to 7)  Digital Input Low Byte (bits 0 to 7)  Digital Input Low Byte (bits 0 to 7)  Digital Input High Byte (bits 8 to 15)  Digital Output Low Byte Bits (0 to 7)  Digital Output Low Byte Bits (0 to 7)  Digital Output High Byte Counter 0  Counter 0  Counter 0  Counter 0  Counter 1  Counter 1  Counter 2  Digital Output High Byte Counter 2  Digital Output High Byte Counter 2  Digital O				
Channel 0 Most Significant Byte (read first) Channel 1 Least Significant Byte (read inst) Channel 1 Reset Channel 1 2nd LS Byte (read third) Channel 1 Reset Channel 1 2nd MS Byte (read second) Channel 1 Reset Channel 1 And LS Byte (read second) Channel 1 Reset Channel 1 And LS Byte (read second) Channel 1 And LS Byte (read first) Channel 2 Reset Channel 3 Reset Channel 4 Reset Channel 7 Reset Ch				
Channel 1 Least Significant Byte (read last)   Channel 4 Reset   Channel 1 2nd LS Byte (read third)   Channel 5 Reset   Channel 1 2nd LS Byte (read third)   Channel 6 Reset   Channel 1 2nd Ms Byte (read first)   Channel 7 Reset   Channel 1 2nd Ms Byte (read first)   Channel 7 Reset   Channel 2 Least Significant Byte (read first)   Channel 7 Reset   Channel 2 Least Significant Byte (read first)   Channel 7 Reset   Channel 2 Least Significant Byte (read first)   Channel 3 Least Significant Byte (read first)   Channel 3 Least Significant Byte (read first)   Channel 3 2nd LS Byte (read first)   Channel 3 2nd LS Byte (read first)   Channel 3 Most Significant Byte (read first)   MUX scan channel 8 range control   A/D high byte   A/D range control   Ribbon Cable   A/D high byte   A/D status Register   Control Register   Counter 1   Counter 1   Counter 2   Counter 2   Counter 3   Counter 2   Counter 2   Counter 3   Counter 4   Counter 5   Counter 6   Counter 7   Cable to Interface Board   Counter 8   Counter 9				
Channel 1 2nd LS Byte (read third) Channel 5 Reset Channel 7 Ind MB Byte (read second) Channel 6 Reset Channel 1 And MB Byte (read second) Channel 7 Reset Channel 2 Channel 2 Special Special Channel 7 Reset Channel 2 Channel 2 Special Special Channel 7 Reset Channel 2 Special S				illie receiver.
Channel 1 2nd MS Byte (read second)   Channel 6 Reset   Channel 1 Channel 1 Most Significant Byte (read first)   Channel 7 Reset   Channel 2 Least Significant Byte (read first)   Channel 7 Reset   Channel 2 MB Byte (read third)   Channel 2 Channel 2 Channel 2 Channel 3 Least Significant Byte (read first)   Channel 3 2nd MS Byte (read second)   Channel 3 2nd MS Byte (read second)   Channel 3 2nd MS Byte (read second)   Channel 3 2nd MS Byte (read first)   Channel 3 Channel 3 Sot Significant Byte (read first)   Channel 3 Chann				Channel 1: Haş line
Channel 1 Most Significant Byte (read first)   Channel 7 Reset   Channel 2 Channel 2 Channel 2 Syte (read third)   Channel 2 Channel 3				receiver but no
Channel 2 Least Significant Byte (read last)   Channel 2 and LS Byte (read third)   Channel 2 and LS Byte (read third)   Channel 2 and LS Byte (read third)   Channel 2 and LS Byte (read first)   Channel 2 and LS Byte (read last)   Channel 2 and LS Byte (read last)   Channel 3 Least Significant Byte (read first)   Channel 3 Least Significant Byte (read first)   Channel 3 and LS Byte (read second)   Channel 3 and MS Byte (read second)   Channel 3 Most Significant Byte (read first)   Channel 3 Most Significant Byte (r				external Cable.
Channel 2 2nd LS Byte (read third)			Chainlei / Reset	
Channel 2 2nd MS Byte (read second)   receiver but no external Cable.   Channel 2 Most Significant Byte (read first)   Channel 3 Least Significant Byte (read last)   Channel 3 Least Significant Byte (read last)   Channel 3 Least Significant Byte (read second)   Channel 3 Most Significant Byte (read first)   Channel 4 Most Significant Byte (read first				
external Cable   channel 3 Least Significant Byte (read last)   Channel 3 and LS Byte (read third)   Channel 3 2nd MS Byte (read second)   receiver.   Channel 3 2nd MS Byte (read second)   receiver.   Channel 3 Most Significant Byte (read first)   Channel 3 Most Significant Byte   Channel 3 Most Most Most Most Most Most Significant Byte   Channel 4 Most Most Most Most Most Most Most Most				
Channel 3 Least Significant Byte (read last)   Channel 3 2nd LS Byte (read third)				external Cable.
Channel 3 2nd LS Byte (read third)   Channel 3 2nd MS Byte (read second)   Connel 3 2nd MS Byte (read second)   Channel 3 Most Significant Byte (read first)				
Channel 3 2nd MS Byte (read second)   receiver.			,	Channel 3: No line
Channel 3 Most Significant Byte (read first)				
Base Address PCM-3718HG - 12 bit Programmable Gain A/D and Digital I/O  300h A/D low nibble & channel Software A/D trigger Ribbon Cable  MUX scan MUX scan channel & range control MUX scan channel & range control pointer  302h MUX scan Digital Input Low Byte (bits 0 to 7) Digital Output Low Byte Bits (0 to 7) Digital Output High Byte (bits 8 to 15) Digital Output High Byte (bits 8 t				
A/D low nibble & channel   Software A/D trigger   A/D range control   Ribbon Cable			oit Programmable Gain A/D an	d Digital I/O
A/D high byte  A/D range control  MUX scan channel & range control  MUX scan channel & range control  MUX scan channel & range control  Digital Output Low Byte Bits (0 to 7)  Digital Output High Byte Coantrol Register  Control Register  Control Register  Digital Output High Byte Coantrol Cable to Interface Board  DA Date Interface Board  Cable to Interface Board  Cable to Interface Board  Cable to Interface Board  Cable to Interface Board  DA Date Interface Board  Cable to Interface Board  Cable to Interface Board  Cable to Interface Board  Cable to Interface Board  DA Date Interface Board  Interface Board  Cable to Interface Board  All East Significant Byte DA DA S East Significant Byte DA S East Significa				
MUX scan channel & range control pointer  Digital Input Low Byte (bits 0 to 7)  Digital Output Low Byte Bits (0 to 7)  Digital Output Low Byte Bits (0 to 7)  Digital Output Low Byte Bits (0 to 7)  Digital Output Low Byte Board  Digital Output Register  Control Register  Control Register  Digital Output High Byte (bits 8 to 15)  Counter 0  Counter 0  Counter 0  Counter 0  Digital Output High Byte (bits 8 to 15)  Counter Output High Byte (bits 8 to 15)  Digital Output High Byte (bits 8				
Digital Input Low Byte (bits 0 to 7)  Digital Output Low Byte Bits (0 to 7)  Digital Output Low Byte Board  Digital Control Register  Control Register  Control Register  Digital Output High Byte (bits 8 to 15)  Digital Output Low Byte (bits 8 to 15)  Digital Output Low Byte (bits 8 to 15)  Digital Output Low Byte (bits 8 to 15)  Digital Output High Byte (bits 8 to 15)  Counter O  Counter O  Counter O  Counter O  Counter O  Counter 1  1 MHz by jumper JP1.  PCLK is set to 1 MHz by jumper JP1.  PCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by				Kibboli Cable
Digital Input Low Byte (bits 0 to 7)  Digital Output Low Byte Bits (0 to 7)  Digital Output Low Byte Bits (0 to 7)  Digital Output Low Byte Bits (0 to 7)  Digital Output Hequest  Control Register  Control Register  Control Register  Control Register  Digital Output High Byte (bits 8 to 15)  Cable to Interface 8  Date of the Missing Interface 10  About Digital Input High Byte (bits 8 to 15)  Digital Output High Byte (bits 6 lother Digital Nibbl	302h	MUX scan		
Digital Input Low Byte (bits 0 to 7)  Digital Culput Low Byte Bits (0 to 7)  Digital Culput Low Byte Bits (0 to 7)  Digital Control Register  Control Register  Control Register  Control Register  Digital Output High Byte (bits 8 to 15)  Digital Output High Byte (bits 8 to 15)  Digital Output High Byte (bits 8 to 15)  Counter 0  Counter 0  Counter 1  Counter 1  Counter 2  Counter 2  Dounter 2  Dounter 2  Dounter 2  Dounter Control  Digital Output High Byte (bits 8 to 15)  Counter 0  FCLK is set to 1 MHz by jumper JP1.  Digital Output High Byte (bits 8 to 15)  Cable to Interface Board  Cable to Interface Board  20 way Grey Ribbon Cable to Interface Board  FCLK is set to 1 MHz by jumper JP1.  DIA 1 Most Significant Byte Dy1.  DIA 1 Least Significant Byte Dy1.  DIA 1 Least Significant Ribble Simultaneous Update if selected DiA 1 Least Significant Byte Connector with Coloured twisted pair ribbon cable.  DIA 2 Least Significant Byte DiA 2 Least Significant Byte Simultaneous Update if selected DiA 3 Least Significant Byte Simultaneous Update if selected DiA 3 Least Significant Byte Simultaneous Update if selected DiA 3 Least Significant Byte Simultaneous Update if selected DiA 3 Least Significant Byte Simultaneous Update if selected DiA 3 Least Significant Byte Simultaneous Update if selected DiA 4 Least Significant Byte Simultaneous Update if selected DiA 5 Least Significant Nibble Simultaneous Update if selected DiA 5 Least Significant Nibble Simultaneous Update if selected DiA 5 Least Significant Nibble Simultaneous Update if selected DiA 5 Most Significant Nibble Simultaneous Update if selected DiA 5 Most Significant Nibble Simultaneous Update if selected DiA 5 Most Significant Nibble Simultaneous Update if selected DiA 5 Most Significant Nibble Simultaneous Update if selected DiA 5 Most Significant Nibble Simultaneous Update if selected DiA 5 Most Significant Nibble Simultaneous Update if selected DiA 5 Most Significant Nibble Simultaneous Update if selected DiA 5 Most Significant Nibble Simultaneous Update if Se			*	20 way Grey Ribbon
308h A/D Status Register Clear interrupt request 309h Control Register Control Register 30Ah Pacer Enable 30Bh Digital Input High Byte (bits 8 to 15) 30Bh Digital Output High Byte (bits 8 to 15) 30Ch Counter 0 30Dh Counter 1 30Eh Counter 2 30Fh Counter 2 30Fh Counter 2 30Fh Counter 2 30Ph Base Address DAC06 - 6 Channel 12 bit D/A 320h Simultaneous Update if selected D/A 0 Most Significant Byte Simultaneous Update if selected D/A 1 Least Significant Nibble Simultaneous Update if selected D/A 2 Most Significant Nibble Simultaneous Update if selected D/A 2 Most Significant Nibble Simultaneous Update if selected D/A 3 Most Significant Nibble Simultaneous Update if selected D/A 3 Most Significant Nibble Simultaneous Update if selected D/A 3 Most Significant Nibble Simultaneous Update if selected D/A 3 Most Significant Nibble Simultaneous Update if selected D/A 4 Least Significant Nibble Simultaneous Update if selected D/A 3 Most Significant Nibble Simultaneous Update if selected D/A 4 Least Significant Nibble Simultaneous Update if selected D/A 4 Least Significant Nibble Simultaneous Update if selected D/A 4 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if selected D/A 5 Least Significant Nibble Simultaneous Update if Selected D/A 5 Least Significant Nibble Simultaneous Update if Selected D/A 5 Least Significant Nibble Simultaneous Update if Selected D/A 5 Least Significant Nibble Simultaneous Updat	303h	Digital Input Low Byte (bits 0 to 7)		
A/D Status Register   Clear interrupt request	(	Signal input Low Byte (Bite 6 to 1)	Bits (0 to 7)	Professional Control of the Control
Control Register   Control Register   Pacer Enable	308h	A/D Status Register	Clear interrupt request	Dould
Digital Input High Byte (bits 8 to 15)  Digital Output High Byte (bits 8 to 15)  Counter 0  Counter 0  Counter 1  Counter 1  Counter 2  Counter 2  Counter Control  D/A 0 Least Significant Byte  D/A 1 Least Significant Byte  D/A 1 Least Significant Byte  D/A 1 Least Significant Byte  D/A 2 Least Significant Byte  D/A 3 Least Significant Byte  D/A 2 Least Significant Byte  D/A 2 Least Significant Byte  D/A 3 Least Significant Byte  D/A 3 Least Significant Byte  D/A 2 Least Significant Byte  D/A 3 Least Significant Byte  D/A 4 Least Significant Byte  D/A 5 Least Significant Byte  D/A 4 Least Significant Byte  D/A 5 Most Significant Nibble  Base Address Quadrature Counter Index Pulses				
Digital Input High Byte (bits 8 to 15)  Digital Output High Byte (bits 8 to 15)  Cable to Interface Board  Counter 0  Counter 1  Counter 1  Counter 2  Counter 2  Counter 2  Counter Control  Counter Countrol  Simultaneous Update if selected  D/A 0 Least Significant Byte  D/A 1 Least Significant Byte  D/A 1 Least Significant Byte  D/A 2 Least Significant Byte  D/A 2 Least Significant Byte  D/A 3 Most Significant Byte  D/A 3 Least Significant Byte  D/A 3 Least Significant Byte  D/A 3 Most Significant Byte  D/A 4 Least Significant Byte  D/A 3 Most Significant Byte  D/A 4 Least Significant Byte  D/A 5 Least Significant Byte  D/A 6 Most Significant Byte  D/A 7 Least Significant Byte  D/A 8 Most Significant Byte  D/A 9 Most Significant Byte  D/A 1 Least Significant Byte  D/A 1 Least Significant Byte  D/A 2 Least Significant Byte  D/A 3 Least Significant Byte  D/A 4 Least Significant Byte  D/A 5 Most Significant Byte  D/A 5 Mos		3.0.0.0		
Digital Input High Byte (bits 8 to 15)  Digital Input High Byte (bits 8 to 15)  Digital Output High Byte (bits 8 to 15)  Cable to Interface Board  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  FCLK is set to 1 MHz by jumper JP1.  Digital Output High Byte (bits 8 to 15)  Cable to Interface Board  FCLK is set to 1 MHz by jumper JP1.  FCLK is				20 way Grey Ribbon
Counter 0   Counter 0   Counter 0   Counter 1   Counter 2   Counter 2   JP1.	30Bh	Digital Input High Byte (bits 8 to 15)		
Counter 0 Counter 1 Counter 2 Counter 2 Counter 2 Counter Control Counter 2 Counter Control Counter 2 Counter Control Counter 2 Counter Control Counter Counter Control Counter Counter Control Counter Counter Counter Control Counter Counter Counter Control Counter Counter Counter Control Counter Counte			(Dits 8 to 15)	Board
Counter 1 Counter 2 Counter 2 Counter 2 Counter Control  Counter 2 Counter Control  Counter 2 Counter Control  Counter 2 Counter Control  Counter Counter Index Pulse Channels 0  A Most Significant Byte D/A 0 Least Significant Byte D/A 1 Least Significant Byte D/A 1 Most Significant Nibble D/A 2 Least Significant Byte Connector with Coloured twisted pair ribbon cable.  Connector with Coloured twisted pair ribbon cable	30Ch	Counter 0	Counter 0	FOLK is sales
Counter 2   Counter Control	30Dh	Counter 1	Counter 1	
Counter Control   320h   Base Address DAC06 - 6 Channel 12 bit D/A	30Eh	Counter 2	Counter 2	
Base Address DAC06 - 6 Channel 12 bit D/A  320h Simultaneous Update if selected D/A 0 Least Significant Byte 321h Simultaneous Update if selected D/A 1 Least Significant Byte 322h Simultaneous Update if selected D/A 1 Least Significant Byte 323h Simultaneous Update if selected D/A 1 Most Significant Nibble 324h Simultaneous Update if selected D/A 2 Least Significant Byte 325h Simultaneous Update if selected D/A 2 Most Significant Nibble 326h Simultaneous Update if selected D/A 3 Least Significant Byte 327h Simultaneous Update if selected D/A 3 Most Significant Nibble 328h Simultaneous Update if selected D/A 4 Least Significant Nibble 329h Simultaneous Update if selected D/A 4 Most Significant Nibble 329h Simultaneous Update if selected D/A 5 Least Significant Nibble 329h Simultaneous Update if selected D/A 5 Most Significant Nibble 329h Simultaneous Update if selected D/A 5 Most Significant Nibble 329h Simultaneous Update if selected D/A 5 Most Significant Nibble 329h Simultaneous Update if selected D/A 5 Most Significant Nibble 329h Simultaneous Update if selected D/A 5 Most Significant Nibble 320h Base Address Quadrature Counter Index Pulses  800h Quadrature Counter Index Pulse Channels 0 and 1  Bit 7 = I <sub>0</sub> <sup>+</sup> , Bit 6 = I <sub>0</sub> Bit 5 = I <sub>1</sub> <sup>+</sup> , Bit 4 = I <sub>1</sub>			Counter Control	JP1.
Simultaneous Update if selected   D/A 0 Least Significant Byte		Base Address DAC06 - 6 Channel 12 bit D/A		
Simultaneous Update if selected  322h Simultaneous Update if selected  323h Simultaneous Update if selected  323h Simultaneous Update if selected  324h Simultaneous Update if selected  325h Simultaneous Update if selected  325h Simultaneous Update if selected  326h Simultaneous Update if selected  327h Simultaneous Update if selected  327h Simultaneous Update if selected  328h Simultaneous Update if selected  328h Simultaneous Update if selected  329h Simultaneous Update if selected  320h Simultaneous Update if selected		Simultaneous Update if selected	D/A 0 Least Significant Byte	
Simultaneous Update if selected  323h Simultaneous Update if selected  324h Simultaneous Update if selected  325h Simultaneous Update if selected  325h Simultaneous Update if selected  326h Simultaneous Update if selected  327h Simultaneous Update if selected  327h Simultaneous Update if selected  328h Simultaneous Update if selected  328h Simultaneous Update if selected  329h Simultaneous Update if selected  329h Simultaneous Update if selected  329h Simultaneous Update if selected  320h Simultaneous Update if selected				1
Simultaneous Update if selected  324h Simultaneous Update if selected  325h Simultaneous Update if selected  326h Simultaneous Update if selected  327h Simultaneous Update if selected  328h Simultaneous Update if selected  328h Simultaneous Update if selected  329h Simultaneous Update if selected  320h Simultaneous Update if selected				
Simultaneous Update if selected  Simultaneous Update if selected  D/A 2 Most Significant Nibble  Simultaneous Update if selected  D/A 3 Least Significant Nibble  D/A 3 Most Significant Nibble  D/A 3 Most Significant Nibble  D/A 4 Least Significant Nibble  D/A 4 Least Significant Nibble  D/A 4 Least Significant Nibble  D/A 4 Most Significant Nibble  D/A 4 Most Significant Nibble  D/A 5 Least Significant Nibble  D/A 5 Most Significa		<u> </u>		A CONTRACTOR OF THE CONTRACTOR
Simultaneous Update if selected  Simultaneous Update if selected  D/A 2 Most Significant Nibble  D/A 3 Least Significant Byte  D/A 3 Most Significant Nibble  D/A 3 Most Significant Nibble  D/A 3 Most Significant Nibble  D/A 4 Least Significant Byte  D/A 4 Least Significant Byte  D/A 4 Most Significant Nibble  D/A 5 Least Significant Nibble  D/A 5 Least Significant Byte  D/A 5 Most Significant Nibble				
Simultaneous Update if selected  D/A 3 Least Significant Byte  D/A 3 Most Significant Nibble  D/A 4 Least Significant Byte  D/A 4 Least Significant Byte  D/A 4 Least Significant Byte  D/A 5 Least Significant Nibble  D/A 5 Least Significant Nibble  D/A 5 Least Significant Byte  D/A 5 Least Significant Byte  D/A 5 Least Significant Byte  D/A 5 Most Significant Nibble				
Simultaneous Update if selected  328h Simultaneous Update if selected  329h Simultaneous Update if selected  329h Simultaneous Update if selected  32Ah Simultaneous Update if selected  32Ah Simultaneous Update if selected  32Bh Simultaneous Update if selected				
Simultaneous Update if selected  D/A 4 Least Significant Byte  Simultaneous Update if selected  D/A 4 Most Significant Nibble  Simultaneous Update if selected  D/A 5 Least Significant Byte  D/A 5 Most Significant Nibble  Base Address Quadrature Counter Index Pulses  Quadrature Counter Index Pulse Channels 0  and 1  Bit 7 = I <sub>0</sub> <sup>+</sup> , Bit 6 = I <sub>0</sub> Bit 5 = I <sub>1</sub> <sup>+</sup> , Bit 4 = I <sub>1</sub>				•
Simultaneous Update if selected  D/A 4 Most Significant Nibble  Simultaneous Update if selected  D/A 5 Least Significant Byte  D/A 5 Most Significant Nibble  Base Address Quadrature Counter Index Pulses  Quadrature Counter Index Pulse Channels 0  and 1  Bit 7 = I <sub>0</sub> <sup>+</sup> , Bit 6 = I <sub>0</sub> <sup>-</sup> Bit 5 = I <sub>1</sub> <sup>+</sup> , Bit 4 = I <sub>1</sub> <sup>-</sup>				
Simultaneous Update if selected  D/A 5 Least Significant Byte  D/A 5 Most Significant Nibble  Base Address Quadrature Counter Index Pulses  Quadrature Counter Index Pulse Channels 0 and 1  Bit 7 = I <sub>0</sub> <sup>+</sup> , Bit 6 = I <sub>0</sub> <sup>-</sup> Bit 5 = I <sub>1</sub> <sup>+</sup> , Bit 4 = I <sub>1</sub> <sup>-</sup>				simultaneous update
Simultaneous Update if selected  Base Address Quadrature Counter Index Pulses  Quadrature Counter Index Pulse Channels 0 and 1  D/A 5 Most Significant Nibble  Bit 7 = I <sub>0</sub> <sup>+</sup> , Bit 6 = I <sub>0</sub> Bit 7 = I <sub>1</sub> <sup>+</sup> , Bit 4 = I <sub>1</sub>	32Ah			1
Base Address Quadrature Counter Index Pulses  Quadrature Counter Index Pulse Channels 0 and 1  Bit 7 = I <sub>0</sub> <sup>+</sup> , Bit 6 = I <sub>0</sub> <sup>-</sup> Bit 5 = I <sub>1</sub> <sup>+</sup> , Bit 4 = I <sub>1</sub> <sup>-</sup>	32Bh			_, 2
Quadrature Counter Index Pulse Channels 0 and 1 Bit $7 = I_0^+$ , Bit $6 = I_0^-$ Bit $5 = I_1^+$ , Bit $4 = I_1^-$				
and 1 Bit $5 = I_1^+$ , Bit $4 = I_1^-$				D37 - 1
Dit 3 - 11, Dit 4 - 11	800h			
801h Quadrature Counter Index Pulse Channel 2				Bit $5 = I_1^-$ , Bit $4 = I_1^-$
Bit $l = l_2$	801h	Quadrature Counter Index Pulse Channel 2		Bit $7 = I_2^+$ , Bit $6 = I_2^-$