UNSW Mechatronics Laboratory L220
PC104 I/O Address Map

Address	I/O Card		Comments
	Read Operation	Write Operation	
200h	**Base Address MSI-404 - 4 channel 32 bit Quadrature Counter**		
200h	Channel 0 Least Significant Byte (read last)	Channel 0 Reset	Channel 0: 8 way SIL Socket via 4 pair Screened Cable to line receiver.
201h	Channel 0 2nd LS Byte (read third)	Channel 1 Reset	
202h	Channel 0 2nd MS Byte (read second)	Channel 2 Reset	
203h	Channel 0 Most Significant Byte (read first)	Channel 3 Reset	
204h	Channel 1 Least Significant Byte (read last)	Channel 4 Reset	Channel 1: Has line receiver but no external Cable.
205h	Channel 1 2nd LS Byte (read third)	Channel 5 Reset	
206h	Channel 1 2nd MS Byte (read second)	Channel 6 Reset	
207h	Channel 1 Most Significant Byte (read first)	Channel 7 Reset	
208h	Channel 2 Least Significant Byte (read last)		Channel 2: Has line receiver but no external Cable.
209h	Channel 2 2nd LS Byte (read third)		
20Ah	Channel 2 2nd MS Byte (read second)		
20Bh	Channel 2 Most Significant Byte (read first)		
20Ch	Channel 3 Least Significant Byte (read last)		Channel 3: No line receiver.
20Dh	Channel 3 2nd LS Byte (read third)		
20Eh	Channel 3 2nd MS Byte (read second)		
20Fh	Channel 3 Most Significant Byte (read first)		
300h	**Base Address PCM-3718HG - 12 bit Programmable Gain A/D and Digital I/O**		
300h	A/D low nibble & channel	Software A/D trigger	20 way Screened Ribbon Cable
301h	A/D high byte	A/D range control	
302h	MUX scan	MUX scan channel & range control pointer	
303h	Digital Input Low Byte (bits 0 to 7)	Digital Output Low Byte Bits (0 to 7)	20 way Grey Ribbon Cable to Interface Board
308h	A/D Status Register	Clear interrupt request	
309h	Control Register	Control Register	
30Ah		Pacer Enable	
30Bh	Digital Input High Byte (bits 8 to 15)	Digital Output High Byte (bits 8 to 15)	20 way Grey Ribbon Cable to Interface Board
30Ch	Counter 0	Counter 0	FCLK is set to 1 MHz by jumper JP1.
30Dh	Counter 1	Counter 1	
30Eh	Counter 2	Counter 2	
30Fh		Counter Control	
320h	**Base Address DAC06 - 6 Channel 12 bit D/A**		
320h	Simultaneous Update if selected	D/A 0 Least Significant Byte	16 way IDC Connector with coloured twisted pair ribbon cable. Jumpers are not set to select simultaneous update.
321h	Simultaneous Update if selected	D/A 0 Most Significant Nibble	
322h	Simultaneous Update if selected	D/A 1 Least Significant Byte	
323h	Simultaneous Update if selected	D/A 1 Most Significant Nibble	
324h	Simultaneous Update if selected	D/A 2 Least Significant Byte	
325h	Simultaneous Update if selected	D/A 2 Most Significant Nibble	
326h	Simultaneous Update if selected	D/A 3 Least Significant Byte	
327h	Simultaneous Update if selected	D/A 3 Most Significant Nibble	
328h	Simultaneous Update if selected	D/A 4 Least Significant Byte	
329h	Simultaneous Update if selected	D/A 4 Most Significant Nibble	
32Ah	Simultaneous Update if selected	D/A 5 Least Significant Byte	
32Bh	Simultaneous Update if selected	D/A 5 Most Significant Nibble	
800h	**Base Address Quadrature Counter Index Pulses**		
800h	Quadrature Counter Index Pulse Channels 0 and 1		Bit 7 = I_0^+, Bit 6 = I_0^- Bit 5 = I_1^+, Bit 4 = I_1^-
801h	Quadrature Counter Index Pulse Channel 2		Bit 7 = I_2^+, Bit 6 = I_2^-