Digital Frequency Multiplier

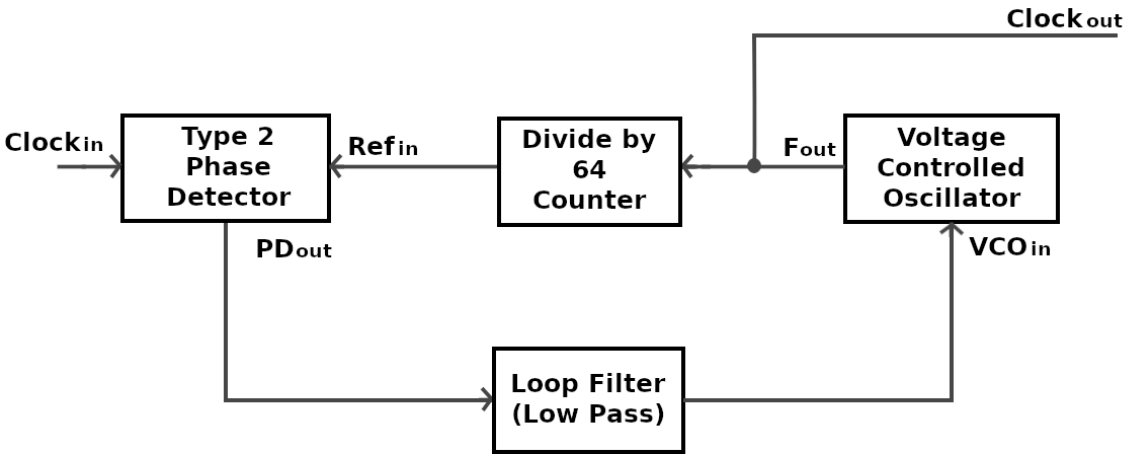
A digital electronics circuit that multiplies an input frequency by 64.

Input Signal Characteristics

- 3.3V peak to peak digital waveform
- Minimum duty cycle of 5%
- Minimum frequency 23.4375 KHz
- Maximum frequency 78.125 KHz

Output Signal Characteristics

- 3.3V peak to peak digital waveform
- Duty cycle of 50%
- Minimum frequency 1.5 MHz
- Maximum frequency 5.0 MHz



Phased Lock Loop as Frequency Synthesizer

Using a Phase Locked Loop as a Frequency Synthesizer

A simplified explanation of the operation of a phase locked loop (PLL) is as follows:
There are three main components:

- Phase Detector (in this case type 2)
- Loop Filter
- Voltage Controlled Oscillator (VCO)

The phase detector compares two input signals, Clock in and Ref in. The difference in phase between the signals is output as a series of pulses, PDout.

A type 2 phase detector outputs ‘positive’ pulses when the phase of Clock in leads that of Ref in and ‘negative’ pulses when it lags that of Ref in.

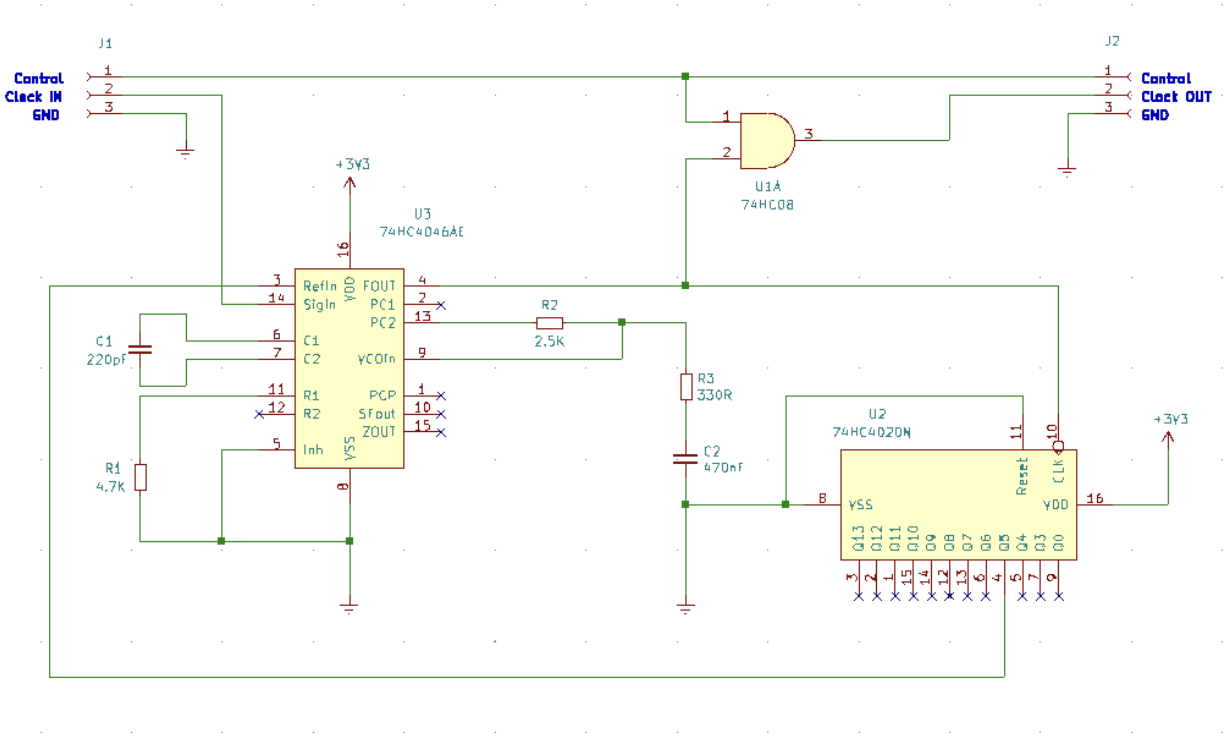
The pulses are converted into a DC voltage by the loop filter, which acts as a low pass filter (integrator). The greater the phase difference, the higher the DC voltage.
The loop filter’s output is the control input voltage to the VCO.

The VCO outputs a frequency that is proportional to the input voltage, the higher the voltage, the greater the frequency.

The addition of a divide by 64 counter in between the output of the VCO and the reference input of the phase detector causes the frequency of the VCO output to be 64 times that of the Clock in.

Circuit Design

The circuit diagram below shows the main components of the frequency multiplier.



Frequency Multiplier Schematic

U3 (74HC4046AE) contains the phase detector and VCO.

The low pass loop filter consists of R2, R3 and C2. The values were chosen using the Nexperia data sheet to produce a settling time of around 1ms.

U2 (74HC4020N) is the divide by 64 counter.

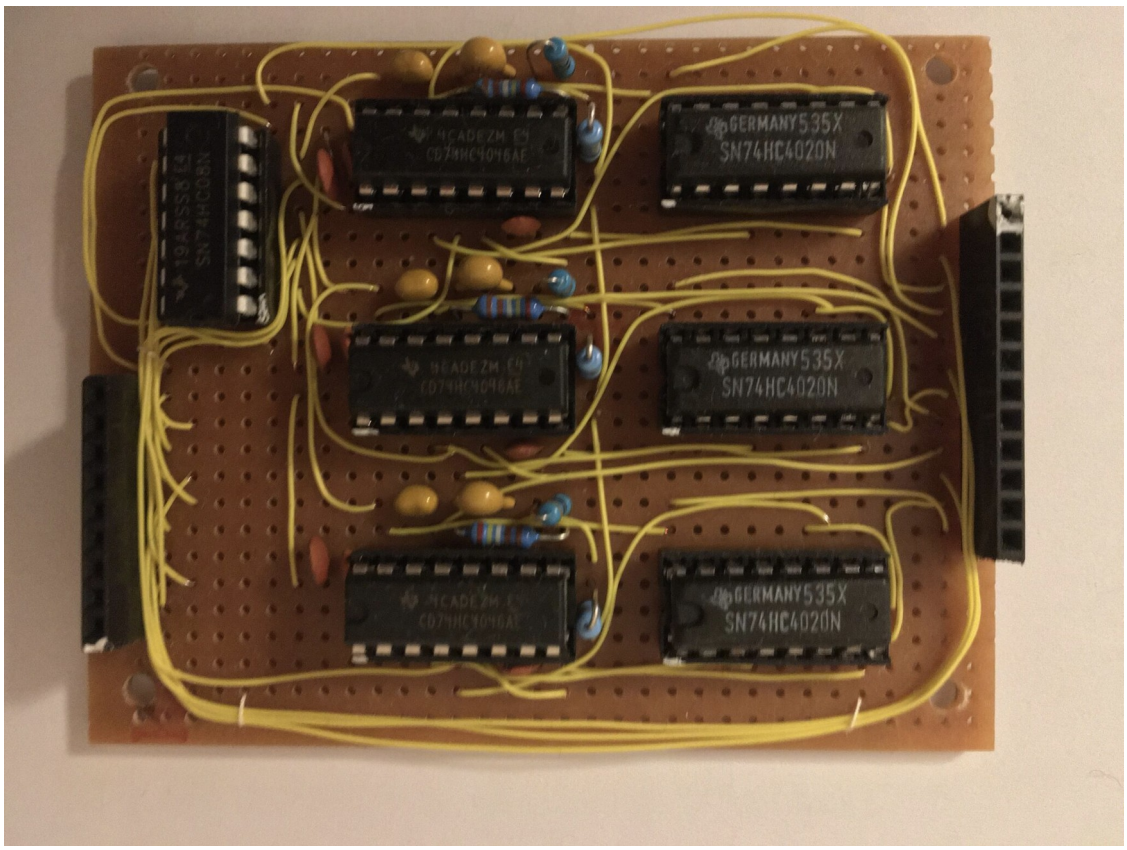
U1A (74HC08), enables the output of the frequency multiplier.

The centre frequency of the VCO is determined by R1 and C1. The values of 4.7K and 220pF resulted in a centre frequency greater than 5MHz.

The ICs are from the same high speed CMOS family.
(1nF and 100nF decoupling capacitors were placed close to the power supply pins of U3).

Prototype

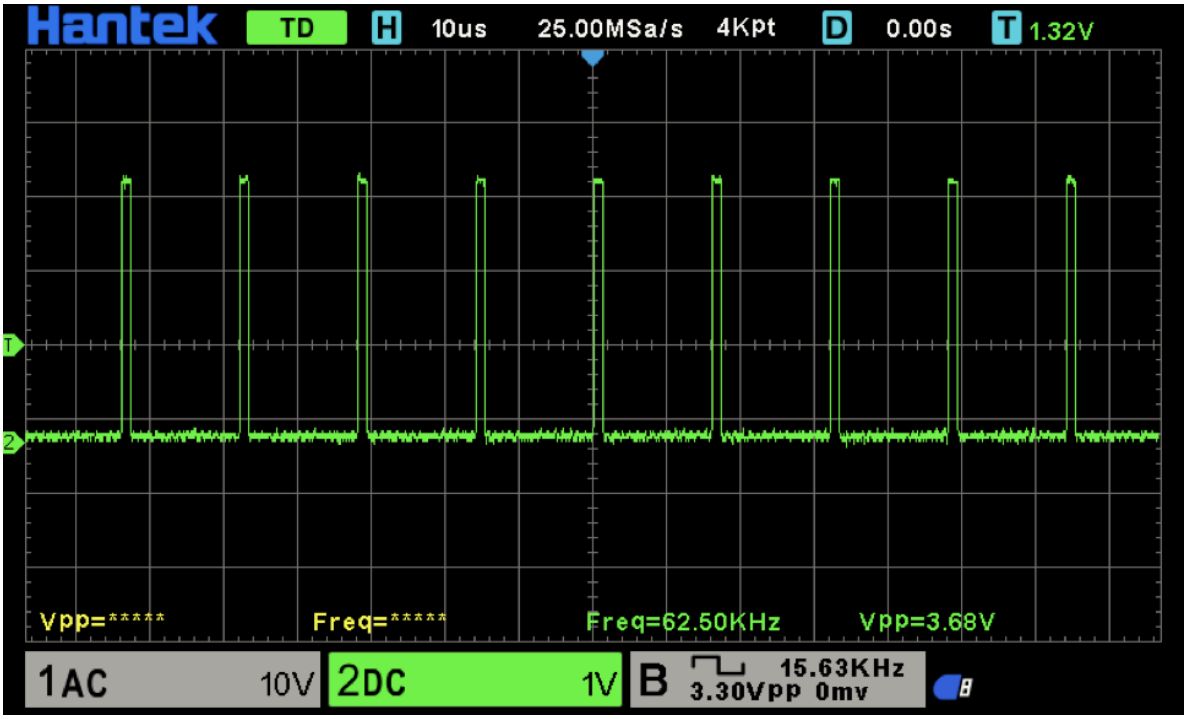
The prototype board contains 3 frequency multipliers and was used in the PTP instrumentation control project



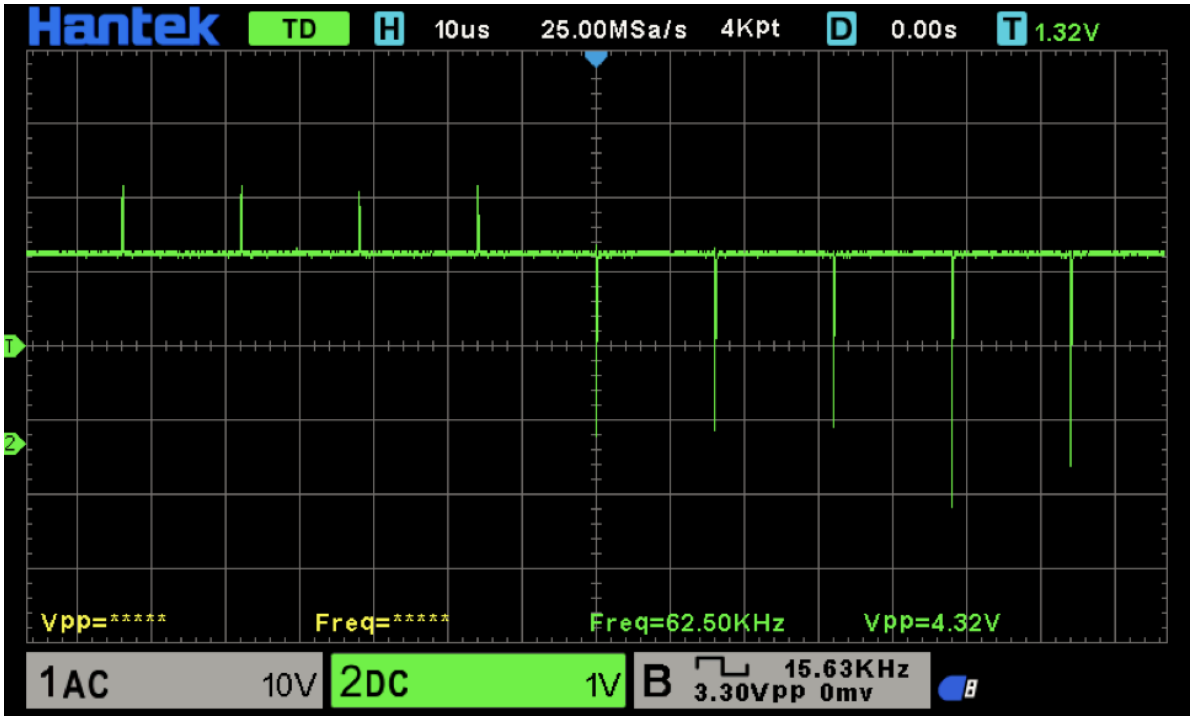
Prototype Hardware

Results

Shown below are the oscilloscope traces for clock in, phase detector output and clock out.

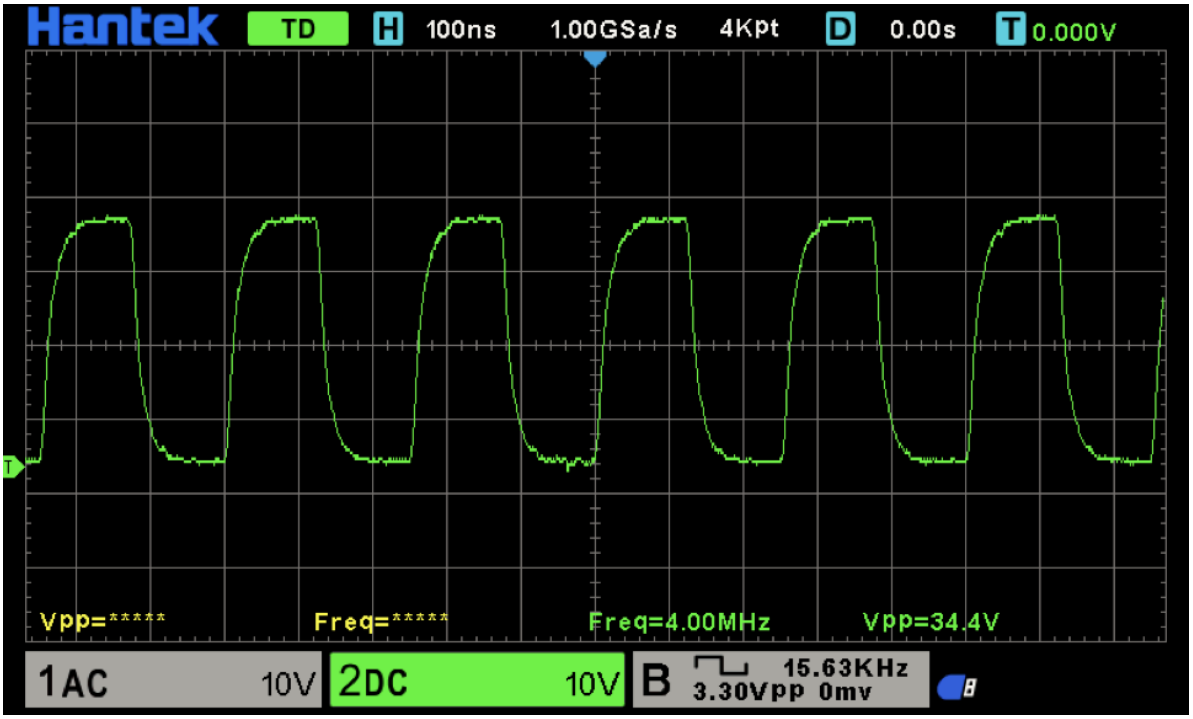


Clock In – 62.50KHz



Phase Detector Output

Note the ‘positive’ and ‘negative’ pulses. This is a characteristic of a type 2 phase detector. The pulses are very narrow because Clock in and Ref in are almost in phase.



Clock Out – 4MHz

Conclusions

An accurate multiplication of an input signal's frequency was possible, producing an output signal with a 50% duty cycle.