Component Name:

Logic chip design: Advanced CPUs

Component ID: N1

Description:

Central processing units ("CPUs") are the dominant general purpose logic chips. Two U.S. firms, Intel and AMD, have long held a duopoly over CPUs used for laptops, desktops, and servers. (China has several ventures, though none are competitive with U.S. firms.) CPUs are often classified into "nodes," which represent technology generations: a chip at a new node (e.g., "5 nm" released in 2020) contains approximately double the transistor density as a previous node (e.g., "7 nm" released in 2018) and is also more cost-effective.

Market Size:

$56.2 billion (microprocessors) (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing SIA, IC Insights, TrendForce, financial statements)

Component Name:

Logic chip design: Discrete GPUs

Component ID: N2

Description:

Discrete graphics processing units ("GPUs") have long been used for graphics processing (for example, in video game consoles) and in the last decade have become the most used chip for training artificial intelligence algorithms. The United States monopolizes the design market for GPUs, including standalone "discrete GPUs," the most powerful GPUs.

Market Size:

$11.9 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing SIA, IC Insights, TrendForce, financial statements)

Component Name:

Logic chip design: FPGAs

Component ID: N3

Description:

Field-programmable gate arrays ("FPGAs"), unlike other chips, can be reprogrammed after deployment to suit specific calculations, such as executing particular algorithms. U.S. firms capture virtually the entire FPGA design market.

Market Size:

$5.7 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing SIA, IC Insights, TrendForce, financial statements)

Component Name:

Logic chip design: AI ASICs

Component ID: N4

Description:

Application-specific integrated circuits for artificial intelligence ("AI ASICs"), a rapidly growing category of logic chips, often achieve greater speed and efficiency for artificial intelligence than GPUs and FPGAs, but are usable only for specific algorithms. ASICs can be easier to design than CPUs, GPUs, and FPGAs, opening the field to a wide range of design startups, including in China. Still, few highly specialized ASICs have been widely commercialized, as their markets are often too small for recouping fixed development costs.

Component Name:

Crystal growing furnaces

Component ID: N8

Description:

Crystal growing furnaces and machining tools are necessary to produce all wafers-thin, disc-shaped materials fabs used to produce chips. The furnace forms a cylindrical ingot of silicon from polycrystalline raw silicon; machining equipment then cuts the ingot into wafers used for chip fabrication. These tools have relatively low value and complexity relative to other semiconductor manufacturing equipment. Japan, Germany, and Switzerland are the main producers.

Market Size:

$21 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Crystal machining tools

Component ID: N9

Description:

Crystal growing furnaces and machining tools are necessary to produce all wafers-thin, disc-shaped materials fabs used to produce chips. The furnace forms a cylindrical ingot of silicon from polycrystalline raw silicon; machining equipment then cuts the ingot into wafers used for chip fabrication. These tools have relatively low value and complexity relative to other semiconductor manufacturing equipment.

Market Size:

$110 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Wafer bonding and aligning tools

Component ID: N10

Description:

Wafer bonders and aligners join silicon wafers. In this visualization, these tools are included as an input to producing wafers, but they may also be used later in the production process, after chips are fabricated in the wafers. Austria, Germany, and the United States produce this equipment.

Market Size:

$140 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Wafer handlers

Component ID: N11

Description:

Wafer and photomask handlers store and transport wafers and photomasks in a fab. Japan, the United States, South Korea, Taiwan, and France produce these relatively less complex tools.

Market Size:

$1.3 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Photomask handlers

Component ID: N12

Description:

Wafer and photomask handlers store and transport wafers and photomasks in a fab. Japan, South Korea, Taiwan, and France produce these relatively less complex tools.

Market Size:

$99 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Ion implanters

Component ID: N17

Description:

Ion implanters embed dopant substances into silicon wafers to give different parts of the wafer different levels of semiconductivity to make functional transistors in chips. Different types of implanters are used for different purposes. Low-to-medium-current ion implanters and high-current ion implanters are most commonly used, with high-current ion implanters capable of greater throughput. Meanwhile, high-voltage ion implanters can implant ions deeply into silicon, and ultra-high-dose doping implanters can achieve greater dopant density than the other tools. The United States is the dominant producer of ion implanters, with Japan and Taiwan rounding out most of global market share.

Market Size:

about $1 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Advanced photolithography equipment

Component ID: N19

Description:

The Netherlands, Japan, and a small number of other countries are the dominant producers of lithography equipment, critical for the production of chips and photomasks. In particular, the Netherlands and Japan are exclusive providers of advanced photolithography scanners, necessary for mass-production of advanced chips.

Photolithography scanners use ultraviolet light to draw intricate, nanoscale patterns into semiconductor wafers, creating the billions of tiny circuits contained in a single advanced logic chip. An extreme ultraviolet (EUV) scanner refracts a beam of 13.5 nm ultraviolet light through a photomask, transferring that pattern to a photoresist chemical applied as a layer on the chip. The light dissolves parts of the photoresist in the circuit pattern. The newly created photoresist pattern is etched into a permanent chip substrate below the photoresist. Throughout this process, the scanner precisely moves the wafer and the photomask helps build the design.

Component Name:

EUV scanners

Component ID: N20

Description:

EUV scanners are the most advanced photolithography equipment currently used in mass semiconductor production. They are the only tools combining leading-edge precision (by producing light with small wavelengths) with high throughput (by using photomasks), and are necessary for mass-producing the most advanced logic chips. They are exclusively built by the Dutch firm ASML. A single EUV scanner costs well over $100 million, ships in 40 freight containers and contains about 100,000 individual parts.

Market Size:

$3.1 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

ArF scanners

Component ID: N21

Description:

ArF scanners and ArF immersion scanners are among the most advanced photolithography equipment currently used in mass semiconductor production, second only to EUV scanners. EUV and ArF immersion scanners are the only lithography tools capable of mass-producing chips at near-cutting edge scale (the absolute cutting edge requires EUV). Only the Dutch firm ASML and the Japanese firm Nikon produce ArF scanners or ArF immersion scanners capable of mass production.

Market Size:

$780 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

ArF immersion scanners

Component ID: N22

Description:

ArF scanners and ArF immersion scanners are among the most advanced photolithography equipment currently used in mass semiconductor production, second only to EUV scanners. EUV and ArF immersion scanners are the only lithography tools capable of mass-producing chips at near-cutting edge scale (the absolute cutting edge requires EUV). Only the Dutch firm ASML and the Japanese firm Nikon produce ArF scanners or ArF immersion scanners capable of mass production.

Market Size:

$5.8 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Photolithography

Component ID: N25

Description:

In photolithography, light is used to draw patterns into semiconductor wafers, creating the tiny circuits that comprise logic chips. A photolithography tool passes light through a photomask-a transparent plate with a circuit pattern-to transfer that pattern to a wafer coated with photoresist chemical. (Photomasks are themselves made with lithography tools.) The light dissolves parts of the photoresist according to the circuit pattern.

Advanced photolithography is critical to mass production of cutting-edge semiconductors. It requires enormously complex, expensive equipment supplied by only a few vendors in Europe and Japan. The most sophisticated photolithography processes involve extreme ultraviolet (EUV) scanners, produced exclusively by the Dutch firm ASML.

Component Name:

Wafer

Component ID: N26

Description:

Silicon wafers are the basic building block for chip production. To produce them, a furnace forms a cylinder of silicon (or other semiconducting materials), which is then cut into disc-shaped wafers. These wafers are then processed, split and packaged into individual chips. Most wafers are made purely of silicon or another material, but others have more complex structures. Dopants, such as boron, aluminum, phosphorous, platinum or other elements, may be added to alter the level of semiconductivity.

300 mm wafers, produced by Japanese, Taiwanese, German, and Korean firms, are used to produce nearly all advanced chips today. Manufacturing the smoothest, high-purity 300 mm wafers-which are necessary for supporting the smallest chip feature sizes-requires considerable tacit know-how. Older-technology wafer sizes include 150 and 200 mm, used for chips with larger feature sizes.

Market Size:

$10.9 billion

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing CSET estimates based on financial statements and wafer production capacities)

Component Name:

Maskless lithography equipment

Component ID: N28

Description:

Maskless lithography equipment draws patterns in a substrate using laser light, electrons, or ions. Unlike photolithography equipment, maskless lithography tools work without masks. This allows them to quickly and cheaply make new patterns, but slows down the process of drawing patterns into the wafer. As a result, maskless lithography tools can cost-effectively produce low-volume items like photomasks, but are are ill-suited to mass chip production.

Component Name:

Electron-beam lithography tools

Component ID: N29

Description:

Electron-beam (or "e-beam") lithography tools draw patterns in a substrate using electrons. They are the dominant tools for photomask production, and are also infrequently used for low-volume chip production. Like other maskless lithography tools, e-beam tools can quickly and cheaply make new patterns, but are slow at drawing patterns into wafers, making them ill-suited to mass chip production.

Market Size:

$510 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Laser lithography tools

Component ID: N30

Description:

Laser lithography tools draw patterns in a substrate using laser light. They are sometimes used to produce photomasks (though less often than e-beam tools). Like other maskless lithography tools, laser lithography tools can quickly and cheaply make new patterns, but are slow at drawing patterns into wafers, making them ill-suited to mass chip production.

Market Size:

$85 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Photoresists

Component ID: N31

Description:

Photoresists are chemicals deposited on a wafer. When exposed to patterned light that has passed through a photomask, they selectively dissolve to form the circuit pattern. Etching is then performed in places where the photoresist has dissolved to transfer the circuit pattern permanently onto the wafer. Photoresists are specific to particular photolithography processes. Japanese firms are the leading producers.

Market Size:

$3.3 billion (all photoresists)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/)

Component Name:

Resist processing tools

Component ID: N32

Description:

Resist processing tools, also called "tracks," coat photoresists on wafers (typically by spin-coating, which spins the wafer to spread deposited photoresist), develop them (dissolve portions hit by light), and bake them (harden undissolved photoresist to prepare for etching). Japan is the sole producer of the most advanced tracks for EUV and ArF immersion photolithography; Germany, South Korea, the United States, and China produce less advanced equipment.

Component Name:

Advanced photomasks

Component ID: N33

Description:

Photomasks are transparent plates containing a circuit pattern to be fabricated in a chip. Photolithography equipment produces light that passes through this pattern so that the photomask's pattern is transferred to the chip. Each photomask is specific to one chip design. Photomasks are produced by captive mask shops (businesses within large semiconductor manufacturing firms) or merchant mask shops (which sell to semiconductor manufacturers). Japan, the United States, Taiwan, and South Korea lead production of leading-edge photomasks.

Market Size:

$4 billion (all photomasks)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/)

Component Name:

Deposition

Component ID: N35

Description:

In the deposition process, specialized tools are used to deposit thin films of materials on a silicon wafer. After lithography and etching, these films become different chip layers, including for transistors, interconnects (wires), and other elements.

Component Name:

Deposition tools

Component ID: N36

Description:

Deposition tools are used to deposit thin films of materials on a silicon wafer. After lithography and etching, these films become different chip layers, including for transistors, interconnects (wires), and other elements.

Component Name:

Plasma CVD tools

Component ID: N38

Description:

Plasma chemical vapor deposition tools are used to deposit for materials requiring low temperatures during the deposition process. They are mostly produced by American firms.

Market Size:

$3.5 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Low-pressure CVD tools

Component ID: N39

Description:

Low-pressure chemical vapor deposition tools are commonly used to deposit polysilicon, tungsten, titanium, and titanium nitride.

Market Size:

$1.4 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

High-temperature CVD tools

Component ID: N40

Description:

High-temperature chemical vapor deposition tools are used to deposit epitaxial layers (layers oriented in a particular way relative to underlying layers).

Market Size:

$970 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Atomic layer deposition tools

Component ID: N41

Description:

Atomic layer deposition (ALD) tools are particularly advanced chemical vapor deposition tools capable of depositing layers a single atom in thickness, and are essential for leading-edge chip designs.

Market Size:

$1.6 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Physical vapor deposition tools

Component ID: N42

Description:

Physical vapor deposition (PVD) tools vaporize a solid or liquid material, which then condenses onto a substrate. The primary PVD method is called "sputtering." The United States controls most of the PVD equipment market, with Japan capturing most of the rest.

Market Size:

$2.4 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Rapid thermal processing tools

Component ID: N43

Description:

Rapid thermal processing (RTP) is critical to several steps in chip manufacturing. RTP tools include lamps, lasers, or other mechanisms to quickly increase the temperature of a wafer in order to change its properties. For instance, RTP tools are used to activate materials (such as dopants in transistors) to change their properties, modify materials, or make deposited films denser to improve their properties. Some RTP tools provide heat for as long as multiple seconds (solely produced by the United States and South Korea); others provide it only for milliseconds (solely produced by the United States and Japan).

Market Size:

$560 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Tube-based diffusion and deposition tools

Component ID: N44

Description:

Tube-based diffusion and deposition systems are called "tube"-based because substrates are loaded in cylindrical chambers for processing, either causing diffusion of dopants into a wafer (tube diffusion systems) or depositing materials for particular applications (tube deposition systems).

Market Size:

$1.5 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Electrochemical coating tools

Component ID: N45

Description:

Electrochemical coating tools use electrolysis to deposit materials. A common application is to deposit copper (used for wiring in chips) across a wafer. However, other techniques, such as chemical vapor deposition, can also deposit copper for some applications.

Market Size:

$290 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Etch and clean

Component ID: N46

Description:

After photolithography creates a pattern in the photoresist coating a wafer, specialized tools etch the pattern into the permanent layer below the photoresist. The photoresist is then removed and the etched material cleaned off of the layer.

Component Name:

Chemical vapor deposition tools

Component ID: N47

Description:

Chemical vapor deposition (CVD) tools create a chemical vapor that deposits films on the wafer atom-by-atom or molecule-by-molecule. CVD is the most widely used deposition technique in chip fabrication. It is used to deposit most dielectrics (a type of insulator), silicon, and some metals.

Component Name:

Dry etching and cleaning tools

Component ID: N48

Description:

Etching and cleaning tools have two main types: dry and wet. Dry etching tools-using gases to etch the substrate-are the most commonly used tool, and are especially necessary for circuit features in advanced chips. Dry etching tools have advantages over wet tools: they are fast and can etch differently depending on the direction of etch ("anisotropic etching"), which enables fine-grained features with complex shapes.

The most advanced dry etching tools are called atomic layer etching (ALE) tools. These tools are important for multiple etching applications in the most advanced chips, and are produced by leading U.S., Japanese, and British firms. Though it doesn't produce ALE tools, Chinas AMEC produces dry etching tools that are perhaps the most advanced SME tools sold by any Chinese firm. They are used for leading Taiwanese chipmaker TSMCs 7 and 5 nm nodes, though not for the finest features, such as in complex transistor structures. Recognizing Chinas competitiveness in dry etching tools, the United States removed these tools from the Commerce Control List in 2016.

Component Name:

Wet etching and cleaning tools

Component ID: N49

Description:

Etching and cleaning tools have two main types: dry and wet. Wet etching tools, using liquids, are less commonly used, and largely for cleaning wafers. Wet etching has advantages compared to dry etching-it is cheaper, risks less damage to substrates, and is more selective, i.e., it can etch a particular material without unintentionally etching nearby materials. However, it is slower and typically cannot etch differently depending on the direction of etch, making it difficult to form complex structures. Therefore, wet etching is not typically used for etching the smallest features in advanced chips.

Market Size:

$3.2 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Conductor etching tools

Component ID: N50

Description:

The main types of dry etching tools are used either for etching conductors or dielectrics. Major subtypes of conductor and dielectric dry etching tools include sputter etching and plasma etching; plasma etching is further divided into reactive ion etching and deep reactive ion etching (a form of reactive ion etching used to make deep wells). The most commonly used form is reactive ion etching.

Market Size:

$6.5 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Dielectric etching tools

Component ID: N51

Description:

The main types of dry etching tools are used either for etching conductors or dielectrics. Major subtypes of conductor and dielectric dry etching tools include sputter etching and plasma etching; plasma etching is further divided into reactive ion etching and deep reactive ion etching (a form of reactive ion etching used to make deep wells). The most commonly used form is reactive ion etching.

Market Size:

$4.3 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Etching and cleaning tools

Component ID: N55

Description:

Etching tools create permanent patterns in chips: after photolithography removes portions of a photoresist deposited on a wafer in a precise pattern, etching tools etch that pattern into a permanent substrate below. Cleaning tools then remove etched materials.

The United States and Japan are the main producers of etch and clean equipment; South Korea and China are also significant suppliers.

Component Name:

Chemical mechanical planarization

Component ID: N57

Description:

After etching and cleaning, the wafer surface is flattened in a process called chemical mechanical planarization (CMP) to allow a new layer of features to be added. CMP tools are critical for chip fabrication, but not as complex as other tools, such as lithography and deposition tools.

Component Name:

Wafer and photomask handling

Component ID: N59

Description:

Storing and transporting wafers and photomasks in a fab requires specific equipment. Although specialized, this equipment is less complex than other tools used in semiconductor manufacturing.

Component Name:

Process control

Component ID: N60

Description:

In semiconductor fabrication, process control involves precisely monitoring wafers, photomasks, and the overall chip manufacturing process to ensure consistency and low manufacturing error rates. Accordingly, process control tools are among the most essential and valuable semiconductor manufacturing equipment.

Component Name:

Wafer inspection equipment

Component ID: N61

Description:

Even the tiniest imperfections can cause serious problems during chip production. Major types of wafer inspection tools include film and wafer measuring tools, critical dimensions measuring tools, defect inspection tools, general-purpose microscopes, and structural inspection tools.

Component Name:

Photomask inspection and repair tools

Component ID: N62

Description:

Photomask inspection and repair tools are similar to those used in wafer inspection, such as microscopes.

Market Size:

$940 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Wafer level packaging inspection tools

Component ID: N63

Description:

These tools inspect parts of wafers that package fabricated chips (dies) before these wafers are "diced" (i.e., cut) into multiple chips.

Market Size:

$200 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Process monitoring equipment

Component ID: N64

Description:

Process monitoring tools, such as curve tracers, are relatively low-value equipment used to measure performance of devices fabricated in wafers during chip manufacturing.

Market Size:

$79 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Film and wafer measuring tools

Component ID: N65

Description:

Film and wafer measuring tools include tools to measure film thickness, makeup, and stack (such as Fourier-transform infrared spectrometers, ellipsometers, opto-acoustic tools, and x-ray tools) and tools to measure wafer surfaces, taper, warpage, and bow (such as wafer flatness mapping tools, surface profiling tools, optical instruments," and atomic force microscopes).

Market Size:

$540 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Critical dimensions measurement tools

Component ID: N66

Description:

Critical dimensions measuring tools (including optical tools and scanning electron microscopes) measure device dimensions and ensure alignment between a photomask and wafer during photolithography.

Market Size:

$1.6 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Defect inspection tools

Component ID: N67

Description:

Defect inspection tools include brightfield inspection tools (using light to scan the wafer), darkfield inspection tools (using lasers), e-beam inspection tools (using electrons), and optical and scanning electron microscopes.

Market Size:

$3 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

General-purpose microscopy tools

Component ID: N68

Description:

General-purpose microscopes used in semiconductor manufacturing include scanning electron microscopes and transmission electron microscopes.

Market Size:

$200 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Assembly and packaging

Component ID: N69

Description:

At the end of the fabrication process, the finished wafer contains dozens of chips in a grid pattern. During assembly and packaging, the wafer is separated into individual chips, or "dies". Each chip is mounted on a frame with wires that connect the chip to external devices, and enclosed in a protective casing. This produces the familiar look of a dark gray rectangle with metal pins at the edges.

Component Name:

Assembly inspection tools

Component ID: N70

Description:

Assembly inspection tools inspect dies, bonding, packages, or wafers for defects throughout the packaging process.

Market Size:

$270 million (2019)

Component Name:

Dicing tools

Component ID: N71

Description:

Dicing tools cut individual chips (dies) in the wafer into separated chips. This process also involves thinning the wafer. Dicing tools include blade saws, laser saws, dicing accessories and backside grinding equipment.

Market Size:

$690 million (2019)

Component Name:

Bonding tools

Component ID: N72

Description:

Bonding tools include die attach tools (to connect dies to lead frames or substrates), wire bonders (to make interconnects between lead frames and die pads), and advanced interconnect tools.

Component Name:

Die attaching tools

Component ID: N73

Description:

Die attaching tools are bonding tools used to connect individual chips, or "dies," to lead frames or substrates.

Market Size:

$800 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Wire bonding tools

Component ID: N74

Description:

Wire bonders are bonding tools used to make interconnects between lead frames and die pads.

Market Size:

$550 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Advanced interconnect tools

Component ID: N75

Description:

Advanced interconnect tools include various bonding tools other than die attach tools and wire bonders.

Market Size:

$68 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Packaging tools

Component ID: N76

Description:

Packaging tools encase dies (individual chips) in packages.

Market Size:

$550 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Integrated assembly tools

Component ID: N77

Description:

Integrated assembly tools integrate different packaging systems.

Market Size:

$34 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Testing

Component ID: N78

Description:

Chips undergo tests requiring a range of specialized equipment, including system-on-a-chip test tools, linear and discrete devices, burn-in tools, and handlers and probers.

Component Name:

SoC test equipment

Component ID: N80

Description:

SoC test tools can test logic, memory, mixed, and analog circuits. As a result, they can test a wide variety of chips, including advanced logic chips like GPUs and other processors.

Market Size:

$2.7 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Burn-in test equipment

Component ID: N81

Description:

Burn-in tools heat devices to check if defects cause the devices to fail.

Market Size:

$220 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Linear and discrete testing tools

Component ID: N82

Description:

Linear testing devices include, for example, operational amplifiers and voltage regulators.

Market Size:

$96 million (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Handlers and probes

Component ID: N83

Description:

Handlers and probes link test tools and tested devices.

Market Size:

$1.8 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Electronic design automation software

Component ID: N84

Description:

Until the 1970s, when chips included few electric components, engineers drew designs manually. Today, chips include billions of interconnected transistors and other electrical components. To manage this complexity, chip designers use sophisticated EDA software to produce logic chip designs.

Only U.S. firms can produce EDA software with the full-spectrum capabilities engineers need to design leading-edge chips. Although the industry is top-heavy, startups frequently enter the EDA space. However, they struggle to compete with top EDA firms that typically acquire them to incorporate the startups' niche functionality to their full-spectrum capabilities.

Market Size:

$6.8 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing Mentor Graphics, Journal of Microelectronic Manufacturing, IPNest, BCG)

Component Name:

Core intellectual property

Component ID: N85

Description:

Core intellectual property (IP) consists of reusable, modular design blocks that chip design firms license for use in their designs. U.S. and U.K. vendors dominate the core IP market; some firms specialize exclusively on core IP, while others combine their offerings with EDA tools. The company ARM is the top core IP vendor, providing an instruction set architecture (ISA) and associated core IP underpinning most of the world's smartphone processors.

Market Size:

$3.9 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing Mentor Graphics, Journal of Microelectronic Manufacturing, IPNest, BCG)

Component Name:

Chemical mechanical planarization tools

Component ID: N86

Description:

After other steps like etching and cleaning, chemical mechanical planarization (CMP) tools flatten the wafer surface. CMP tools are critical for chip fabrication, but not as complex as other tools, such as lithography and deposition tools.

Market Size:

$1.4 billion (2019)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing VLSI Research)

Component Name:

Deposition materials

Component ID: N88

Description:

Deposition materials include materials such as sputtering targets, which are used in physical vapor deposition. In this process, argon ions are fired at the target, whose atoms are stripped off and deposited as a thin film on the wafer. Other deposition materials can be used to form interconnects, which are wires that connect devices within a chip, or for deposition of insulators that form layers within transistors and also between interconnects.

Many other materials used in deposition are simply purified versions of raw materials such as aluminum, copper, tantalum, and titanium.

Market Size:

$1 billion (sputtering targets)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/)

Component Name:

CMP materials

Component ID: N90

Description:

Chemical mechanical planarization (CMP) is a process that makes layers produced during fabrication flat so lithography can successfully be performed on them. The highest-value materials used in chemical mechanical planarization are chemical slurries, which often include rare earth minerals, and polishing pads. During fabrication, a wafer is placed on the pad along with the slurry, and a polishing head presses against the wafer and rotates to planarize the wafer.

Market Size:

$2.5 billion (slurries and pads)

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/)

Component Name:

Electronic gases

Component ID: N91

Description:

Gases are widely used in semiconductor fabrication, including common gases like nitrogen, hydrogen, helium, argon helium, and carbon dioxide as well as speciality electronic gases like nitrogen trifluoride, tungsten hexafluoride, hydrogen chloride, ammonia, disilane, germane, high-purity carbon dioxide, and nitrous oxide. In particular, the photolithography process uses various noble gases, such as neon, argon, and krypton, to create lasers to draw circuit patterns on wafers. (However, the most advanced photolithography equipment, EUV, uses a tin light source rather than a gas-based light source.)

Market Size:

$6 billion

Source:

[CSET](https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/) (citing SEMI)

Component Name:

Wet chemicals

Component ID: N92

Description:

Wet chemicals, such as sulfuric acid, isopropyl alcohol, ammonium hydroxide, phosphoric acid, nitric acid, hydrochloric acid, and acetic acid, are widely used in semiconductor manufacturing.

Component Name:

Lead frames

Component ID: N93

Description:

A lead frame transfers data between a chip and external devices.

Component Name:

Bond wires

Component ID: N94

Description:

A bond wire, typically made of aluminum, copper, silver, or gold, attaches the chip to a lead frame.

Component Name:

Ceramic packages

Component ID: N95

Description:

Protective ceramic packages, plastic substrates, or encapsulant resins may be bonded to a chip during the packaging process.

Component Name:

Substrates

Component ID: N96

Description:

Protective ceramic packages, plastic substrates, or encapsulant resins may be bonded to a chip during the packaging process.

Component Name:

Encapsulation resins

Component ID: N97

Description:

Protective ceramic packages, plastic substrates, or encapsulant resins may be bonded to a chip during the packaging process.

Component Name:

Die attach materials

Component ID: N98

Description:

Die attach materials, including polymers and eutectic alloys, are used to attach chips to packages or substrates.

Component Name:

Finished logic chip

Component ID: N99

Description:

The production of a single logic chip often requires more than 1,000 steps, passing through international borders 70 or more times, before reaching an end customer. The result of this complex, $500 billion supply chain is a resource fundamental to virtually every aspect of modern life.

Component Name:

Packaging materials

Component ID: N100

Description:

Semiconductor packaging involves several steps to bond a fabricated chip to an encasing package, each requiring different materials. For example, a bond wire, typically made of aluminum, copper, silver, or gold, attaches the chip to a lead frame. The lead frame transfers data between the chip and external devices. A protective ceramic package, plastic substrate, or encapsulant resin can also be bonded to the chip. Die attach materials including polymers and eutectic alloys are used to attach the chip to packages or substrates.