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Assignment 5 CS 3339 – Spring 2019

Due: Friday, 4/12/18 @ 11:55pm

40 points (late until noon 11/10 -10 pts)

All submissions must be written in very neat handwriting and scanned (or typed) and submitted in PDF format to TRACS with the filename of Ax_netID.pdf. You may submit as many times as you like prior to the deadline; only the most recent submittal will be graded. All assignments must be submitted individually and reflect your own work; however, you are encouraged to work in groups and discuss the problems with your classmates.

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1) [6 points] Dissassemble `00100100 : 152affe6` (written as 32-bit MIPS addr:instr in hex)

0001 0101 0010 1010 | 1111 1111 1110 0110

9 10

bne $t1, $t2, 00011110

2) [6 points] Unroll the following loop four times and optimize the resulting instruction sequence. Assume the loop count is a multiple of four. Further assume the 5-stage MIPS pipeline with ID-stage branch resolution, and make sure that no bubbles need to be generated by the CPU. [Hint: There is a source dependency on $t0; be careful about bubbles from this!]

```
loop:  sw   $a1, 0($t0)
       addi $t0, $t0, 4
       bne  $t0, $a0, loop
```

```
sw a1, 0($t0)
addi $t0, $t0, 4
lw/sw
lw/sw
addi $t0, $t0, 4
lw/sw
lw/sw
addi $t0, $t0, 4
lw/sw
lw/sw
bne $t0, $a0, loop
```

3) [6 points] Pipeline implementations introduce three types of hazards. The MIPS architecture avoids structural hazards by including all necessary hardware. Complete the following statements with respect to the other two types of hazards.

Structural hazards exist when a prior instructions results are not available for a current instruction. These hazards are corrected by adding stall/lw/sw cycles. In order to gain back some performance forwarding paths are implemented.

Control hazards exist when the next instruction executed is not located at PC+4. These hazards are corrected using _____ cycles. In order to gain back some performance branch prediction is implemented.

4) [4 points] Assume a processor with a 2.0 GHz clock. The cache has a base cache access time (including hit detection) of 1 clock cycle, and L1 miss penalty of 10 cycles, and an L2 miss penalty of 40 cycles. Assume that 8% of read accesses to the L1 data cache miss and that 20% of read accesses to the L2 miss Compute the average number of clock cycles required for a load instruction.

$1+(.08 \cdot 10)+(.08 \cdot .2 \cdot 40) = 2.44$

What is the average memory access time per load instruction in nanoseconds?

$\frac{2.44}{2 \cdot 10^9} = 1.22 \text{ nanoseconds}$

5) [4 points] A 4-way set associative write-back cache is implemented on a system with 32-bit words and addresses. It is organized with 16 words per block and has a total of 64 blocks. Show how the address bits A[31] to A[0] would map to the tag, index, word offset, and byte offset fields.

tag | word offset | byte offset | index

$\leftarrow A_{31} \mid A_{30} A_{29} A_{28} A_{27} \mid A_{26} A_{25} A_{24} \mid A_{23} A_{22} A_{21} A_{20}$

6) [4 points] Describe a pattern of memory access that would exhibit the types of locality listed below.

Temporal Locality

If data was repeatedly being accessed in a certain location, that data is higher in hierarchy

Spatial Locality

If data is recently used, then data nearby will be accessed. Ex: incrementing elements of array.

7) [4 points] Even without prefetching it is possible for the first-ever access to a word to hit in the cache. What allows this to happen?

No, the cache doesn't have anything in it, so it will never be able to get a hit

8) [6 points] Given a direct mapped cache with one word per block and four blocks with the following accesses, circle the cycles/addresses that are cache hits.

`0x0, 0x18, 0xC, 0x20, (0x18,) 0x38, (0xC,) 0x18, (0x20,) 0x38`

What is the hit ratio?

$\frac{3}{10} = .3$