Name Zachary Golla Assignment 1 CS 3339 – Spring 2019

netID ztg5 Due: Friday, 2/1/19 @ 11:55pm

(email not long Axxxxx number) 40 points (late until noon 2/2 -10 points)

All submissions must be written in very neat handwriting and scanned (or typed) and submitted in PDF format to TRACS with the filename of Ax_netID.pdf. You may submit as many times as you like prior to the deadline; only the most recent submittal will be graded. All assignments must be submitted individually and reflect your own work; however, I encourage you to work in groups and discuss the problems with your classmates.

Questions are 4pts each unless otherwise noted – you must show work to support your answers.

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1) Circle RISC or CISC for each of the statements below.
   - RISC / CISC Came first. i.e. was the first technique used for Instruction Set Architectures.
   - RISC / CISC Is easier to implement in hardware.
   - RISC / CISC Would have fewer machine instructions and higher code density.
   - RISC / CISC Is the type of ISA most likely being run on a server in a datacenter.

2) You fell into the hot tub time machine and find yourself back in 1986. Current chips have 140,000 transistors and your boss wants to know how many transistors are likely to be on a chip 10 years from now. Grab a Jolt Cola, pop Peter Gabriel's new 'So' album in the Sony Discman and get calculating. Your answer is? [Assume Gordon Moore said "... every 2 years"] currently 140,000. Moore's Law says double every 2 years, so: $(140{,}000) \cdot 2^5 = 14{,}480{,}000$

3) Welcome back to 2019. According to https://hothardware.com/reviews/amd-ryzen-threadripper-2950x-and-2990wx-review?page=8 the "beastly" AMD Threadripper 2990WX has 19.2 billion transistors. If you built a giant size model of the die with the transistors arranged in an n x n grid and each transistor was 145mm x 68mm (about the size of the Google Pixel 3 phone) what would be the model's width & length in meters?

Consider, 19.2 billion transistors,
∴ for n x n die $n = \sqrt{19.2 \text{ billion}}$.
That is, $n = 138{,}564.06$

So, width = 145mm · 138,564.06 = 20,091.79 meters
length = 68mm · 138,564.06 = 9,422.36 meters

4) Transistor scaling has continued to allow more transistors per CPU die with each new chip generation. Starting in 2004, the additional transistors have been primarily used to:
   a) add more pipeline stages
   b) increase the precision of floating point calculations
   c) add non-volatile (flash) storage
   d) put multiple CPU cores on each chip
   e) spread out the heat generated

1) D

5) Why did processor clock speeds, which had increased for decades, finally stop increasing around year 2004?
   a) Environmental regulations required yearly power reductions
   b) The higher frequencies interfered with cellular and WiFi radios
   c) Processors were already memory bound so higher frequencies didn't improve performance
   d) The inability to lower voltages further causes the processors to consume too much power
   e) Silicon atoms have a fundamental limitation oscillating above 4 GHz

1) D

6) The Raspberry Pi 3 B+ runs at a max clock frequency of 1.4 GHz. Calculate the cycle time in picoseconds. For fun reference https://www.raspberrypi.org/products/raspberry-pi-3-model-b-plus/

$\text{cycle time} = \frac{1}{\text{clock frequency}} \Rightarrow \text{cycle time} = \frac{1}{1.4 \times 10^9 \text{ GHz}}$

= 714.28 picoseconds

7) Your code executes a 4 million instruction sequence with a CPI of 2, followed by a 6 million instruction sequence with a CPI of 4, followed another 4 million instruction sequence with a CPI of 2. What is the CPI of the full code? Express answer to 2 decimal places.

8 million cycles + 24 million cycle + 8 millions cycles

So, full code is 40 million cycles with 14 million instructions.

That is, $CPI = \frac{40,000,000}{14,000,000} = 2.857$

8) Calculate the average CPI of a processor where 35% of the instructions take 1 cycle to execute, 20% take 2 cycles, 20% take 3 cycles, 15% take 4 cycles, and 10% take 5 cycles. Express answer to 2 decimal places.

Say 1000 instructions, so,

350 in 1 cycles
200 in 2 cycles
200 in 3 cycles
150 in 4 cycles
100 in 5 cycles

+350
+400
+600
+600
+500
2450

That is

2450 cycles / 1000 instructions

= 2.45 average CPI

9) Processor A has a clock speed of 1.5 GHz and 4 classes of instructions, with CPIs of 1, 2, 3, and 4 respectively. Processor B has a clock speed of 2.0 GHz and the same 4 classes of instructions, with CPIs of 2, 3, 4, and 5. If the number of instructions executed in a program is divided equally among the 4 classes of instructions, which processor is faster and by how much? Express your answer as ratio e.g. 2.1x faster. *Hint: choose a number of instructions so you can use the classic performance equation on L1 slide 24*

Let number of instructions per each class of instruction = 16 million, so 4 million instructions

$\text{Instructions}_A = 16\text{mil}$ $A_{CPI} = 2.5$ cycle time $_B = .5\text{ns}$

$\text{Instructions}_B = 16\text{mil}$ $B_{CPI} = 3.5$ cycle time $_A = .666\text{ns}$

So, $\text{CPU}_A = (16 \cdot 10^6)(2.5)(.666 \times 10^{-9})$

$= 6.66\text{ms}$

$\text{CPU time}_B = (16 \cdot 10^6)(3.5)(.5 \times 10^{-9})$

$= 7\text{ms}$

∴ processor B is 1.05x faster than processor A.

10) Dynamic Voltage and Frequency Scaling (DVFS) is a technique widely used to lower power, especially in large datacenters. In order to conserve electricity both the frequency and voltage of the processor are reduced. If a processor using 200W of power running at 2V and 4 GHz is reduced to 1.5V at 2GHz how much power in Watts will be saved? [Note: Assume 100% of power is dynamic – ignore leakage power]
Hint – see L1 slide 21, the capacitance if a function of the chip and will not change with voltage or freq.

Ignore leakage power,

$\therefore P = \frac{1}{2} C V_{DD}^2 f$

We know the processor A uses 200W at 2V and 4GHz.

That is, $200 = \frac{1}{2} C (2)^2 \cdot 4\text{GHz}$

$\Rightarrow 100 = (4 \times 10^9) C$

$\frac{25}{10^9} = C$

So, if the voltage is reduced to $\frac{1}{2}$ and frequency 2GHz,

$P = \frac{1}{2}\left(\frac{25}{10^9}\right)\left(\frac{2}{2}\right)^2 \cdot (2 \cdot 10^9)$

$= \frac{1}{2}(25)\left(\frac{9}{4}\right)2 = \frac{25 \cdot 9}{4} = \frac{225}{4}$

$= 56.25$ *

* If the first power was 200 W and now power is 56.25, then,

200 − 56.25 = 143.75W will be saved.