

CSCI 223 Computer Org. & Assembly Language

Homework #8

Name:

Due: 9:30am on Thursday 4/4/2024

Submission: Type your answer using any text editor (no handwriting) and upload the file to the Blackboard. No late submission will be accepted

Suppose we have a system with the following properties:

- The memory is byte addressable
- Memory accesses are to 1-byte words (not to 4-byte words)
- Addresses are 12 bits wide
- The cache is 2-way set associative with a 4-byte block size and 4 sets

The contents of the cache are as follows, with all addresses, tags, and values given in hexadecimal notation:

Set index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	00	1	40	41	42	43
	83	1	FE	97	CC	D0
1	00	1	44	45	46	47
	83	0	--	--	--	--
2	00	1	48	49	4A	4B
	40	0	--	--	--	--
3	FF	1	9A	C0	03	FF
	00	0	--	--	--	--

A. The following diagram shows the format of an address (one bit per box). Indicate (by labeling the diagram) the fields that would be used to determine the following:

- CO The cache block offset
CI The cache set index
CT The cache tag

11	10	9	8	7	6	5	4	3	2	1	0

B. For each of the following memory accesses indicate if it will be a cache hit or miss when **carried out in sequence** as listed. Also give the value of a read if it can be inferred from the information in the cache. Show your work or no point will be given.

Operation	Address	Hit?	Read value (or unknown)
Read	0x834		
Write	0x836		
Read	0xFFD		