# EE 502

# Computer Architecture

## Lab Assignment #3

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Electrical and Computer Engineering

Temple University

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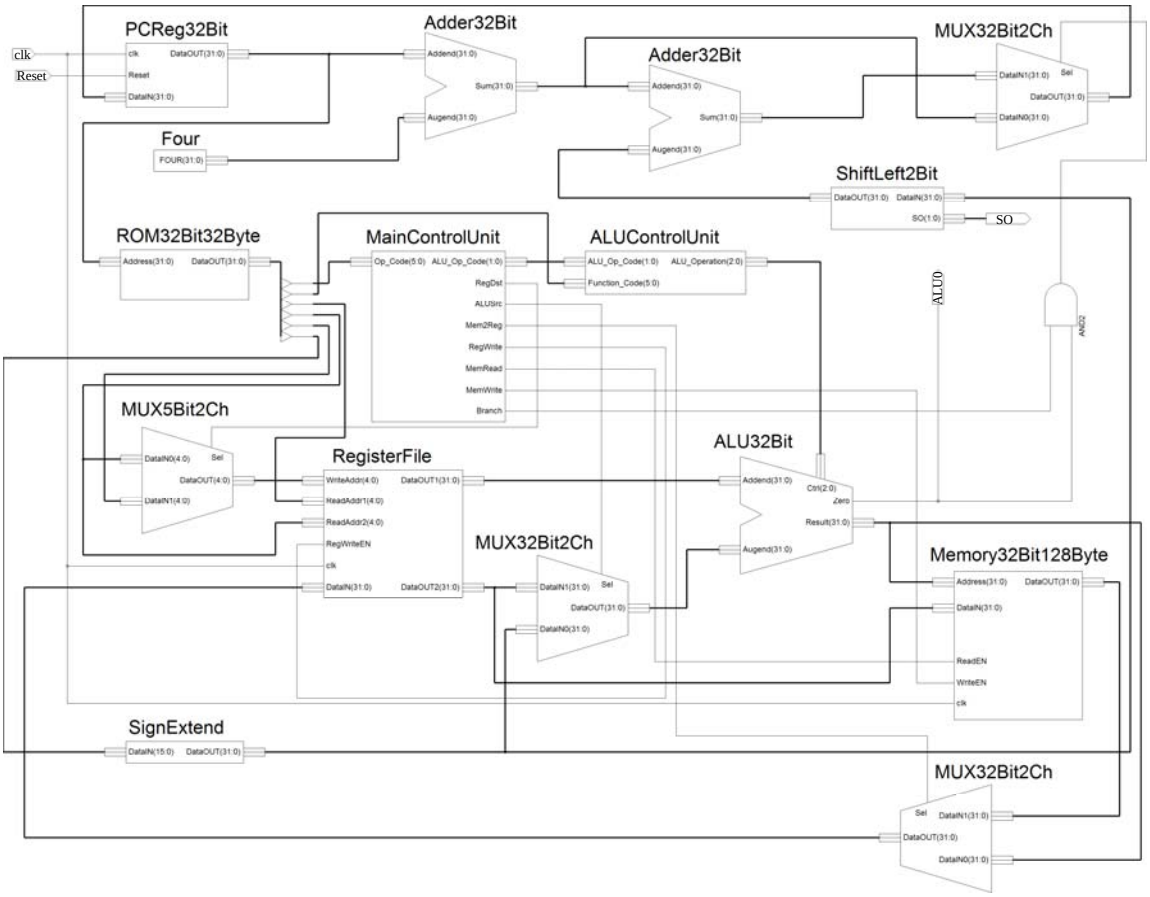
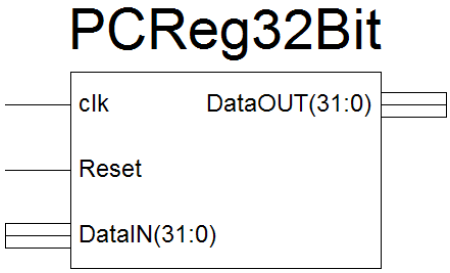
1. **(150 points) Use Verilog or VHDL to implement a functional Single-Cycle Computer with the simplified MISP ISA described in the textbook.**

### 1.1 Top-level block diagram of the design.




### 1.2 Design source codes in Verilog/VHDL with comments whenever possible.

#### 1.2.1 Program Counter (PC)




```
//////////////////////////////////////////////////////////////////////////////////
// Company:           Temple University
// Student:           Zexi Liu
// Create Date:       12:12:53 03/07/2007
// Design Name:       Single Cycle Computer
// Module Name:       PC    Reg32Bit
// Project Name:      Single Cycle Computer
// Target Devices:    Spartan-3 XC3S400
// Tool versions:     Xilinx ISE 8.2i
// Description:       32-bit      Register for PC
//////////////////////////////////////////////////////////////////////////////////
module PC Reg32Bit(DataIN, DataOUT, clk,        Reset);
      input       clk;
      input       Reset;
      input       [31:0] DataIN;
      output      [31:0] DataOUT;
      Reg         [31:0] DataOUT;
```

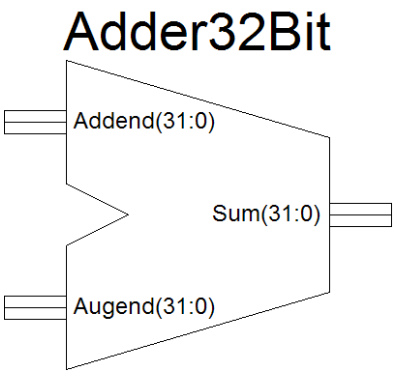
```
    always @(negedge clk or negedge      Reset)
    begin
        if(   Reset == 0)
            DataOUT <= 0;
        else
            DataOUT <= DataIN;
    end
endmodule
```

### 1.2.2 32-bit Adder

```
//////////////////////////////////////////////////////////////////////////////////
// Company:          Temple University
// Student:          Zexi Liu
// Create Date:      11:12:08 03/07/2007
// Design Name:      Single Cycle Computer
// Module Name:      Adder32Bit
// Project Name:     Single Cycle Computer
// Target Devices:   Spartan-3 XC3S400
// Tool versions:    Xilinx ISE 8.2i
// Description:      This is a 32-bit adder
//////////////////////////////////////////////////////////////////////////////////
module Adder32Bit(Addend, Augend, Sum);
    input [31:0] Addend;
    input [31:0] Augend;
    output [31:0] Sum;

    assign Sum = Addend + Augend;

endmodule
```

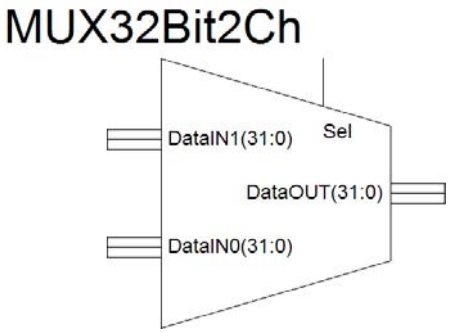



### 1.2.3 32-bit 2-1 Multiplexer

```
//////////////////////////////////////////////////////////////////////////////////
// Company:          Temple University
// Student:          Zexi Liu
// Create Date:      11:22:54 03/07/2007
// Design Name:      Single Cycle Computer
// Module Name:      MUX32Bit2Ch
// Project Name:     Single Cycle Computer
// Target Devices:   Spartan-3 XC3S400
// Tool versions:    Xilinx ISE 8.2i
// Description:      32-bit MUX
//////////////////////////////////////////////////////////////////////////////////
module MUX32Bit2Ch(Sel, DataIN0, DataIN1, DataOUT);
    parameter bitwidth = 32;
    input [bitwidth-1:0] DataIN0;
    input [bitwidth-1:0] DataIN1;
    input Sel;
    output [bitwidth-1:0] DataOUT;

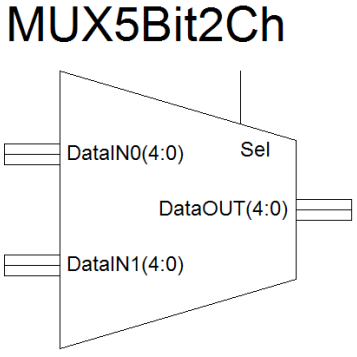
    assign DataOUT = Sel ? DataIN1 : DataIN0;

endmodule
```




### 1.2.4 5-bit 2-1 Multiplexer

```
//////////////////////////////////////////////////////////////////////////////////
// Company:          Temple University
// Student:          Zexi Liu
// Create Date:      22:44:05 03/07/2007
// Design Name:      Single Cycle Computer
// Module Name:      MUX5Bit2Ch
// Project Name:     Single Cycle Computer
```

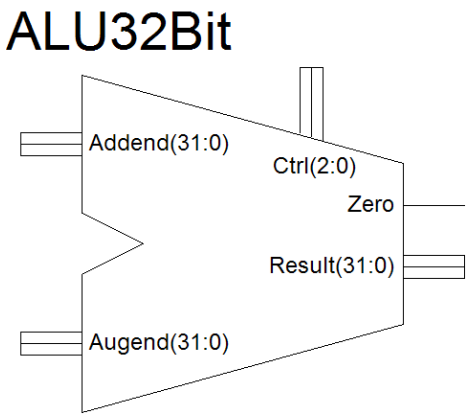


```
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         5-bit MUX
//////////////////////////////////////////////////////////////////////////////
module MUX5Bit2Ch(Sel, DataIN0, DataIN1, DataOUT);
    parameter bitwidth = 5;
    input [bitwidth-1:0] DataIN0;
    input [bitwidth-1:0] DataIN1;
    input Sel;
    output [bitwidth-1:0] DataOUT;

    assign DataOUT = Sel ? DataIN1 : DataIN0;

endmodule
```

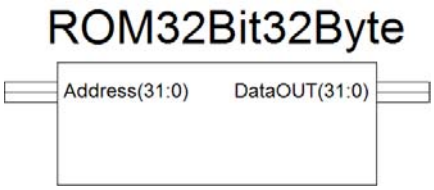
### 1.2.5 32-bit ALU




```
//////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:         Zexi Liu
// Create Date:         11:25:48 03/05/2007
// Design Name:         Single Cycle Computer
// Module Name: ALU32Bit
// Project Name:  Single Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         This is a 32-bit ALU
//////////////////////////////////////////////////////////////////////////////
module ALU32Bit(Ctrl, Addend, Augend,    Result, Zero);
    input       [2:0]       Ctrl;
    input       [31:0]      Addend;
    input       [31:0]      Augend;
    output      [31:0]          Result;
    output      Zero;
        Reg     [31:0]          Result;
        Reg     Zero;
    always @(Addend or Augend or Ctrl or        Result)
    begin
        case (Ctrl)
            3'b000 :    Result = Addend & Augend;       // AND
            3'b001 :    Result = Addend | Augend;   // OR
            3'b010 :    Result = Addend + Augend;       // ADD
            3'b110 :    Result = Addend - Augend;  // SUBTRACT
            3'b111 :
                if (Addend < Augend)
                        Result = 32'd1;                 // SLT
                else
                        Result = 32'd0;             // SLT
            default :   Result = 32'hxxxxxxxx;
        endcase
        if (    Result == 32'd0)                        // Branch
            Zero = 1;
        else
            Zero = 0;
    end
endmodule
```

### 1.2.6 32-bit ROM

```
//////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         14:12:02 03/07/2007
// Design Name:         Single Cycle Computer
```




```
// Module Name: ROM32Bit32Byte
// Project Name:        Single Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         sto    Re the instructions
//////////////////////////////////////////////////////////////////////////////////
module ROM32Bit32Byte(Add    Ress, DataOUT);
    input [31:0] Add Ress;
    output [31:0] DataOUT;
        Reg [31:0] DataOUT;

    parameter BaseAdd    Ress = 25'd0; // Add    Ress that applies to this memory

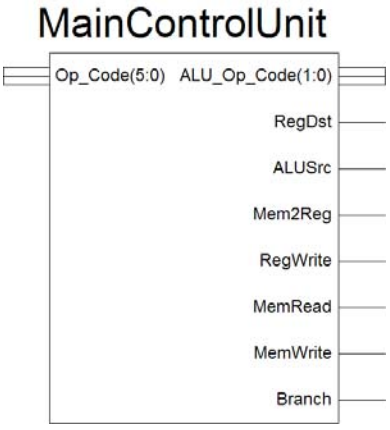
    wi    Re [4:0] MemoryOffset;
    wi    Re Add    RessSelect;

    assign MemoryOffset = Add Ress[6:2];    // to get word offset

    // Add      Ress decoding
    assign Add RessSelect = (Add      Ress[31:7] == BaseAdd      Ress);

    always @(Add    RessSelect or MemoryOffset)
    begin
        if ((Add    Ress % 4) != 0)
        begin
            $display($time, " rom32 error: unaligned Add Ress %d", Add    Ress);
        end
        if (Add    RessSelect == 1)
        begin
            case (MemoryOffset)
                5'd0 : DataOUT = { 6'd35, 5'd0, 5'd2, 16'd4 };          // lw $2, 4($0) # r2 = 1
                5'd1 : DataOUT = { 6'd35, 5'd0, 5'd3, 16'd8 };          // lw $3, 8($0) # r3 = 2
                5'd2 : DataOUT = { 6'd35, 5'd0, 5'd4, 16'd20 };         // lw $4, 20($0)    # r4 = 5
                5'd3 : DataOUT = { 6'd0, 5'd0, 5'd0, 5'd5, 5'd0, 6'd32 }; // add $5, $0, $0 # r5 = 0
                5'd4 : DataOUT = { 6'd0, 5'd5, 5'd2, 5'd5, 5'd0, 6'd32 }; // add $5, $5, $2 # r5 = r5 + 1
                5'd5 : DataOUT = { 6'd0, 5'd4, 5'd5, 5'd6, 5'd0, 6'd42 };    // slt $6, $4, $5 # r5 >= 5?
                5'd6 : DataOUT = { 6'd4, 5'd6, 5'd0, -16'd3 };  // beq $6, $zero -3 # if not go back 2
                5'd7 : DataOUT = { 6'd43, 5'd0, 5'd5, 16'd0 }; // sw $5, 0($zero) # MEM[0] = $5 = 6
                default DataOUT = 32'hxxxx;
            endcase
            $display($time, "       Reading data: rom32[%h] => %h", Add Ress, DataOUT);
        end
    end
endmodule
```

### 1.2.7 Main Control Unit




```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         14:38:19 03/07/2007
// Design Name:         Single Cycle Computer
// Module Name:         Main Control Unit
// Project Name:        Single Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         Generate main control signal
//////////////////////////////////////////////////////////////////////////////////
module MainControlUnit(Op_Code,      RegDst, ALUSrc, Mem2      Reg,
    RegWrite, Mem  Read, MemWrite, Branch, ALU_Op_Code);
    input       [5:0] Op_Code;
    output      RegDst;
    output      ALUSrc;
    output      Mem2Reg;
```

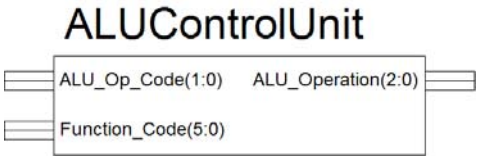
```
output      RegWrite;
output      MemRead;
output      MemWrite;
output      Branch;
output      [1:0] ALU_Op_Code;
Reg         RegDst;
Reg         ALUSrc;
Reg         Mem2Reg;
Reg         RegWrite;
Reg         MemRead;
Reg         MemWrite;
Reg         Branch;
Reg         [1:0] ALU_Op_Code;

parameter R_FORMAT      = 6'd0;
parameter LW            = 6'd35;
parameter SW            = 6'd43;
parameter BEQ           = 6'd4;

always @(Op_Code)
begin
      case (Op_Code)
            R_FORMAT :                    // R fomat instruction
            begin
                  RegDst          =     1'b1;
                  ALUSrc          =     1'b1;
                  Mem2Reg         =     1'b0;
                  RegWrite        =     1'b1;
                  Mem Read        =     1'b0;
                  MemWrite        =     1'b0;
                  Branch          =     1'b0;
                  ALU_Op_Code     =     2'b10;
            end
            LW :                          // load instruction
            begin
                  RegDst          =     1'b0;
                  ALUSrc          =     1'b0;
                  Mem2Reg         =     1'b1;
                  RegWrite        =     1'b1;
                  Mem Read        =     1'b1;
                  MemWrite        =     1'b0;
                  Branch          =     1'b0;
                  ALU_Op_Code     =     2'b00;
            end
            SW :                          // sto Re instruction
            begin
                  RegDst          =     1'bx;
                  ALUSrc          =     1'b1;
                  Mem2Reg         =     1'bx;
                  RegWrite        =     1'b0;
                  Mem Read        =     1'b0;
                  MemWrite        =     1'b1;
                  Branch          =     1'b0;
                  ALU_Op_Code     =     2'b00;
            end
            BEQ :                         // brance on equal instruction
            begin
                  RegDst          =     1'bx;
                  ALUSrc          =     1'b1;
                  Mem2Reg         =     1'bx;
                  RegWrite        =     1'b0;
                  Mem Read        =     1'b0;
                  MemWrite        =     1'b0;
                  Branch          =     1'b1;
```

```
                ALU_Op_Code     =   2'b01;
            end
            default :                   // default
            begin
                $display("Main_Control unimplemented Op_Code %d", Op_Code);
                RegDst          =   1'bx;
                ALUSrc          =   1'bx;
                Mem2Reg         =   1'bx;
                RegWrite        =   1'bx;
                Mem Read        =   1'bx;
                MemWrite        =   1'bx;
                Branch          =   1'bx;
                ALU_Op_Code     =   2'bxx;
            end
        endcase
    end
endmodule
```

### 1.2.8 ALU Control Unit




```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         14:31:57 03/07/2007
// Design Name:         Single Cycle Computer
// Module Name: ALU Control Unit
// Project Name:        Single Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         Generate ALU control signal
//////////////////////////////////////////////////////////////////////////////////
module ALUControlUnit(ALU_Op_Code, Function_Code, ALU_Operation);
    input [1:0] ALU_Op_Code;
    input       [5:0] Function_Code;
    output      [2:0] ALU_Operation;
        Reg  [2:0] ALU_Operation;

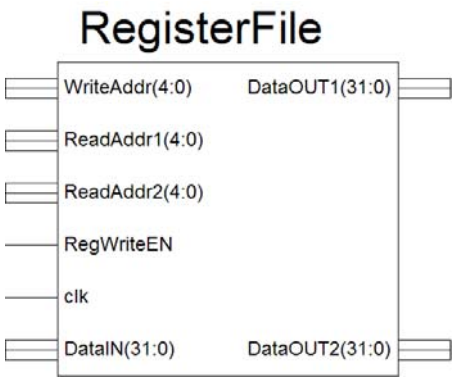
    // symbolic constants for instruction function code
    parameter Funct_add  =   6'd32;
    parameter Funct_sub  =   6'd34;
    parameter Funct_and  =   6'd36;
    parameter Funct_or   =   6'd37;
    parameter Funct_slt  =   6'd42;

    // symbolic constants for ALU Operations
    parameter ALU_add    =   3'b010;
    parameter ALU_sub    =   3'b110;
    parameter ALU_and    =   3'b000;
    parameter ALU_or     =   3'b001;
    parameter ALU_slt        =   3'b111;

    always @(ALU_Op_Code or Function_Code)
    begin
        case (ALU_Op_Code)
            2'b00 : ALU_Operation = ALU_add;                    // "+"
            2'b01 : ALU_Operation = ALU_sub;                    // "-"
            2'b10 :
                case (Function_Code)
                    Funct_add  : ALU_Operation = ALU_add;   // "+"
                    Funct_sub      : ALU_Operation = ALU_sub;   // "-"
                    Funct_and      : ALU_Operation = ALU_and;   // AND
                    Funct_or       : ALU_Operation = ALU_or;    // or
                    Funct_slt      : ALU_Operation = ALU_slt;   // slt
                    default        : ALU_Operation = 3'bxxx;  // default
```

```
                endcase
            default ALU_Operation = 3'bxxx;
        endcase
    end
endmodule
```

### 1.2.9 Register File




```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         13:55:00 03/07/2007
// Design Name:         Single Cycle Computer
// Module Name:         RegisterFile
// Project Name:        Single Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:                 Register file
//////////////////////////////////////////////////////////////////////////////////
module  RegisterFile(clk,       RegWriteEN,     ReadAddr1,
    ReadAddr2, WriteAddr, DataOUT1, DataOUT2, DataIN);
    input clk;
    input [31:0] DataIN;
    input       RegWriteEN;
    input [4:0] WriteAddr;
    input [4:0]     ReadAddr1;
    input [4:0]     ReadAddr2;
    output [31:0] DataOUT1;
    output [31:0] DataOUT2;

        Reg [31:0] DataOUT1, DataOUT2;
        Reg [31:0] File_Array [31:1];

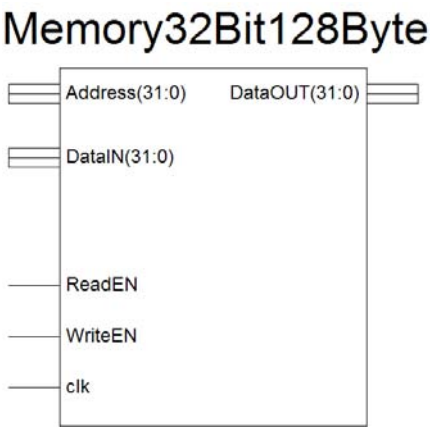
    always @(  ReadAddr1 or File_Array[    ReadAddr1])
    begin
        if (    ReadAddr1 == 0)
            DataOUT1 = 32'd0;     //$zero     Register = 0
        else
            DataOUT1 = File_Array[     ReadAddr1];
        $display($time, "       Reg_File[%d] => %d (Port 1)",     ReadAddr1, DataOUT1);
    end

    always @(  ReadAddr2 or File_Array[    ReadAddr2])
    begin
    if (    ReadAddr2 == 0)
        DataOUT2 = 32'd0;           //$zero     Register = 0
    else
        DataOUT2 = File_Array[     ReadAddr2];
        $display($time, "       Reg_File[%d] => %d (Port 2)",     ReadAddr2, DataOUT2);
    end

    always @(negedge clk)           // write    Register
    if (    RegWriteEN && (WriteAddr != 0))
    begin
        File_Array[WriteAddr] <= DataIN;
        $display($time, "       Reg_File[%d] <= %d (Write)", WriteAddr, DataIN);
    end
endmodule
```

### 1.2.10 Memory

```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:         Zexi Liu
```




```
// Create Date:            13:21:30 03/07/2007
// Design Name:            Single Cycle Computer
// Module Name: Memory32Bit128Byte
// Project Name:           Single Cycle Computer
// Target Devices:         Spartan-3 XC3S400
// Tool versions:          Xilinx ISE 8.2i
// Description:            Data memory
//////////////////////////////////////////////////////////////////////////////////
module Memory32Bit128Byte(clk,      ReadEN, WriteEN, Add
      Ress, DataIN, DataOUT);
      input       clk;
      input       ReadEN;
      input       WriteEN;
      input       [31:0] Add Ress;
      input       [31:0] DataIN;
      output      [31:0] DataOUT;
      Reg         [31:0] DataOUT;

      parameter BASE_ADD      RESS = 25'd0;
      Reg [31:0] Memory_Array [0:31];
      wi    Re [4:0] Memory_Offset;
      wi    Re Add    Ress_Select;
      assign Memory_Offset = Add      Ress[6:2];

      assign Add Ress_Select = (Add    Ress[31:7] == BASE_ADD  RESS);   // add   Ress decoding

      // for         ReadEN operations
      always @(  ReadEN or Add  Ress_Select or Memory_Offset or Memory_Array[Memory_Offset] or Add
      Ress)
      begin
            if (    ReadEN == 1'b1 && Add    Ress_Select == 1'b1)
            begin
                  if ((Add    Ress % 4) != 0)
                        $display($time, " rom32 error: unaligned add  Ress %h", Add   Ress);
                        DataOUT = Memory_Array[Memory_Offset];
                        $display($time, "       Reading data: Mem[%h] => %h", Add   Ress, DataOUT);
                  end
                  else
                        DataOUT = 32'hxxxxxxxx;
            end

      // for WriteEN operations
      always @(negedge clk)
      begin
            if (WriteEN == 1'b1 && Add      Ress_Select == 1'b1)
            begin
                  $display($time, " Writing data: Mem[%h] <= %h", Add   Ress, DataIN);
                  Memory_Array[Memory_Offset] <= DataIN;
            end
      end

      // initialize with some arbitrary values
      integer i;
      initial
      begin
            for (i=0; i<7; i=i+1)
                  Memory_Array[i] = i;
      end
endmodule
```

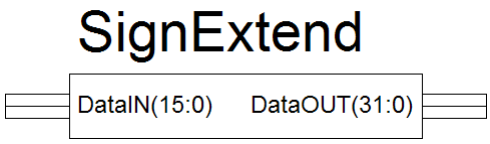
### 1.2.11 Sign Extend

```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
```

```
// Student:                Zexi Liu
// Create Date:            23:03:12 03/07/2007
// Design Name:            Single Cycle Computer
// Module Name: SignExtend
// Project Name:           Single Cycle Computer
// Target Devices:         Spartan-3 XC3S400
// Tool versions:          Xilinx ISE 8.2i
// Description:            sign extend
//////////////////////////////////////////////////////////////////////////////////
module SignExtend(DataIN, DataOUT);
        input [15:0] DataIN;
        output [31:0] DataOUT;
        wi     Re [31:0] DataOUT;

        assign DataOUT = { {16{DataIN[15]}}, DataIN };

endmodule
```

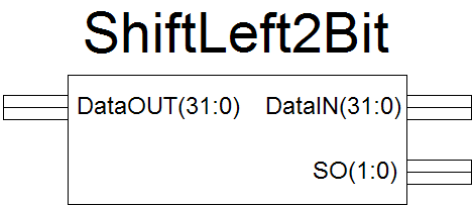



### 1.2.12 Shift Left 2 bits

```
//////////////////////////////////////////////////////////////////////////////////
// Company:                Temple University
// Student:          Zexi Liu
// Create Date:            22:49:04 03/07/2007
// Design Name:            Single cycle computer
// Module Name:            ShiftLeft2Bit
// Project Name:           Single cycle computer
// Target Devices:         Spartan-3 XC3S400
// Tool versions:          Xilinx ISE 8.2i
// Description:            Shift the input 32-bit data left by 2 bits
//////////////////////////////////////////////////////////////////////////////////
module ShiftLeft2Bit(DataIN, DataOUT, SO);
        input [31:0] DataIN;
        output [31:0] DataOUT;
        output [1:0] SO;
        wi     Re [31:0] DataOUT;
        wi     Re [1:0] SO;

        assign SO = DataIN[31:30];
        assign DataOUT = DataIN << 2;    // shift left 2 bits

endmodule
```




## 1.3 Testbench for top module of the design.

```
//////////////////////////////////////////////////////////////////////////////////
// Copyright (c) 1995-2003 Xilinx, Inc.
// All Right          Reserved.
//////////////////////////////////////////////////////////////////////////////////
//   ____  ____
//  /   /\/   /
// /___/  \  /          Vendor:          Xilinx
// \   \   \/           Version :        Xilinx ISE 8.2i
//  \   \               Filename :       SCC_top_tbw.tfw
//  /   /               Timestamp :      Sat Apr 28 14:22:07 2007
// /___/   /\
// \   \  /  \
//  \___\/\___\
//
//Design Name:  SCC_top_tbw_tb_0
//Device: Xilinx: Spartan-3 XC3S400
//
`timescale 1ns/1ps
```

```
module SCC_top_tbw_tb_0;
	 Reg clk = 1'b0;
	 Reg   Reset = 1'b1;
	wi	Re ALU0;
	wi	Re [1:0] SO;

	parameter PERIOD = 200;
	parameter    Real DUTY_CYCLE = 0.5;
	parameter OFFSET = 0;

	initial	// Clock process for clk
	begin
		#OFFSET;
		fo	Rever
		begin
			clk = 1'b0;
			#(PERIOD-(PERIOD*DUTY_CYCLE)) clk = 1'b1;
			#(PERIOD*DUTY_CYCLE);
		end
	end

	Single_Cycle_Computer_top UUT (
		.clk(clk),
		. Reset(	Reset),
		.ALU0(ALU0),
		.SO(SO));

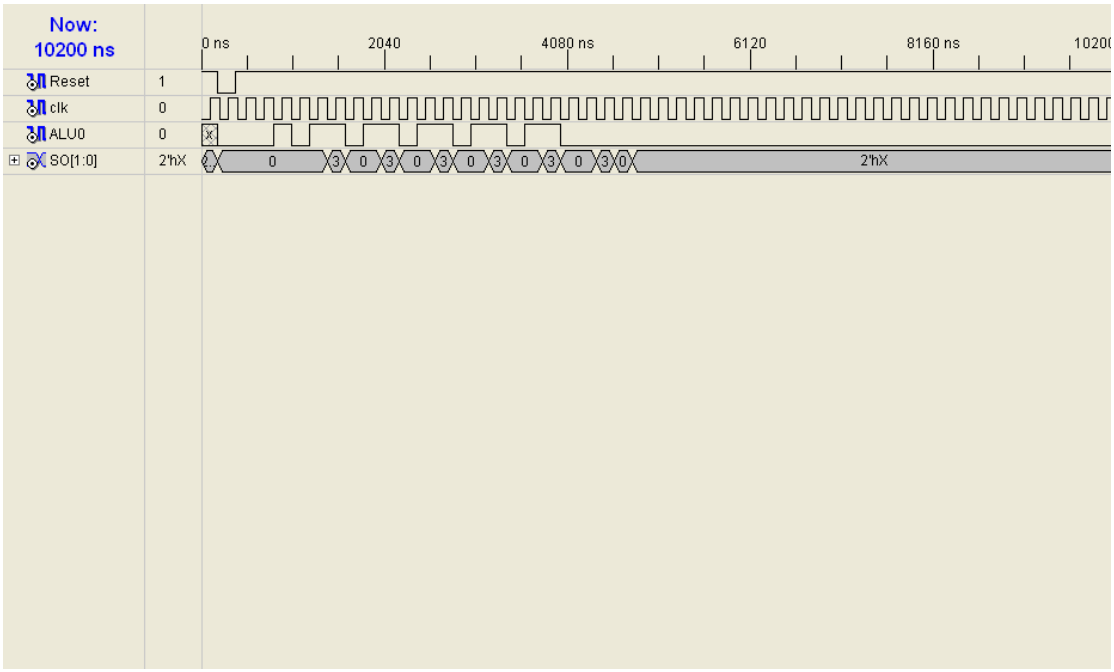
	integer TX_FILE = 0;
	integer TX_ERROR = 0;

	initial begin    // Open the	Results file...
		TX_FILE = $fopen("	Results.txt");
		#10200 // Final time:    10200 ns
		if (TX_ERROR == 0) begin
			$display("No errors or warnings.");
			$fdisplay(TX_FILE, "No errors or warnings.");
		end else begin
			$display("%d errors found in simulation.", TX_ERROR);
			$fdisplay(TX_FILE, "%d errors found in simulation.", TX_ERROR);
		end
		$fclose(TX_FILE);
		$stop;
	end

	initial begin
		// -------------    CurRent Time:    185ns
		#185;
		  Reset = 1'b0;
		// ---------------------------------------
		// -------------    CurRent Time:    385ns
		#200;
		  Reset = 1'b1;
		// ---------------------------------------
	end

endmodule
```

## 1.4 Simulation waveforms of the top-level design - behavioral simulation.




| Time | Operation |
|---|---|
| 185 | Reading data: rom32[00000000] => 8c020004 |
| 185 | Reg_File[2] => x (Port 2) |
| 185 | Reg_File[0] => 0 (Port 1) |
| 185 | Reading data: Mem[00000004] => 00000001 |
| 200 | Reg_File[2] <= 1 (Write) |
| 200 | Reg_File[0] => 0 (Port 1) |
| 200 | Reg_File[2] => 1 (Port 2) |
| 400 | Reg_File[2] <= 1 (Write) |
| 400 | Reading data: rom32[00000004] => 8c030008 |
| 400 | Reg_File[3] => x (Port 2) |
| 400 | Reading data: Mem[00000008] => 00000002 |
| 600 | Reg_File[3] <= 2 (Write) |
| 600 | Reg_File[0] => 0 (Port 1) |
| 600 | Reg_File[3] => 2 (Port 2) |
| 600 | Reading data: rom32[00000008] => 8c040014 |
| 600 | Reg_File[4] => x (Port 2) |
| 600 | Reading data: Mem[00000014] => 00000005 |
| 800 | Reg_File[4] <= 5 (Write) |
| 800 | Reg_File[0] => 0 (Port 1) |
| 800 | Reg_File[4] => 5 (Port 2) |
| 800 | Reading data: rom32[0000000c] => 00002820 |
| 800 | Reg_File[0] => 0 (Port 2) |
| 1000 | Reg_File[5] <= 0 (Write) |
| 1000 | Reg_File[0] => 0 (Port 1) |
| 1000 | Reg_File[0] => 0 (Port 2) |
| 1000 | Reading data: rom32[00000010] => 00a22820 |
| 1000 | Reg_File[2] => 1 (Port 2) |
| 1000 | Reg_File[5] => 0 (Port 1) |
| 1200 | Reg_File[5] <= 1 (Write) |

```
1200    Reg_File[5] =>          1 (Port 1)
1200    Reg_File[2] =>          1 (Port 2)
1200    Reading data: rom32[00000014] => 0085302a
1200    Reg_File[5] =>          1 (Port 2)
1200    Reg_File[4] =>          5 (Port 1)
1400    Reg_File[6] <=          0 (Write)
1400    Reg_File[4] =>          5 (Port 1)
1400    Reg_File[5] =>          1 (Port 2)
1400    Reading data: rom32[00000018] => 10c0fffd
1400    Reg_File[0] =>          0 (Port 2)
1400    Reg_File[6] =>          0 (Port 1)
1600    Reading data: rom32[00000010] => 00a22820
1600    Reg_File[2] =>          1 (Port 2)
1600    Reg_File[5] =>          1 (Port 1)
1800    Reg_File[5] <=          2 (Write)
1800    Reg_File[5] =>          2 (Port 1)
1800    Reg_File[2] =>          1 (Port 2)
1800    Reading data: rom32[00000014] => 0085302a
1800    Reg_File[5] =>          2 (Port 2)
1800    Reg_File[4] =>          5 (Port 1)
2000    Reg_File[6] <=          0 (Write)
2000    Reading data: rom32[00000018] => 10c0fffd
2000    Reg_File[0] =>          0 (Port 2)
2000    Reg_File[6] =>          0 (Port 1)
2200    Reading data: rom32[00000010] => 00a22820
2200    Reg_File[2] =>          1 (Port 2)
2200    Reg_File[5] =>          2 (Port 1)
2400    Reg_File[5] <=          3 (Write)
2400    Reg_File[5] =>          3 (Port 1)
2400    Reg_File[2] =>          1 (Port 2)
2400    Reading data: rom32[00000014] => 0085302a
2400    Reg_File[5] =>          3 (Port 2)
2400    Reg_File[4] =>          5 (Port 1)
2600    Reg_File[6] <=          0 (Write)
2600    Reading data: rom32[00000018] => 10c0fffd
2600    Reg_File[0] =>          0 (Port 2)
2600    Reg_File[6] =>          0 (Port 1)
2800    Reading data: rom32[00000010] => 00a22820
2800    Reg_File[2] =>          1 (Port 2)
2800    Reg_File[5] =>          3 (Port 1)
3000    Reg_File[5] <=          4 (Write)
3000    Reg_File[5] =>          4 (Port 1)
3000    Reg_File[2] =>          1 (Port 2)
3000    Reading data: rom32[00000014] => 0085302a
3000    Reg_File[5] =>          4 (Port 2)
3000    Reg_File[4] =>          5 (Port 1)
3200    Reg_File[6] <=          0 (Write)
3200    Reading data: rom32[00000018] => 10c0fffd
3200    Reg_File[0] =>          0 (Port 2)
3200    Reg_File[6] =>          0 (Port 1)
3400    Reading data: rom32[00000010] => 00a22820
3400    Reg_File[2] =>          1 (Port 2)
3400    Reg_File[5] =>          4 (Port 1)
3600    Reg_File[5] <=          5 (Write)
```

```
3600    Reg_File[5] =>          5 (Port 1)
3600    Reg_File[2] =>          1 (Port 2)
3600    Reading data: rom32[00000014] => 0085302a
3600    Reg_File[5] =>          5 (Port 2)
3600    Reg_File[4] =>          5 (Port 1)
3800    Reg_File[6] <=          0 (Write)
3800    Reading data: rom32[00000018] => 10c0fffd
3800    Reg_File[0] =>          0 (Port 2)
3800    Reg_File[6] =>          0 (Port 1)
4000    Reading data: rom32[00000010] => 00a22820
4000    Reg_File[2] =>          1 (Port 2)
4000    Reg_File[5] =>          5 (Port 1)
4200    Reg_File[5] <=          6 (Write)
4200    Reg_File[5] =>          6 (Port 1)
4200    Reg_File[2] =>          1 (Port 2)
4200    Reading data: rom32[00000014] => 0085302a
4200    Reg_File[5] =>          6 (Port 2)
4200    Reg_File[4] =>          5 (Port 1)
4400    Reg_File[6] <=          1 (Write)
4400    Reg_File[4] =>          5 (Port 1)
4400    Reg_File[5] =>          6 (Port 2)
4400    Reading data: rom32[00000018] => 10c0fffd
4400    Reg_File[0] =>          0 (Port 2)
4400    Reg_File[6] =>          1 (Port 1)
4600    Reading data: rom32[0000001c] => ac050000
4600    Reg_File[5] =>          6 (Port 2)
4600    Reg_File[0] =>          0 (Port 1)
4800    Writing data: Mem[00000006] <= 00000006
```

## 1.5 Synthesis Report of the implementation. The design must be synthesizable.

```
Release    - xst I.31
Copyright (c) 1995-2006 Xilinx, Inc.    All rights          Reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
CPU : 0.00 / 0.24 s | Elapsed : 0.00 / 0.00 s

--> Parameter xsthdpdir set to ./xst
CPU : 0.00 / 0.24 s | Elapsed : 0.00 / 0.00 s

-->      Reading design: Single_Cycle_Computer_top.prj

TABLE OF CONTENTS
   1) Synthesis Options Summary
   2) HDL Compilation
   3) Design Hierarchy Analysis
   4) HDL Analysis
   5) HDL Synthesis
        5.1) HDL Synthesis   Report
   6) Advanced HDL Synthesis
        6.1) Advanced HDL Synthesis        Report
   7) Low Level Synthesis
   8) Partition          Report
   9) Final      Report
        9.1) Device utilization summary
        9.2) TIMING           RePORT


=========================================================================
*                            Synthesis Options Summary                  *
=========================================================================
---- Source Parameters
Input File Name                    : "Single_Cycle_Computer_top.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "Single_Cycle_Computer_top"
Output Format                      : NGC
Target Device                      : xc3s400-5-ft256

---- Source Options
```

```
Top Module Name                    : Single_Cycle_Computer_top
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
FSM Style                          : lut
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : YES
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : YES
Resource Sharing                   : YES
Multiplier Style                   : auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 500
Add Generic Clock Buffer(BUFG)     : 8
Register Duplication               : YES
Slice Packing                      : YES
Pack IO Registers into IOBs        : auto
Equivalent Register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Keep Hierarchy                     : NO
RTL Output                         : Yes
Global Optimization                : AllClockNets
Write Timing Constraints           : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : maintain
Slice Utilization Ratio            : 100
Slice Utilization Ratio Delta      : 5

---- Other Options
lso                                : Single_Cycle_Computer_top.lso
Read Cores                         : YES
cross_clock_analysis               : NO
verilog2001                        : YES
safe_implementation                : No
Optimize Instantiated Primitives   : NO
use_clock_enable                   : Yes
use_sync_set                       : Yes
use_sync_reset                     : Yes

=========================================================================


=========================================================================
*                            HDL Compilation                            *
=========================================================================
Compiling verilog file "SignExtend.v" in library work
Compiling verilog file "ShiftLeft2Bit.v" in library work
Module <SignExtend> compiled
Compiling verilog file "RegisterFile.v" in library work
Module <ShiftLeft2Bit> compiled
Compiling verilog file "ROM32Bit32Byte.v" in library work
Module <RegisterFile> compiled
Compiling verilog file "PCReg32Bit.v" in library work
Module <ROM32Bit32Byte> compiled
Compiling verilog file "Memory32Bit128Byte.v" in library work
Module <PCReg32Bit> compiled
Compiling verilog file "MainControlUnit.v" in library work
Module <Memory32Bit128Byte> compiled
Compiling verilog file "MUX5Bit2Ch.v" in library work
Module <MainControlUnit> compiled
Compiling verilog file "MUX32Bit2Ch.v" in library work
Module <MUX5Bit2Ch> compiled
Compiling verilog file "Four.v" in library work
Module <MUX32Bit2Ch> compiled
Compiling verilog file "Adder32Bit.v" in library work
Module <Four> compiled
Compiling verilog file "ALUControlUnit.v" in library work
Module <Adder32Bit> compiled
Compiling verilog file "ALU32Bit.v" in library work
Module <ALUControlUnit> compiled
Compiling verilog file "Single_Cycle_Computer_top.vf" in library work
Module <ALU32Bit> compiled
Module <Single_Cycle_Computer_top> compiled
No errors in compilation
Analysis of file <"Single_Cycle_Computer_top.prj"> succeeded.


=========================================================================
*                        Design Hierarchy Analysis                      *
```

```
=========================================================================
Analyzing hierarchy for module <Single_Cycle_Computer_top> in library <work>.

Analyzing hierarchy for module <Adder32Bit> in library <work>.

Analyzing hierarchy for module <ALU32Bit> in library <work>.

Analyzing hierarchy for module <ALUControlUnit> in library <work> with parameters.
        ALU_add = "010"
        ALU_and = "000"
        ALU_or = "001"
        ALU_slt = "111"
        ALU_sub = "110"
        Funct_add = "100000"
        Funct_and = "100100"
        Funct_or = "100101"
        Funct_slt = "101010"
        Funct_sub = "100010"

Analyzing hierarchy for module <MainControlUnit> in library <work> with parameters.
        LW = "100011"
        BEQ = "000100"
        R_FORMAT = "000000"
        SW = "101011"

Analyzing hierarchy for module <Memory32Bit128Byte> in library <work> with parameters.
        BASE_ADDRESS = "00000000000000000000000000"

Analyzing hierarchy for module <MUX5Bit2Ch> in library <work> with parameters.
        bitwidth = "00000000000000000000000000000101"

Analyzing hierarchy for module <MUX32Bit2Ch> in library <work> with parameters.
        bitwidth = "00000000000000000000000000100000"

Analyzing hierarchy for module <PCReg32Bit> in library <work>.

Analyzing hierarchy for module <Four> in library <work>.

Analyzing hierarchy for module <RegisterFile> in library <work>.

Analyzing hierarchy for module <ROM32Bit32Byte> in library <work> with parameters.
        BaseAddress = "00000000000000000000000000"

Analyzing hierarchy for module <ShiftLeft2Bit> in library <work>.

Analyzing hierarchy for module <SignExtend> in library <work>.

Building hierarchy successfully finished.

=========================================================================
*                            HDL Analysis                               *
=========================================================================
Analyzing top module <Single_Cycle_Computer_top>.
Module <Single_Cycle_Computer_top> is correct for synthesis.

Analyzing module <Adder32Bit> in library <work>.
Module <Adder32Bit> is correct for synthesis.

Analyzing module <ALU32Bit> in library <work>.
Module <ALU32Bit> is correct for synthesis.

Analyzing module <ALUControlUnit> in library <work>.
        Funct_add = 6'b100000
        Funct_sub = 6'b100010
        Funct_and = 6'b100100
        Funct_or = 6'b100101
        Funct_slt = 6'b101010
        ALU_add = 3'b010
        ALU_sub = 3'b110
        ALU_and = 3'b000
        ALU_or = 3'b001
        ALU_slt = 3'b111
Module <ALUControlUnit> is correct for synthesis.

Analyzing module <MainControlUnit> in library <work>.
        R_FORMAT = 6'b000000
        LW = 6'b100011
        SW = 6'b101011
        BEQ = 6'b000100
WARNING:Xst:2323 - "MainControlUnit.v" line 86: Parameter 2 is not constant in call of system task $display.
"MainControlUnit.v" line 86: $display : Main_Control unimplemented Op_Code %d
Module <MainControlUnit> is correct for synthesis.

Analyzing module <Memory32Bit128Byte> in library <work>.
        BASE_ADDRESS = 25'b0000000000000000000000000
WARNING:Xst:2319 - "Memory32Bit128Byte.v" line 61: Signal Memory_Array in initial block is partially initialized. The initialization will
be ignored.
WARNING:Xst:2321 - "Memory32Bit128Byte.v" line 38: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 38: Parameter 3 is not constant in call of system task $display.
"Memory32Bit128Byte.v" line 38: $display :    rom32 error: unaligned address %h
WARNING:Xst:2321 - "Memory32Bit128Byte.v" line 40: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 40: Parameter 3 is not constant in call of system task $display.
```

```
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 40: Parameter 4 is not constant in call of system task $display.
"Memory32Bit128Byte.v" line 40: $display :      Reading data: Mem[%h] => %h
WARNING:Xst:905 - "Memory32Bit128Byte.v" line 34: The signals <Memory_Array> are missing in the sensitivity list of always block.
WARNING:Xst:2321 - "Memory32Bit128Byte.v" line 51: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 51: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 51: Parameter 4 is not constant in call of system task $display.
"Memory32Bit128Byte.v" line 51: $display :    Writing data: Mem[%h] <= %h
Module <Memory32Bit128Byte> is correct for synthesis.

Analyzing module <MUX5Bit2Ch> in library <work>.
        bitwidth = 32'sb00000000000000000000000000000101
Module <MUX5Bit2Ch> is correct for synthesis.

Analyzing module <MUX32Bit2Ch> in library <work>.
        bitwidth = 32'sb00000000000000000000000000100000
Module <MUX32Bit2Ch> is correct for synthesis.

Analyzing module <PCReg32Bit> in library <work>.
Module <PCReg32Bit> is correct for synthesis.

Analyzing module <Four> in library <work>.
Module <Four> is correct for synthesis.

Analyzing module <RegisterFile> in library <work>.
WARNING:Xst:2321 - "RegisterFile.v" line 32: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "RegisterFile.v" line 32: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "RegisterFile.v" line 32: Parameter 4 is not constant in call of system task $display.
"RegisterFile.v" line 32: $display :          Reg_File[%d] => %d (Port 1)
WARNING:Xst:905 - "RegisterFile.v" line 27: The signals <File_Array, DataOUT1> are missing in the sensitivity list of always block.
WARNING:Xst:2321 - "RegisterFile.v" line 41: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "RegisterFile.v" line 41: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "RegisterFile.v" line 41: Parameter 4 is not constant in call of system task $display.
"RegisterFile.v" line 41: $display :          Reg_File[%d] => %d (Port 2)
WARNING:Xst:905 - "RegisterFile.v" line 36: The signals <File_Array, DataOUT2> are missing in the sensitivity list of always block.
WARNING:Xst:2321 - "RegisterFile.v" line 48: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "RegisterFile.v" line 48: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "RegisterFile.v" line 48: Parameter 4 is not constant in call of system task $display.
"RegisterFile.v" line 48: $display :          Reg_File[%d] <= %d (Write)
Module <RegisterFile> is correct for synthesis.

Analyzing module <ROM32Bit32Byte> in library <work>.
        BaseAddress = 25'b0000000000000000000000000
WARNING:Xst:2321 - "ROM32Bit32Byte.v" line 32: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "ROM32Bit32Byte.v" line 32: Parameter 3 is not constant in call of system task $display.
"ROM32Bit32Byte.v" line 32: $display :    rom32 error: unaligned Address %d
WARNING:Xst:2321 - "ROM32Bit32Byte.v" line 47: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "ROM32Bit32Byte.v" line 47: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "ROM32Bit32Byte.v" line 47: Parameter 4 is not constant in call of system task $display.
"ROM32Bit32Byte.v" line 47: $display :          Reading data: rom32[%h] => %h
WARNING:Xst:905 - "ROM32Bit32Byte.v" line 29: The signals <Address, DataOUT> are missing in the sensitivity list of always block.
Module <ROM32Bit32Byte> is correct for synthesis.

Analyzing module <ShiftLeft2Bit> in library <work>.
Module <ShiftLeft2Bit> is correct for synthesis.

Analyzing module <SignExtend> in library <work>.
Module <SignExtend> is correct for synthesis.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port        Resolution...

Synthesizing Unit <Adder32Bit>.
        Related source file is "Adder32Bit.v".
    Found 32-bit adder for signal <Sum>.
    Summary:
      inferred     1 Adder/Subtractor(s).
Unit <Adder32Bit> synthesized.


Synthesizing Unit <ALU32Bit>.
        Related source file is "ALU32Bit.v".
    Found 32-bit addsub for signal <$addsub0000>.
    Found 32-bit comparator less for signal <$cmp_lt0000> created at line 29.
    Summary:
      inferred     1 Adder/Subtractor(s).
      inferred     1 Comparator(s).
Unit <ALU32Bit> synthesized.


Synthesizing Unit <ALUControlUnit>.
        Related source file is "ALUControlUnit.v".
    Found 3-bit 3-to-1 multiplexer for signal <ALU_Operation>.
    Summary:
      inferred     3 Multiplexer(s).
Unit <ALUControlUnit> synthesized.


Synthesizing Unit <MainControlUnit>.
```

```
        Related source file is "MainControlUnit.v".
Unit <MainControlUnit> synthesized.


Synthesizing Unit <Memory32Bit128Byte>.
        Related source file is "Memory32Bit128Byte.v".
WARNING:Xst:647 - Input <Address<1:0>> is never used.
WARNING:Xst:1872 - Variable <i> is used but never assigned.
    Found 32x32-bit single-port distributed RAM for signal <Memory_Array>.
    ----------------------------------------------------------------------
    | ram_style                  | Auto                                  |                |
    ----------------------------------------------------------------------
    | Port A                                                             |
    |     aspect ratio     | 32-word x 32-bit                          |                |
    |     clkA                   | connected to signal <clk>             | fall         |
    |     weA                    | connected to internal node            | high         |
    |     addrA                  | connected to signal <Memory_Offset>   |                |
    |     diA                    | connected to signal <DataIN>          |                |
    |     doA                    | connected to internal node            |                |
    ----------------------------------------------------------------------
INFO:Xst:1442 - HDL ADVISOR - The RAM contents appears to be           Read asynchronously. A synchronous      Read would allow you
to take advantage of available block RAM          Resources, for optimized device usage and improved timings. Please  Refer to your
documentation for coding guidelines.
    Summary:
      inferred     1 RAM(s).
Unit <Memory32Bit128Byte> synthesized.


Synthesizing Unit <MUX5Bit2Ch>.
        Related source file is "MUX5Bit2Ch.v".
Unit <MUX5Bit2Ch> synthesized.


Synthesizing Unit <MUX32Bit2Ch>.
        Related source file is "MUX32Bit2Ch.v".
Unit <MUX32Bit2Ch> synthesized.


Synthesizing Unit <PCReg32Bit>.
        Related source file is "PCReg32Bit.v".
    Found 32-bit     Register for signal <DataOUT>.
    Summary:
      inferred    32 D-type flip-flop(s).
Unit <PCReg32Bit> synthesized.


Synthesizing Unit <Four>.
        Related source file is "Four.v".
Unit <Four> synthesized.


Synthesizing Unit <RegisterFile>.
        Related source file is "RegisterFile.v".
    Found 31x32-bit dual-port distributed RAM for signal <File_Array>.
    ----------------------------------------------------------------------
    | ram_style                  | Auto                                  |                |
    ----------------------------------------------------------------------
    | Port A                                                             |
    |     aspect ratio     | 31-word x 32-bit                          |                |
    |     clkA                   | connected to signal <clk>             | fall         |
    |     weA                    | connected to internal node            | high         |
    |     addrA                  | connected to signal <WriteAddr>       |                |
    |     diA                    | connected to signal <DataIN>          |                |
    ----------------------------------------------------------------------
    | Port B                                                             |
    |     aspect ratio     | 31-word x 32-bit                          |                |
    |     addrB                  | connected to signal <ReadAddr1>       |                |
    |     doB                    | connected to internal node            |                |
    ----------------------------------------------------------------------
INFO:Xst:1442 - HDL ADVISOR - The RAM contents appears to be           Read asynchronously. A synchronous      Read would allow you
to take advantage of available block RAM          Resources, for optimized device usage and improved timings. Please  Refer to your
documentation for coding guidelines.
    Found 31x32-bit dual-port distributed RAM for signal <File_Array>.
    ----------------------------------------------------------------------
    | ram_style                  | Auto                                  |                |
    ----------------------------------------------------------------------
    | Port A                                                             |
    |     aspect ratio     | 31-word x 32-bit                          |                |
    |     clkA                   | connected to signal <clk>             | fall         |
    |     weA                    | connected to internal node            | high         |
    |     addrA                  | connected to signal <WriteAddr>       |                |
    |     diA                    | connected to signal <DataIN>          |                |
    ----------------------------------------------------------------------
    | Port B                                                             |
    |     aspect ratio     | 31-word x 32-bit                          |                |
    |     addrB                  | connected to signal <ReadAddr2>       |                |
    |     doB                    | connected to internal node            |                |
    ----------------------------------------------------------------------
INFO:Xst:1442 - HDL ADVISOR - The RAM contents appears to be           Read asynchronously. A synchronous      Read would allow you
to take advantage of available block RAM          Resources, for optimized device usage and improved timings. Please  Refer to your
documentation for coding guidelines.
    Summary:
```

```
        inferred      2 RAM(s).
Unit <RegisterFile> synthesized.


Synthesizing Unit <ROM32Bit32Byte>.
        Related source file is "ROM32Bit32Byte.v".
WARNING:Xst:647 - Input <Address<1:0>> is never used.
WARNING:Xst:737 - Found 32-bit latch for signal <DataOUT>.
      Found 8x32-bit ROM for signal <$old_DataOUT_5>.
      Summary:
        inferred      1 ROM(s).
Unit <ROM32Bit32Byte> synthesized.


Synthesizing Unit <ShiftLeft2Bit>.
        Related source file is "ShiftLeft2Bit.v".
Unit <ShiftLeft2Bit> synthesized.


Synthesizing Unit <SignExtend>.
        Related source file is "SignExtend.v".
Unit <SignExtend> synthesized.


Synthesizing Unit <Single_Cycle_Computer_top>.
        Related source file is "Single_Cycle_Computer_top.vf".
Unit <Single_Cycle_Computer_top> synthesized.

INFO:Xst:1767 - HDL ADVISOR -         Resource sharing has identified that some arithmetic operations in this design can share the same
physical         Resources for           Reduced device utilization. For improved clock frequency you may try to disable     Resource sharing.

=========================================================================
HDL Synthesis         Report

Macro Statistics
# RAMs                                                  : 3
  31x32-bit dual-port distributed RAM                   : 2
  32x32-bit single-port distributed RAM                 : 1
# ROMs                                                  : 1
  8x32-bit ROM                                          : 1
# Adders/Subtractors                                    : 3
  32-bit adder                                          : 2
  32-bit addsub                                         : 1
#         Registers                                     : 1
  32-bit          Register                              : 1
# Latches                                               : 1
  32-bit latch                                          : 1
# Comparators                                           : 1
  32-bit comparator less                                : 1
# Multiplexers                                          : 1
  3-bit 3-to-1 multiplexer                              : 1

=========================================================================

=========================================================================
*                                Advanced HDL Synthesis                                 *
=========================================================================

Loading device for application Rf_Device from file '3s400.nph' in environment F:\Xilinx.

=========================================================================
Advanced HDL Synthesis   Report

Macro Statistics
# RAMs                                                  : 3
  31x32-bit dual-port distributed RAM                   : 2
  32x32-bit single-port distributed RAM                 : 1
# ROMs                                                  : 1
  8x32-bit ROM                                          : 1
# Adders/Subtractors                                    : 3
  32-bit adder                                          : 2
  32-bit addsub                                         : 1
#         Registers                                     : 32
  Flip-Flops                                            : 32
# Latches                                               : 1
  32-bit latch                                          : 1
# Comparators                                           : 1
  32-bit comparator less                                : 1
# Multiplexers                                          : 1
  3-bit 3-to-1 multiplexer                              : 1

=========================================================================

=========================================================================
*                                Low Level Synthesis                                    *
=========================================================================
WARNING:Xst:1710 - FF/Latch    <ROM/DataOUT_25> (without init value) has a constant value of 0 in block
<Single_Cycle_Computer_top>.
WARNING:Xst:1710 - FF/Latch    <ROM/DataOUT_24> (without init value) has a constant value of 0 in block
<Single_Cycle_Computer_top>.
WARNING:Xst:1710 - FF/Latch    <ROM/DataOUT_20> (without init value) has a constant value of 0 in block
<Single_Cycle_Computer_top>.
```

WARNING:Xst:1710 - FF/Latch <ROM/DataOUT_19> (without init value) has a constant value of 0 in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <ROM/DataOUT_30> is unconnected in block <Single_Cycle_Computer_top>.

Optimizing unit <Single_Cycle_Computer_top> ...

Optimizing unit <ALU32Bit> ...

Optimizing unit <RegisterFile> ...

Optimizing unit <PCReg32Bit> ...

Optimizing unit <MUX32Bit2Ch> ...

Optimizing unit <Memory32Bit128Byte> ...

Mapping all equations...
WARNING:Xst:1291 - FF/Latch <PC/DataOUT_0> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/DataOUT_1> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem321> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem351> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem331> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem341> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem381> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem361> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem371> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem411> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem391> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem401> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem441> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem421> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem431> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem471> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem451> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem461> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem501> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem481> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem491> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem531> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem511> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem521> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem561> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem541> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem551> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem591> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem571> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem581> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem621> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem601> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem611> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem631> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem961> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem991> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem971> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem981> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1021> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1001> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1011> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1051> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1031> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1041> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1081> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1061> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1071> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1111> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1091> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1101> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1141> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1121> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1131> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1171> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1151> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1161> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1201> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1181> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1191> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1231> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1211> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1221> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1261> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1241> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1251> is unconnected in block <Single_Cycle_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1271> is unconnected in block <Single_Cycle_Computer_top>.
Building and optimizing final netlist ...
INFO:Xst:2261 - The FF/Latch <ROM/DataOUT_13> in Unit <Single_Cycle_Computer_top> is equivalent to the following FF/Latch, which will be Removed : <ROM/DataOUT_5>
INFO:Xst:2261 - The FF/Latch <ROM/DataOUT_28> in Unit <Single_Cycle_Computer_top> is equivalent to the following 9 FFs/Latches, which will be Removed : <ROM/DataOUT_22> <ROM/DataOUT_15> <ROM/DataOUT_14> <ROM/DataOUT_10> <ROM/DataOUT_9> <ROM/DataOUT_8> <ROM/DataOUT_7> <ROM/DataOUT_6> <ROM/DataOUT_0>
INFO:Xst:2261 - The FF/Latch <ROM/DataOUT_31> in Unit <Single_Cycle_Computer_top> is equivalent to the following 2 FFs/Latches, which will be Removed : <ROM/DataOUT_27> <ROM/DataOUT_26>
Found area constraint ratio of 100 (+ 5) on block Single_Cycle_Computer_top, actual ratio is 8.

```
Latch ROM/DataOUT_28 has been          Replicated 2 time(s) to handle iob=true attribute.

Final Macro Processing ...

=========================================================================
Final   Register         Report

Macro Statistics
#       Registers                                               : 30
  Flip-Flops                                                    : 30

=========================================================================

=========================================================================
*                                 Partition          Report                                 *
=========================================================================

Partition Implementation Status
-------------------------------

   No Partitions were found in this design.

-------------------------------

=========================================================================
*                                   Final            Report                                 *
=========================================================================
Final   Results
RTL Top Level Output File Name         : Single_Cycle_Computer_top.ngr
Top Level Output File Name             : Single_Cycle_Computer_top
Output Format                           : NGC
Optimization Goal                       : Speed
Keep Hierarchy                          : NO

Design Statistics
# IOs                                   : 5

Cell Usage :
# BELS                                  : 717
#       AND2                            : 1
#       GND                             : 1
#       INV                             : 4
#       LUT1                            : 29
#       LUT2                            : 42
#       LUT3                            : 77
#       LUT4                            : 257
#       LUT4_D                          : 23
#       LUT4_L                          : 49
#       MUXCY                           : 143
#       VCC                             : 1
#       XORCY                           : 90
# FlipFlops/Latches                     : 47
#       FDC_1                           : 30
#       LD                              : 17
# RAMS                                  : 96
#       RAM16X1D                        : 64
#       RAM32X1S                        : 32
# Clock Buffers                         : 1
#       BUFGP                           : 1
# IO Buffers                            : 4
#       IBUF                            : 1
#       OBUF                            : 3
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s400ft256-5

 Number of Slices:                       351  out of   3584     9%
 Number of Slice Flip Flops:             45   out of   7168     0%
 Number of 4 input LUTs:                 673  out of   7168     9%
    Number used as logic:                481
    Number used as RAMs:                 192
 Number of IOs:                           5
 Number of bonded IOBs:                   5  out of    173     2%
    IOB Flip Flops:                       2
 Number of GCLKs:                         1  out of      8    12%


=========================================================================
TIMING       RePORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE       ReFER TO THE TRACE    RePORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------------------------+------------------------+-------+
Clock Signal                                         | Clock buffer(FF name)  | Load  |
-----------------------------------------------------+------------------------+-------+
```

```
ROM/AddressSelect_wg_cy<6>(ROM/AddressSelect_wg_cy<6>:O)| NONE(*)(ROM/DataOUT_4) | 17    |
clk                                                     | BUFGP                 | 126   |
--------------------------------------------------------+-----------------------+-------+
(*) This 1 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR    Resources. Please use
the buffer_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------+-------------------------+-------+
Control Signal                     | Buffer(FF name)         | Load  |
-----------------------------------+-------------------------+-------+
PC/Reset_inv(PC/Reset_inv1_INV_0:O)| NONE(PC/DataOUT_10)     | 30    |
-----------------------------------+-------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

     Minimum period: 13.920ns (Maximum Frequency: 71.840MHz)
     Minimum input arrival time before clock: No path found
     Maximum output          Required time after clock: 21.293ns
     Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
   Clock period: 13.920ns (frequency: 71.840MHz)
   Total number of paths / destination ports: 218999 / 318
-------------------------------------------------------------------------
Delay:                  13.920ns (Levels of Logic = 23)
   Source:                RegFile/inst_Mram_mem128 (RAM)
   Destination:           PC/DataOUT_2 (FF)
   Source Clock:          clk falling
   Destination Clock: clk falling

   Data Path:          RegFile/inst_Mram_mem128 to PC/DataOUT_2
                                          Gate         Net
      Cell:in->out          fanout      Delay      Delay   Logical Name (Net Name)
      ----------------------------------- ------------
       RAM16X1D:WCLK->DPO       1      1.552      0.704     RegFile/inst_Mram_mem128 (RegFile/N9)
       LUT4:I3->O               3      0.479      0.941     RegFile/_old_DataOUT1_3<0>1 (XLXN_22<0>)
       LUT3:I1->O               1      0.479      0.000     ALU/Maddsub__addsub0000_lut<0> (ALU/N5)
       MUXCY:S->O                 1      0.435      0.000     ALU/Maddsub__addsub0000_cy<0> (ALU/Maddsub__addsub0000_cy<0>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<1> (ALU/Maddsub__addsub0000_cy<1>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<2> (ALU/Maddsub__addsub0000_cy<2>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<3> (ALU/Maddsub__addsub0000_cy<3>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<4> (ALU/Maddsub__addsub0000_cy<4>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<5> (ALU/Maddsub__addsub0000_cy<5>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<6> (ALU/Maddsub__addsub0000_cy<6>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<7> (ALU/Maddsub__addsub0000_cy<7>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<8> (ALU/Maddsub__addsub0000_cy<8>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<9> (ALU/Maddsub__addsub0000_cy<9>)
       MUXCY:CI->O                1      0.056      0.000     ALU/Maddsub__addsub0000_cy<10> (ALU/Maddsub__addsub0000_cy<10>)
       XORCY:CI->O                1      0.786      0.704     ALU/Maddsub__addsub0000_xor<11> (ALU/_addsub0000<11>)
       LUT4:I3->O               3      0.479      0.830     ALU/_old_Result_1<11> (XLXN_28<11>)
       LUT4:I2->O               1      0.479      0.704     ALU/_old_Result_1<29>_SW1 (N377)
       LUT4:I3->O               1      0.479      0.000     ALU/_cmp_eq0000_wg_lut<4> (N151)
       MUXCY:S->O                 1      0.435      0.000     ALU/_cmp_eq0000_wg_cy<4> (ALU/_cmp_eq0000_wg_cy<4>)
       MUXCY:CI->O                1      0.056      0.000     ALU/_cmp_eq0000_wg_cy<5> (ALU/_cmp_eq0000_wg_cy<5>)
       MUXCY:CI->O                1      0.056      0.000     ALU/_cmp_eq0000_wg_cy<6> (ALU/_cmp_eq0000_wg_cy<6>)
       MUXCY:CI->O                2      0.265      0.745     ALU/_cmp_eq0000_wg_cy<7> (ALU/_cmp_eq0000_wg_cy<7>)
       AND2:I0->O              30      0.479      1.624     ANDBr (XLXN_237)
       LUT3:I2->O               1      0.479      0.000     MUX_3/DataOUT<31>1 (XLXN_18<31>)
       FDC_1:D                            0.176                PC/DataOUT_31
      ----------------------------------------
      Total                            13.920ns (7.667ns logic, 6.252ns route)
                                               (55.1% logic, 44.9% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'ROM/AddressSelect_wg_cy<6>'
   Total number of paths / destination ports: 23161 / 3
-------------------------------------------------------------------------
Offset:                 21.293ns (Levels of Logic = 24)
   Source:                ROM/DataOUT_28 (LATCH)
   Destination:           ALU0 (PAD)
   Source Clock:          ROM/AddressSelect_wg_cy<6> falling

   Data Path: ROM/DataOUT_28 to ALU0
                                          Gate         Net
      Cell:in->out          fanout      Delay      Delay   Logical Name (Net Name)
      ----------------------------------- ------------
       LD:G->Q                159      0.551      2.253     ROM/DataOUT_28 (ROM/DataOUT_28)
       LUT3:I2->O               1      0.479      0.704     XLXN_68<1>_SW1 (N423)
       LUT4:I3->O              75      0.479      2.080     XLXN_68<1> (XLXN_68<1>)
       LUT3:I0->O              33      0.479      1.875     ALU/_mux00001 (ALU/_mux0000)
       LUT3:I0->O               1      0.479      0.000     ALU/Maddsub__addsub0000_lut<0> (ALU/N5)
```

```
    MUXCY:S->O            1    0.435    0.000   ALU/Maddsub__addsub0000_cy<0> (ALU/Maddsub__addsub0000_cy<0>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<1> (ALU/Maddsub__addsub0000_cy<1>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<2> (ALU/Maddsub__addsub0000_cy<2>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<3> (ALU/Maddsub__addsub0000_cy<3>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<4> (ALU/Maddsub__addsub0000_cy<4>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<5> (ALU/Maddsub__addsub0000_cy<5>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<6> (ALU/Maddsub__addsub0000_cy<6>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<7> (ALU/Maddsub__addsub0000_cy<7>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<8> (ALU/Maddsub__addsub0000_cy<8>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<9> (ALU/Maddsub__addsub0000_cy<9>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<10> (ALU/Maddsub__addsub0000_cy<10>)
    XORCY:CI->O           1    0.786    0.704   ALU/Maddsub__addsub0000_xor<11> (ALU/_addsub0000<11>)
    LUT4:I3->O            3    0.479    0.830   ALU/_old_Result_1<11> (XLXN_28<11>)
    LUT4:I2->O            1    0.479    0.704   ALU/_old_Result_1<29>_SW1 (N377)
    LUT4:I3->O            1    0.479    0.000   ALU/_cmp_eq0000_wg_lut<4> (N151)
    MUXCY:S->O            1    0.435    0.000   ALU/_cmp_eq0000_wg_cy<4> (ALU/_cmp_eq0000_wg_cy<4>)
    MUXCY:CI->O           1    0.056    0.000   ALU/_cmp_eq0000_wg_cy<5> (ALU/_cmp_eq0000_wg_cy<5>)
    MUXCY:CI->O           1    0.056    0.000   ALU/_cmp_eq0000_wg_cy<6> (ALU/_cmp_eq0000_wg_cy<6>)
    MUXCY:CI->O           2    0.265    0.745   ALU/_cmp_eq0000_wg_cy<7> (ALU/_cmp_eq0000_wg_cy<7>)
    OBUF:I->O                  4.909           ALU0_OBUF (ALU0)
    ----------------------------------------
    Total                     21.293ns (11.400ns logic, 9.894ns route)
                                       (53.5% logic, 46.5% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 1716 / 1
--------------------------------------------------------------------------
Offset:              16.070ns (Levels of Logic = 22)
  Source:            RegFile/inst_Mram_mem128 (RAM)
  Destination:       ALU0 (PAD)
  Source Clock:      clk falling

  Data Path:         RegFile/inst_Mram_mem128 to ALU0
                                  Gate     Net
    Cell:in->out      fanout   Delay   Delay   Logical Name (Net Name)
    ----------------------------------------  ------------
    RAM16X1D:WCLK->DPO    1    1.552    0.704   RegFile/inst_Mram_mem128 (RegFile/N9)
    LUT4:I3->O            3    0.479    0.941   RegFile/_old_DataOUT1_3<0>1 (XLXN_22<0>)
    LUT3:I1->O            1    0.479    0.000   ALU/Maddsub__addsub0000_lut<0> (ALU/N5)
    MUXCY:S->O            1    0.435    0.000   ALU/Maddsub__addsub0000_cy<0> (ALU/Maddsub__addsub0000_cy<0>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<1> (ALU/Maddsub__addsub0000_cy<1>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<2> (ALU/Maddsub__addsub0000_cy<2>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<3> (ALU/Maddsub__addsub0000_cy<3>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<4> (ALU/Maddsub__addsub0000_cy<4>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<5> (ALU/Maddsub__addsub0000_cy<5>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<6> (ALU/Maddsub__addsub0000_cy<6>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<7> (ALU/Maddsub__addsub0000_cy<7>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<8> (ALU/Maddsub__addsub0000_cy<8>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<9> (ALU/Maddsub__addsub0000_cy<9>)
    MUXCY:CI->O           1    0.056    0.000   ALU/Maddsub__addsub0000_cy<10> (ALU/Maddsub__addsub0000_cy<10>)
    XORCY:CI->O           1    0.786    0.704   ALU/Maddsub__addsub0000_xor<11> (ALU/_addsub0000<11>)
    LUT4:I3->O            3    0.479    0.830   ALU/_old_Result_1<11> (XLXN_28<11>)
    LUT4:I2->O            1    0.479    0.704   ALU/_old_Result_1<29>_SW1 (N377)
    LUT4:I3->O            1    0.479    0.000   ALU/_cmp_eq0000_wg_lut<4> (N151)
    MUXCY:S->O            1    0.435    0.000   ALU/_cmp_eq0000_wg_cy<4> (ALU/_cmp_eq0000_wg_cy<4>)
    MUXCY:CI->O           1    0.056    0.000   ALU/_cmp_eq0000_wg_cy<5> (ALU/_cmp_eq0000_wg_cy<5>)
    MUXCY:CI->O           1    0.056    0.000   ALU/_cmp_eq0000_wg_cy<6> (ALU/_cmp_eq0000_wg_cy<6>)
    MUXCY:CI->O           2    0.265    0.745   ALU/_cmp_eq0000_wg_cy<7> (ALU/_cmp_eq0000_wg_cy<7>)
    OBUF:I->O                  4.909           ALU0_OBUF (ALU0)
    ----------------------------------------
    Total                     16.070ns (11.442ns logic, 4.628ns route)
                                       (71.2% logic, 28.8% route)

==========================================================================
CPU : 15.05 / 15.31 s | Elapsed : 15.00 / 15.00 s

-->

Total memory usage is 141064 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :  103 (   0 filtered)
Number of infos    :    8 (   0 filtered)
```

## 1.6 Identify the critical path using the STA tool of Xilinx ISE.

Maximum delay is 13.924ns.

---

Delay: 13.924ns (data path - clock path skew + uncertainty)
- Source: RegFile/inst_Mram_mem671.SLICEM_F (RAM)
- Destination: RegFile/inst_Mram_mem710.SLICEM_F (RAM)
- Data Path Delay: 13.924ns (Levels of Logic = 10)
- Clock Path Skew: 0.000ns
- Source Clock: clk_BUFGP falling
- Destination Clock: clk_BUFGP falling

Clock Uncertainty: 0.000ns

Constraint Improvement Wizard

Data Path: RegFile/inst_Mram_mem671.SLICEM_F to RegFile/inst_Mram_mem710.SLICEM_F

| Delay type | Delay(ns) | Logical Resource(s) |
|---|---|---|
| Tshcko | 1.552 | RegFile/inst_Mram_mem671.WE |
| | | RegFile/inst_Mram_mem671.SLICEM_F |
| net (fanout=2) | 0.949 | RegFile/N147 |
| Tilo | 0.529 | MUX_2/DataOUT<3>1 |
| net (fanout=3) | 0.827 | XLXN_26<3> |
| Topcyg | 0.954 | ALU/Maddsub_addsub0000_lut<3> |
| | | ALU/Maddsub_addsub0000_cy<3> |
| net (fanout=1) | 0.000 | ALU/Maddsub_addsub0000_cy<3> |
| Tbyp | 0.104 | ALU/Maddsub_addsub0000_cy<4> |
| | | ALU/Maddsub_addsub0000_cy<5> |
| net (fanout=1) | 0.000 | ALU/Maddsub_addsub0000_cy<5> |
| Tbyp | 0.104 | ALU/Maddsub_addsub0000_cy<6> |
| | | ALU/Maddsub_addsub0000_cy<7> |
| net (fanout=1) | 0.000 | ALU/Maddsub_addsub0000_cy<5> |
| Tbyp | 0.104 | ALU/Maddsub_addsub0000_cy<6> |
| | | ALU/Maddsub_addsub0000_cy<7> |
| net (fanout=1) | 0.000 | ALU/Maddsub_addsub0000_cy<7> |
| Tcinx | 0.786 | ALU/Maddsub_addsub0000_xor<8> |
| net (fanout=1) | 1.554 | ALU/_addsub0000<8> |
| Tilo | 0.479 | ALU/_old_Result_1<8> |
| net (fanout=3) | 0.315 | XLXN_28<8> |
| Tilo | 0.479 | ALU/_old_Result_1<31>_SW2 |
| net (fanout=1) | 0.014 | N371 |
| Topxb | 1.026 | Memory/Address_Select_wg_lut<6> |
| | | Memory/Address_Select_wg_cy<6> |
| net (fanout=36) | 2.428 | Memory/Address_Select_wg_cy<6> |
| Tilo | 0.479 | MUX_4/DataOUT<7>1 |
| net (fanout=2) | 0.893 | XLXN_34<7> |
| Tds | 0.452 | RegFile/inst_Mram_mem710.SLICEM_F |
| Total | 13.924ns | (6.944ns logic, 6.980ns route) |
| | | (49.9% logic, 50.1% route) |

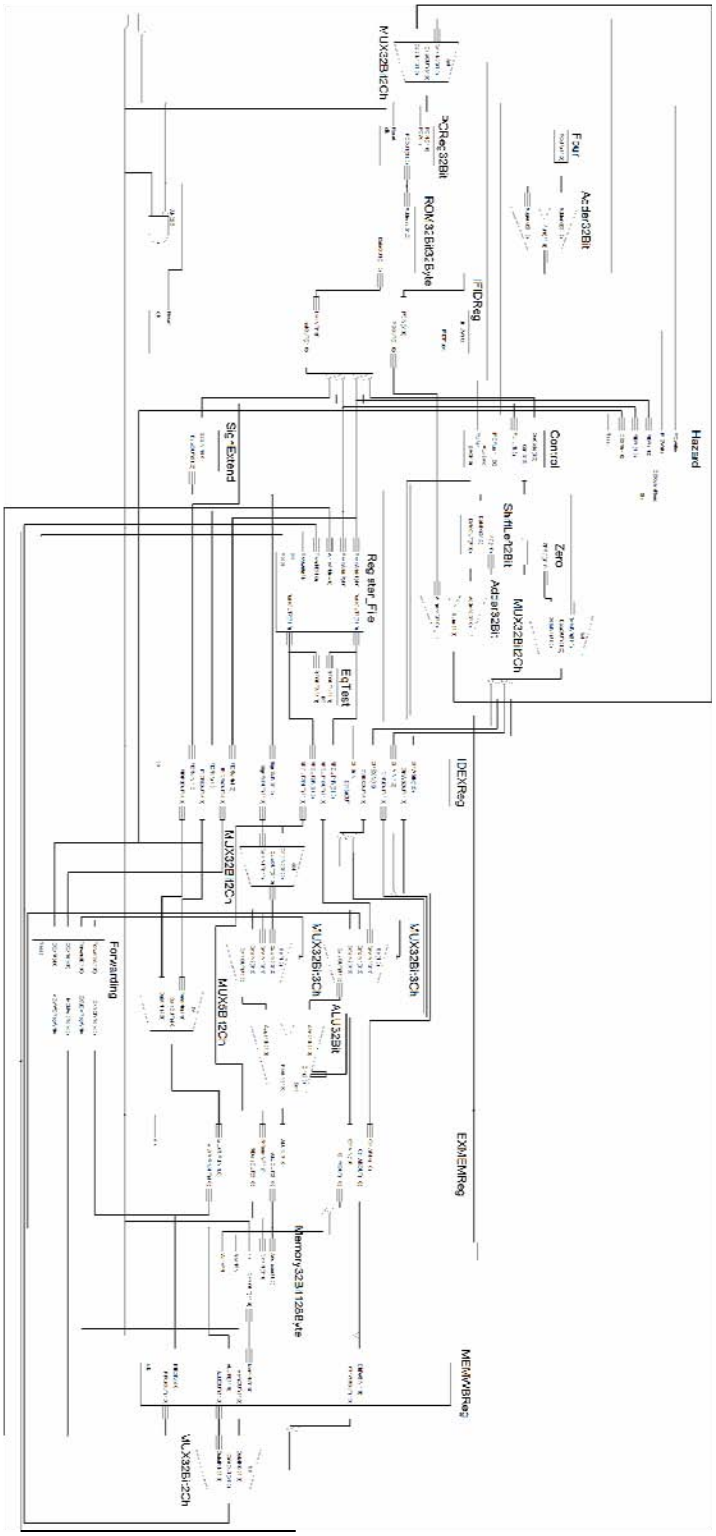
## 1.7 Calculate the highest clock rate of the hardware.

Timing Summary:
---
Speed Grade: -5

Minimum period: 13.920ns (Maximum Frequency: 71.840MHz)
Minimum input arrival time before clock: No path found
Maximum output Required time after clock: 21.293ns
Maximum combinational path delay: No path found

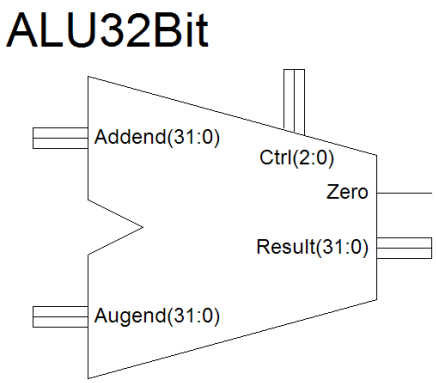
## 2. (Extra Credit) Chap 6. Exercise 6.46 Pipelined Single-Cycle Computer Behavioral simulation only but make sure that your design is synthesizable.

### 2.1 Top-level block diagram



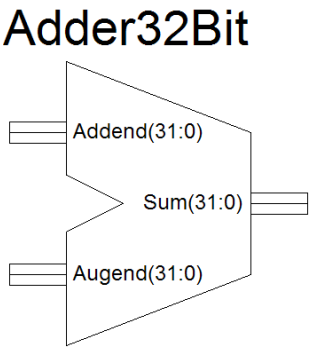
## 2.2 Design source codes in Verilog

### ALU



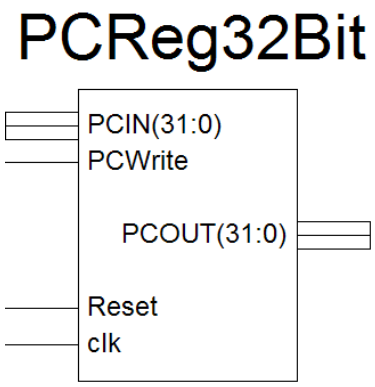

```
//////////////////////////////////////////////////////////////////////////////////
// Company:           Temple University
// Engineer:          Zexi Liu
// Create Date:       11:25:48 03/05/2007
// Design Name:       Pipelined Single-Cycle Computer
// Module Name:       ALU32Bit
// Project Name:      Pipelined Single-Cycle Computer
// Target Devices:    Spartan-3 XC3S400
// Tool versions:     Xilinx ISE 8.2i
// Description:       32-bit ALU
//////////////////////////////////////////////////////////////////////////////////
module ALU32Bit(Ctrl, Addend, Augend,     Result, Zero);
    input     [2:0]     Ctrl;
    input     [31:0]    Addend;
    input     [31:0]    Augend;
    output    [31:0]    Result;
    output    Zero;
    reg  [31:0]    Result;
    reg  Zero;
    always @(Addend or Augend or Ctrl or      Result)
    begin
        case (Ctrl)
            3'b000 :    Result = Addend & Augend;       // AND
            3'b001 :    Result = Addend | Augend;  // OR
            3'b010 :    Result = Addend + Augend;       // ADD
            3'b110 :    Result = Addend - Augend;  // SUBTRACT
            3'b111 :
                if (Addend < Augend)
                    Result = 32'd1;             //SLT
                else
                    Result = 32'd0;             //SLT
            default :   Result = 32'hxxxxxxxx;
        endcase
        if (Result == 32'd0)
            Zero = 1;
        else
            Zero = 0;
    end
endmodule
```

### 32-bit Adder




```
//////////////////////////////////////////////////////////////////////////////////
// Company:           Temple University
// Student:           Zexi Liu
// Create Date:       11:12:08 03/07/2007
// Design Name:       Pipelined Single-Cycle Computer
// Module Name:       Adder32Bit
// Project Name:      Pipelined Single-Cycle Computer
// Target Devices:    Spartan-3 XC3S400
// Tool versions:     Xilinx ISE 8.2i
// Description:       This is a 32-bit adder
//////////////////////////////////////////////////////////////////////////////////
module Adder32Bit(Addend, Augend, Sum);
    input [31:0] Addend;
    input [31:0] Augend;
    output [31:0] Sum;
    assign Sum = Addend + Augend;
endmodule
```

### 32-bit PC Register

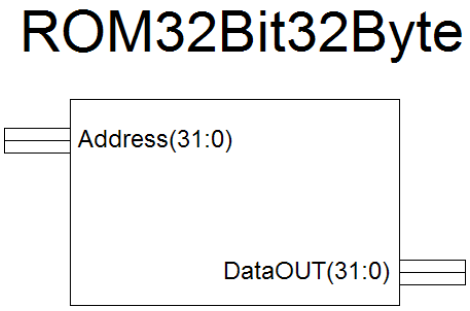



```
//////////////////////////////////////////////////////////////////////////////////
// Company:           Temple University
// Student:           Zexi Liu
// Create Date:       12:12:53 03/07/2007
// Design Name:       Pipelined Single-Cycle Computer
// Module Name:       PCReg32Bit
// Project Name:      Pipelined Single-Cycle Computer
// Target Devices:    Spartan-3 XC3S400
// Tool versions:     Xilinx ISE 8.2i
// Description:       32-bit      Register for PC
//////////////////////////////////////////////////////////////////////////////////
module PC Reg32Bit(DataIN, DataOUT, clk,        Reset);
    input       clk;
    input       Reset;
    input       [31:0] DataIN;
    output      [31:0] DataOUT;
    Reg         [31:0] DataOUT;

    always @(negedge clk or negedge       Reset)
    begin
        if(   Reset == 0)
            DataOUT <= 0;
        else
            DataOUT <= DataIN;
    end

endmodule
```

### 32-bit ROM




```
//////////////////////////////////////////////////////////////////////////////////
// Company:           Temple University
// Student:           Zexi Liu
// Create Date:       14:12:02 03/07/2007
// Design Name:       Pipelined Single-Cycle Computer
// Module Name:       ROM32Bit32Byte
// Project Name:      Pipelined Single-Cycle Computer
// Target Devices:    Spartan-3 XC3S400
// Tool versions:     Xilinx ISE 8.2i
// Description:       store the instructions
//////////////////////////////////////////////////////////////////////////////////
module ROM32Bit32Byte(Address, DataOUT);
    input [31:0] Address;
    output [31:0] DataOUT;
    reg [31:0] DataOUT;

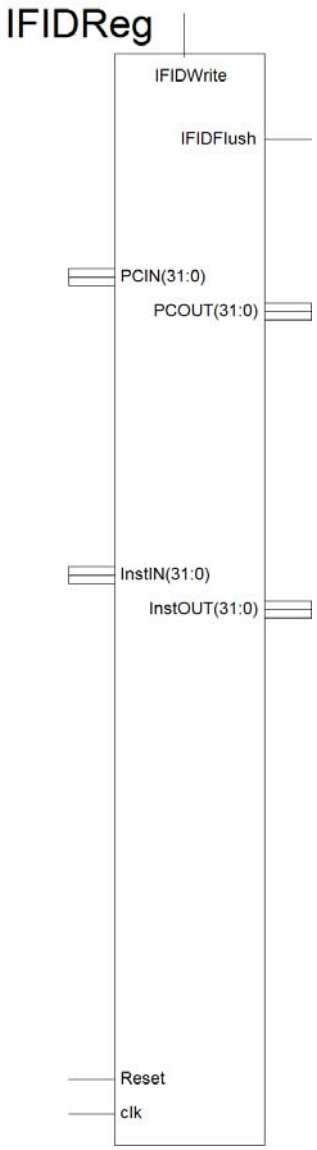
    always @(Address or DataOUT)
    begin
        if ((Address % 4) != 0)
        begin
            $display($time, " rom32 error: unaligned Address %d", Address);
            DataOUT = 32'd0;
        end
        else
        begin
            case (Address[6:2])
                5'd0 : DataOUT = { 6'd35, 5'd0, 5'd2, 16'd4 }; // lw $2, 4($0)          r2 = 1
                5'd1 : DataOUT = { 6'd35, 5'd0, 5'd3, 16'd8 }; // lw $3, 8($0)          r3 = 2
                5'd2 : DataOUT = { 6'd35, 5'd0, 5'd4, 16'd20 };// lw $4, 20($0)         r4 = 5
                5'd3 : DataOUT = { 6'd0, 5'd0, 5'd0, 5'd5, 5'd0, 6'd32 };   // add $5, $0, $0          r5 = 0
                5'd4 : DataOUT = { 6'd0, 5'd5, 5'd2, 5'd5, 5'd0, 6'd32 };   // add $5, $5, $2          r5 = r5 + 1
                5'd5 : DataOUT = { 6'd0, 5'd4, 5'd5, 5'd6, 5'd0, 6'd42 };   // slt  $6, $4, $5         r5 >= 5?
```

```
                5'd6 : DataOUT = { 6'd4, 5'd6, 5'd0, -16'd3 };  // beq $6, $zero -3       if not go back 2
                5'd7 : DataOUT = { 6'd43, 5'd0, 5'd5, 16'd0 }; // sw $5, 0($zero)        MEM[0] = $5 = 6
                default DataOUT = 32'h0000;
            endcase
            $display($time, "       Reading data: rom32[%h] => %h", Address, DataOUT);
        end
    end
endmodule
```

## IF/ID Register

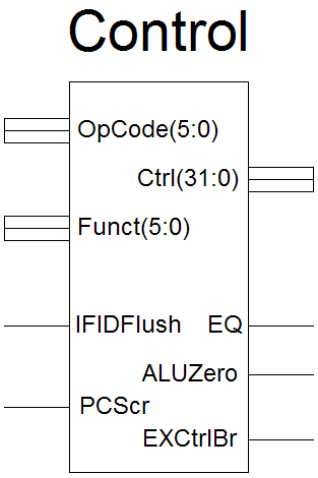
```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         14:12:02 03/07/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         IFIDReg
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         register between IF and ID stage
//////////////////////////////////////////////////////////////////////////////////
module IFIDReg(PCIN, PCOUT, InstIN, InstOUT, IFIDWrite, IFIDFlush, clk,
    Reset);
    input [31:0] PCIN;
    output [31:0] PCOUT;
    input [31:0] InstIN;
    output [31:0] InstOUT;
    input IFIDWrite;
    input IFIDFlush;
     input clk;
     input      Reset;
     reg   [31:0] PCOUT;
     reg   [31:0] InstOUT;

    always @(negedge clk or posedge      Reset) // or posedge IFIDFlush)
    begin
        if(Reset == 1'b1)
        begin
            InstOUT <= 32'b111111xxxxxxxxxxxxxxxxxxxxxxxxxx;
            PCOUT <= 32'd0;
        end
        else
        begin
            if(IFIDFlush == 1'b1)
            begin
                PCOUT <= 32'd0;
                InstOUT <= 32'd0;
            end
            else
            begin
                if(IFIDWrite == 1'b1)
                begin
                    PCOUT <= PCIN;
                    InstOUT <= InstIN;
                end
                else
                begin
                    PCOUT <= PCOUT;
                    InstOUT <= InstOUT;
                end
            end
        end
    end
```



endmodule

## Control Module




```
//////////////////////////////////////////////////////////////////////////////////
// Company:           Temple University
// Student:           Zexi Liu
// Create Date:       19:14:56 04/06/2007
// Design Name:       Pipelined Single-Cycle Computer
// Module Name:       Control
// Project Name:      Pipelined Single-Cycle Computer
// Target Devices:    Spartan-3 XC3S400
// Tool versions:     Xilinx ISE 8.2i
// Description:       Generate Control signal
//////////////////////////////////////////////////////////////////////////////////
module Control(OpCode, Funct, Ctrl, EQ, ALUZero, IFIDFlush, PCScr,
EXCtrlBr);
    input [5:0] OpCode;
    input [5:0] Funct;
    input EQ;
    input ALUZero;
    input EXCtrlBr;
    output [31:0] Ctrl;
    output IFIDFlush;
    output PCScr;
    reg [31:0] Ctrl;
    reg IFIDFlush;
    reg PCScr;

    parameter R_FORMAT      = 6'd0;
    parameter LW            = 6'd35;
    parameter SW            = 6'd43;
    parameter BEQ           = 6'd4;
    parameter Init          = 6'b111111;

    // symbolic constants for instruction function code
    parameter Funct_add   = 6'd32;
    parameter Funct_sub   = 6'd34;
    parameter Funct_and   = 6'd36;
    parameter Funct_or    = 6'd37;
    parameter Funct_slt   = 6'd42;

    // symbolic constants for ALU Operations
    parameter ALU_add   = 3'b010;
    parameter ALU_sub   = 3'b110;
    parameter ALU_and   = 3'b000;
    parameter ALU_or    = 3'b001;
    parameter ALU_slt   = 3'b111;

    always @(OpCode)
    begin
        case (OpCode)
            R_FORMAT :
            begin
                Ctrl[0]     = 1'b0;     // Branch       =   1'b0;   ID
                Ctrl[1]     = 1'b1;     //   RegDst     =   1'b1;   ID
                Ctrl[2]     = 1'b0;     // ALUSrc       =   1'b1;   EX
                Ctrl[3]     = 1'b1;     // RorI         =   1'b1;   EX
                //Ctrl[6:4]                                        EX
                Ctrl[7]     = 1'b0;     // MemRead      =   1'b0;   MEM
                Ctrl[8]     = 1'b0;     // MemWrite     =   1'b0;   MEM
                Ctrl[9]     = 1'b1;     // Mem2Reg      =   1'b0;   WB
                Ctrl[10]    = 1'b1;     //   RegWrite   =   1'b1;   WB
                Ctrl[12:11] = 2'b10;    // ALU_Op_Code  =   2'b10;
```

```
end
LW :
begin
	Ctrl[0]	= 1'b0;		// Branch	=	1'b0;	ID
	Ctrl[1]	= 1'b0;		//	RegDst	=	1'b0;	ID
	Ctrl[2]	= 1'b1;		// ALUSrc	=	1'b0;	EX
	Ctrl[3]	= 1'b0;		// RorI	=	1'b0;	EX
	//Ctrl[6:4]				EX
	Ctrl[7]	= 1'b1;		// MemRead	=	1'b1;	MEM
	Ctrl[8]	= 1'b0;		// MemWrite	=	1'b0;	MEM
	Ctrl[9]	= 1'b0;		// Mem2Reg	=	1'b1;	WB
	Ctrl[10]	= 1'b1;		//	RegWrite	=	1'b1;	WB
	Ctrl[12:11] = 2'b00;	// ALU_Op_Code	=	2'b00;
end
SW :
begin
	Ctrl[0]	= 1'b0;		// Branch	=	1'b0;	ID
	Ctrl[1]	= 1'bx;		//	RegDst	=	1'bx;	ID
	Ctrl[2]	= 1'b1;		// ALUSrc	=	1'b1;	EX
	Ctrl[3]	= 1'b0;		// RorI	=	1'b0;	EX
	//Ctrl[6:4]				EX
	Ctrl[7]	= 1'b0;		// MemRead	=	1'b0;	MEM
	Ctrl[8]	= 1'b1;		// MemWrite	=	1'b1;	MEM
	Ctrl[9]	= 1'bx;		// Mem2Reg	=	1'bx;	WB
	Ctrl[10]	= 1'b0;		//	RegWrite	=	1'b0;	WB
	Ctrl[12:11] = 2'b00;	// ALU_Op_Code	=	2'b00;
end
BEQ :
begin
	Ctrl[0]	= 1'b1;		// Branch	=	1'b1;	ID
	Ctrl[1]	= 1'bx;		//	RegDst	=	1'bx;	ID
	Ctrl[2]	= 1'b0;		// ALUSrc	=	1'b1;	EX
	Ctrl[3]	= 1'b0;		// RorI	=	1'b0;	EX
	//Ctrl[6:4]				EX
	Ctrl[7]	= 1'b0;		// MemRead	=	1'b0;	MEM
	Ctrl[8]	= 1'b0;		// MemWrite	=	1'b0;	MEM
	Ctrl[9]	= 1'bx;		// Mem2Reg	=	1'bx;	WB
	Ctrl[10]	= 1'b0;		//	RegWrite	=	1'b0;	WB
	Ctrl[12:11] = 2'b01;	// ALU_Op_Code	=	2'b01;
end
Init :
begin
	$display($time, " Control unit initialization.");
	Ctrl[0]	= 1'b0;		// Branch	=	1'b0;	ID
	Ctrl[1]	= 1'b0;		//	RegDst	=	1'b0;	ID
	Ctrl[2]	= 1'b0;		// ALUSrc	=	1'b0;	EX
	Ctrl[3]	= 1'b0;		// RorI	=	1'b0;	EX
	//Ctrl[6:4]				EX
	Ctrl[7]	= 1'b0;		// MemRead	=	1'b0;	MEM
	Ctrl[8]	= 1'b0;		// MemWrite	=	1'b0;	MEM
	Ctrl[9]	= 1'b0;		// Mem2Reg	=	1'b0;	WB
	Ctrl[10]	= 1'b0;		//	RegWrite	=	1'b0;	WB
	Ctrl[12:11] = 2'b11;	// ALU_Op_Code	=	2'b11;
end
default :
begin
	$display($time, " Control unit unimplemented OpCode %d", OpCode);
	Ctrl[0]	= 1'b0;		// Branch	=	1'b0;	ID
	Ctrl[1]	= 1'b0;		//	RegDst	=	1'bx;	ID
	Ctrl[2]	= 1'b0;		// ALUSrc	=	1'bx;	EX
	Ctrl[3]	= 1'b0;		// RorI	=	1'bx;	EX
	//Ctrl[6:4]				EX
	Ctrl[7]	= 1'b0;		// MemRead	=	1'bx;	MEM
	Ctrl[8]	= 1'b0;		// MemWrite	=	1'bx;	MEM
```

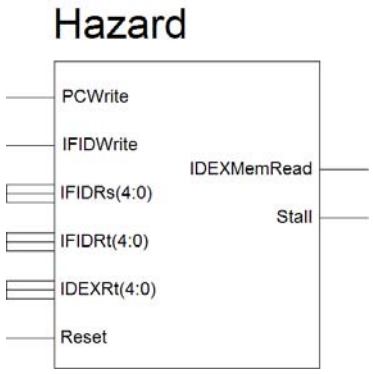
```
                Ctrl[9]     = 1'b0;          // Mem2Reg     =   1'bx;     WB
                Ctrl[10]    = 1'b0;          //     RegWrite  =   1'bx;     WB
                Ctrl[12:11] = 2'b00;    // ALU_Op_Code     =   2'bxx;
            end
        endcase
        Ctrl[31:13] = 20'd0;
    end

    always @(Ctrl or Funct)
    begin
        case (Ctrl[12:11])
            2'b00 : Ctrl[6:4] = ALU_add;                    // ALU_Operation = ALU_add;
            2'b01 : Ctrl[6:4] = ALU_sub;                    // ALU_Operation = ALU_sub;
            2'b10 :
                case (Funct)
                    Funct_add   : Ctrl[6:4] = ALU_add;      // ALU_Operation = ALU_add;
                    Funct_sub   : Ctrl[6:4] = ALU_sub;      // ALU_Operation = ALU_sub;
                    Funct_and   : Ctrl[6:4] = ALU_and;      // ALU_Operation = ALU_and;
                    Funct_or    : Ctrl[6:4] = ALU_or;       // ALU_Operation = ALU_or;
                    Funct_slt   : Ctrl[6:4] = ALU_slt;      // ALU_Operation = ALU_slt;
                    default     : Ctrl[6:4] = 3'b000;       // ALU_Operation = 3'bxxx;
                endcase
            default Ctrl[6:4] = 3'b000;                     // ALU_Operation = 3'bxxx;
        endcase
        Ctrl[31:13] = 20'd0;
    end

    always @(ALUZero or Ctrl[0])                            // Branch <-> Ctrl[0]
    begin
        if(ALUZero == 1'b1 && Ctrl[0] == 1'b1)
        begin
            PCScr = 1'b1;
            IFIDFlush = 1'b1;
        end
        else
        begin
            PCScr = 1'b0;
            IFIDFlush = 1'b0;
        end
    end
endmodule
```

## Hazard Unit

```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         16:48:26 04/08/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         Hazard
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         Hazard detection
//////////////////////////////////////////////////////////////////////////////////
module Hazard(IDEXMemRead, IDEXRt, IFIDRs, IFIDRt, PCWrite,
IFIDWrite, Stall,       Reset);
    input IDEXMemRead;
    input [4:0] IDEXRt;
    input [4:0] IFIDRs;
    input [4:0] IFIDRt;
     input      Reset;
    output PCWrite;
    output IFIDWrite;
```



```
        output Stall;
        reg PCWrite;
        Reg IFIDWrite;
        Reg Stall;

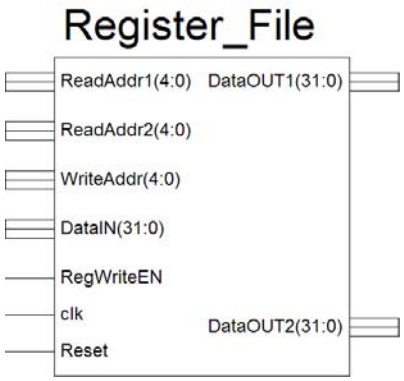
        always @(IDEXMemRead or IDEXRt or IFIDRs or IFIDRt or  Reset)
        begin
                if(Reset == 1'b1)
                begin
                        Stall = 1'b0;
                        PCWrite = 1'b1;
                        IFIDWrite = 1'b1;
                end
                else
                begin
                        if((IDEXMemRead == 1'b1) && ((IDEXRt == IFIDRs) || (IDEXRt == IFIDRt)))
                        begin
                                Stall = 1'b1;
                                PCWrite = 1'b0;
                                IFIDWrite = 1'b0;
                        end
                        else
                        begin
                                Stall = 1'b0;
                                PCWrite = 1'b1;
                                IFIDWrite = 1'b1;
                        end
                end
        end
endmodule
```

## Register File

```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         16:48:26 04/08/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         Register_File
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         Register File
//////////////////////////////////////////////////////////////////////////////////
module      Register_File(clk,      RegWriteEN,     ReadAddr1,
        ReadAddr2, WriteAddr, DataOUT1, DataOUT2, DataIN,
        Reset);
        input clk;
        input [31:0] DataIN;
        input        RegWriteEN;
        input [4:0] WriteAddr;
        input [4:0]         ReadAddr1;
        input [4:0]         ReadAddr2;
        input        Reset;
        output [31:0] DataOUT1;
        output [31:0] DataOUT2;

        reg [31:0] DataOUT1, DataOUT2;
        reg [31:0] File_Array [31:0];

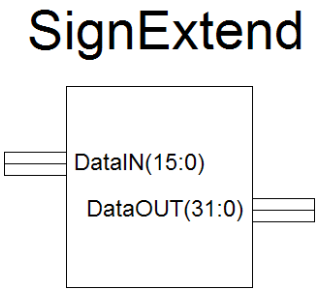
        always @(posedge clk)
        begin
                if (RegWriteEN && (WriteAddr != 0))
                begin
```



```
                File_Array[WriteAddr] <= DataIN;
                $display($time, "       Reg_File[%d] <= %d (Write)", WriteAddr, DataIN);
            end
        end

        always @(File_Array[WriteAddr] or     ReadAddr1 or     ReadAddr2)
        begin
            // if(clk == 1'b1)
            begin
                // if (Reset != 1'b1)
                begin
                    if (ReadAddr1 == 0)
                    begin
                        DataOUT1 = 32'd0;     //$zero      Register = 0
                        $display($time, "       Reg_File[%d] => %d (Port 1)",     ReadAddr1, DataOUT1);
                    end
                    else
                    begin
                        DataOUT1 = File_Array[ReadAddr1];
                        $display($time, "       Reg_File[%d] => %d (Port 1)",     ReadAddr1, DataOUT1);
                    end
                    if (ReadAddr2 == 0)
                    begin
                        DataOUT2 = 32'd0;    //$zero       Register = 0
                        $display($time, "       Reg_File[%d] => %d (Port 2)",     ReadAddr2, DataOUT2);
                    end
                    else
                    begin
                        DataOUT2 = File_Array[ReadAddr2];
                        $display($time, "       Reg_File[%d] => %d (Port 2)",     ReadAddr2, DataOUT2);
                    end
                end
            end
        end
endmodule
```

## Sign Extend




```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         23:03:12 03/07/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         SignExtend
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         sign extend
//////////////////////////////////////////////////////////////////////////////////
module SignExtend(DataIN, DataOUT);
    input [15:0] DataIN;
    output [31:0] DataOUT;
    wi     Re [31:0] DataOUT;
    assign DataOUT = { {16{DataIN[15]}}, DataIN };
endmodule
```

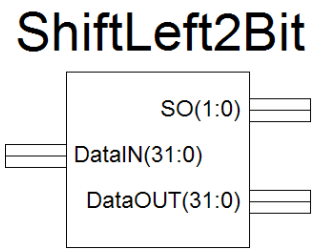
## Shift left 2 bits

```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         22:49:04 03/07/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         ShiftLeft2Bit
```

```
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         Shift the input 32-bit data left by 2 bits
//////////////////////////////////////////////////////////////////////////////////
module ShiftLeft2Bit(DataIN, DataOUT, SO);
        input [31:0] DataIN;
        output [31:0] DataOUT;
        output [1:0] SO;
        wi     Re [31:0] DataOUT;
        wi     Re [1:0] SO;

        assign SO = DataIN[31:30];
        assign DataOUT = DataIN << 2;    // shift left 2 bits

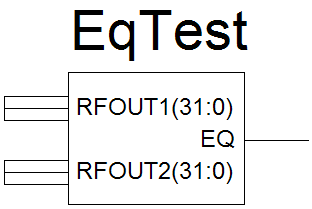
endmodule
```




### Equality Test

```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         22:49:04 03/07/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         EqTest
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         Test if two inputs are equal
//////////////////////////////////////////////////////////////////////////////////
module EqTest(RFOUT1, RFOUT2, EQ);
       input [31:0] RFOUT1;
       input [31:0] RFOUT2;
       output EQ;
        reg EQ;

        always @(RFOUT1 or RFOUT2)
        begin
              if(RFOUT1 == RFOUT2)
                    EQ = 1'b1;
              else
                    EQ = 1'b0;
        end
endmodule
```



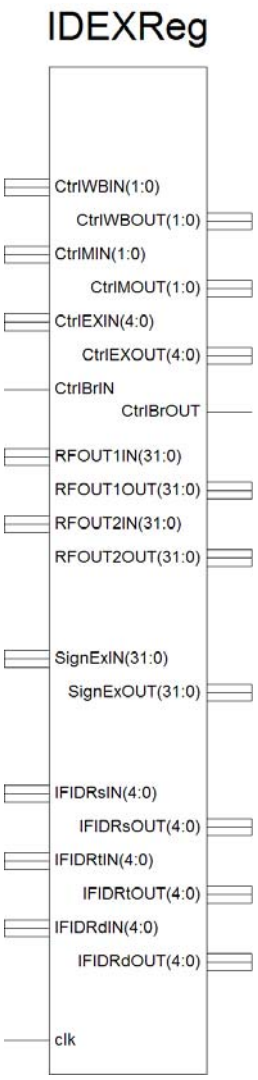

### ID/EX Register

```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         16:17:12 04/06/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         IDEXReg
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         register between ID and EX stage
//////////////////////////////////////////////////////////////////////////////////
module IDEXReg(CtrlWBIN, CtrlMIN, CtrlEXIN, RFOUT1IN, RFOUT2IN, RFOUT1OUT, RFOUT2OUT,
SignExIN, SignExOUT, IFIDRsIN, IFIDRsOUT, IFIDRtIN, IFIDRtOUT, IFIDRdIN, IFIDRdOUT, clk, CtrlWBOUT,
CtrlMOUT, CtrlEXOUT, CtrlBrIN, CtrlBrOUT);
       input [1:0] CtrlWBIN;
       input [1:0] CtrlMIN;
       input [4:0] CtrlEXIN;
```

```
        input [31:0] RFOUT1IN;
        input [31:0] RFOUT2IN;
        output [31:0] RFOUT1OUT;
        output [31:0] RFOUT2OUT;
        input [31:0] SignExIN;
        output [31:0] SignExOUT;
        input [4:0] IFIDRsIN;
        output [4:0] IFIDRsOUT;
        input [4:0] IFIDRtIN;
        output [4:0] IFIDRtOUT;
        input [4:0] IFIDRdIN;
        output [4:0] IFIDRdOUT;
        input clk;
        output [1:0] CtrlWBOUT;
        output [1:0] CtrlMOUT;
        output [4:0] CtrlEXOUT;
         input CtrlBrIN;
         output CtrlBrOUT;

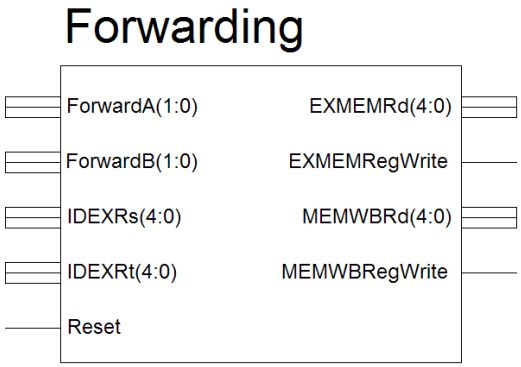
         reg [31:0] RFOUT1OUT;
         Reg [31:0] RFOUT2OUT;
         reg [31:0] SignExOUT;
         reg [4:0] IFIDRsOUT;
         reg [4:0] IFIDRtOUT;
         reg [4:0] IFIDRdOUT;
         reg [1:0] CtrlWBOUT;
         Reg [1:0] CtrlMOUT;
         Reg [4:0] CtrlEXOUT;
         reg CtrlBrOUT;

         always @(negedge clk)
         begin
                RFOUT1OUT <= RFOUT1IN;
                RFOUT2OUT <= RFOUT2IN;
                SignExOUT <= SignExIN;
                IFIDRsOUT <= IFIDRsIN;
                IFIDRtOUT <= IFIDRtIN;
                IFIDRdOUT <= IFIDRdIN;
                CtrlWBOUT <= CtrlWBIN;
                CtrlMOUT    <= CtrlMIN;
                CtrlEXOUT <= CtrlEXIN;
                CtrlBrOUT <= CtrlBrIN;
        end
endmodule
```




## Forwarding Unit

```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         16:17:12 04/06/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         Forwarding
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         Forwarding Unit
//////////////////////////////////////////////////////////////////////////////////
module Forwarding(IDEXRs, IDEXRt, EXMEMRd,
MEMWBRd, EXMEMRegWrite, MEMWBRegWrite,
ForwardA, ForwardB,          Reset);
        input [4:0] IDEXRs;
        input [4:0] IDEXRt;
        input [4:0] EXMEMRd;
```



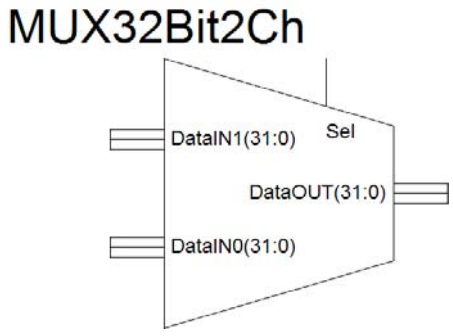
```
        input [4:0] MEMWBRd;
        input EXMEMRegWrite;
        input MEMWBRegWrite;
         input          Reset;
        output [1:0] ForwardA;
        output [1:0] ForwardB;
         Reg [1:0] ForwardA;
         Reg [1:0] ForwardB;

         always @(IDEXRs or IDEXRt or EXMEMRd or MEMWBRd or EXMEMRegWrite or MEMWBRegWrite or
         Reset)
         begin
                if(Reset == 1'b1)
                begin
                        ForwardA = 2'b00;
                        ForwardB = 2'b00;
                end
                else
                begin
                        if((EXMEMRegWrite == 1'b1) && (EXMEMRd != 5'b0) && (EXMEMRd == IDEXRs))
                        begin
                                ForwardA = 2'b01;
                                ForwardB = 2'b00;
                        end
                        else if((EXMEMRegWrite == 1'b1) && (EXMEMRd != 5'b0) && (EXMEMRd == IDEXRt))
                        begin
                                ForwardA = 2'b00;
                                ForwardB = 2'b01;
                        end
                        else if((MEMWBRegWrite == 1'b1) && (MEMWBRd != 5'b0) && (EXMEMRd != IDEXRs) &&
(MEMWBRd == IDEXRs))
                        begin
                                ForwardA = 2'b10;
                                ForwardB = 2'b00;
                        end
                        else if((MEMWBRegWrite == 1'b1) && (MEMWBRd != 5'b0) && (EXMEMRd != IDEXRt) &&
(MEMWBRd == IDEXRt))
                        begin
                                ForwardA = 2'b00;
                                ForwardB = 2'b10;
                        end
                        else
                        begin
                                ForwardA = 2'b00;
                                ForwardB = 2'b00;
                        end
                end
        end

endmodule
```

## 32-bit 2-1 Multiplexer

```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         11:22:54 03/07/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         MUX32Bit2Ch
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         32-bit MUX 2-in 1-out
//////////////////////////////////////////////////////////////////////////////////
```



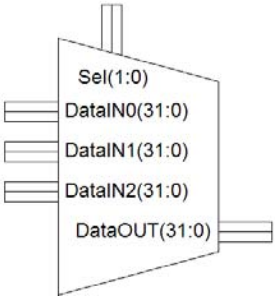
```
module MUX32Bit2Ch(Sel, DataIN0, DataIN1, DataOUT);
	parameter bitwidth = 32;
	input [bitwidth-1:0] DataIN0;
	input [bitwidth-1:0] DataIN1;
	input Sel;
	output [bitwidth-1:0] DataOUT;

	assign DataOUT = Sel ? DataIN1 : DataIN0;

endmodule
```

## 32-bit 3-1 Multiplexer

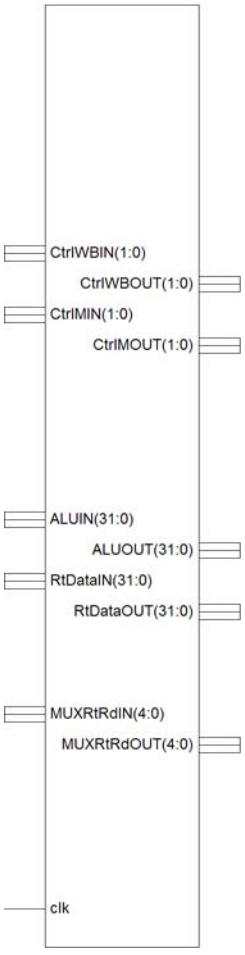
MUX32Bit3Ch




```
//////////////////////////////////////////////////////////////////////////////////
// Company:		Temple University
// Student:		Zexi Liu
// Create Date:		11:22:54 03/07/2007
// Design Name:		Pipelined Single-Cycle Computer
// Module Name:		MUX32Bit3Ch
// Project Name:	Pipelined Single-Cycle Computer
// Target Devices:	Spartan-3 XC3S400
// Tool versions:	Xilinx ISE 8.2i
// Description:		32-bit MUX 3-in 1-out
//////////////////////////////////////////////////////////////////////////////////
module MUX32Bit3Ch(Sel, DataIN0, DataIN1, DataIN2, DataOUT);
	parameter bitwidth = 32;
	input [bitwidth-1:0] DataIN0;
	input [bitwidth-1:0] DataIN1;
	input [bitwidth-1:0] DataIN2;
	input [1:0] Sel;
	output [bitwidth-1:0] DataOUT;
	reg [bitwidth-1:0] DataOUT;

	always @(Sel or DataIN0 or DataIN1 or DataIN2)
	begin
		case (Sel)
		2'd0:	DataOUT = DataIN0;
		2'd1:	DataOUT = DataIN1;
		2'd2:	DataOUT = DataIN2;
		default:	DataOUT = 32'hxxxx;
		endcase
	end
endmodule
```

EXMEMReg




## EX/MEM Register

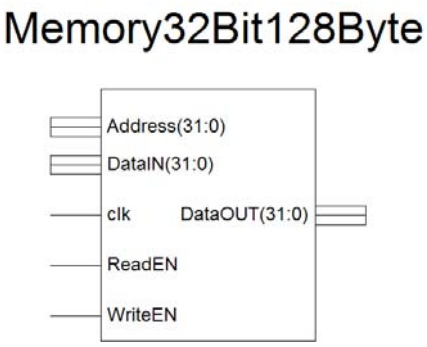
```
//////////////////////////////////////////////////////////////////////////////////
// Company:		Temple University
// Student:		Zexi Liu
// Create Date:		16:17:12 04/06/2007
// Design Name:		Pipelined Single-Cycle Computer
// Module Name:		EXMEMReg
// Project Name:	Pipelined Single-Cycle Computer
// Target Devices:	Spartan-3 XC3S400
// Tool versions:	Xilinx ISE 8.2i
// Description:		register between EX and MEM stage
//////////////////////////////////////////////////////////////////////////////////
module EXMEMReg(CtrlWBIN, CtrlWBOUT, CtrlMIN, CtrlMOUT, ALUIN, ALUOUT,
MUXRtRdIN, MUXRtRdOUT, RtDataIN, RtDataOUT, clk);
	input [1:0] CtrlWBIN;
	output [1:0] CtrlWBOUT;
	input [1:0] CtrlMIN;
	output [1:0] CtrlMOUT;
```

```
    input [31:0] ALUIN;
    output [31:0] ALUOUT;
    input [4:0] MUXRtRdIN;
    output [4:0] MUXRtRdOUT;
     input [31:0] RtDataIN;
     output [31:0] RtDataOUT;
    input clk;

     Reg [1:0] CtrlWBOUT;
     Reg [1:0] CtrlMOUT;
     Reg [31:0] ALUOUT;
     Reg [4:0] MUXRtRdOUT;
     reg [31:0] RtDataOUT;

     always @(negedge clk)
     begin
          CtrlWBOUT    <= CtrlWBIN;
          CtrlMOUT     <= CtrlMIN;
          ALUOUT        <= ALUIN;
          MUXRtRdOUT <= MUXRtRdIN;
          RtDataOUT     <= RtDataIN;
     end
endmodule
```

## Memory




```
//////////////////////////////////////////////////////////////////////////////////
// Company:             Temple University
// Student:             Zexi Liu
// Create Date:         16:17:12 04/06/2007
// Design Name:         Pipelined Single-Cycle Computer
// Module Name:         Memory32Bit128Byte
// Project Name:        Pipelined Single-Cycle Computer
// Target Devices:      Spartan-3 XC3S400
// Tool versions:       Xilinx ISE 8.2i
// Description:         Data memory
//////////////////////////////////////////////////////////////////////////////////
module Memory32Bit128Byte(clk,       ReadEN, WriteEN, Address,
DataIN, DataOUT);
     input      clk;
     input      ReadEN;
     input      WriteEN;
     input      [31:0] Address;
     input      [31:0] DataIN;
     output     [31:0] DataOUT;
     reg        [31:0] DataOUT;

     parameter BASE_ADDRESS = 25'd0;

     reg [31:0] Memory_Array [0:31];
     wire [4:0] Memory_Offset;
     wire Address_Select;

     assign Memory_Offset = Address[6:2];

     assign Address_Select = (Address[31:7] == BASE_ADDRESS);    // address decoding

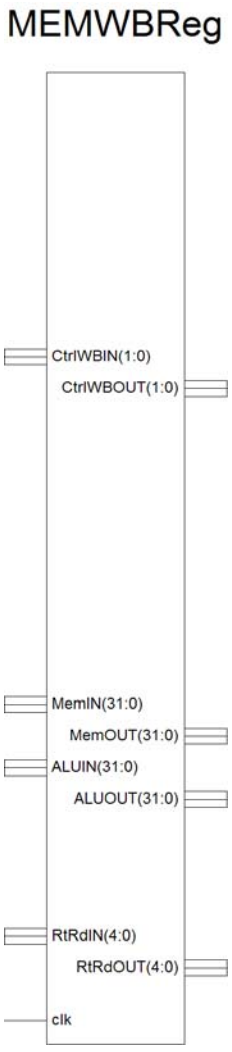
     // for      ReadEN operations
     always @(ReadEN or Address_Select or Memory_Offset or Memory_Array[Memory_Offset] or Address)
     begin
          if (ReadEN == 1'b1 && Address_Select == 1'b1)
          begin
               if ((Address % 4) != 0)
               begin
```

```
                $display($time, " rom32 error: unaligned address %h", Address);
                DataOUT = 32'hxxxxxxxx;
            end
            else
            begin
                DataOUT = Memory_Array[Memory_Offset];
                $display($time, "       Reading data: Mem[%h] => %h", Address, DataOUT);
            end
        end
        else
        begin
            DataOUT = 32'hxxxxxxxx;
        end
    end

    // for WriteEN operations
    always @(negedge clk)
    begin
        if (WriteEN == 1'b1 && Address_Select == 1'b1)
        begin
            $display($time, " Writing data: Mem[%h] <= %h", Address, DataIN);
            Memory_Array[Memory_Offset] <= DataIN;
        end
    end

    // initialize with some arbitrary values
    integer i;
    initial
    begin
        for (i=0; i<7; i=i+1)
            Memory_Array[i] = i;
    end
endmodule
```

## MEM/WB Register




```
//////////////////////////////////////////////////////////////////////////////////
// Company:           Temple University
// Student:           Zexi Liu
// Create Date:       16:17:12 04/06/2007
// Design Name:       Pipelined Single-Cycle Computer
// Module Name:       MEMWBReg
// Project Name:      Pipelined Single-Cycle Computer
// Target Devices:    Spartan-3 XC3S400
// Tool versions:     Xilinx ISE 8.2i
// Description:       register between MEM and WB stage
//////////////////////////////////////////////////////////////////////////////////
module MEMWBReg(CtrlWBIN, CtrlWBOUT, MemIN, MemOUT, ALUIN, ALUOUT,
RtRdIN, RtRdOUT, clk);
    input [1:0] CtrlWBIN;
    output [1:0] CtrlWBOUT;
    input [31:0] MemIN;
    output [31:0] MemOUT;
    input [31:0] ALUIN;
    output [31:0] ALUOUT;
    input [4:0] RtRdIN;
    output [4:0] RtRdOUT;
    input clk;

     Reg [1:0] CtrlWBOUT;
     Reg [31:0] MemOUT;
     Reg [31:0] ALUOUT;
     Reg [4:0] RtRdOUT;
```

```
        always @(negedge clk)
        begin
                CtrlWBOUT <= CtrlWBIN;
                MemOUT    <= MemIN;
                ALUOUT    <= ALUIN;
                RtRdOUT   <= RtRdIN;
        end
endmodule
```

## 2.3 Testbench for Top-level design

```
//////////////////////////////////////////////////////////////////////////////
// Copyright (c) 1995-2003 Xilinx, Inc.
// All Right         Reserved.
//////////////////////////////////////////////////////////////////////////////
//   ____    ____
//  /   /\/   /
// /___/  \  /              Vendor: Xilinx
// \   \   \/               Version : 8.2i
//  \   \                   
//  /   /                   Filename : PSCC_top_tbw.tfw
// /___/   /\               Timestamp : Sat Apr 28 17:16:20 2007
// \   \  /  \
//  \___\/\___\
//
//Design Name: PSCC_top_tbw_tb_0
//Device: Xilinx

`timescale 1ns/1ps

module PSCC_top_tbw_tb_0;
        Reg clk = 1'b0;
        Reg   Reset = 1'b0;
       wire ALU0;
       wire [1:0] SO;

       parameter PERIOD = 200;
       parameter    Real DUTY_CYCLE = 0.5;
       parameter OFFSET = 0;

       initial       // Clock process for clk
       begin
             #OFFSET;
             forever
             begin
                   clk = 1'b0;
                   #(PERIOD-(PERIOD*DUTY_CYCLE)) clk = 1'b1;
                   #(PERIOD*DUTY_CYCLE);
             end
       end

       Pipelined_SC_Computer_top UUT (
             .clk(clk),
             .Reset(Reset),
             .ALU0(ALU0),
             .SO(SO));

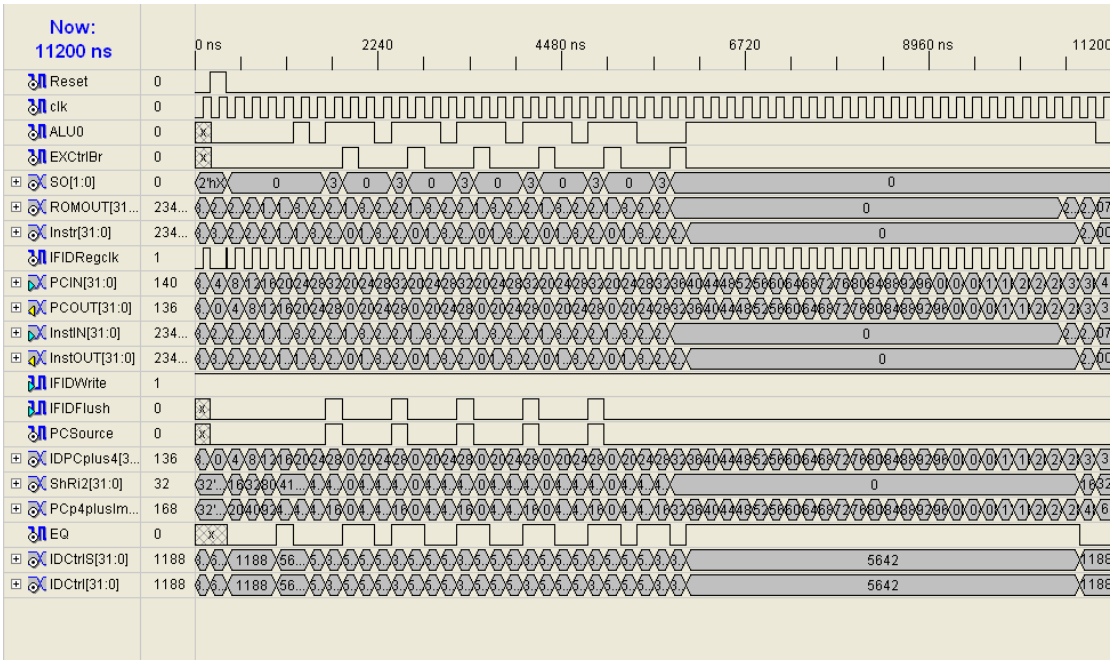
       integer TX_FILE = 0;
       integer TX_ERROR = 0;

       initial begin    // Open the       Results file...
             TX_FILE = $fopen("results.txt");
             #11200 // Final time:    11200 ns
             if (TX_ERROR == 0) begin
```

```
            $display("No errors or warnings.");
            $fdisplay(TX_FILE, "No errors or warnings.");
        end else begin
            $display("%d errors found in simulation.", TX_ERROR);
            $fdisplay(TX_FILE, "%d errors found in simulation.", TX_ERROR);
        end
        $fclose(TX_FILE);
        $stop;
    end

    initial begin
        // -------------  Current Time:  185ns
        #185;
          Reset = 1'b1;
        // ---------------------------------------
        // -------------  Current Time:  385ns
        #170;
          Reset = 1'b0;
        // ---------------------------------------
    end
endmodule
```

## 2.4 Behavioral simulation waveforms of the top-level design




| Time | Operation |
|---|---|
| 185 | Control unit initialization. |
| 185 | Reading data: rom32[00000000] => 8c020004 |
| 400 | Reading data: rom32[00000004] => 8c030008 |
| 400 | Reg_File[ 0] => 0 (Port 1) |
| 400 | Reg_File[ 2] => x (Port 2) |
| 600 | Reading data: rom32[00000008] => 8c040014 |
| 600 | Reg_File[ 0] => 0 (Port 1) |
| 600 | Reg_File[ 3] => x (Port 2) |
| 800 | Reading data: rom32[0000000c] => 00002820 |
| 800 | Reg_File[ 0] => 0 (Port 1) |
| 800 | Reg_File[ 4] => x (Port 2) |

```
800     Reading data: Mem[00000004] => 00000001
1000    Reading data: Mem[00000008] => 00000002
1000    Reg_File[ 0] =>         0 (Port 1)
1000    Reg_File[ 0] =>         0 (Port 2)
1000    Reading data: rom32[00000010] => 00a22820
1100    Reg_File[ 2] <=         1 (Write)
1100    Reg_File[ 0] =>         0 (Port 1)
1100    Reg_File[ 0] =>         0 (Port 2)
1200    Reading data: Mem[00000014] => 00000005
1200    Reg_File[ 5] =>         x (Port 1)
1200    Reg_File[ 2] =>         1 (Port 2)
1200    Reading data: rom32[00000014] => 0085302a
1300    Reg_File[ 3] <=         2 (Write)
1300    Reg_File[ 5] =>         x (Port 1)
1300    Reg_File[ 2] =>         1 (Port 2)
1400    Reg_File[ 4] =>         x (Port 1)
1400    Reg_File[ 5] =>         x (Port 2)
1400    Reading data: rom32[00000018] => 10c0fffd
1500    Reg_File[ 4] <=         5 (Write)
1500    Reg_File[ 4] =>         5 (Port 1)
1500    Reg_File[ 5] =>         x (Port 2)
1600    Reg_File[ 6] =>         x (Port 1)
1600    Reg_File[ 0] =>         0 (Port 2)
1600    Reading data: rom32[0000001c] => ac050000
1700    Reg_File[ 5] <=         0 (Write)
1700    Reg_File[ 6] =>         x (Port 1)
1700    Reg_File[ 0] =>         0 (Port 2)
1800    Reading data: rom32[00000010] => 00a22820
1800    Reg_File[ 0] =>         0 (Port 1)
1800    Reg_File[ 0] =>         0 (Port 2)
1900    Reg_File[ 5] <=         1 (Write)
1900    Reg_File[ 0] =>         0 (Port 1)
1900    Reg_File[ 0] =>         0 (Port 2)
2000    Reg_File[ 5] =>         1 (Port 1)
2000    Reg_File[ 2] =>         1 (Port 2)
2000    Reading data: rom32[00000014] => 0085302a
2100    Reg_File[ 6] <=         0 (Write)
2100    Reg_File[ 5] =>         1 (Port 1)
2100    Reg_File[ 2] =>         1 (Port 2)
2200    Reg_File[ 4] =>         5 (Port 1)
2200    Reg_File[ 5] =>         1 (Port 2)
2200    Reading data: rom32[00000018] => 10c0fffd
2400    Reading data: rom32[0000001c] => ac050000
2400    Reg_File[ 6] =>         0 (Port 1)
2400    Reg_File[ 0] =>         0 (Port 2)
2600    Reg_File[ 0] =>         0 (Port 1)
2600    Reg_File[ 0] =>         0 (Port 2)
2600    Reading data: rom32[00000010] => 00a22820
2700    Reg_File[ 5] <=         2 (Write)
2700    Reg_File[ 0] =>         0 (Port 1)
2700    Reg_File[ 0] =>         0 (Port 2)
2800    Reg_File[ 5] =>         2 (Port 1)
2800    Reg_File[ 2] =>         1 (Port 2)
2800    Reading data: rom32[00000014] => 0085302a
```

```
2900    Reg_File[ 6] <=         0 (Write)
3000    Reg_File[ 4] =>         5 (Port 1)
3000    Reg_File[ 5] =>         2 (Port 2)
3000    Reading data: rom32[00000018] => 10c0fffd
3200    Reading data: rom32[0000001c] => ac050000
3200    Reg_File[ 6] =>         0 (Port 1)
3200    Reg_File[ 0] =>         0 (Port 2)
3400    Reg_File[ 0] =>         0 (Port 1)
3400    Reg_File[ 0] =>         0 (Port 2)
3400    Reading data: rom32[00000010] => 00a22820
3500    Reg_File[ 5] <=         3 (Write)
3500    Reg_File[ 0] =>         0 (Port 1)
3500    Reg_File[ 0] =>         0 (Port 2)
3600    Reg_File[ 5] =>         3 (Port 1)
3600    Reg_File[ 2] =>         1 (Port 2)
3600    Reading data: rom32[00000014] => 0085302a
3700    Reg_File[ 6] <=         0 (Write)
3800    Reg_File[ 4] =>         5 (Port 1)
3800    Reg_File[ 5] =>         3 (Port 2)
3800    Reading data: rom32[00000018] => 10c0fffd
4000    Reading data: rom32[0000001c] => ac050000
4000    Reg_File[ 6] =>         0 (Port 1)
4000    Reg_File[ 0] =>         0 (Port 2)
4200    Reg_File[ 0] =>         0 (Port 1)
4200    Reg_File[ 0] =>         0 (Port 2)
4200    Reading data: rom32[00000010] => 00a22820
4300    Reg_File[ 5] <=         4 (Write)
4300    Reg_File[ 0] =>         0 (Port 1)
4300    Reg_File[ 0] =>         0 (Port 2)
4400    Reg_File[ 5] =>         4 (Port 1)
4400    Reg_File[ 2] =>         1 (Port 2)
4400    Reading data: rom32[00000014] => 0085302a
4500    Reg_File[ 6] <=         0 (Write)
4600    Reg_File[ 4] =>         5 (Port 1)
4600    Reg_File[ 5] =>         4 (Port 2)
4600    Reading data: rom32[00000018] => 10c0fffd
4800    Reading data: rom32[0000001c] => ac050000
4800    Reg_File[ 6] =>         0 (Port 1)
4800    Reg_File[ 0] =>         0 (Port 2)
5000    Reg_File[ 0] =>         0 (Port 1)
5000    Reg_File[ 0] =>         0 (Port 2)
5000    Reading data: rom32[00000010] => 00a22820
5100    Reg_File[ 5] <=         5 (Write)
5100    Reg_File[ 0] =>         0 (Port 1)
5100    Reg_File[ 0] =>         0 (Port 2)
5200    Reg_File[ 5] =>         5 (Port 1)
5200    Reg_File[ 2] =>         1 (Port 2)
5200    Reading data: rom32[00000014] => 0085302a
5300    Reg_File[ 6] <=         0 (Write)
5400    Reg_File[ 4] =>         5 (Port 1)
5400    Reg_File[ 5] =>         5 (Port 2)
5400    Reading data: rom32[00000018] => 10c0fffd
5600    Reading data: rom32[0000001c] => ac050000
5600    Reg_File[ 6] =>         0 (Port 1)
```

```
5600        Reg_File[ 0] =>             0 (Port 2)
5800        Reg_File[ 0] =>             0 (Port 1)
5800        Reg_File[ 5] =>             5 (Port 2)
5800        Reading data: rom32[00000020] => 00000000
5900        Reg_File[ 5] <=             6 (Write)
5900        Reg_File[ 0] =>             0 (Port 1)
5900        Reg_File[ 5] =>             6 (Port 2)
6000        Reg_File[ 0] =>             0 (Port 1)
6000        Reg_File[ 0] =>             0 (Port 2)
6000        Reading data: rom32[00000024] => 00000000
6100        Reg_File[ 6] <=             1 (Write)
6100        Reg_File[ 0] =>             0 (Port 1)
6100        Reg_File[ 0] =>             0 (Port 2)
6200        Reg_File[ 0] =>             0 (Port 1)
6200        Reg_File[ 0] =>             0 (Port 2)
6200        Reading data: rom32[00000028] => 00000000
6400        Writing data: Mem[00000000] <= 00000006
```

## 2.5 Synthesis report using Xilinx Spartan-3 XC3S400 as the target device.

```
Release    - xst I.31
Copyright (c) 1995-2006 Xilinx, Inc.    All rights reserved.
--> Parameter TMPDIR set to ./xst/projnav.tmp
CPU : 0.00 / 0.23 s | Elapsed : 0.00 / 0.00 s

--> Parameter xsthdpdir set to ./xst
CPU : 0.00 / 0.23 s | Elapsed : 0.00 / 0.00 s

--> Reading design: Pipelined_SC_Computer_top.prj

TABLE OF CONTENTS
   1) Synthesis Options Summary
   2) HDL Compilation
   3) Design Hierarchy Analysis
   4) HDL Analysis
   5) HDL Synthesis
        5.1) HDL Synthesis Report
   6) Advanced HDL Synthesis
        6.1) Advanced HDL Synthesis Report
   7) Low Level Synthesis
   8) Partition Report
   9) Final Report
        9.1) Device utilization summary
        9.2) TIMING REPORT


=========================================================================
*                            Synthesis Options Summary                  *
=========================================================================
---- Source Parameters
Input File Name                    : "Pipelined_SC_Computer_top.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "Pipelined_SC_Computer_top"
Output Format                      : NGC
Target Device                      : xc3s400-5-ft256

---- Source Options
Top Module Name                    : Pipelined_SC_Computer_top
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
FSM Style                          : lut
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : YES
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : YES
Resource Sharing                   : YES
Multiplier Style                   : auto
Automatic Register Balancing       : No
```

```
---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 500
Add Generic Clock Buffer(BUFG)     : 8
Register Duplication               : YES
Slice Packing                      : YES
Pack IO Registers into IOBs        : auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Keep Hierarchy                     : NO
RTL Output                         : Yes
Global Optimization                : AllClockNets
Write Timing Constraints           : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : maintain
Slice Utilization Ratio            : 100
Slice Utilization Ratio Delta      : 5

---- Other Options
lso                                : Pipelined_SC_Computer_top.lso
Read Cores                         : YES
cross_clock_analysis               : NO
verilog2001                        : YES
safe_implementation                : No
Optimize Instantiated Primitives   : NO
use_clock_enable                   : Yes
use_sync_set                       : Yes
use_sync_reset                     : Yes

=========================================================================


=========================================================================
*                            HDL Compilation                            *
=========================================================================
Compiling verilog file "Zero.v" in library work
Compiling verilog file "SignExtend.v" in library work
Module <Zero> compiled
Compiling verilog file "ShiftLeft2Bit.v" in library work
Module <SignExtend> compiled
Compiling verilog file "Register_File.v" in library work
Module <ShiftLeft2Bit> compiled
Compiling verilog file "ROM32Bit32Byte.v" in library work
Module <Register_File> compiled
Compiling verilog file "PCReg32Bit.v" in library work
Module <ROM32Bit32Byte> compiled
Compiling verilog file "Memory32Bit128Byte.v" in library work
Module <PCReg32Bit> compiled
Compiling verilog file "MUX5Bit2Ch.v" in library work
Module <Memory32Bit128Byte> compiled
Compiling verilog file "MUX32Bit3Ch.v" in library work
Module <MUX5Bit2Ch> compiled
Compiling verilog file "MUX32Bit2Ch.v" in library work
Module <MUX32Bit3Ch> compiled
Compiling verilog file "MEMWBReg.v" in library work
Module <MUX32Bit2Ch> compiled
Compiling verilog file "IFIDReg.v" in library work
Module <MEMWBReg> compiled
Compiling verilog file "IDEXReg.v" in library work
Module <IFIDReg> compiled
Compiling verilog file "Hazard.v" in library work
Module <IDEXReg> compiled
Compiling verilog file "Four.v" in library work
Module <Hazard> compiled
Compiling verilog file "Forwarding.v" in library work
Module <Four> compiled
Compiling verilog file "EqTest.v" in library work
Module <Forwarding> compiled
Compiling verilog file "EXMEMReg.v" in library work
Module <EqTest> compiled
Compiling verilog file "Control.v" in library work
Module <EXMEMReg> compiled
Compiling verilog file "Adder32Bit.v" in library work
Module <Control> compiled
Compiling verilog file "ALU32Bit.v" in library work
Module <Adder32Bit> compiled
Compiling verilog file "Pipelined_SC_Computer_top.vf" in library work
Module <ALU32Bit> compiled
Module <Pipelined_SC_Computer_top> compiled
No errors in compilation
Analysis of file <"Pipelined_SC_Computer_top.prj"> succeeded.


=========================================================================
*                     Design Hierarchy Analysis                         *
=========================================================================
Analyzing hierarchy for module <Pipelined_SC_Computer_top> in library <work>.
```

```
Analyzing hierarchy for module <Adder32Bit> in library <work>.

Analyzing hierarchy for module <ALU32Bit> in library <work>.

Analyzing hierarchy for module <Control> in library <work> with parameters.
        ALU_add = "010"
        ALU_and = "000"
        ALU_or = "001"
        ALU_slt = "111"
        ALU_sub = "110"
        BEQ = "000100"
        Funct_add = "100000"
        Funct_and = "100100"
        Funct_or = "100101"
        Funct_slt = "101010"
        Funct_sub = "100010"
        Init = "111111"
        LW = "100011"
        R_FORMAT = "000000"
        SW = "101011"

Analyzing hierarchy for module <Memory32Bit128Byte> in library <work> with parameters.
        BASE_ADDRESS = "00000000000000000000000000"

Analyzing hierarchy for module <EqTest> in library <work>.

Analyzing hierarchy for module <EXMEMReg> in library <work>.

Analyzing hierarchy for module <Forwarding> in library <work>.

Analyzing hierarchy for module <Zero> in library <work>.

Analyzing hierarchy for module <Hazard> in library <work>.

Analyzing hierarchy for module <IDEXReg> in library <work>.

Analyzing hierarchy for module <IFIDReg> in library <work>.

Analyzing hierarchy for module <ROM32Bit32Byte> in library <work>.

Analyzing hierarchy for module <MEMWBReg> in library <work>.

Analyzing hierarchy for module <MUX32Bit3Ch> in library <work> with parameters.
        bitwidth = "00000000000000000000000000100000"

Analyzing hierarchy for module <MUX32Bit2Ch> in library <work> with parameters.
        bitwidth = "00000000000000000000000000100000"

Analyzing hierarchy for module <MUX5Bit2Ch> in library <work> with parameters.
        bitwidth = "00000000000000000000000000000101"

Analyzing hierarchy for module <PCReg32Bit> in library <work>.

Analyzing hierarchy for module <Four> in library <work>.

Analyzing hierarchy for module <Register_File> in library <work>.

Analyzing hierarchy for module <ShiftLeft2Bit> in library <work>.

Analyzing hierarchy for module <SignExtend> in library <work>.

Building hierarchy successfully finished.

=========================================================================
*                                HDL Analysis                           *
=========================================================================
Analyzing top module <Pipelined_SC_Computer_top>.
Module <Pipelined_SC_Computer_top> is correct for synthesis.

Analyzing module <Adder32Bit> in library <work>.
Module <Adder32Bit> is correct for synthesis.

Analyzing module <ALU32Bit> in library <work>.
Module <ALU32Bit> is correct for synthesis.

Analyzing module <Control> in library <work>.
        R_FORMAT = 6'b000000
        LW = 6'b100011
        SW = 6'b101011
        BEQ = 6'b000100
        Init = 6'b111111
        Funct_add = 6'b100000
        Funct_sub = 6'b100010
        Funct_and = 6'b100100
        Funct_or = 6'b100101
        Funct_slt = 6'b101010
        ALU_add = 3'b010
        ALU_sub = 3'b110
        ALU_and = 3'b000
        ALU_or = 3'b001
        ALU_slt = 3'b111
```

```
WARNING:Xst:2321 - "Control.v" line 111: Parameter 1 ($time) is not supported in call of system task $display.
"Control.v" line 111: $display :    Control unit initialization.
WARNING:Xst:2321 - "Control.v" line 125: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Control.v" line 125: Parameter 3 is not constant in call of system task $display.
"Control.v" line 125: $display :    Control unit unimplemented OpCode %d
Module <Control> is correct for synthesis.

Analyzing module <Memory32Bit128Byte> in library <work>.
        BASE_ADDRESS = 25'b0000000000000000000000000
WARNING:Xst:2319 - "Memory32Bit128Byte.v" line 77: Signal Memory_Array in initial block is partially initialized. The initialization will
be ignored.
WARNING:Xst:2321 - "Memory32Bit128Byte.v" line 47: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 47: Parameter 3 is not constant in call of system task $display.
"Memory32Bit128Byte.v" line 47: $display :    rom32 error: unaligned address %h
WARNING:Xst:2321 - "Memory32Bit128Byte.v" line 53: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 53: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 53: Parameter 4 is not constant in call of system task $display.
"Memory32Bit128Byte.v" line 53: $display :    Reading data: Mem[%h] => %h
WARNING:Xst:905 - "Memory32Bit128Byte.v" line 42: The signals <Memory_Array> are missing in the sensitivity list of always block.
WARNING:Xst:2321 - "Memory32Bit128Byte.v" line 67: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 67: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "Memory32Bit128Byte.v" line 67: Parameter 4 is not constant in call of system task $display.
"Memory32Bit128Byte.v" line 67: $display :    Writing data: Mem[%h] <= %h
Module <Memory32Bit128Byte> is correct for synthesis.

Analyzing module <EqTest> in library <work>.
Module <EqTest> is correct for synthesis.

Analyzing module <EXMEMReg> in library <work>.
Module <EXMEMReg> is correct for synthesis.

Analyzing module <Forwarding> in library <work>.
Module <Forwarding> is correct for synthesis.

Analyzing module <Zero> in library <work>.
Module <Zero> is correct for synthesis.

Analyzing module <Hazard> in library <work>.
Module <Hazard> is correct for synthesis.

Analyzing module <IDEXReg> in library <work>.
Module <IDEXReg> is correct for synthesis.

Analyzing module <IFIDReg> in library <work>.
Module <IFIDReg> is correct for synthesis.

Analyzing module <ROM32Bit32Byte> in library <work>.
WARNING:Xst:2321 - "ROM32Bit32Byte.v" line 30: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "ROM32Bit32Byte.v" line 30: Parameter 3 is not constant in call of system task $display.
"ROM32Bit32Byte.v" line 30: $display :    rom32 error: unaligned Address %d
WARNING:Xst:2321 - "ROM32Bit32Byte.v" line 46: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "ROM32Bit32Byte.v" line 46: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "ROM32Bit32Byte.v" line 46: Parameter 4 is not constant in call of system task $display.
"ROM32Bit32Byte.v" line 46: $display :    Reading data: rom32[%h] => %h
Module <ROM32Bit32Byte> is correct for synthesis.

Analyzing module <MEMWBReg> in library <work>.
Module <MEMWBReg> is correct for synthesis.

Analyzing module <MUX32Bit3Ch> in library <work>.
        bitwidth = 32'sb00000000000000000000000000100000
Module <MUX32Bit3Ch> is correct for synthesis.

Analyzing module <MUX32Bit2Ch> in library <work>.
        bitwidth = 32'sb00000000000000000000000000100000
Module <MUX32Bit2Ch> is correct for synthesis.

Analyzing module <MUX5Bit2Ch> in library <work>.
        bitwidth = 32'sb00000000000000000000000000000101
Module <MUX5Bit2Ch> is correct for synthesis.

Analyzing module <PCReg32Bit> in library <work>.
Module <PCReg32Bit> is correct for synthesis.

Analyzing module <Four> in library <work>.
Module <Four> is correct for synthesis.

Analyzing module <Register_File> in library <work>.
WARNING:Xst:2321 - "Register_File.v" line 161: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Register_File.v" line 161: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "Register_File.v" line 161: Parameter 4 is not constant in call of system task $display.
"Register_File.v" line 161: $display :    Reg_File[%d] <= %d (Write)
WARNING:Xst:2321 - "Register_File.v" line 174: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Register_File.v" line 174: Parameter 3 is not constant in call of system task $display.
"Register_File.v" line 174: $display :    Reg_File[%d] =>                0 (Port 1)
WARNING:Xst:2321 - "Register_File.v" line 179: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Register_File.v" line 179: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "Register_File.v" line 179: Parameter 4 is not constant in call of system task $display.
"Register_File.v" line 179: $display :    Reg_File[%d] => %d (Port 1)
WARNING:Xst:2321 - "Register_File.v" line 184: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Register_File.v" line 184: Parameter 3 is not constant in call of system task $display.
"Register_File.v" line 184: $display :    Reg_File[%d] =>                0 (Port 2)
```

```
WARNING:Xst:2321 - "Register_File.v" line 189: Parameter 1 ($time) is not supported in call of system task $display.
WARNING:Xst:2323 - "Register_File.v" line 189: Parameter 3 is not constant in call of system task $display.
WARNING:Xst:2323 - "Register_File.v" line 189: Parameter 4 is not constant in call of system task $display.
"Register_File.v" line 189: $display :    Reg_File[%d] => %d (Port 2)
WARNING:Xst:905 - "Register_File.v" line 166: The signals <File_Array> are missing in the sensitivity list of always block.
Module <Register_File> is correct for synthesis.

Analyzing module <ShiftLeft2Bit> in library <work>.
Module <ShiftLeft2Bit> is correct for synthesis.

Analyzing module <SignExtend> in library <work>.
Module <SignExtend> is correct for synthesis.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <Adder32Bit>.
    Related source file is "Adder32Bit.v".
    Found 32-bit adder for signal <Sum>.
    Summary:
      inferred     1 Adder/Subtractor(s).
Unit <Adder32Bit> synthesized.


Synthesizing Unit <ALU32Bit>.
    Related source file is "ALU32Bit.v".
    Found 32-bit addsub for signal <$addsub0000>.
    Found 32-bit comparator less for signal <$cmp_lt0000> created at line 37.
    Summary:
      inferred     1 Adder/Subtractor(s).
      inferred     1 Comparator(s).
Unit <ALU32Bit> synthesized.


Synthesizing Unit <Control>.
    Related source file is "Control.v".
WARNING:Xst:647 - Input <EXCtrlBr> is never used.
WARNING:Xst:647 - Input <EQ> is never used.
    Found 4x1-bit ROM for signal <$mux0000>.
    Found 4x1-bit ROM for signal <$mux0001>.
    Found 4x1-bit ROM for signal <$mux0002>.
    Found 3-bit 4-to-1 multiplexer for signal <Ctrl<6:4>>.
    Summary:
      inferred     3 ROM(s).
      inferred     3 Multiplexer(s).
Unit <Control> synthesized.


Synthesizing Unit <Memory32Bit128Byte>.
    Related source file is "Memory32Bit128Byte.v".
WARNING:Xst:1872 - Variable <i> is used but never assigned.
    Found 32x32-bit single-port distributed RAM for signal <Memory_Array>.
    ----------------------------------------------------------------------
    | ram_style                  | Auto                                  |                 |
    ----------------------------------------------------------------------
    | Port A                                                             |                 |
    |         aspect ratio       | 32-word x 32-bit                      |                 |
    |         clkA               | connected to signal <clk>             | fall        |
    |         weA                | connected to internal node            | high        |
    |         addrA              | connected to signal <Memory_Offset>   |                 |
    |         diA                | connected to signal <DataIN>          |                 |
    |         doA                | connected to internal node            |                 |
    ----------------------------------------------------------------------
INFO:Xst:1442 - HDL ADVISOR - The RAM contents appears to be read asynchronously. A synchronous read would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.
    Found 32-bit 4-to-1 multiplexer for signal <DataOUT>.
    Summary:
      inferred     1 RAM(s).
      inferred    32 Multiplexer(s).
Unit <Memory32Bit128Byte> synthesized.


Synthesizing Unit <EqTest>.
    Related source file is "EqTest.v".
    Found 32-bit comparator equal for signal <$cmp_eq0000> created at line 29.
    Summary:
      inferred     1 Comparator(s).
Unit <EqTest> synthesized.


Synthesizing Unit <EXMEMReg>.
    Related source file is "EXMEMReg.v".
    Found 2-bit register for signal <CtrlMOUT>.
    Found 32-bit register for signal <RtDataOUT>.
    Found 32-bit register for signal <ALUOUT>.
    Found 2-bit register for signal <CtrlWBOUT>.
    Found 5-bit register for signal <MUXRtRdOUT>.
```

```
    Summary:
      inferred    73 D-type flip-flop(s).
Unit <EXMEMReg> synthesized.


Synthesizing Unit <Forwarding>.
    Related source file is "Forwarding.v".
    Found 5-bit comparator equal for signal <$cmp_eq0000> created at line 43.
    Found 5-bit comparator equal for signal <$cmp_eq0001> created at line 48.
    Found 5-bit comparator equal for signal <$cmp_eq0002> created at line 53.
    Found 5-bit comparator equal for signal <$cmp_eq0003> created at line 58.
    Found 5-bit comparator not equal for signal <$cmp_ne0002> created at line 53.
    Found 5-bit comparator not equal for signal <$cmp_ne0003> created at line 58.
    Summary:
      inferred     6 Comparator(s).
Unit <Forwarding> synthesized.


Synthesizing Unit <Zero>.
    Related source file is "Zero.v".
Unit <Zero> synthesized.


Synthesizing Unit <Hazard>.
    Related source file is "Hazard.v".
    Found 4x3-bit ROM for signal <$rom0000>.
    Found 5-bit comparator equal for signal <$cmp_eq0000> created at line 44.
    Found 5-bit comparator equal for signal <$cmp_eq0001> created at line 44.
    Summary:
      inferred     1 ROM(s).
      inferred     2 Comparator(s).
Unit <Hazard> synthesized.


Synthesizing Unit <IDEXReg>.
    Related source file is "IDEXReg.v".
    Found 5-bit register for signal <IFIDRsOUT>.
    Found 1-bit register for signal <CtrlBrOUT>.
    Found 32-bit register for signal <RFOUT1OUT>.
    Found 32-bit register for signal <SignExOUT>.
    Found 2-bit register for signal <CtrlMOUT>.
    Found 5-bit register for signal <IFIDRdOUT>.
    Found 5-bit register for signal <CtrlEXOUT>.
    Found 5-bit register for signal <IFIDRtOUT>.
    Found 2-bit register for signal <CtrlWBOUT>.
    Found 32-bit register for signal <RFOUT2OUT>.
    Summary:
      inferred 121 D-type flip-flop(s).
Unit <IDEXReg> synthesized.


Synthesizing Unit <IFIDReg>.
    Related source file is "IFIDReg.v".
    Found 32-bit register for signal <PCOUT>.
    Found 32-bit register for signal <InstOUT>.
    Summary:
      inferred    64 D-type flip-flop(s).
Unit <IFIDReg> synthesized.


Synthesizing Unit <ROM32Bit32Byte>.
    Related source file is "ROM32Bit32Byte.v".
Unit <ROM32Bit32Byte> synthesized.


Synthesizing Unit <MEMWBReg>.
    Related source file is "MEMWBReg.v".
    Found 5-bit register for signal <RtRdOUT>.
    Found 32-bit register for signal <ALUOUT>.
    Found 2-bit register for signal <CtrlWBOUT>.
    Found 32-bit register for signal <MemOUT>.
    Summary:
      inferred    71 D-type flip-flop(s).
Unit <MEMWBReg> synthesized.


Synthesizing Unit <MUX32Bit3Ch>.
    Related source file is "MUX32Bit3Ch.v".
    Found 32-bit 3-to-1 multiplexer for signal <DataOUT>.
    Summary:
      inferred    32 Multiplexer(s).
Unit <MUX32Bit3Ch> synthesized.


Synthesizing Unit <MUX32Bit2Ch>.
    Related source file is "MUX32Bit2Ch.v".
Unit <MUX32Bit2Ch> synthesized.


Synthesizing Unit <MUX5Bit2Ch>.
    Related source file is "MUX5Bit2Ch.v".
Unit <MUX5Bit2Ch> synthesized.
```

```
Synthesizing Unit <PCReg32Bit>.
    Related source file is "PCReg32Bit.v".
    Found 32-bit register for signal <PCOUT>.
    Summary:
      inferred    32 D-type flip-flop(s).
Unit <PCReg32Bit> synthesized.


Synthesizing Unit <Four>.
    Related source file is "Four.v".
Unit <Four> synthesized.


Synthesizing Unit <Register_File>.
    Related source file is "Register_File.v".
WARNING:Xst:647 - Input <Reset> is never used.
    Found 32x32-bit dual-port distributed RAM for signal <File_Array>.
    -----------------------------------------------------------------------
    | ram_style                  | Auto                                   |               |
    -----------------------------------------------------------------------
    | Port A                                                                                |
    |         aspect ratio       | 32-word x 32-bit                       |               |
    |         clkA               | connected to signal <clk>              | rise          |
    |         weA                | connected to internal node             | high          |
    |         addrA              | connected to signal <WriteAddr>        |               |
    |         diA                | connected to signal <DataIN>           |               |
    -----------------------------------------------------------------------
    | Port B                                                                                |
    |         aspect ratio       | 32-word x 32-bit                       |               |
    |         addrB              | connected to signal <ReadAddr1>        |               |
    |         doB                | connected to internal node             |               |
    -----------------------------------------------------------------------
INFO:Xst:1442 - HDL ADVISOR - The RAM contents appears to be read asynchronously. A synchronous read would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.
    Found 32x32-bit dual-port distributed RAM for signal <File_Array>.
    -----------------------------------------------------------------------
    | ram_style                  | Auto                                   |               |
    -----------------------------------------------------------------------
    | Port A                                                                                |
    |         aspect ratio       | 32-word x 32-bit                       |               |
    |         clkA               | connected to signal <clk>              | rise          |
    |         weA                | connected to internal node             | high          |
    |         addrA              | connected to signal <WriteAddr>        |               |
    |         diA                | connected to signal <DataIN>           |               |
    -----------------------------------------------------------------------
    | Port B                                                                                |
    |         aspect ratio       | 32-word x 32-bit                       |               |
    |         addrB              | connected to signal <ReadAddr2>        |               |
    |         doB                | connected to internal node             |               |
    -----------------------------------------------------------------------
INFO:Xst:1442 - HDL ADVISOR - The RAM contents appears to be read asynchronously. A synchronous read would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.
    Summary:
      inferred     2 RAM(s).
Unit <Register_File> synthesized.


Synthesizing Unit <ShiftLeft2Bit>.
    Related source file is "ShiftLeft2Bit.v".
Unit <ShiftLeft2Bit> synthesized.


Synthesizing Unit <SignExtend>.
    Related source file is "SignExtend.v".
Unit <SignExtend> synthesized.


Synthesizing Unit <Pipelined_SC_Computer_top>.
    Related source file is "Pipelined_SC_Computer_top.vf".
WARNING:Xst:646 - Signal <IDCtrlS<31:11>> is assigned but never used.
WARNING:Xst:646 - Signal <IDCtrlS<1>> is assigned but never used.
Unit <Pipelined_SC_Computer_top> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduced device utilization. For improved clock frequency you may try to disable resource sharing.

=========================================================================
HDL Synthesis Report

Macro Statistics
# RAMs                                                  : 3
  32x32-bit dual-port distributed RAM                   : 2
  32x32-bit single-port distributed RAM                 : 1
# ROMs                                                  : 4
  4x1-bit ROM                                           : 3
  4x3-bit ROM                                           : 1
# Adders/Subtractors                                    : 3
  32-bit adder                                          : 2
```

```
  32-bit addsub                                         : 1
# Registers                                            : 53
  1-bit register                                        : 33
  2-bit register                                        : 5
  32-bit register                                       : 9
  5-bit register                                        : 6
# Comparators                                          : 10
  32-bit comparator equal                               : 1
  32-bit comparator less                                : 1
  5-bit comparator equal                                : 6
  5-bit comparator not equal                            : 2
# Multiplexers                                         : 6
  1-bit 4-to-1 multiplexer                              : 3
  32-bit 3-to-1 multiplexer                             : 2
  32-bit 4-to-1 multiplexer                             : 1

=========================================================================

=========================================================================
*                            Advanced HDL Synthesis                     *
=========================================================================

Loading device for application Rf_Device from file '3s400.nph' in environment F:\Xilinx.
WARNING:Xst:1291 - FF/Latch <CtrlBrOUT> is unconnected in block <IDEX>.
WARNING:Xst:1290 - Hierarchical block <F0> is unconnected in block <Pipelined_SC_Computer_top>.
    It will be removed from the design.

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 3
  32x32-bit dual-port distributed RAM                   : 2
  32x32-bit single-port distributed RAM                 : 1
# ROMs                                                 : 4
  4x1-bit ROM                                           : 3
  4x3-bit ROM                                           : 1
# Adders/Subtractors                                   : 3
  32-bit adder                                          : 2
  32-bit addsub                                         : 1
# Registers                                            : 361
  Flip-Flops                                            : 361
# Comparators                                          : 10
  32-bit comparator equal                               : 1
  32-bit comparator less                                : 1
  5-bit comparator equal                                : 6
  5-bit comparator not equal                            : 2
# Multiplexers                                         : 6
  1-bit 4-to-1 multiplexer                              : 3
  32-bit 3-to-1 multiplexer                             : 2
  32-bit 4-to-1 multiplexer                             : 1

=========================================================================

=========================================================================
*                            Low Level Synthesis                        *
=========================================================================
WARNING:Xst:1988 - Unit <Forwarding>: instances <Mcompar__cmp_eq0000>, <Mcompar__cmp_ne0002> of unit <LPM_COMPARE_3>
and unit <LPM_COMPARE_4> are dual, second instance is removed
WARNING:Xst:1988 - Unit <Forwarding>: instances <Mcompar__cmp_eq0001>, <Mcompar__cmp_ne0003> of unit <LPM_COMPARE_3>
and unit <LPM_COMPARE_4> are dual, second instance is removed
INFO:Xst:2261 - The FF/Latch <SignExOUT_12> in Unit <IDEXReg> is equivalent to the following FF/Latch, which will be removed :
<IFIDRdOUT_1>
INFO:Xst:2261 - The FF/Latch <SignExOUT_11> in Unit <IDEXReg> is equivalent to the following FF/Latch, which will be removed :
<IFIDRdOUT_0>
INFO:Xst:2261 - The FF/Latch <SignExOUT_14> in Unit <IDEXReg> is equivalent to the following FF/Latch, which will be removed :
<IFIDRdOUT_3>
INFO:Xst:2261 - The FF/Latch <SignExOUT_13> in Unit <IDEXReg> is equivalent to the following FF/Latch, which will be removed :
<IFIDRdOUT_2>
INFO:Xst:2261 - The FF/Latch <SignExOUT_15> in Unit <IDEXReg> is equivalent to the following 17 FFs/Latches, which will be removed :
<SignExOUT_16> <SignExOUT_17> <SignExOUT_18> <SignExOUT_19> <SignExOUT_20> <SignExOUT_21> <SignExOUT_22>
<SignExOUT_23> <SignExOUT_24> <SignExOUT_25> <SignExOUT_26> <SignExOUT_27> <SignExOUT_28> <SignExOUT_29>
<SignExOUT_30> <SignExOUT_31> <IFIDRdOUT_4>

Optimizing unit <Pipelined_SC_Computer_top> ...

Optimizing unit <Register_File> ...

Optimizing unit <ROM32Bit32Byte> ...

Optimizing unit <MUX32Bit2Ch> ...

Optimizing unit <PCReg32Bit> ...

Optimizing unit <EXMEMReg> ...

Optimizing unit <MEMWBReg> ...

Optimizing unit <IFIDReg> ...

Optimizing unit <IDEXReg> ...
```

Optimizing unit <ALU32Bit> ...

Optimizing unit <Control> ...

Mapping all equations...
WARNING:Xst:1710 - FF/Latch <IFID/InstOUT_25> (without init value) has a constant value of 0 in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1710 - FF/Latch <IFID/InstOUT_24> (without init value) has a constant value of 0 in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1710 - FF/Latch <IFID/InstOUT_20> (without init value) has a constant value of 0 in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1710 - FF/Latch <IFID/InstOUT_19> (without init value) has a constant value of 0 in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <IDEX/IFIDRsOUT_3> (without init value) has a constant value of 0 in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <IDEX/IFIDRsOUT_4> (without init value) has a constant value of 0 in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <IDEX/IFIDRtOUT_3> (without init value) has a constant value of 0 in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <IDEX/IFIDRtOUT_4> (without init value) has a constant value of 0 in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_7> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_8> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_9> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_10> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_11> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_12> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_13> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_14> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_15> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_16> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_17> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_18> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_19> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_20> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_21> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_22> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_23> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_24> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_25> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_26> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_27> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_28> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_29> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_30> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <PC/PCOUT_31> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_7> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_8> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_9> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_10> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_11> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_12> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_13> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_14> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_15> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_16> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_17> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_18> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_19> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_20> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_21> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_22> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_23> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_24> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_25> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_26> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_27> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_28> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_29> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_30> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IFID/PCOUT_31> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <IDEX/CtrlBrOUT> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem129> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem510> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem310> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem710> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1110> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem910> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem131> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem171> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem151> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem191> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem231> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem211> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem251> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem291> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem271> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem311> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem351> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem331> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem371> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem411> is unconnected in block <Pipelined_SC_Computer_top>.

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WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem391> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem431> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem471> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem451> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem491> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem531> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem511> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem551> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem591> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem571> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem611> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem631> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem651> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem691> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem671> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem711> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem751> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem731> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem771> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem811> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem791> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem831> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem871> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem851> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem891> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem931> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem911> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem951> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem991> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem971> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1011> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1051> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1031> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1071> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1111> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1091> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1131> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1171> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1151> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1191> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1231> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1211> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1251> is unconnected in block <Pipelined_SC_Computer_top>.
WARNING:Xst:1291 - FF/Latch <RegFile/inst_Mram_mem1271> is unconnected in block <Pipelined_SC_Computer_top>.
Building and optimizing final netlist ...
INFO:Xst:2261 - The FF/Latch <IFID/InstOUT_22> in Unit <Pipelined_SC_Computer_top> is equivalent to the following 8 FFs/Latches,
which will be removed : <IFID/InstOUT_15> <IFID/InstOUT_14> <IFID/InstOUT_10> <IFID/InstOUT_9> <IFID/InstOUT_8>
<IFID/InstOUT_7> <IFID/InstOUT_6> <IFID/InstOUT_0>
INFO:Xst:2261 - The FF/Latch <IFID/InstOUT_31> in Unit <Pipelined_SC_Computer_top> is equivalent to the following 2 FFs/Latches,
which will be removed : <IFID/InstOUT_27> <IFID/InstOUT_26>
INFO:Xst:2261 - The FF/Latch <IDEX/CtrlWBOUT_0> in Unit <Pipelined_SC_Computer_top> is equivalent to the following FF/Latch,
which will be removed : <IDEX/CtrlEXOUT_1>
INFO:Xst:2261 - The FF/Latch <IFID/InstOUT_13> in Unit <Pipelined_SC_Computer_top> is equivalent to the following FF/Latch, which
will be removed : <IFID/InstOUT_5>
INFO:Xst:2261 - The FF/Latch <IDEX/SignExOUT_0> in Unit <Pipelined_SC_Computer_top> is equivalent to the following 8 FFs/Latches,
which will be removed : <IDEX/SignExOUT_6> <IDEX/SignExOUT_7> <IDEX/SignExOUT_8> <IDEX/SignExOUT_9>
<IDEX/SignExOUT_10> <IDEX/SignExOUT_14> <IDEX/SignExOUT_15> <IDEX/IFIDRsOUT_1>
INFO:Xst:2261 - The FF/Latch <IDEX/SignExOUT_5> in Unit <Pipelined_SC_Computer_top> is equivalent to the following FF/Latch,
which will be removed : <IDEX/SignExOUT_13>
INFO:Xst:2261 - The FF/Latch <EXMEM/MUXRtRdOUT_3> in Unit <Pipelined_SC_Computer_top> is equivalent to the following FF/Latch,
which will be removed : <EXMEM/MUXRtRdOUT_4>
INFO:Xst:2261 - The FF/Latch <MEMWB/RtRdOUT_3> in Unit <Pipelined_SC_Computer_top> is equivalent to the following FF/Latch,
which will be removed : <MEMWB/RtRdOUT_4>
Found area constraint ratio of 100 (+ 5) on block Pipelined_SC_Computer_top, actual ratio is 11.
FlipFlop EXMEM/ALUOUT_2 has been replicated 2 time(s)
FlipFlop EXMEM/ALUOUT_3 has been replicated 1 time(s)
FlipFlop IDEX/CtrlEXOUT_0 has been replicated 2 time(s)
FlipFlop IDEX/CtrlEXOUT_2 has been replicated 1 time(s)
FlipFlop IDEX/CtrlEXOUT_3 has been replicated 1 time(s)
FlipFlop IDEX/SignExOUT_0 has been replicated 4 time(s)
FlipFlop MEMWB/CtrlWBOUT_0 has been replicated 1 time(s)
FlipFlop MEMWB/RtRdOUT_0 has been replicated 1 time(s)
FlipFlop MEMWB/RtRdOUT_1 has been replicated 1 time(s)
FlipFlop MEMWB/RtRdOUT_2 has been replicated 2 time(s)
FlipFlop MEMWB/RtRdOUT_3 has been replicated 2 time(s)

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                          : 276
  Flip-Flops                                         : 276

=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
```

```
---------------------------------

   No Partitions were found in this design.

---------------------------------

================================================================================
*                                Final Report                                  *
================================================================================
Final Results
RTL Top Level Output File Name         : Pipelined_SC_Computer_top.ngr
Top Level Output File Name             : Pipelined_SC_Computer_top
Output Format                          : NGC
Optimization Goal                      : Speed
Keep Hierarchy                         : NO

Design Statistics
# IOs                                  : 5

Cell Usage :
# BELS                                 : 786
#      AND2B1                          : 1
#      GND                             : 1
#      INV                             : 3
#      LUT1                            : 4
#      LUT2                            : 24
#      LUT2_D                          : 1
#      LUT2_L                          : 1
#      LUT3                            : 161
#      LUT3_D                          : 11
#      LUT3_L                          : 5
#      LUT4                            : 332
#      LUT4_D                          : 51
#      LUT4_L                          : 43
#      MUXCY                           : 86
#      MUXF5                           : 21
#      VCC                             : 1
#      XORCY                           : 40
# FlipFlops/Latches                    : 276
#      FD_1                            : 201
#      FDCE_1                          : 14
#      FDPE_1                          : 4
#      FDR_1                           : 11
#      FDRE_1                          : 13
#      FDRS_1                          : 1
#      FDS_1                           : 32
# RAMS                                 : 96
#      RAM16X1D                        : 64
#      RAM32X1S                        : 32
# Clock Buffers                        : 2
#      BUFG                            : 1
#      BUFGP                           : 1
# IO Buffers                           : 4
#      IBUF                            : 1
#      OBUF                            : 3
================================================================================

Device utilization summary:
---------------------------

Selected Device : 3s400ft256-5


 Number of Slices:                      438  out of   3584    12%
 Number of Slice Flip Flops:            276  out of   7168     3%
 Number of 4 input LUTs:                828  out of   7168    11%
    Number used as logic:               636
    Number used as RAMs:                192
 Number of IOs:                           5
 Number of bonded IOBs:                   5  out of    173     2%
 Number of GCLKs:                         2  out of      8    25%


================================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 348   |
IFIDRegclk1(ANDnot1:O)             | BUFG(*)(IFID/InstOUT_12)| 24    |
-----------------------------------+------------------------+-------+
(*) This 1 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.

Asynchronous Control Signals Information:
```

```
----------------------------------------
-----------------------------------+------------------------+-------+
Control Signal                     | Buffer(FF name)        | Load  |
-----------------------------------+------------------------+-------+
Reset                              | IBUF                   | 18    |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 16.234ns (Maximum Frequency: 61.600MHz)
   Minimum input arrival time before clock: 17.526ns
   Maximum output required time after clock: 20.465ns
   Maximum combinational path delay: 19.775ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 16.234ns (frequency: 61.600MHz)
  Total number of paths / destination ports: 970108 / 882
-------------------------------------------------------------------------
Delay:               16.234ns (Levels of Logic = 24)
  Source:            IDEX/IFIDRtOUT_1 (FF)
  Destination:       PC/PCOUT_0 (FF)
  Source Clock:      clk falling
  Destination Clock: clk falling

  Data Path: IDEX/IFIDRtOUT_1 to PC/PCOUT_0
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD_1:C->Q             5    0.626   1.078  IDEX/IFIDRtOUT_1 (IDEX/IFIDRtOUT_1)
     LUT4_D:I0->O          2    0.479   0.768  ForwardingUnit/_cmp_eq0001526 (ForwardingUnit/_cmp_eq00015_map343)
     LUT4:I3->O           10    0.479   1.134  ForwardingUnit/_xor0001_1 (ForwardingUnit/_xor00011)
     LUT3:I1->O           12    0.479   1.009  ForwardingUnit/ForwardA<1>1_SW0_1 (ForwardingUnit/ForwardA<1>1_SW0)
     LUT4:I2->O            3    0.479   0.941  ALUAddend<0> (ALUAddend<0>)
     LUT3:I1->O            1    0.479   0.000  ALU/Maddsub__addsub0000_lut<0> (ALU/N5)
     MUXCY:S->O            1    0.435   0.000  ALU/Maddsub__addsub0000_cy<0> (ALU/Maddsub__addsub0000_cy<0>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Maddsub__addsub0000_cy<1> (ALU/Maddsub__addsub0000_cy<1>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Maddsub__addsub0000_cy<2> (ALU/Maddsub__addsub0000_cy<2>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Maddsub__addsub0000_cy<3> (ALU/Maddsub__addsub0000_cy<3>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Maddsub__addsub0000_cy<4> (ALU/Maddsub__addsub0000_cy<4>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Maddsub__addsub0000_cy<5> (ALU/Maddsub__addsub0000_cy<5>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Maddsub__addsub0000_cy<6> (ALU/Maddsub__addsub0000_cy<6>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Maddsub__addsub0000_cy<7> (ALU/Maddsub__addsub0000_cy<7>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Maddsub__addsub0000_cy<8> (ALU/Maddsub__addsub0000_cy<8>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Maddsub__addsub0000_cy<9> (ALU/Maddsub__addsub0000_cy<9>)
     XORCY:CI->O           1    0.786   0.704  ALU/Maddsub__addsub0000_xor<10> (ALU/_addsub0000<10>)
     LUT4:I3->O            2    0.479   0.915  ALU/_old_Result_1<10> (EXALUOUT<10>)
     LUT4:I1->O            1    0.479   0.704  ALU/_old_Result_1<29>_SW1 (N1875)
     LUT4:I3->O            1    0.479   0.000  ALU/_cmp_eq0000_wg_lut<4> (N171)
     MUXCY:S->O            1    0.435   0.000  ALU/_cmp_eq0000_wg_cy<4> (ALU/_cmp_eq0000_wg_cy<4>)
     MUXCY:CI->O           1    0.056   0.000  ALU/_cmp_eq0000_wg_cy<5> (ALU/_cmp_eq0000_wg_cy<5>)
     MUXCY:CI->O           1    0.056   0.000  ALU/_cmp_eq0000_wg_cy<6> (ALU/_cmp_eq0000_wg_cy<6>)
     MUXCY:CI->O          20    0.265   1.336  ALU/_cmp_eq0000_wg_cy<7> (ALU/_cmp_eq0000_wg_cy<7>)
     LUT4:I3->O            1    0.479   0.000  MUX_8/DataOUT<5>1 (PCIN<5>)
     FDCE_1:D                   0.176          PC/PCOUT_5
    ----------------------------------------
    Total                      16.234ns (7.644ns logic, 8.590ns route)
                                        (47.1% logic, 52.9% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'IFIDRegclk1'
  Clock period: 9.219ns (frequency: 108.475MHz)
  Total number of paths / destination ports: 352 / 47
-------------------------------------------------------------------------
Delay:               9.219ns (Levels of Logic = 5)
  Source:            IFID/InstOUT_17 (FF)
  Destination:       IFID/InstOUT_29 (FF)
  Source Clock:      IFIDRegclk1 falling
  Destination Clock: IFIDRegclk1 falling

  Data Path: IFID/InstOUT_17 to IFID/InstOUT_29
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE_1:C->Q          66    0.626   1.911  IFID/InstOUT_17 (IFID/InstOUT_17)
     LUT4:I1->O            2    0.479   0.804  HarzardDUnit/_and000085 (HarzardDUnit/_and0000_map59)
     LUT3:I2->O            1    0.479   0.000  HarzardDUnit/_and0000102_F (N2138)
     MUXF5:I0->O           2    0.314   0.804  HarzardDUnit/_and0000102 (HarzardDUnit/_and0000_map61)
     LUT3:I2->O           21    0.479   1.347  HarzardDUnit/Mrom__rom00001 (N4)
     LUT3:I2->O           11    0.479   0.972  IFID/_not00011 (IFID/_not0001)
     FDPE_1:CE                  0.524          IFID/InstOUT_29
    ----------------------------------------
    Total                       9.219ns (3.380ns logic, 5.839ns route)
                                        (36.7% logic, 63.3% route)

=========================================================================
```

```
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 30417 / 61
--------------------------------------------------------------------------------
Offset:              15.544ns (Levels of Logic = 40)
  Source:            Reset (PAD)
  Destination:       PC/PCOUT_0 (FF)
  Destination Clock: clk falling

  Data Path: Reset to PC/PCOUT_0
                                   Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O           104    0.715   2.221  Reset_IBUF (Reset_IBUF)
     LUT4:I0->O            2    0.479   0.915  ForwardingUnit/ForwardB<1>112_SW6 (N1881)
     LUT4:I1->O           51    0.479   1.691  ForwardingUnit/ForwardB<1>1111 (ForwardB<1>)
     LUT4_D:I3->O          1    0.479   0.740  ALUAugend<1>50 (ALUAugend<1>)
     LUT4:I2->O            1    0.479   0.000  ALU/Mcompar__cmp_lt0000_lut<1> (ALU/N38)
     MUXCY:S->O            1    0.435   0.000  ALU/Mcompar__cmp_lt0000_cy<1> (ALU/Mcompar__cmp_lt0000_cy<1>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<2> (ALU/Mcompar__cmp_lt0000_cy<2>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<3> (ALU/Mcompar__cmp_lt0000_cy<3>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<4> (ALU/Mcompar__cmp_lt0000_cy<4>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<5> (ALU/Mcompar__cmp_lt0000_cy<5>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<6> (ALU/Mcompar__cmp_lt0000_cy<6>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<7> (ALU/Mcompar__cmp_lt0000_cy<7>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<8> (ALU/Mcompar__cmp_lt0000_cy<8>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<9> (ALU/Mcompar__cmp_lt0000_cy<9>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<10> (ALU/Mcompar__cmp_lt0000_cy<10>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<11> (ALU/Mcompar__cmp_lt0000_cy<11>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<12> (ALU/Mcompar__cmp_lt0000_cy<12>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<13> (ALU/Mcompar__cmp_lt0000_cy<13>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<14> (ALU/Mcompar__cmp_lt0000_cy<14>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<15> (ALU/Mcompar__cmp_lt0000_cy<15>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<16> (ALU/Mcompar__cmp_lt0000_cy<16>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<17> (ALU/Mcompar__cmp_lt0000_cy<17>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<18> (ALU/Mcompar__cmp_lt0000_cy<18>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<19> (ALU/Mcompar__cmp_lt0000_cy<19>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<20> (ALU/Mcompar__cmp_lt0000_cy<20>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<21> (ALU/Mcompar__cmp_lt0000_cy<21>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<22> (ALU/Mcompar__cmp_lt0000_cy<22>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<23> (ALU/Mcompar__cmp_lt0000_cy<23>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<24> (ALU/Mcompar__cmp_lt0000_cy<24>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<25> (ALU/Mcompar__cmp_lt0000_cy<25>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<26> (ALU/Mcompar__cmp_lt0000_cy<26>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<27> (ALU/Mcompar__cmp_lt0000_cy<27>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<28> (ALU/Mcompar__cmp_lt0000_cy<28>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<29> (ALU/Mcompar__cmp_lt0000_cy<29>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<30> (ALU/Mcompar__cmp_lt0000_cy<30>)
     MUXCY:CI->O           1    0.265   0.740  ALU/Mcompar__cmp_lt0000_cy<31> (ALU/Mcompar__cmp_lt0000_cy<31>)
     LUT4_D:I2->O          1    0.479   0.704  ALU/_old_Result_1<0>33 (ALU/_old_Result_1<0>_map631)
     LUT4:I3->O            1    0.479   0.000  ALU/_cmp_eq0000_wg_lut<7> (N201)
     MUXCY:S->O           20    0.644   1.336  ALU/_cmp_eq0000_wg_cy<7> (ALU/_cmp_eq0000_wg_cy<7>)
     LUT4:I3->O            1    0.479   0.000  MUX_8/DataOUT<5>1 (PCIN<5>)
     FDCE_1:D                   0.176          PC/PCOUT_5
    ----------------------------------------
    Total                     15.544ns (7.197ns logic, 8.347ns route)
                                       (46.3% logic, 53.7% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'IFIDRegclk1'
  Total number of paths / destination ports: 128952 / 47
--------------------------------------------------------------------------------
Offset:              17.526ns (Levels of Logic = 40)
  Source:            Reset (PAD)
  Destination:       IFID/InstOUT_23 (FF)
  Destination Clock: IFIDRegclk1 falling

  Data Path: Reset to IFID/InstOUT_23
                                   Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O           104    0.715   2.221  Reset_IBUF (Reset_IBUF)
     LUT4:I0->O            2    0.479   0.915  ForwardingUnit/ForwardB<1>112_SW6 (N1881)
     LUT4:I1->O           51    0.479   1.691  ForwardingUnit/ForwardB<1>1111 (ForwardB<1>)
     LUT4_D:I3->O          1    0.479   0.740  ALUAugend<1>50 (ALUAugend<1>)
     LUT4:I2->O            1    0.479   0.000  ALU/Mcompar__cmp_lt0000_lut<1> (ALU/N38)
     MUXCY:S->O            1    0.435   0.000  ALU/Mcompar__cmp_lt0000_cy<1> (ALU/Mcompar__cmp_lt0000_cy<1>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<2> (ALU/Mcompar__cmp_lt0000_cy<2>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<3> (ALU/Mcompar__cmp_lt0000_cy<3>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<4> (ALU/Mcompar__cmp_lt0000_cy<4>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<5> (ALU/Mcompar__cmp_lt0000_cy<5>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<6> (ALU/Mcompar__cmp_lt0000_cy<6>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<7> (ALU/Mcompar__cmp_lt0000_cy<7>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<8> (ALU/Mcompar__cmp_lt0000_cy<8>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<9> (ALU/Mcompar__cmp_lt0000_cy<9>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<10> (ALU/Mcompar__cmp_lt0000_cy<10>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<11> (ALU/Mcompar__cmp_lt0000_cy<11>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<12> (ALU/Mcompar__cmp_lt0000_cy<12>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<13> (ALU/Mcompar__cmp_lt0000_cy<13>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<14> (ALU/Mcompar__cmp_lt0000_cy<14>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<15> (ALU/Mcompar__cmp_lt0000_cy<15>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<16> (ALU/Mcompar__cmp_lt0000_cy<16>)
     MUXCY:CI->O           1    0.056   0.000  ALU/Mcompar__cmp_lt0000_cy<17> (ALU/Mcompar__cmp_lt0000_cy<17>)
```

```
    MUXCY:CI->O           1     0.055     0.000   ALU/Mcompar__cmp_lt0000_cy<18> (ALU/Mcompar__cmp_lt0000_cy<18>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<19> (ALU/Mcompar__cmp_lt0000_cy<19>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<20> (ALU/Mcompar__cmp_lt0000_cy<20>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<21> (ALU/Mcompar__cmp_lt0000_cy<21>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<22> (ALU/Mcompar__cmp_lt0000_cy<22>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<23> (ALU/Mcompar__cmp_lt0000_cy<23>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<24> (ALU/Mcompar__cmp_lt0000_cy<24>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<25> (ALU/Mcompar__cmp_lt0000_cy<25>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<26> (ALU/Mcompar__cmp_lt0000_cy<26>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<27> (ALU/Mcompar__cmp_lt0000_cy<27>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<28> (ALU/Mcompar__cmp_lt0000_cy<28>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<29> (ALU/Mcompar__cmp_lt0000_cy<29>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Mcompar__cmp_lt0000_cy<30> (ALU/Mcompar__cmp_lt0000_cy<30>)
    MUXCY:CI->O           1     0.265     0.740   ALU/Mcompar__cmp_lt0000_cy<31> (ALU/Mcompar__cmp_lt0000_cy<31>)
    LUT4_D:I2->O          1     0.479     0.704   ALU/_old_Result_1<0>33 (ALU/_old_Result_1<0>_map631)
    LUT4:I3->O            1     0.479     0.000   ALU/_cmp_eq0000_wg_lut<7> (N201)
    MUXCY:S->O           20     0.644     1.608   ALU/_cmp_eq0000_wg_cy<7> (ALU/_cmp_eq0000_wg_cy<7>)
    LUT2:I0->O           13     0.479     0.994   Ctrl/_and00001 (IFIDFlush)
    FDRE_1:R                    0.892             IFID/InstOUT_23
    ----------------------------------------
    Total                      17.526ns (7.913ns logic, 9.613ns route)
                                       (45.1% logic, 54.9% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 120598 / 1
--------------------------------------------------------------------------
Offset:                 20.465ns (Levels of Logic = 24)
  Source:               IDEX/IFIDRtOUT_1 (FF)
  Destination:          ALU0 (PAD)
  Source Clock:         clk falling

  Data Path: IDEX/IFIDRtOUT_1 to ALU0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay   Logical Name (Net Name)
    ----------------------------------------  ------------
    FD_1:C->Q             5     0.626     1.078   IDEX/IFIDRtOUT_1 (IDEX/IFIDRtOUT_1)
    LUT4_D:I0->O          2     0.479     0.768   ForwardingUnit/_cmp_eq0001526 (ForwardingUnit/_cmp_eq00015_map343)
    LUT4:I3->O           10     0.479     1.134   ForwardingUnit/_xor0001_1 (ForwardingUnit/_xor00011)
    LUT3:I1->O           12     0.479     1.009   ForwardingUnit/ForwardA<1>1_SW0_1 (ForwardingUnit/ForwardA<1>1_SW0)
    LUT4:I2->O            3     0.479     0.941   ALUAddend<0> (ALUAddend<0>)
    LUT3:I1->O            1     0.479     0.000   ALU/Maddsub__addsub0000_lut<0> (ALU/N5)
    MUXCY:S->O            1     0.435     0.000   ALU/Maddsub__addsub0000_cy<0> (ALU/Maddsub__addsub0000_cy<0>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Maddsub__addsub0000_cy<1> (ALU/Maddsub__addsub0000_cy<1>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Maddsub__addsub0000_cy<2> (ALU/Maddsub__addsub0000_cy<2>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Maddsub__addsub0000_cy<3> (ALU/Maddsub__addsub0000_cy<3>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Maddsub__addsub0000_cy<4> (ALU/Maddsub__addsub0000_cy<4>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Maddsub__addsub0000_cy<5> (ALU/Maddsub__addsub0000_cy<5>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Maddsub__addsub0000_cy<6> (ALU/Maddsub__addsub0000_cy<6>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Maddsub__addsub0000_cy<7> (ALU/Maddsub__addsub0000_cy<7>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Maddsub__addsub0000_cy<8> (ALU/Maddsub__addsub0000_cy<8>)
    MUXCY:CI->O           1     0.056     0.000   ALU/Maddsub__addsub0000_cy<9> (ALU/Maddsub__addsub0000_cy<9>)
    XORCY:CI->O           1     0.786     0.704   ALU/Maddsub__addsub0000_xor<10> (ALU/_addsub0000<10>)
    LUT4:I3->O            2     0.479     0.915   ALU/_old_Result_1<10> (EXALUOUT<10>)
    LUT4:I1->O            1     0.479     0.704   ALU/_old_Result_1<29>_SW1 (N1875)
    LUT4:I3->O            1     0.479     0.000   ALU/_cmp_eq0000_wg_lut<4> (N171)
    MUXCY:S->O            1     0.435     0.000   ALU/_cmp_eq0000_wg_cy<4> (ALU/_cmp_eq0000_wg_cy<4>)
    MUXCY:CI->O           1     0.056     0.000   ALU/_cmp_eq0000_wg_cy<5> (ALU/_cmp_eq0000_wg_cy<5>)
    MUXCY:CI->O           1     0.056     0.000   ALU/_cmp_eq0000_wg_cy<6> (ALU/_cmp_eq0000_wg_cy<6>)
    MUXCY:CI->O          20     0.265     1.313   ALU/_cmp_eq0000_wg_cy<7> (ALU/_cmp_eq0000_wg_cy<7>)
    OBUF:I->O                   4.909             ALU0_OBUF (ALU0)
    ----------------------------------------
    Total                      20.465ns (11.898ns logic, 8.567ns route)
                                       (58.1% logic, 41.9% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'IFIDRegclk1'
  Total number of paths / destination ports: 2 / 2
--------------------------------------------------------------------------
Offset:                 7.324ns (Levels of Logic = 1)
  Source:               IFID/InstOUT_22 (FF)
  Destination:          SO<1> (PAD)
  Source Clock:         IFIDRegclk1 falling

  Data Path: IFID/InstOUT_22 to SO<1>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay   Logical Name (Net Name)
    ----------------------------------------  ------------
    FDRE_1:C->Q          76     0.626     1.789   IFID/InstOUT_22 (IFID/InstOUT_22)
    OBUF:I->O                   4.909             SO_1_OBUF (SO<1>)
    ----------------------------------------
    Total                       7.324ns (5.535ns logic, 1.789ns route)
                                       (75.6% logic, 24.4% route)

==========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 3792 / 1
--------------------------------------------------------------------------
Delay:                  19.775ns (Levels of Logic = 40)
  Source:               Reset (PAD)
  Destination:          ALU0 (PAD)
```

```
Data Path: Reset to ALU0
                                          Gate         Net
   Cell:in->out          fanout     Delay     Delay    Logical Name (Net Name)
   ----------------------------------------  ------------
    IBUF:I->O                104     0.715     2.221    Reset_IBUF (Reset_IBUF)
    LUT4:I0->O                 2     0.479     0.915    ForwardingUnit/ForwardB<1>112_SW6 (N1881)
    LUT4:I1->O                51     0.479     1.691    ForwardingUnit/ForwardB<1>1111 (ForwardB<1>)
    LUT4_D:I3->O               1     0.479     0.740    ALUAugend<1>50 (ALUAugend<1>)
    LUT4:I2->O                 1     0.479     0.000    ALU/Mcompar__cmp_lt0000_lut<1> (ALU/N38)
    MUXCY:S->O                 1     0.435     0.000    ALU/Mcompar__cmp_lt0000_cy<1> (ALU/Mcompar__cmp_lt0000_cy<1>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<2> (ALU/Mcompar__cmp_lt0000_cy<2>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<3> (ALU/Mcompar__cmp_lt0000_cy<3>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<4> (ALU/Mcompar__cmp_lt0000_cy<4>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<5> (ALU/Mcompar__cmp_lt0000_cy<5>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<6> (ALU/Mcompar__cmp_lt0000_cy<6>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<7> (ALU/Mcompar__cmp_lt0000_cy<7>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<8> (ALU/Mcompar__cmp_lt0000_cy<8>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<9> (ALU/Mcompar__cmp_lt0000_cy<9>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<10> (ALU/Mcompar__cmp_lt0000_cy<10>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<11> (ALU/Mcompar__cmp_lt0000_cy<11>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<12> (ALU/Mcompar__cmp_lt0000_cy<12>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<13> (ALU/Mcompar__cmp_lt0000_cy<13>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<14> (ALU/Mcompar__cmp_lt0000_cy<14>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<15> (ALU/Mcompar__cmp_lt0000_cy<15>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<16> (ALU/Mcompar__cmp_lt0000_cy<16>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<17> (ALU/Mcompar__cmp_lt0000_cy<17>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<18> (ALU/Mcompar__cmp_lt0000_cy<18>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<19> (ALU/Mcompar__cmp_lt0000_cy<19>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<20> (ALU/Mcompar__cmp_lt0000_cy<20>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<21> (ALU/Mcompar__cmp_lt0000_cy<21>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<22> (ALU/Mcompar__cmp_lt0000_cy<22>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<23> (ALU/Mcompar__cmp_lt0000_cy<23>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<24> (ALU/Mcompar__cmp_lt0000_cy<24>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<25> (ALU/Mcompar__cmp_lt0000_cy<25>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<26> (ALU/Mcompar__cmp_lt0000_cy<26>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<27> (ALU/Mcompar__cmp_lt0000_cy<27>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<28> (ALU/Mcompar__cmp_lt0000_cy<28>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<29> (ALU/Mcompar__cmp_lt0000_cy<29>)
    MUXCY:CI->O                1     0.056     0.000    ALU/Mcompar__cmp_lt0000_cy<30> (ALU/Mcompar__cmp_lt0000_cy<30>)
    MUXCY:CI->O                1     0.264     0.740    ALU/Mcompar__cmp_lt0000_cy<31> (ALU/Mcompar__cmp_lt0000_cy<31>)
    LUT4_D:I2->O               1     0.479     0.704    ALU/_old_Result_1<0>33 (ALU/_old_Result_1<0>_map631)
    LUT4:I3->O                 1     0.479     0.000    ALU/_cmp_eq0000_wg_lut<7> (N201)
    MUXCY:S->O                20     0.644     1.313    ALU/_cmp_eq0000_wg_cy<7> (ALU/_cmp_eq0000_wg_cy<7>)
    OBUF:I->O                        4.909              ALU0_OBUF (ALU0)
   ----------------------------------------
   Total                            19.775ns (11.451ns logic, 8.324ns route)
                                            (57.9% logic, 42.1% route)

========================================================================
CPU : 22.34 / 22.61 s | Elapsed : 23.00 / 23.00 s

-->

Total memory usage is 143112 kilobytes

Number of errors     :       0 (     0 filtered)
Number of warnings :     165 (     0 filtered)
Number of infos      :      17 (     0 filtered)
```

## 2.6 Identify the critical path using the STA tool of Xilinx ISE.

Maximum delay is 17.804ns.

---

| | |
|---|---|
| Delay: | 17.804ns (data path - clock path skew + uncertainty) |
| Source: | IDEX/CtrlEXOUT_4 (FF) |
| Destination: | IFID/InstOUT_13 (FF) |
| Data Path Delay: | 17.804ns (Levels of Logic = 13) |
| Clock Path Skew: | 0.000ns |
| Source Clock: | clk_BUFGP falling |
| Destination Clock: | IFIDRegclk falling |
| Clock Uncertainty: | 0.000ns |

Constraint Improvement Wizard

Data Path: IDEX/CtrlEXOUT_4 to IFID/InstOUT_13

| Delay type | Delay(ns) | Logical Resource(s) |
|---|---|---|
| Tcko | 0.626 | IDEX/CtrlEXOUT_4 |
| net (fanout=5) | 1.618 | IDEX/CtrlEXOUT<4> |
| Tilo | 0.529 | ALU/_mux00001 |
| net (fanout=46) | 1.752 | ALU/_mux0000 |
| Tilo | 0.479 | ALUAugend<17>50_SW1 |
| net (fanout=1) | 3.334 | N2049 |
| Topcyg | 0.954 | ALU/Maddsub__addsub0000_lut<17> |

| | | |
|---|---|---|
| | | ALU/Maddsub__addsub0000_cy<17> |
| net (fanout=1) | 0.000 | ALU/Maddsub__addsub0000_cy<17> |
| Tbyp | 0.104 | ALU/Maddsub__addsub0000_cy<18> |
| | | ALU/Maddsub__addsub0000_cy<19> |
| net (fanout=1) | 0.000 | ALU/Maddsub__addsub0000_cy<19> |
| Tbyp | 0.104 | ALU/Maddsub__addsub0000_cy<20> |
| | | ALU/Maddsub__addsub0000_cy<21> |
| net (fanout=1) | 0.000 | ALU/Maddsub__addsub0000_cy<21> |
| Tbyp | 0.104 | ALU/Maddsub__addsub0000_cy<22> |
| | | ALU/Maddsub__addsub0000_cy<23> |
| net (fanout=1) | 0.000 | ALU/Maddsub__addsub0000_cy<19> |
| Tbyp | 0.104 | ALU/Maddsub__addsub0000_cy<20> |
| | | ALU/Maddsub__addsub0000_cy<21> |
| net (fanout=1) | 0.000 | ALU/Maddsub__addsub0000_cy<21> |
| Tbyp | 0.104 | ALU/Maddsub__addsub0000_cy<22> |
| | | ALU/Maddsub__addsub0000_cy<23> |
| net (fanout=1) | 0.000 | ALU/Maddsub__addsub0000_cy<23> |
| Tcinx | 0.786 | ALU/Maddsub__addsub0000_xor<24> |
| net (fanout=1) | 0.809 | ALU/_addsub0000<24> |
| Tilo | 0.479 | ALU/_old_Result_1<24> |
| net (fanout=1) | .512 | EXALUOUT<24> |
| Topcyf | 0.944 | ALU/_cmp_eq0000_wg_lut<0> |
| | | ALU/_cmp_eq0000_wg_cy<0> |
| | | ALU/_cmp_eq0000_wg_cy<1> |
| net (fanout=1) | 0.000 | ALU/_cmp_eq0000_wg_cy<1> |
| Tbyp | 0.104 | ALU/_cmp_eq0000_wg_cy<2> |
| | | ALU/_cmp_eq0000_wg_cy<3> |
| net (fanout=1) | 0.000 | ALU/_cmp_eq0000_wg_cy<3> |
| Tbyp | 0.104 | ALU/_cmp_eq0000_wg_cy<4> |
| | | ALU/_cmp_eq0000_wg_cy<5> |
| net (fanout=1) | 0.000 | ALU/_cmp_eq0000_wg_cy<5> |
| Tbyp | 0.104 | ALU/_cmp_eq0000_wg_cy<6> |
| | | ALU/_cmp_eq0000_wg_cy<7> |
| net (fanout=20) | 1.476 | ALU/_cmp_eq0000_wg_cy<7> |
| Tilo | 0.479 | Ctrl/_and00001 |
| net (fanout=7) | 1.511 | IFIDFlush |
| Tsrck | 0.892 | IFID/InstOUT_13 |
| --- | --- | --- |
| Total | 17.804ns | (6.792ns logic, 11.012ns route) |
| | | (38.1% logic, 61.9% route) |

## 2.7 Calculate the highest clock rate of the multiplication hardware.

Timing Summary:
---
Speed Grade: -5

Minimum period: 17.804ns (Maximum Frequency: 56.167MHz)
Minimum input arrival time before clock: 17.526ns
Maximum output required time after clock: 20.465ns
Maximum combinational path delay: 19.775ns