EE502
SPRING 2007
Lab 2
Total 100 Points
Shift-add Multiplication Hardware Design
Due: Mar 20, 2007

Part I (10 points): Develop a multiplication algorithm for the refined multiplication hardware in Figure 3.7. It is similar to the multiplication algorithm shown in Figure 3.6. Please also derive a STG (state transition graph), ASM or ASMD (algorithmic state machine and datapath) for your algorithm. In your STG/ASM/ASMD, please clearly describe the states and data transfer movements.

Part II (90 points): Implement the shift-add multiplication hardware using the multiplication algorithm developed in Part I. The datapath of the multiplication hardware is in Figure 3.7 of the textbook. Please design the multiplication hardware in either Verilog or VHDL. Please provide the followings in your lab report:

a) Top-level block diagram of your design with connection between control and datapath of your multiplication hardware.

b) Design source codes in Verilog/VHDL with comments wherever possible.

- Attach the STG/ASMD drawing from Part I.

c) Testbench(es) for various modules of your design.

- Be sure to verify using some corner cases, such as maximum integer, ***negative number (please ignore signed multiplication for this problem for now)***, zero etc.
- Please make your testbench easy to be modified, such as File I/O, so that I can put two numbers to run on your design.

d) Simulation waveforms of your top-level design --- behavioral simulation.

e) Synthesis report of your implementation --- please use Xilinx Spartan-3 XC3S200 as the target device. Your design must be synthesizable.

f) Perform post-synthesis simulation --- simulation waveform of your post-synthesis top-level design.

g) Identify the critical path in your design using the static timing analysis (STA) tool of Xilinx ISE.

h) Calculate the highest clock rate of your multiplication hardware.