EE502
SPRING 2007
Lab 3
Total 150 Points
Simplied MIPS Single-Cycle Computer
Due: May 1, 2007

1. (150 points) Use Verilog or VHDL to implement a functional Single-Cycle Computer with the simplified MIPS ISA described in the textbook.

Please provide the followings in your lab report:

a) Top-level block diagram of your design.

b) Design source codes in Verilog/VHDL with comments wherever possible.

c) Testbench(es) for various modules of your design.

d) Simulation waveforms of your top-level design --- behavioral simulation.

e) Synthesis report of your implementation. Your design must be synthesizable.

f) No need to perform post-synthesis simulation for this lab.

g) Identify the critical path in your design using the static timing analysis (STA) tool of Xilinx ISE.

h) Calculate the highest clock rate of your multiplication hardware.

2. (Extra Credit) Chap 6. Exercise 6.46 Pipelined Single-Cycle Computer

Behavioral simulation only but make sure that your design is synthesizable.