EE502
Computer Architecture

Spring 2007
Temple ECE
Tuesdays 6:00pm-8:30pm
Room ???, Fort Washington

Description: Principles of computer organization and design: instruction set architecture, computer arithmetic, CPU datapath and control unit design, performance and pipelining, memory hierarchy, I/O organization and advanced multiprocessors.

Prerequisite: Advanced Processor Systems EE500

Textbook: *Computer Organization and Design, The Hardware/Software Interface, 3rd edition*
By Patterson and Hennessy

Credit Distribution:

- Three Lab Assignments **25%**
- Written Assignments and Quizzes
  - Six Written Assignments **12%**
    - Will be graded by yourself.
    - Once a graded complete written assignment turned in, you will get 2% credit.
    - Suggested solutions will be posted on the weekend prior to the deadline.
  - Two Quizzes **(close book)** **18%**
    - Quizzes based on written assignments and lecture materials
- Two Exams **(open book)**
  - Midterm **20%**
  - Final (comprehensive) **25%**

No late assignments will be accepted!
No cheating and plagiarisms!

Instructor: Dr. Chen-Huan Chiang
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Please always start **with EE502 in the subject**.
Email to chenhuan@temple.edu will be forwarded automatically to my work email chenhuan@alcatel-lucent.com

Office Hours: Tuesdays 5pm-6pm and by appointment
Location: Room 115, Fort Washington
Telephone: 215-283-1637

LiveMeeting/Skype: In case of snow or any reason that in-class presence is not permitted.
Skype account: chenhuan_temple
Livemeeting notice and conference call number will be posted on BlackBoard

Any student who has a need for accommodation based on the impact of a disability should contact me privately to discuss the specific situation as soon as possible.

Schedule:

Week	*Date*	*Topics*
1	1/16	Introduction (Chap 1)
		Instruction Set Architecture (Chap 2)
		Start HW1
		Start Lab#1, especially tool installation and get familiar with tools
2	1/23	ISA
		SPIM, SimpleScalar demo
		[1/29 Last day to drop]
3	1/30	Computer Arithmetic (Chap 3)
		HW1 due
		Start HW2
4	2/6	Performance (Chap 4)
		Quiz
		HW2 due
		Start HW3
5	2/13	CPU datapath and control (Chap5)
		Lab#1 due.
		Start Lab#2
6	2/20	CPU datapath and control
		HW3 due
		Start HW4
7	2/27	CPU datapath and control
		Midterm
		Start Lab#3, start planning as soon as you can
		[3/6 Spring Recess]
8	3/13	Pipelining (Chap 6)
		HW4 due
		Start HW5
9	3/20	Pipelining
		Lab#2 due
10	3/27	Pipelining
		Memory Hierarchy (Chap 7)
11	4/3	Memory Hierarchy
		Quiz
		HW5 due
		Start HW6
12	4/10	Memory Hierarchy
13	4/17	Memory Hierarchy
14	4/24	IO design (Chap 8)
		Multiprocessor (Chap 9)
		HW6 due
15	5/1	**Final**
		Lab#3 due