LAB Assignment #1, for ECE 338

Assigned Sept 14th
Due ~~Sept 20th~~ Oct 3rd

Description: Create a project with behavioral VHDL and evaluate the behavioral-to-hardware translation process.

Use Vivado to create a project. Add the following VHDL code which uses an if statement within a process block. Open 'elaborated design' and identify components of the schematic that correspond to elements of the VHDL code. Please include your name and the title "Lab #1: Behavioral-to-Schematic Translation, If Statement".

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity FA_ED is
    Port ( a : in STD_LOGIC;
           b : in STD_LOGIC;
           c : in STD_LOGIC;
           ctrl : in STD_LOGIC;
           Cout : out STD_LOGIC;
           sum : out STD_LOGIC
   );
end FA_ED;

architecture rtl of FA_ED is
begin

   process (a, b, c, ctrl)
      begin
      Cout <= '0';
      sum <= '0';

      if (ctrl = '0') then
         Cout <= ((a and b) or (a and c) or (b and c)) and (not a
and not b and not c);
         sum <= '0';
      else
         Cout <= (a and b) or (a and c) or (b and c);
         sum <= a xor b xor c;
      end if;
      end process;
end rtl;
```

This lab is worth 10 points.