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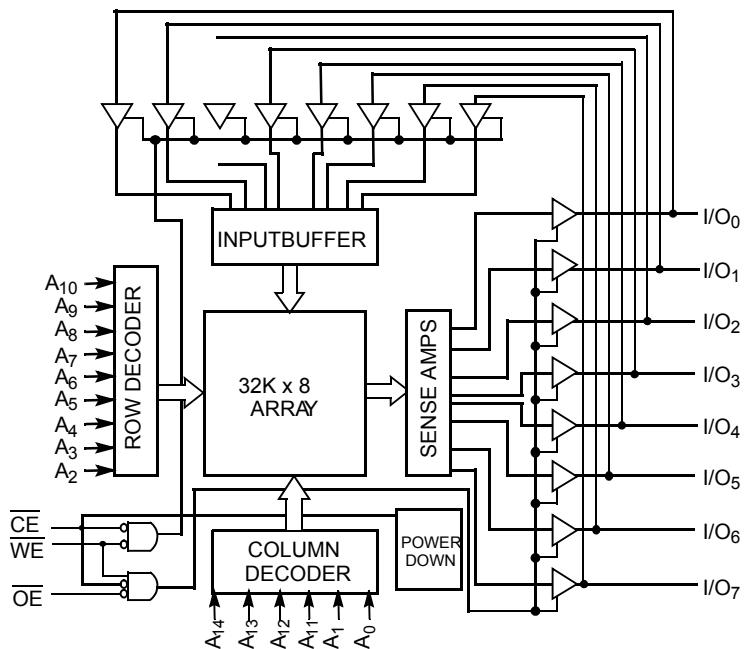
**Continuity of ordering part numbers**

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## Features

- Temperature ranges
  - Commercial: 0 °C to +70 °C
  - Industrial: -40 °C to +85 °C
  - Automotive-A: -40 °C to +85 °C
  - Automotive-E: -40 °C to +125 °C
- High speed: 55 ns
- Voltage range: 4.5 V to 5.5 V operation
- Low active power
  - 275 mW (max)
- Low standby power (LL version)
  - 82.5 µW (max)
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  Features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Available in Pb-free and non Pb-free 28-pin (600-mil) PDIP, 28-pin (300-mil) narrow SOIC, 28-pin TSOP I, and 28-pin reverse TSOP I packages

## Logic Block Diagram



## Functional Description

The CY62256N is a high performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and active LOW output enable ( $\overline{OE}$ ) and tristate drivers. This device has an automatic power-down feature, reducing the power consumption by 99.9 percent when deselected.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory location addressed by the address present on the address pins (A<sub>0</sub> through A<sub>14</sub>). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

For a complete list of related documentation, click [here](#).

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## Product Portfolio

Product		$V_{CC}$ Range (V)			Speed (ns)	Power Dissipation			
					Speed (ns)	Operating, $I_{CC}$ (mA)		Standby, $I_{SB2}$ ( $\mu$ A)	
		Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY62256NLL	Commercial	4.5	5.0	5.5	70	25	50	0.1	5
CY62256NLL	Industrial					25	50	0.1	10
CY62256NLL	Automotive-A					25	50	0.1	10
CY62256NLL	Automotive-E					55	25	0.1	15

## Pin Configurations

Figure 1. 28-pin DIP and Narrow SOIC pinout

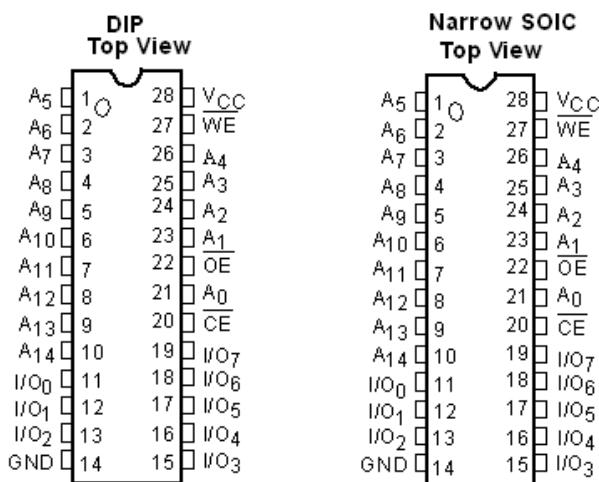
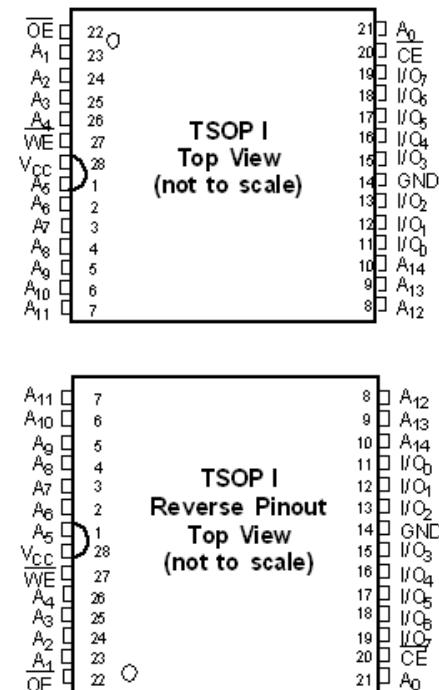


Figure 2. 28-pin TSOP I and Reverse TSOP I pinout



## Pin Definitions

Pin Number	Type	Description
1–10, 21, 23–26	Input	<b>A<sub>0</sub>–A<sub>14</sub></b> . Address Inputs
11–13, 15–19,	Input/Output	<b>I/O<sub>0</sub>–I/O<sub>7</sub></b> . Data lines. Used as input or output lines depending on operation
27	Input/Control	<b>WE</b> . When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
20	Input/Control	<b>CE</b> . When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	<b>OE</b> . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins
14	Ground	<b>GND</b> . Ground for the device
28	Power Supply	<b>V<sub>CC</sub></b> . Power supply for the device

### Note

1. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions ( $T_A = 25^\circ\text{C}$ ,  $V_{CC}$ ). Parameters are guaranteed by design and characterization, and not 100% tested.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.	
Storage temperature	..... $-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Ambient temperature with power applied	..... $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Supply voltage to ground potential (pin 28 to pin 14) <sup>[2]</sup>	..... $-0.5\text{ V}$ to $+7.0\text{ V}$
DC voltage applied to outputs in high Z State <sup>[2]</sup>	..... $-0.5\text{ V}$ to $V_{\text{CC}} + 0.5\text{ V}$
DC input voltage <sup>[2]</sup>	..... $-0.5\text{ V}$ to $V_{\text{CC}} + 0.5\text{ V}$

Output current into outputs (LOW)	..... 20 mA
Static discharge voltage (per MIL-STD-883, method 3015)	..... $> 2001\text{ V}$
Latch-up current	..... $> 200\text{ mA}$

## Operating Range

Range	Ambient Temperature ( $T_A$ ) <sup>[3]</sup>	$V_{\text{CC}}$
Commercial	0 $^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	5 V $\pm 10\%$
Industrial	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	5 V $\pm 10\%$
Automotive-A	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	5 V $\pm 10\%$
Automotive-E	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	5 V $\pm 10\%$

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-55			-70			Unit	
			Min	Typ <sup>[4]</sup>	Max	Min	Typ <sup>[4]</sup>	Max		
$V_{\text{OH}}$	Output HIGH voltage	$V_{\text{CC}} = \text{Min}$ , $I_{\text{OH}} = -1.0\text{ mA}$	2.4	—	—	2.4	—	—	V	
$V_{\text{OL}}$	Output LOW voltage	$V_{\text{CC}} = \text{Min}$ , $I_{\text{OL}} = 2.1\text{ mA}$	—	—	0.4	—	—	0.4	V	
$V_{\text{IH}}$	Input HIGH voltage		2.2	—	$V_{\text{CC}} + 0.5$	2.2	—	$V_{\text{CC}} + 0.5$	V	
$V_{\text{IL}}$	Input LOW voltage		-0.5	—	0.8	-0.5	—	0.8	V	
$I_{\text{IX}}$	Input leakage current	$\text{GND} \leq V_I \leq V_{\text{CC}}$	-0.5	—	+0.5	-0.5	—	+0.5	$\mu\text{A}$	
$I_{\text{OZ}}$	Output leakage current	$\text{GND} \leq V_O \leq V_{\text{CC}}$ , output disabled	-0.5	—	+0.5	-0.5	—	+0.5	$\mu\text{A}$	
$I_{\text{CC}}$	$V_{\text{CC}}$ operating supply current	$V_{\text{CC}} = \text{Max}$ , $I_{\text{OUT}} = 0\text{ mA}$ , $f = f_{\text{MAX}} = 1/t_{\text{RC}}$	LL - Commercial	—	—	—	25	50	mA	
			LL - Industrial	—	25	50	—	25	50	mA
			LL - Automotive-A	—	25	50	—	25	50	mA
			LL - Automotive-E	—	25	50	—	—	—	mA
$I_{\text{SB1}}$	Automatic CE power-down current – TTL inputs	$\text{Max. } V_{\text{CC}}, \overline{\text{CE}} \geq V_{\text{IH}}$ , $V_{\text{IN}} \geq V_{\text{IH}}$ or $V_{\text{IN}} \leq V_{\text{IL}}$ , $f = f_{\text{MAX}}$	LL - Commercial	—	—	—	0.3	0.5	mA	
			LL - Industrial	—	0.3	0.5	—	0.3	0.5	mA
			LL - Automotive-A	—	0.3	0.5	—	0.3	0.5	mA
			LL - Automotive-E	—	0.3	0.5	—	—	—	mA
$I_{\text{SB2}}$	Automatic CE power-down current – CMOS inputs	$\text{Max. } V_{\text{CC}}, \overline{\text{CE}} \geq V_{\text{CC}} - 0.3\text{ V}$ , $V_{\text{IN}} \geq V_{\text{CC}} - 0.3\text{ V}$ , or $V_{\text{IN}} \leq 0.3\text{ V}$ , $f = 0$	LL - Commercial	—	—	—	0.1	5	$\mu\text{A}$	
			LL - Industrial	—	0.1	10	—	0.1	10	$\mu\text{A}$
			LL - Automotive-A	—	0.1	10	—	0.1	10	$\mu\text{A}$
			LL - Automotive-E	—	0.1	15	—	—	—	$\mu\text{A}$

### Notes

2.  $V_{\text{IL}}(\text{min}) = -2.0\text{ V}$  for pulse durations of less than 20 ns.
3.  $T_A$  is the "Instant-On" case temperature.
4. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions ( $T_A = 25^{\circ}\text{C}$ ,  $V_{\text{CC}}$ ). Parameters are guaranteed by design and characterization, and not 100% tested.

## Capacitance

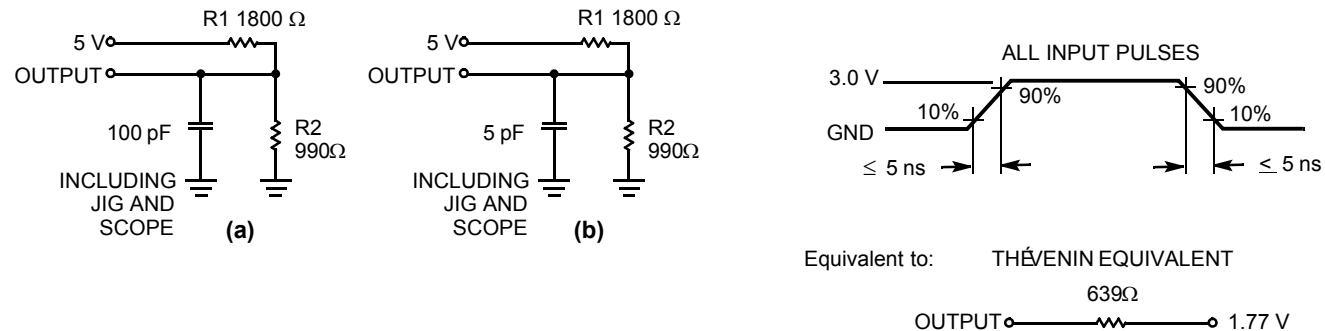
Parameter [5]	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 5.0 \text{ V}$	6	pF
$C_{OUT}$	Output capacitance		8	pF

## Thermal Resistance

Parameter [5]	Description	Test Conditions	DIP	SOIC	TSOP	RTSOP	Unit
$\theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a $4.25 \times 1.125$ inch, 4-layer printed circuit board	75.61	76.56	93.89	93.89	$^\circ\text{C/W}$
$\theta_{JC}$	Thermal resistance (junction to case)		43.12	36.07	24.64	24.64	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



### Note

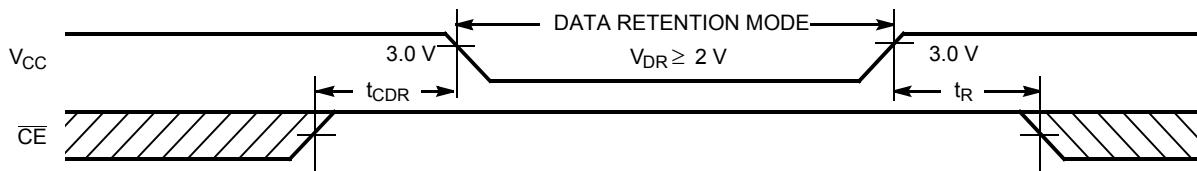
5. Tested initially and after any design or process changes that may affect these parameters.

## Data Retention Characteristics

Parameter	Description		Conditions <sup>[6]</sup>	Min	Typ <sup>[7]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention			2.0	—	—	V
$I_{CCDR}$	Data retention current	LL – Commercial	$V_{CC} = 2.0\text{ V}$ , $CE \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ , or $V_{IN} \leq 0.3\text{ V}$	—	0.1	5	$\mu\text{A}$
		LL – Industrial/Automotive-A		—	0.1	10	$\mu\text{A}$
		LL – Automotive-E		—	0.1	10	$\mu\text{A}$
$t_{CDR}$ <sup>[7]</sup>	Chip deselect to data retention time			0	—	—	ns
$t_R$ <sup>[7]</sup>	Operation recovery time		CY62256NLL-55	55	—	—	ns
			CY62256NLL-70	70	—	—	

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

6. No input may exceed  $V_{CC} + 0.5\text{ V}$ .
7. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions ( $T_A = 25^\circ\text{C}$ ,  $V_{CC}$ ). Parameters are guaranteed by design and characterization, and not 100% tested.

## Switching Characteristics

Over the Operating Range

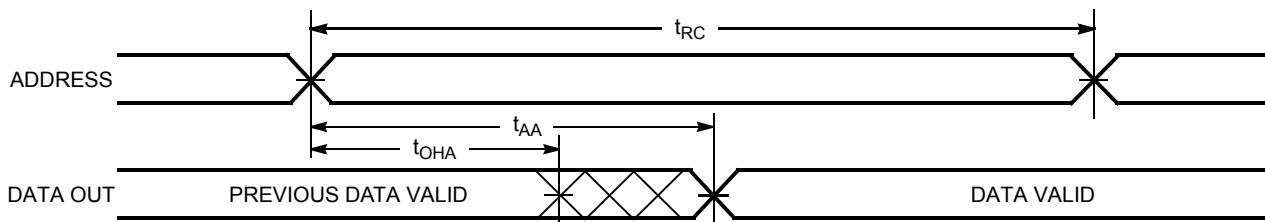
Parameter <sup>[8]</sup>	Description	CY62256N-55		CY62256N-70		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	55	—	70	—	ns
$t_{AA}$	Address to data valid	—	55	—	70	ns
$t_{OHA}$	Data hold from address change	5	—	5	—	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	—	55	—	70	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	—	25	—	35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[9]</sup>	5	—	5	—	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[9, 10]</sup>	—	20	—	25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[9]</sup>	5	—	5	—	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[9, 10]</sup>	—	20	—	25	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	—	0	—	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down	—	55	—	70	ns
<b>Write Cycle</b> <sup>[11, 12]</sup>						
$t_{WC}$	Write cycle time	55	—	70	—	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	45	—	60	—	ns
$t_{AW}$	Address setup to write end	45	—	60	—	ns
$t_{HA}$	Address hold from write end	0	—	0	—	ns
$t_{SA}$	Address setup to write start	0	—	0	—	ns
$t_{PWE}$	$\overline{WE}$ pulse width	40	—	50	—	ns
$t_{SD}$	Data setup to write end	25	—	30	—	ns
$t_{HD}$	Data hold from write end	0	—	0	—	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[9, 10]</sup>	—	20	—	25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[9]</sup>	5	—	5	—	ns

### Notes

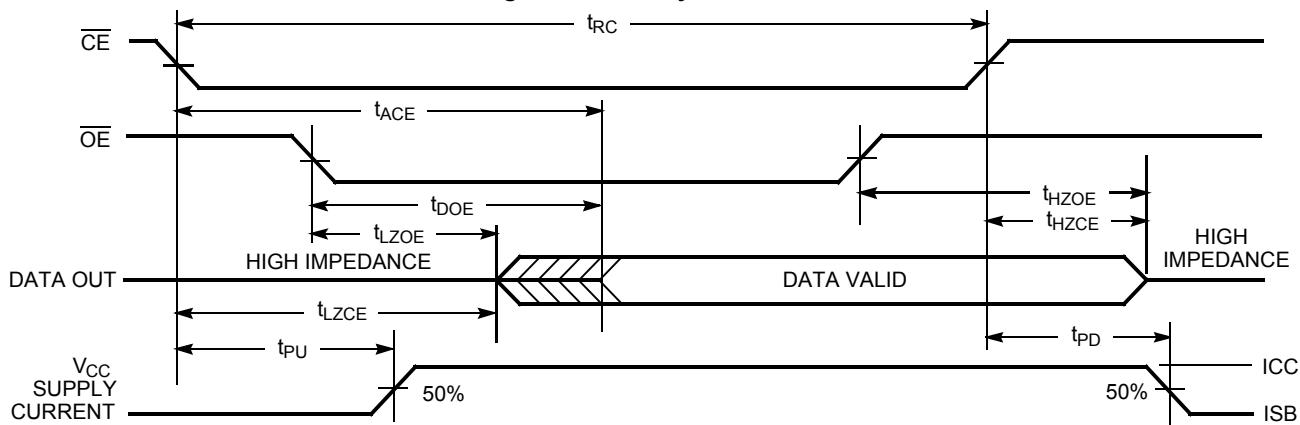
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 100-pF load capacitance.
9. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
10.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5 \text{ pF}$  as in (b) of AC Test Loads. Transition is measured  $\pm 500 \text{ mV}$  from steady-state voltage.
11. The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the Write.
12. The minimum write cycle time for Write Cycle No. 3 (WE Controlled, OE LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

**Figure 5. Read Cycle No. 1** [13, 14]



**Figure 6. Read Cycle No. 2** [14, 15]

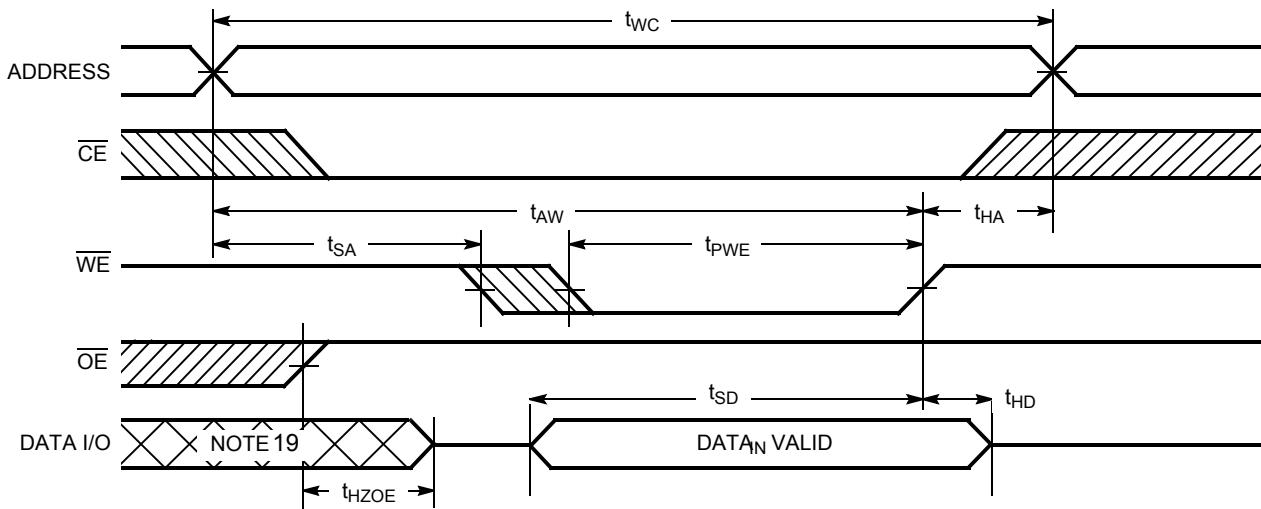


### Notes

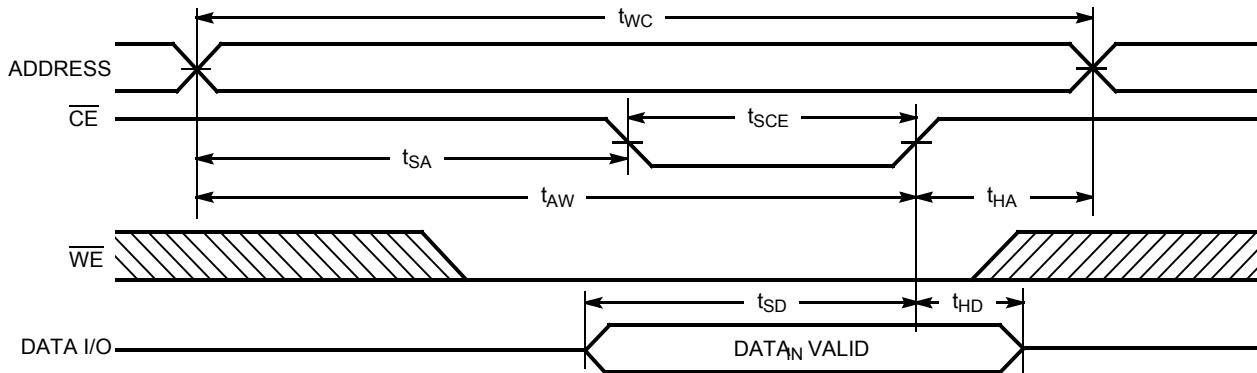
13. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
14. WE is HIGH for Read cycle.
15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms (continued)

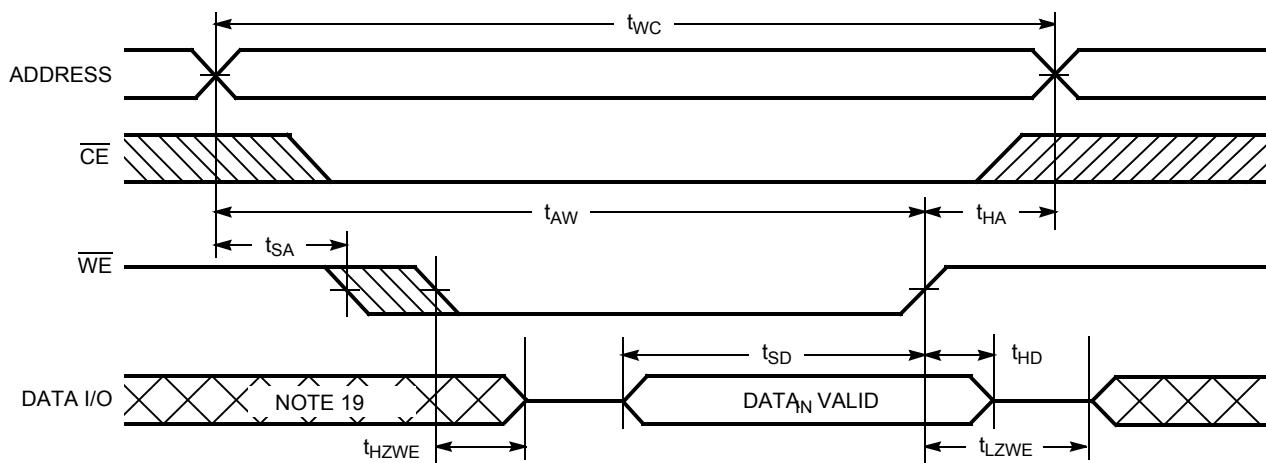
**Figure 7. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled) [16, 17, 18]**



**Figure 8. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled) [16, 17, 18]**



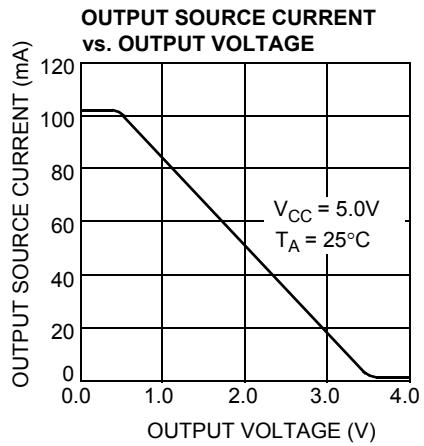
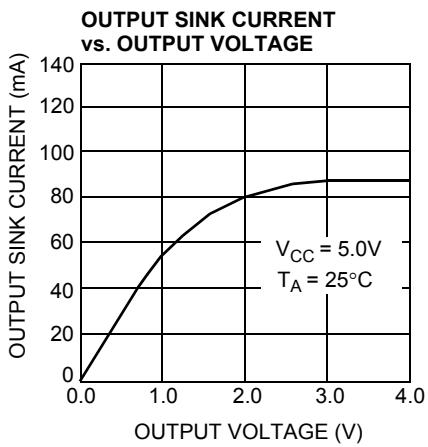
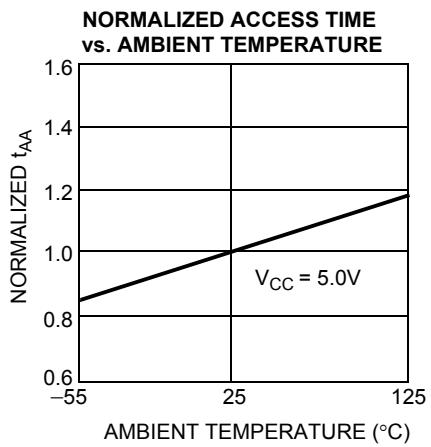
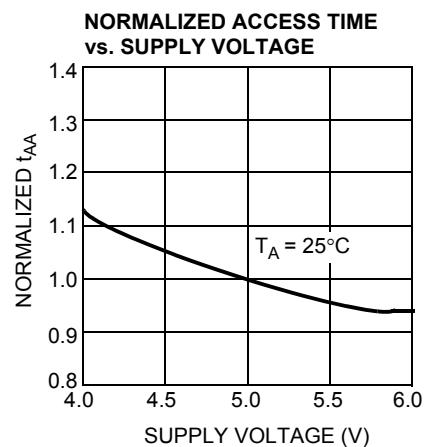
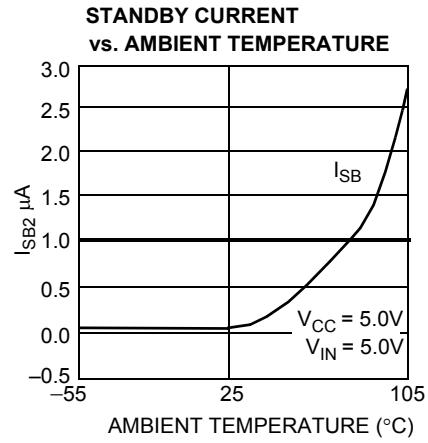
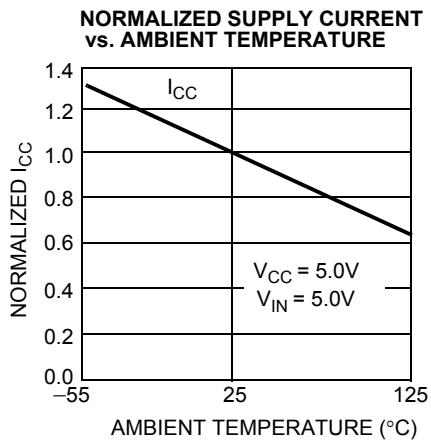
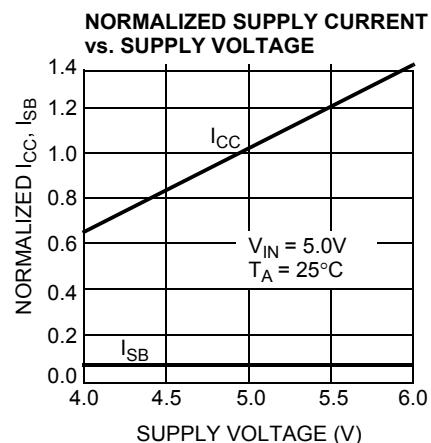
**Figure 9. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [18, 20]**



### Notes

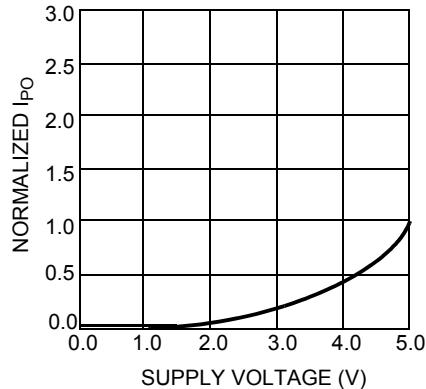
16. The internal Write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the Write.
17. Data I/O is high impedance if  $\text{OE} = V_{IH}$ .
18. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.
20. The minimum write cycle pulse width should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Typical DC and AC Characteristics

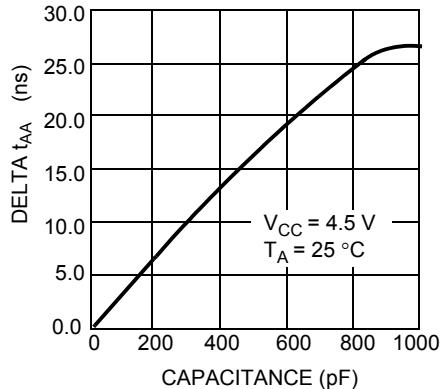


### Typical DC and AC Characteristics (continued)

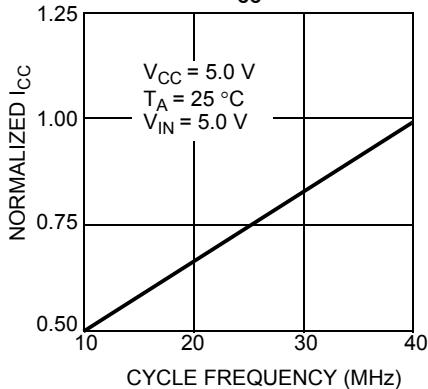
TYPICAL POWER-ON CURRENT  
vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE  
vs. OUTPUT LOADING



NORMALIZED  $I_{CC}$  vs. CYCLE TIME



### Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/power-down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62256NLL-55SNXI	51-85092	28-pin SNC (300 Mils) Narrow Body (Pb-free)	Industrial
	CY62256NLL-55ZXI	51-85071	28-pin TSOP I (Pb-free)	
	CY62256NLL-55ZXA	51-85071	28-pin TSOP I (Pb-free)	Automotive-A
	CY62256NLL-55SNXE	51-85092	28-pin SNC (300 Mils) Narrow Body (Pb-free)	Automotive-E
	CY62256NLL-55ZXE	51-85071	28-pin TSOP I (Pb-free)	
70	CY62256NLL-70PXC	51-85017	28-pin (600 Mil) Molded DIP (Pb-free)	Commercial
	CY62256NLL-70SNXC	51-85092	28-pin SNC (300 Mils) Narrow Body (Pb-free)	
	CY62256NLL-70ZRXI	51-85074	28-pin Reverse TSOP I (Pb-free)	Industrial
	CY62256NLL-70SNXA	51-85092	28-pin SNC (300 Mils) Narrow Body (Pb-free)	Automotive-A

## Ordering Code Definitions

CY 62 256 N LL - XX XXX X

Temperature Grade: X = C or I or A or E  
C = Commercial = 0 °C to +70 °C; I = Industrial = -40 °C to +85 °C;  
A = Automotive-A = -40 °C to +85 °C; E = Automotive-E = -40 °C to +125 °C

Package Type: XXX = SNX or ZX or PX or ZRX  
SNX = 28-pin SNC (Pb-free)  
ZX= 28-pin TSOP I (Pb-free)  
PX = 28-pin Molded DIP (Pb-free)  
ZRX = 28-pin Reverse TSOP I (Pb-free)

Speed Grade: XX = 55 ns or 70 ns

Low Power

Nitride Seal Mask fix

Density: 256 kbit

Family Code: MoBL SRAM family

Company ID: CY = Cypress

## Package Diagrams

Figure 10. 28-pin PDIP (1.480 × 0.550 × 0.195 Inches) P28.6/PZ28.6 Package Outline, 51-85017

28 Lead (600 Mil) PDIP — P15

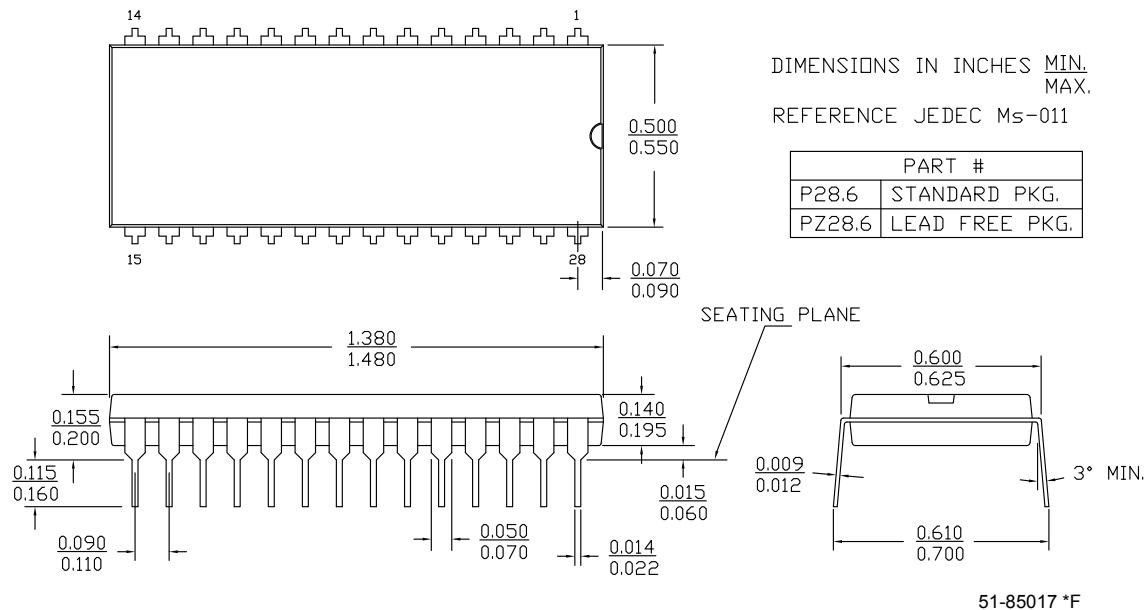
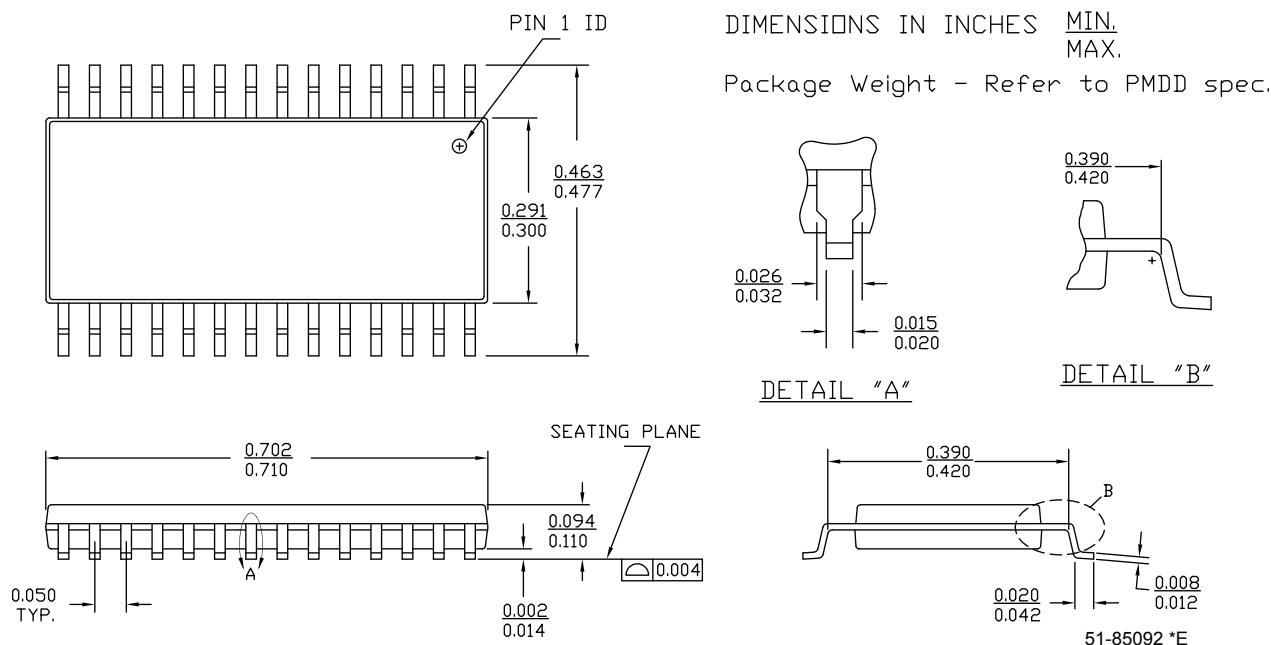


Figure 11. 28-pin SNC (300 Mils) SN28.3 (Narrow Body) Package Outline, 51-85092



## Package Diagrams (continued)

Figure 12. 28-pin TSOP I (8 × 13.4 × 1.2 mm) Z28 (Standard) Package Outline, 51-85071

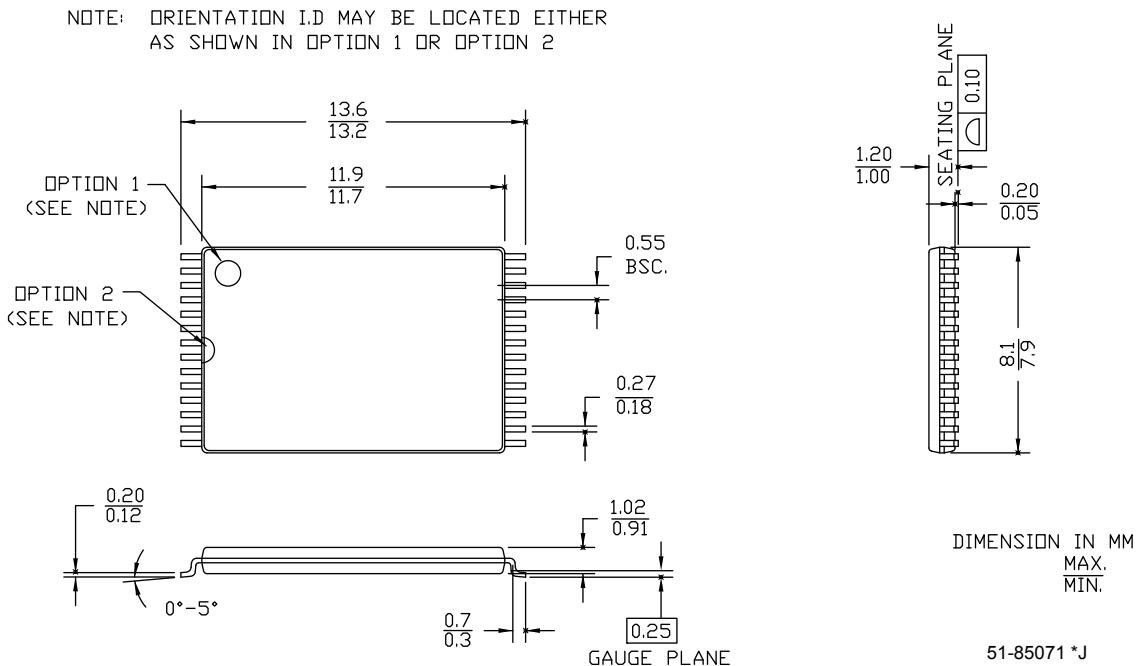
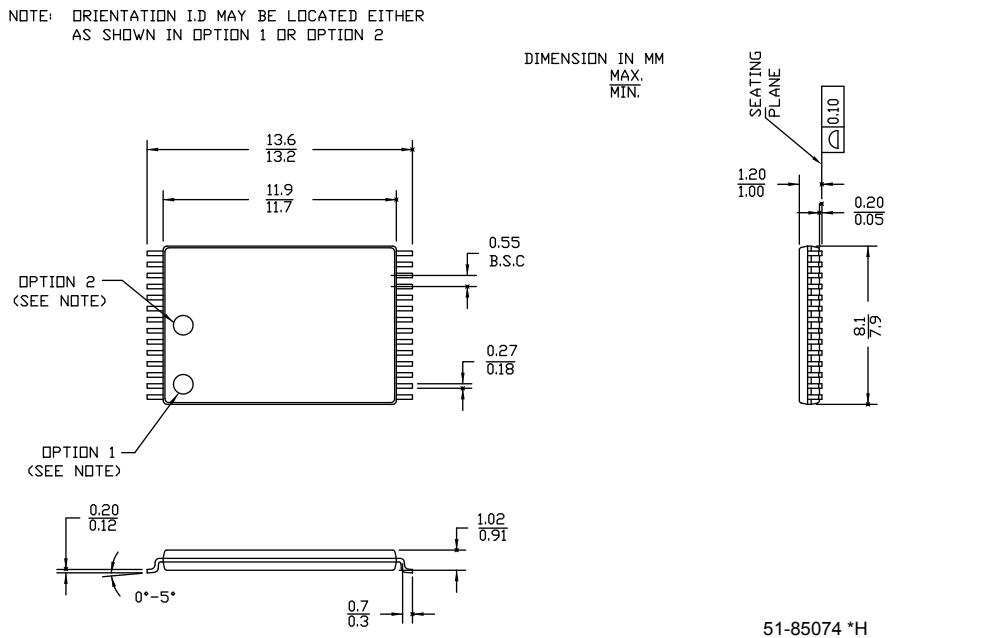


Figure 13. 28-pin TSOP I (8 × 13.4 mm) Package Outline - Reverse, 51-85074



## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
mA	milliampere
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY62256N, 256-Kbit (32 K × 8) Static RAM  
Document Number: 001-06511

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	426504	NXR	See ECN	New data sheet.
*A	488954	NXR	See ECN	Added Automotive product Updated ordering Information table
*B	2715270	VKN / AESA	06/05/2009	Updated POD of 28-Pin (600-Mil) Molded DIP package (Spec# 51-85017)
*C	2891344	VKN	03/12/2010	Added Table of Contents Removed "L" product information Updated Ordering Information table Updated Package Diagrams (Figure 10, Figure 11, and Figure 12) Updated Sales, Solutions, and Legal Information
*D	3119519	AJU	01/04/2011	Updated <a href="#">Ordering Information</a> . Added <a href="#">Ordering Code Definitions</a> .
*E	3329873	RAME	07/27/11	Updated template and styles according to current Cypress standards. Added acronyms and units. Removed reference to AN1064 SRAM system guidelines. Updated operation recovery time parameter under <a href="#">Data Retention Characteristics on page 6</a> .
*F	3433878	TAVA	11/09/11	Updated <a href="#">Package Diagrams</a> .
*G	4122787	VINI	09/13/2013	Updated <a href="#">Package Diagrams</a> : spec 51-85092 – Changed revision from *D to *E. Updated in new template. Completing Sunset Review.
*H	4525875	VINI	10/06/2014	Updated <a href="#">Maximum Ratings</a> : Referred Note 2 in "Supply voltage to ground potential (pin 28 to pin 14)". Updated <a href="#">Package Diagrams</a> : spec 51-85071 – Changed revision from *I to *J. spec 51-85074 – Changed revision from *G to *H. Completing Sunset Review.
*I	4576406	VINI	01/16/2015	Added related documentation hyperlink in page 1. Added Note 12 in <a href="#">Switching Characteristics</a> . Added note reference 12 in the <a href="#">Switching Characteristics</a> table. Added Note 20 in <a href="#">Switching Waveforms</a> . Added note reference 20 in <a href="#">Figure 9</a> . Updated <a href="#">Figure 10 in Package Diagrams</a> (spec 51-85017 *E to *F).
*J	5718683	AESATMP7	04/28/2017	Updated Cypress Logo and Copyright.

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