Homework for Module 7

1. Design a 2-stage downsampler for M=16 that minimizes the overall computation rate. Use the Parks-McClellan design algorithm for each filter stage. The requirements for the anti-aliasing filter are as follows: $\omega_p=7/8\ \pi/M$, $\omega_s=\pi/M$, $\delta_1=0.01$, $\delta_2=0.001$. Show clearly that your design meets all specifications by plotting the specification template on the frequency response graph. Compare the computation rate for the single-stage implementation with your design.
2. Determine the Type I polyphase representation for each filter stage designed in Part 1 and plot the magnitude and phase response for each polyphase section.