RedPitaya - Timing Module

Firmware

Data types

Definition: *boolean* = 1bit logical, *int* = 4byte integer, *long* = 8byte integer.
Using *int* as data type for DELAY and TIMES limits the maximal duration to little more than 3.5 minutes. Considering quasi continuous pulses, *long* is used. Since some diagnostics require arbitrarily distributed clocks the maximum number of elements the Sequence vector is maxed out to hardware constrains of the FPGA (54272 @ 40bit).

private parameters - registers

address	name	type	description
0x0000	STATUS[8]	byte	Status register stores debug and state information of the FPGA.
0x0008	INIT	bool	Used to arm the device or abort an executed program.
0x0009	TRIG	bool	Used to software trigger the device.
0x000A	CLEAR	bool	Used to clear error from the status register.
0x000B	SAVE	bool	Used to set up reinit mode.
0x000C	EXTCLK	bool	Controls clock source: 0:internal (10Mhz), 1:external.
0x000D	INVERT	byte	Stores bit information of channels that are set up for inverted output.
0x000E	GATE	byte	Stores bit information of channels that are set up for gate mode.
0x000F	GATE2	byte	Stores bit information of channels that are set up for gate2 mode.
0x0010	DELAY	long	Number of tick between the input trigger and the beginning of the first sequence.
0x0018	WIDTH	int	Number of ticks the output remains high after raised.
0x0020	PERIOD	int	Minimum number of ticks between two raising edges: 1. defines the rate of the pulse train. 2. defines when the gate closes after the last pulse.
0x0028	BURST	long	Number of pulses in a pulse train.
0x0030	CYCLE	long	Total number of ticks before the cycle repeats.
0x0038	REPEAT	int	Number of cycle repetitions.
0x003C	COUNT	int	Number of pulse trains in a sequence.
0x0040	TIMES	long[]	Increasing tick counts since cycle beginning to raising edge of the first pulse in a train.

LED and DIO connections

ribbon	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
bank	0		1		2		3		4		5		6		7	
led	*trigger*		clock		signal		gate		armed		reinit		ext_clk		error	
p(inner)	**trig**		**clk**		ch0		ch1		ch2		ch3		ch4		ch5	
n(outer)		**gnd**		**gnd**		gnd		gnd		gnd		gnd		gnd		gnd

input, output, *inverted*

Channels ch0-ch5 can be inverted or switched to gate mode using the invert() and gate() method, respectively.

Parameter contrains/defaults

These constrains should be checked against by the driver before programming.

name	constrain	default	default*
DELAY	≥ 0	0	$60,000,000$
WIDTH	≥ 1	WIDTH/2	5
PERIOD	$>$ WIDTH	10	10
BURST	≥ 0	1	0
CYCLE	$\geq$ COUNT $*$ PERIOD $*$ BURST	COUNT $*$ PERIOD $*$ BURST	0
	$\geq$ TIMES[end] + PERIOD $*$ BURST	TIMES[end] + PERIOD $*$ BURST	-
REPEAT	≥ 0	1	0
COUNT	≥ 0	1	1
	≥ 0, $\leq$ len(TIMES)	len(TIMES)	-

*) default value if nothing or only DELAY is provided, only valid for makeClock.
The remote programming is currently available via mdsip with provided tdi functions.

Methods (public methods)

makeClock (method = 'C')

The parameters DELAY, WIDTH, PERIOD, BURST, CYCLE, and REPEAT are transmitted. TIMES defaults to [0].

makeSequence (method = 'S')

The parameters DELAY, WIDTH, PERIOD, BURST, CYCLE, REPEAT, COUNT, and TIMES are transmitted.

arm (method = 'A')

INIT is set. This will cause the program to react on trig events.

disarm (method = 'D')

INIT is cleared. This will interrupt the program if running. The device is idling until the next init.

trig (method = 'T')

TRIG is set and if armed the device will start the program, i.e. software trigger.

reinit (method = 'R')

REINIT mode is set up (DELAY ≥ 0) or deactivated (-1/None).

disarm (method = 'E')

EXT_CLK is configured. This selects between internal 10MHz (0) and external (1) clock.

gate (method = 'G')

GATE is configured as bit register controlling the output channels whether to be in signal (0) or gate (1) mode.

gate2 (method = 'H')

GATE2 is configured as bit register controlling the output channels whether to be in signal (0) or gate2 (1) mode.

invert (method = 'I')

INVERT is configured as bit register controlling the output channels whether to be in normal (0) or inverted (1) mode.

state (method = 's')

Requests the current state of the device.

params (method = 'p')

Requests the parameters the device is currently configured with.

error (method = 'e')

Requests the error/message string.

Timing

The board cycle can be synchronized to an external clock or will use its internal 10Mhz clock. The jitter is minimal. The timestamps of the TTLs can be calculate with little uncertainty based on the clock. The uncertainty is mainly influenced by the quality of edge of the pulse.

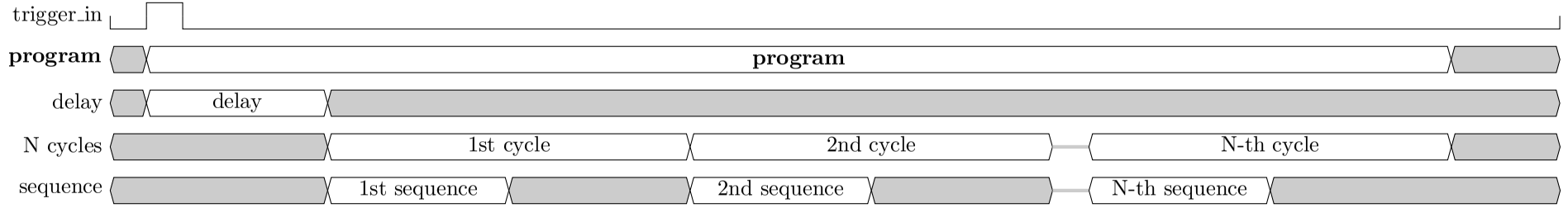
Trigger schema in reinit mode

At W7X there will be a trigger $T_0 = -60$s before the experiment starts at $T_1 = 0$s. This trigger will engage the initialization of all diagnostics as well as the timing module. In order to supports output signals even seconds before T_1 it is required to trigger the timing module with T_0. In reinit mode the triggered module enters the delay phase set to 60s. During the delay phase the module accepts a reconfiguration (makeClock, makeSequence) without loosing track of the tick count with respect to T_0. The updated delay and timing configuration are used for the rest of the program. If the device is not configured before the end of delay, it returns to armed state without generating any pulse.

Timing

Program

A program contains the list of strictly monotonic increasing tick counts relative to the trigger input for all pulses that will be generated when a trigger arrives. It is the lowest level of control. A program can be compiled as a initial DELAY and REPEAT identical, subsequent cycles.

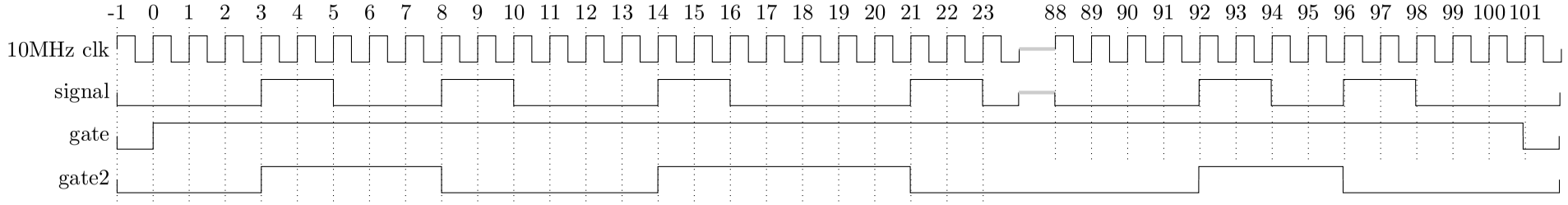


Cycle

During every cycle a digital signal is generated. A gate signal will be high during the sequence and low during idle time. The duration of one cycle is defined by CYCLE and controls the repetition rate.

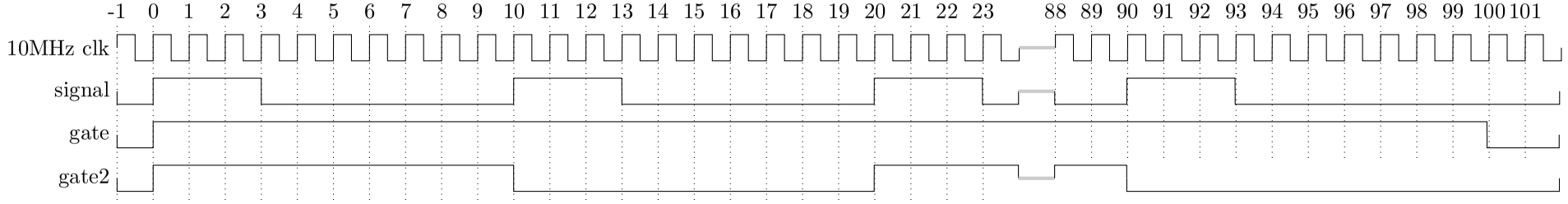
Sequence $(\mathrm{WIDTH} = 2, \mathrm{PERIOD} = 5, \mathrm{TIMES} = [3, 8, 14, 21, \cdots, 92, 96])$, makeSequence

The digital signal is generated as a sequence of pulses of a given WIDTH. The timing of the pulses is defined by TIMES that contains tick counts relative to the beginning of the cycle. The low-high transition of the gate is defined by the beginning of the cycle. The high-low transition is defined by the last element of TIMES plus PERIOD.



Pulse train $(\mathrm{WIDTH} = 3, \mathrm{PERIOD} = 10, \mathrm{BURST} = 10)$, makeClock

In pulse train mode the parameter PERIOD and BURST are used generate a sequence of equidistant pulses. TIMES = [0]



Samples

Simple sample to test-trigger a RedPitaya from within python

```
from LocalDevices.w7x_timing import remote
rp = remote('10.44.2.122')
# MAKE CLOCK: DELAY: 0, WIDTH: 100, PERIOD: 200, BURST: 1, CYCLE: 200, REPEAT: 1, COUNT: 1
rp.makeClock(width=100)  # single 10us pulse
rp.arm()                 # arms the device
rp.trig()                # simulates a trigger input to the device
```