



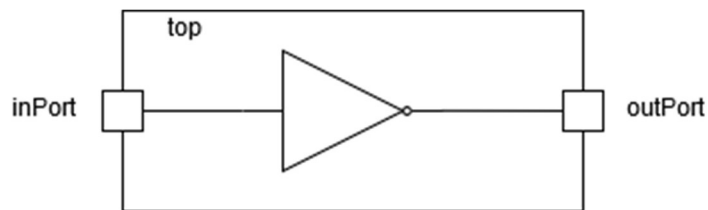
Quick Start Quartus

Write A VHDL Design



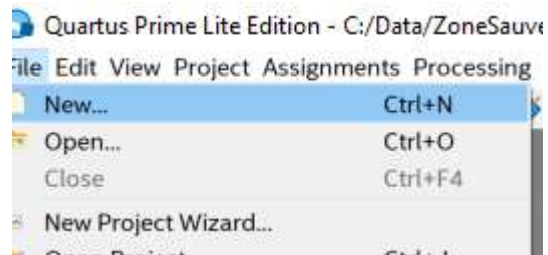
Create a VHDL file:

We want to create this design:



There is one input "inPort" and one output "outPort". outPort is connected to the output of an inverter which is connected to inPort. So we can say : outPort = NOT inPort.

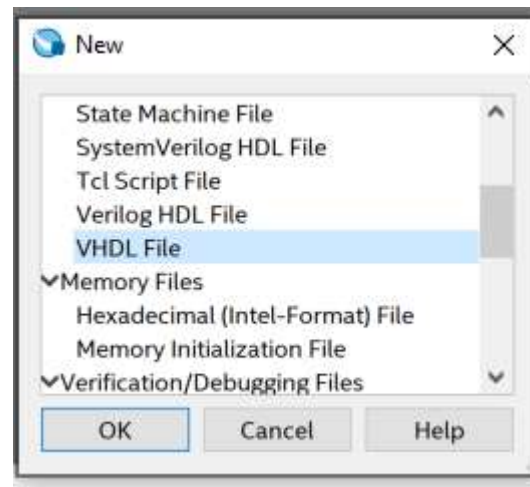
This design is called "top". The design name will be used for the entity name.



Select "File->New"

Select "VHDL File"

Click "OK"



```

1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.NUMERIC_STD.ALL;
4
5 entity top is
6     Port (
7         inPort : in  STD_LOGIC;
8         outPort : out STD_LOGIC );
9 end top;
10
11 architecture vhd1 of top is
12 begin
13
14     outPort <= not inPort;
15
16 end vhd1;

```

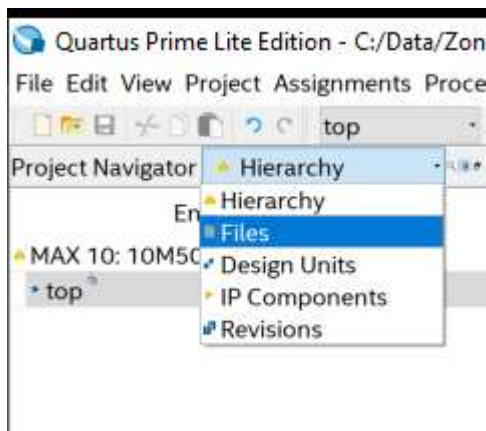
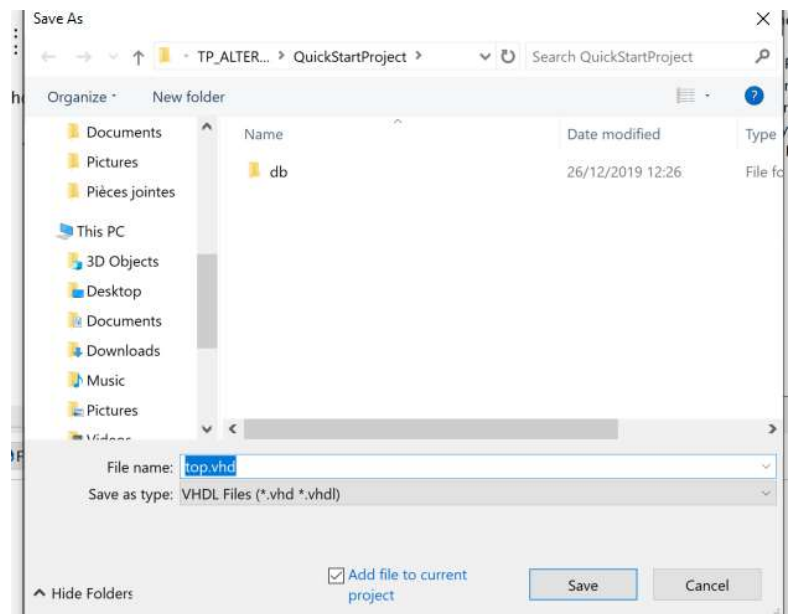
An editor will be opened.

Write the code of the design.

And save (disk icon or ctrl-s)

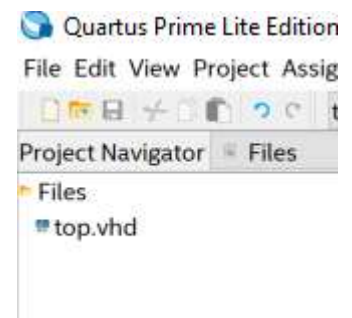
It will open a save window. Save your file as **top.vhd**.

Click “Save”



Choose “Files” in the design window.

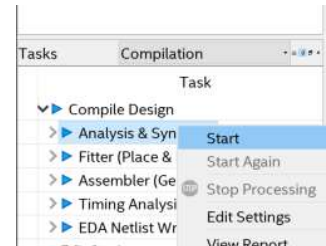
You should see your file.



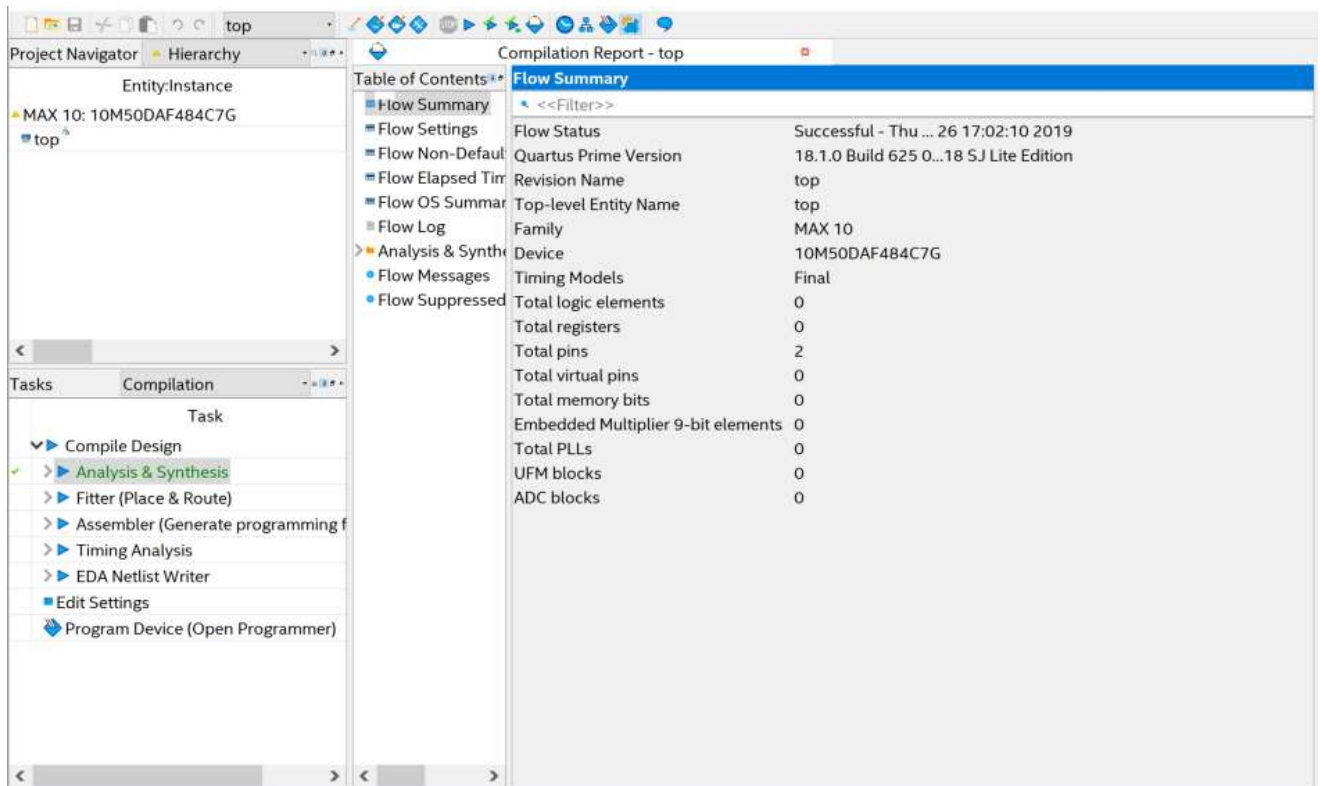
Verify the design.

In order to verify the code we run a Synthesis.

Right click on “Analysis & Synthesis” and select “Start”



If you have no error in your design you should see that:



The “Analysis & Synthesis” has turned green.

We have also a short report on the resources used by our design.

In this case it only use 2 pins (or PADs)