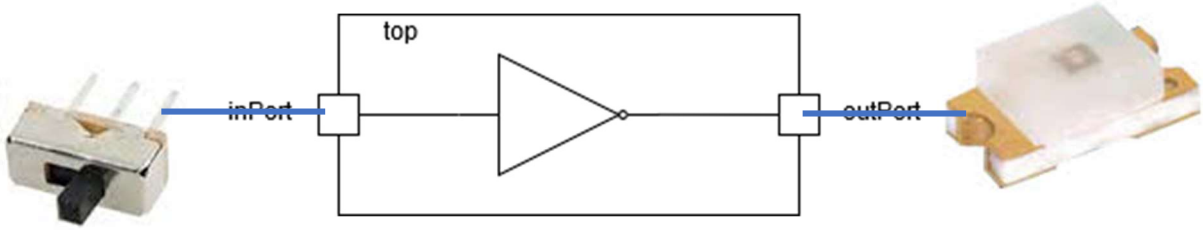
Quick Start Quartus

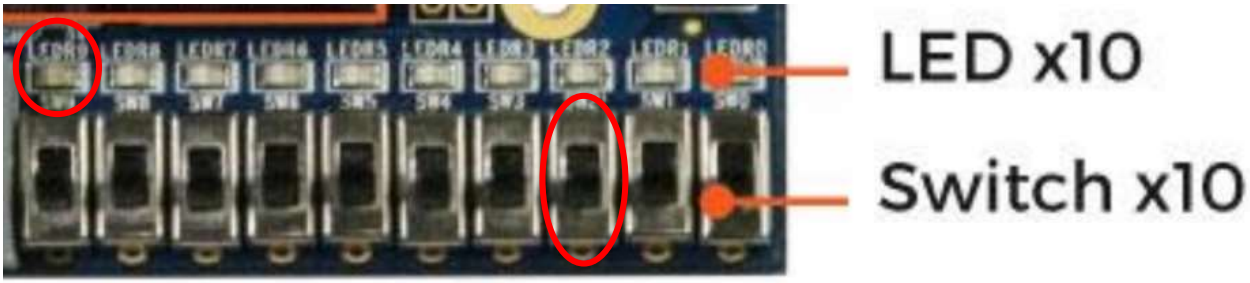
Pin Assignment

Pin Assignment :

Our design has been written and checked by simulation.

We want to connect the input on a switch (also called slide button) and the output on a LED. We must have a look to the data sheet to know how the FPGA pins are connected.





We want to connect the input on switch2 (SW2) and output on LEDR9.

The datasheet says:

“If the LEDR9 you want to use, the PIN B11 you will connect”

And if we want to use SW2 we have to connect the inPort on PIN D12.

Figure 3-15 Connections between the slide switches and MAX 10 FPGA

Table 3-4 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTL
SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTL
SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTL
SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTL
SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTL
SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTL
SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTL
SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTL
SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTL
SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTL

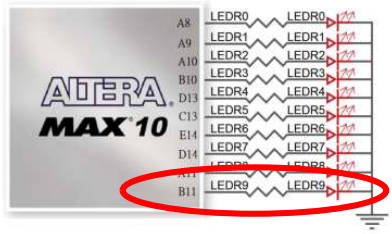
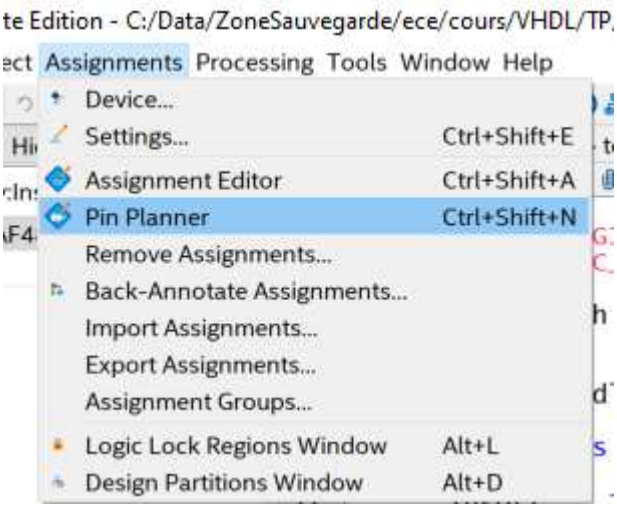


Figure 3-16 Connections between the LEDs and MAX 10 FPGA

Table 3-5 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR0	PIN_A8	LED [0]	3.3-V LVTTL
LEDR1	PIN_A9	LED [1]	3.3-V LVTTL
LEDR2	PIN_A10	LED [2]	3.3-V LVTTL
LEDR3	PIN_B10	LED [3]	3.3-V LVTTL
LEDR4	PIN_D13	LED [4]	3.3-V LVTTL
LEDR5	PIN_C13	LED [5]	3.3-V LVTTL
LEDR6	PIN_E14	LED [6]	3.3-V LVTTL
LEDR7	PIN_D14	LED [7]	3.3-V LVTTL
LEDR8	PIN_A11	LED [8]	3.3-V LVTTL
LEDR9	PIN_B11	LED [9]	3.3-V LVTTL



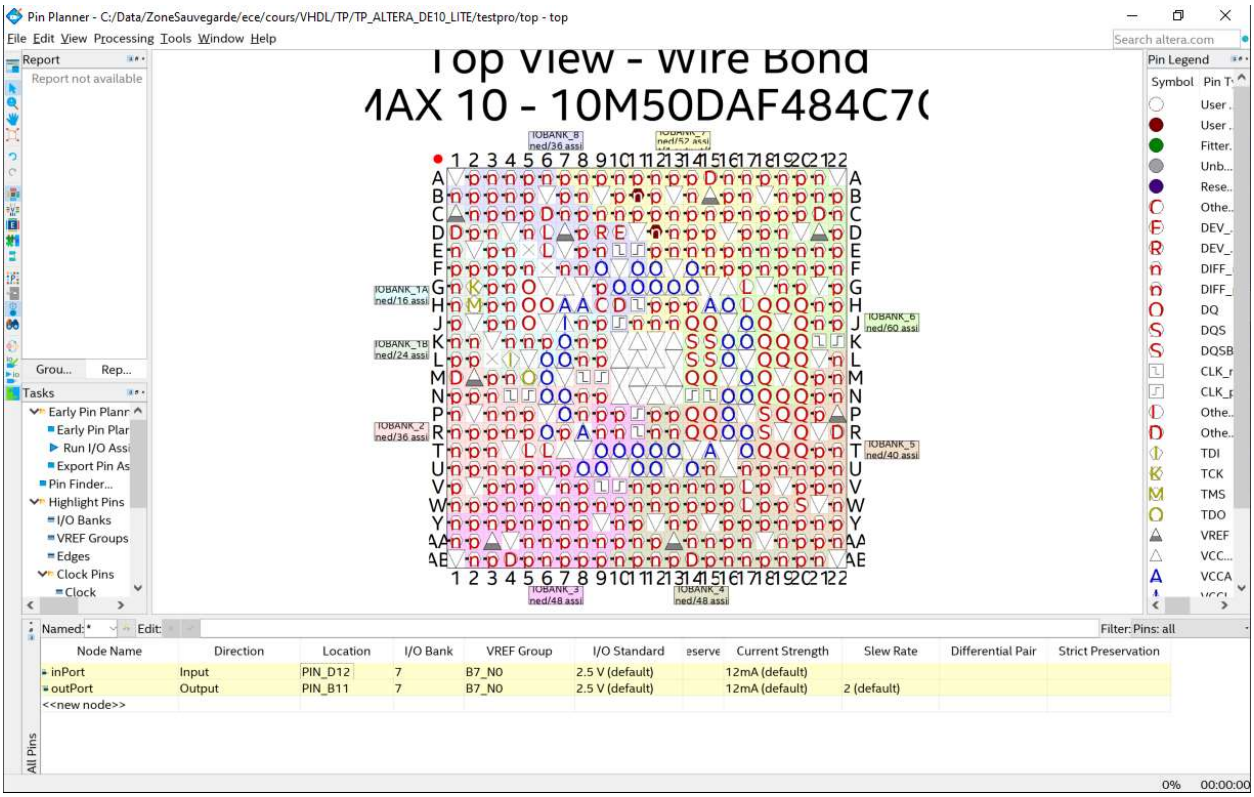
Select “Assignments -> Pin Planner”

A new window will open. This tool allows to see where we are affecting the pins. In our case it is not too important. The main reason to use this tool is to assign a specific pin to a port.

inPort will be connected to the pin location “PIN_D12”. The routing of the DE10 board connects the PIN_D12 to the slide switch.

outPort will be connected to the pin location “PIN_B11”.

You have to edit the location field of inPort and outPort.



Once the location filled, click somewhere else in the window in order to record your choice.

You can close this window. A file has been modified with your choice : top.qsf

You can open it and verify if your choice has been taken into account. You should see somewhere in the file :

set_instance_assignment -name PARTITION_HIERARCHY root_partition -to | -section_id Top

set_location_assignment PIN_D12 -to inPort

set_location_assignment PIN_B11 -to outPort