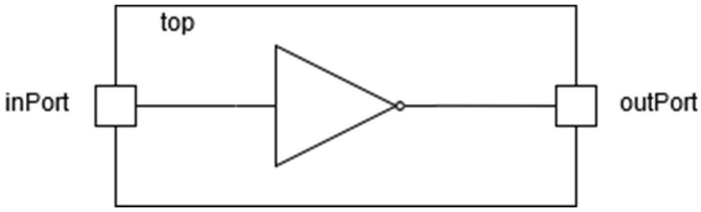
Quick Start Quartus

Write A VHDL Design

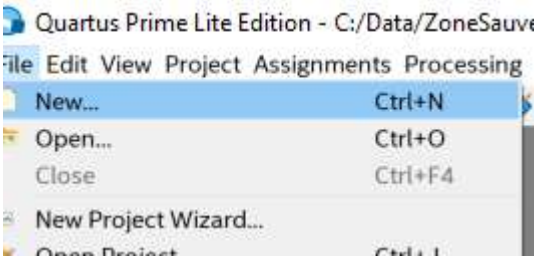
Create a VHDL file:

We want to create this design:

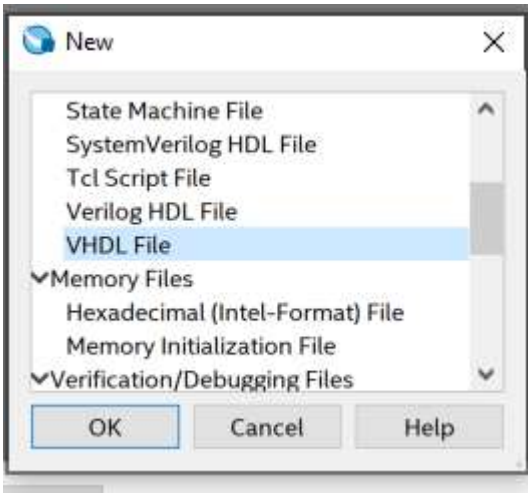


There is one input “inPort” and one output “outPort”. outPort is connected to the output of an inverter wich is connected to inPort. So we can say : outPort = NOT inPort.

This design is called “top”. The design name will be used for the entity name.

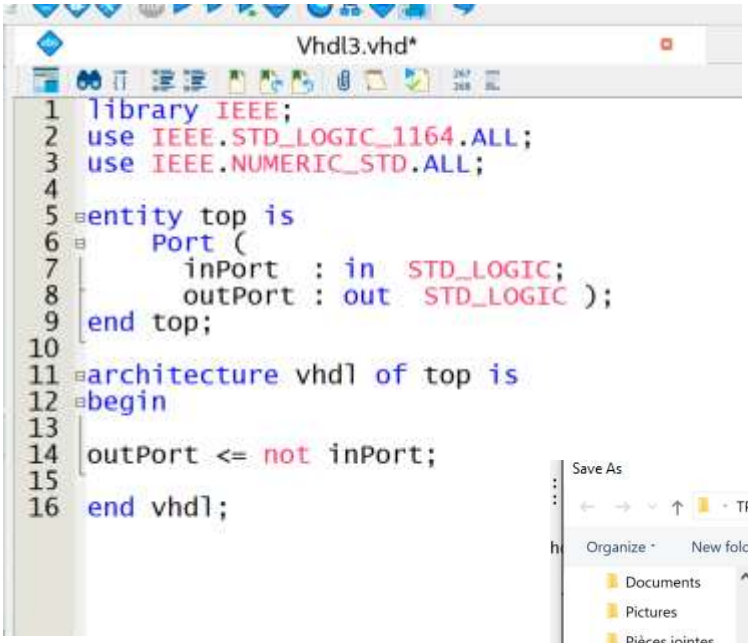


Select “File->New”



Select “VHDL File”

Click “OK”



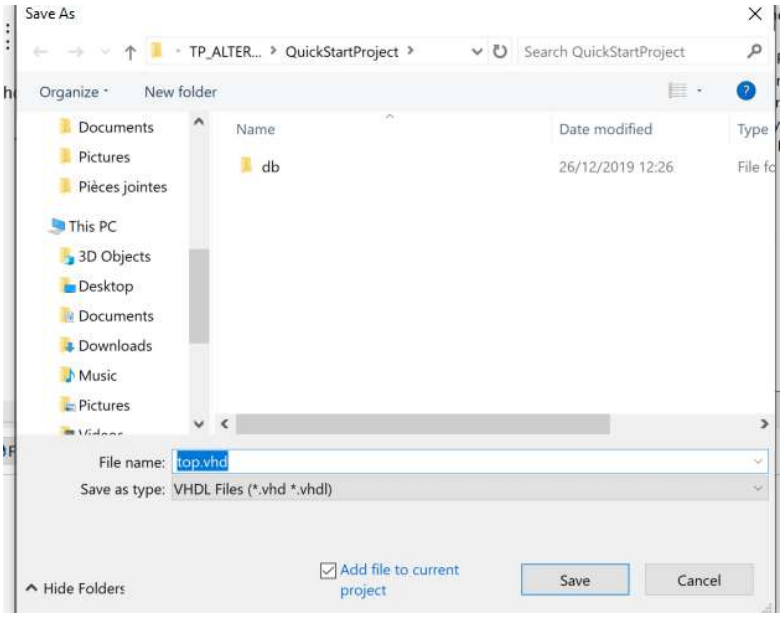
An editor will be opened.

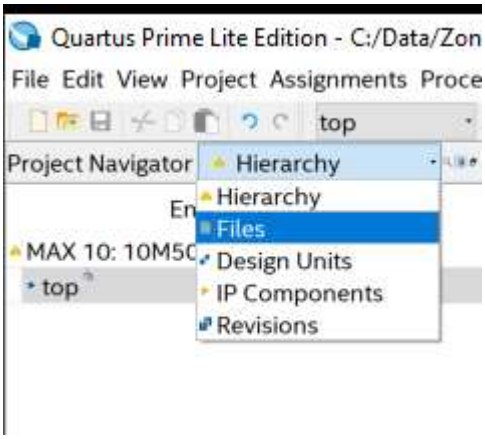
Write the code of the design.

And save (disk icon or ctrl-s)

It will open a save window. Save your file as top.vhd.

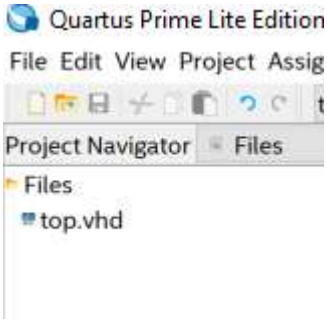
Click “Save”





Choose “Files” in the design window.

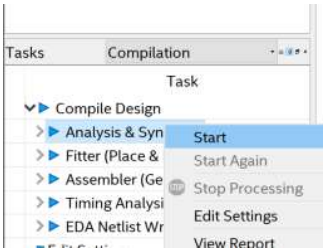
You should see your file.



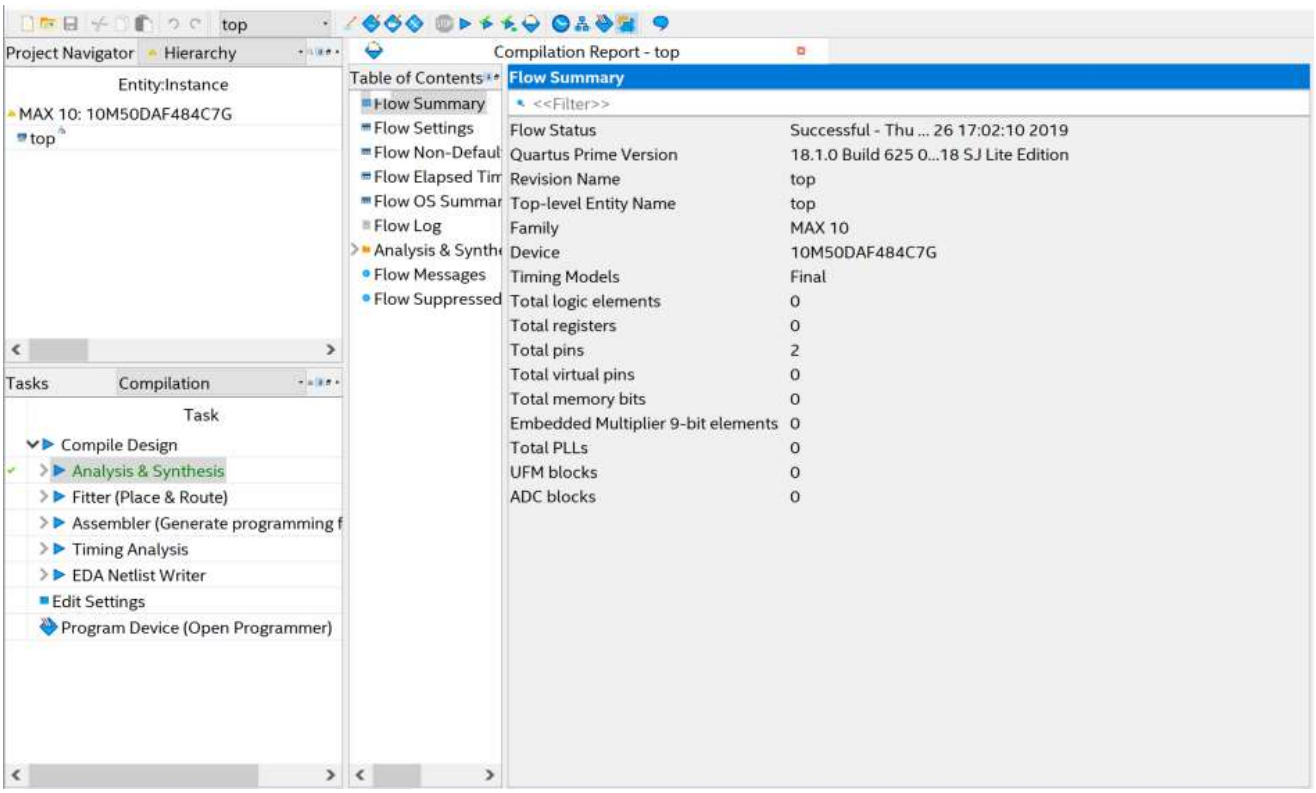
Verify the design.

In order to verify the code we run a Synthesis.

Right click on “Analysis & Synthesis” and select “Start”



If you have no error in your design you should see that:



The “Analysis & Synthesis” has turned green.

We have also a short report on the resources used by our design.

In this case it only use 2 pins (or PADs)