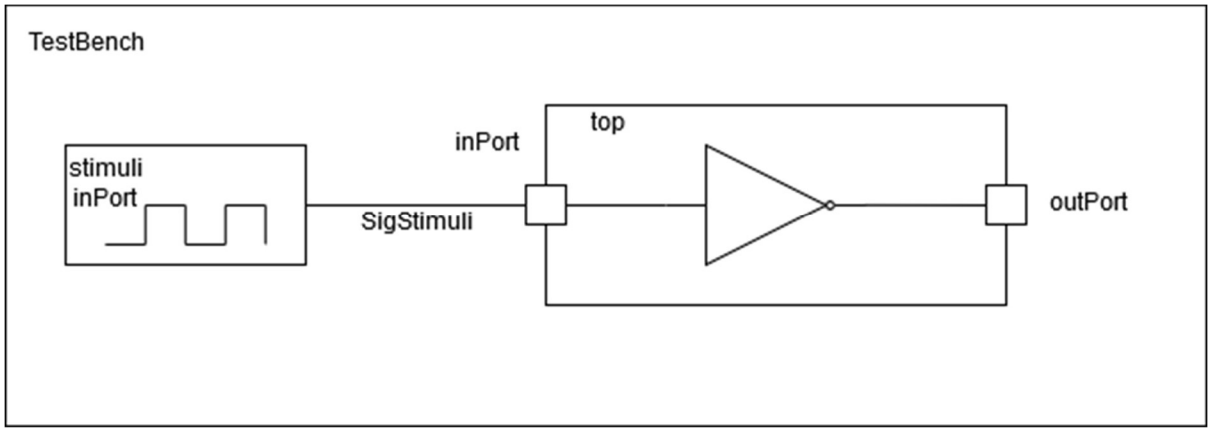
Quick Start Quartus

Write A VHDL Design

Create a Test Bench :

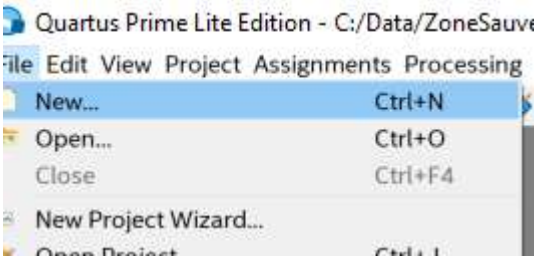
The Test Bench is used to verify the behavior of a design by using a VHDL simulator.

In our case the design is “top”. It has one input and one output. To verify its behavior we are going to generate some signals (called stimuli or test vectors) on the input and , with the help of the VHDL simulator, we will verify the output.

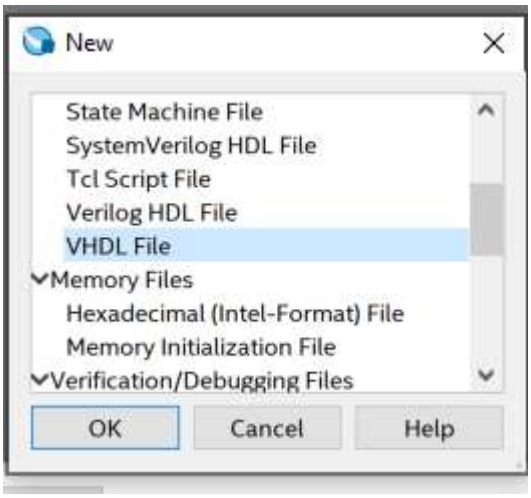


There is one input “inPort” and one output “outPort”. outPort is connected to the output of an inverter wich is connected to inPort. So we can say : outPort = NOT inPort.

This design is called “top”. The design name will be used for the entity name.

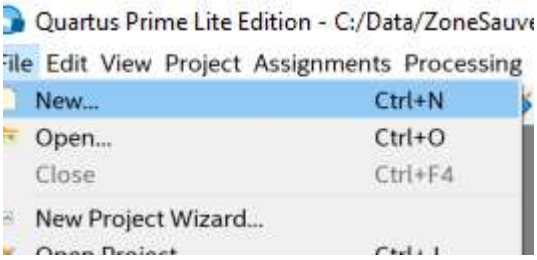


Select “File->New”

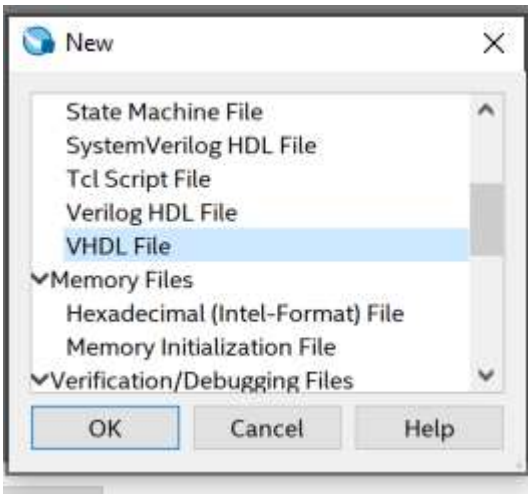


Select “VHDL File”

Click “OK”



Select “File->New”



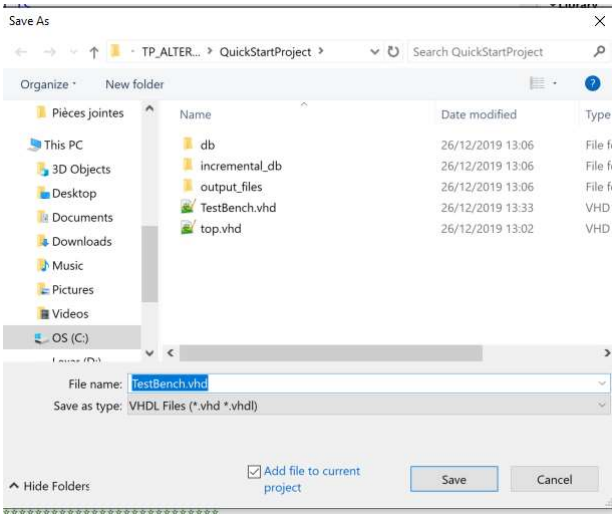
Select “VHDL File”

Click “OK”

top.vhd | Vhdl4.vhd*

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.NUMERIC_STD.ALL;
4
5  entity TestBench is
6  end
7
8  architecture vhdl of TestBench is
9
10 component top is
11     Port (
12       inPort  : in  STD_LOGIC;
13       outPort : out  STD_LOGIC );
14 end component;
15
16 signal SigStimuli : std_logic;
17
18 begin
19
20 -- create stimuli (or test vectors) for all inputs
21 stimuli_inport : process
22    SigStimuli <= '0';
23    wait for 100ns;
24    SigStimuli <= '1';
25    wait for 100ns;
26 end process;
27
28 -- use structural view (port map) to instanciate the "top" entity
29 -- connect the input "inPort" on the stimuli signal "SigStimuli"
30 i1 : top port map ( inPort => SigStimuli );
31
32
33 end vhdl;
```

Copy this code and try to understand what it means.



Save it as “TestBench.vhd”.

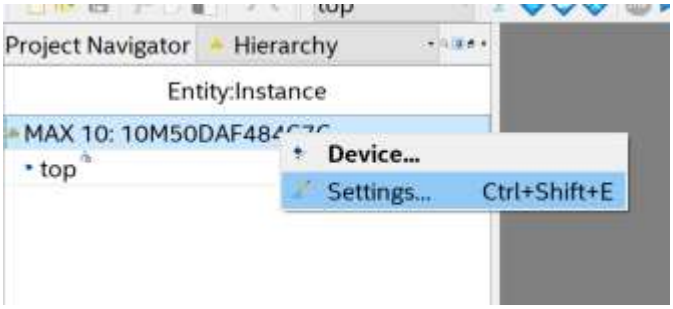
Beware of case : it is case sensitive!

Configure Tool :

The Simulation tool “ModelSim Altera” is launch from Quartus. In order to correctly Run the simulator we have to configure some parameters in Quartus.

TestBench configuration:

First we have to set the TestBench name of our design. In our case the test bench entity name is “TestBench” and is written in “TestBench.vhd” (take care of cases!)

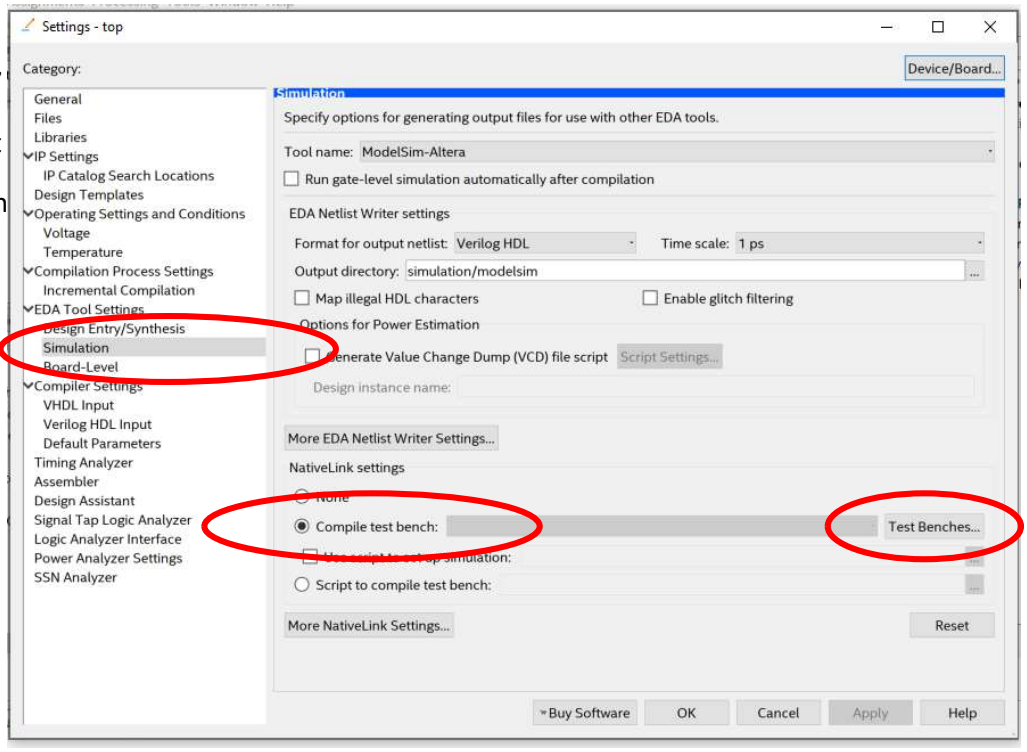


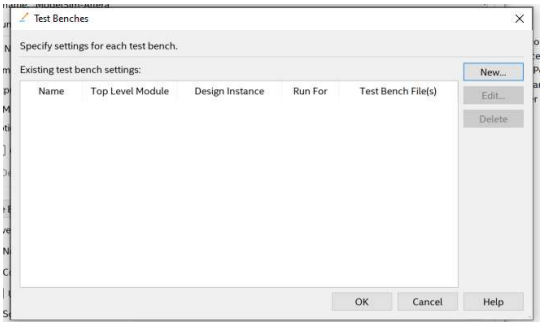
Right Click on device name and select “Settings…”

Select “Simulation”

Select Compile test

Click on “TestBench





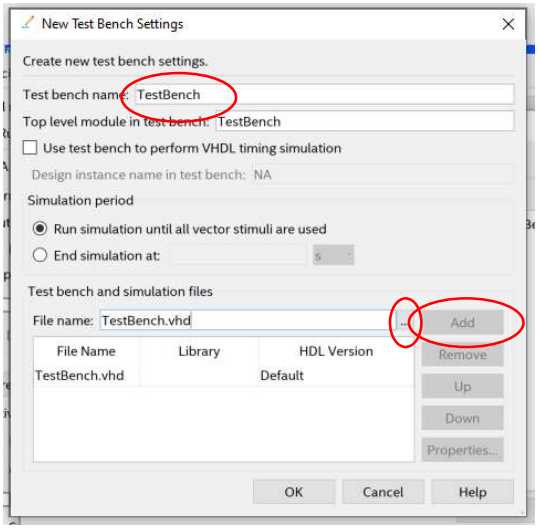
Click “New”

Write “TestBench” in “test bench name”. This the name of your test bench entity.

Click “…” in File name and seach for your test bench VHDL file.

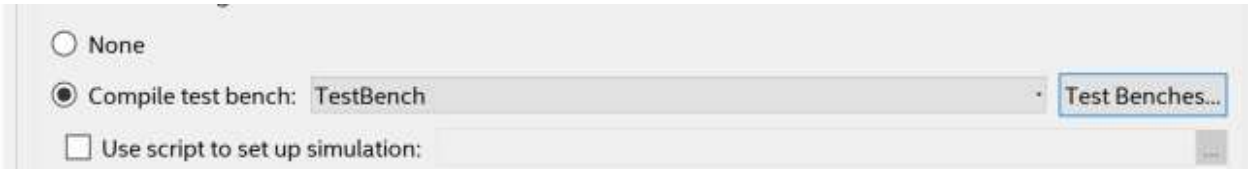
Then click “Add”

And click “OK”



Click “OK” another time for the parent window (“specify settings…”).

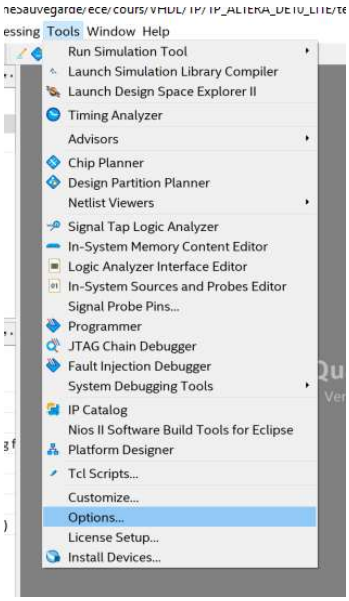
You should see “TestBench” in the settings window:



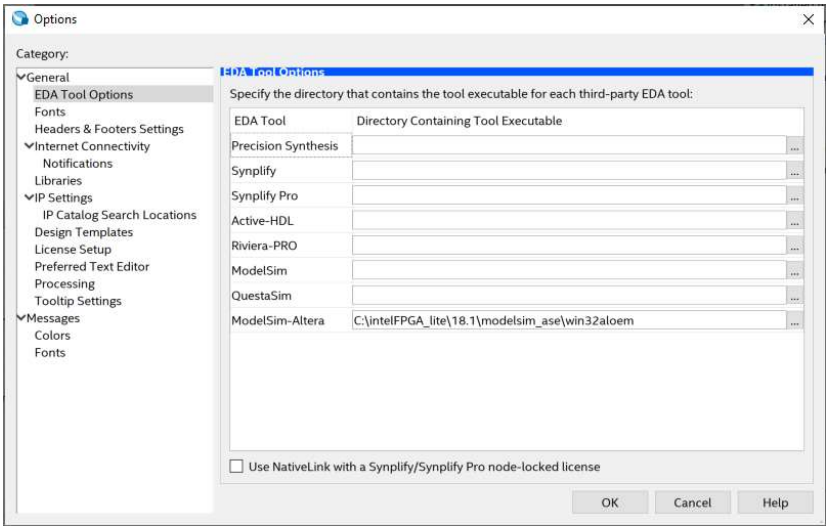
Click “OK”.

Executable configuration

ModelSim is an independent simulator and your are not forced to use the one provided with Quartus. So you can configure the path to the ModelSim executable. By default this path is empty and we have to set it to the ModelSim provided with Quartus.



Select “Tools -> Options…”



Select EDA Tool Options

Set the path of “ModelSim-Altera” where ModelSim.exe can be found.

In this case it is:

C:\intelFPGA_lite\18.1\modelsim_ase\win32aloem

Click “OK”