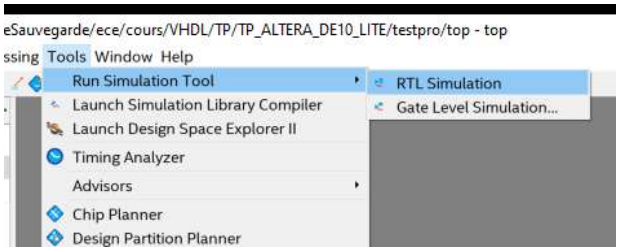
Quick Start Quartus

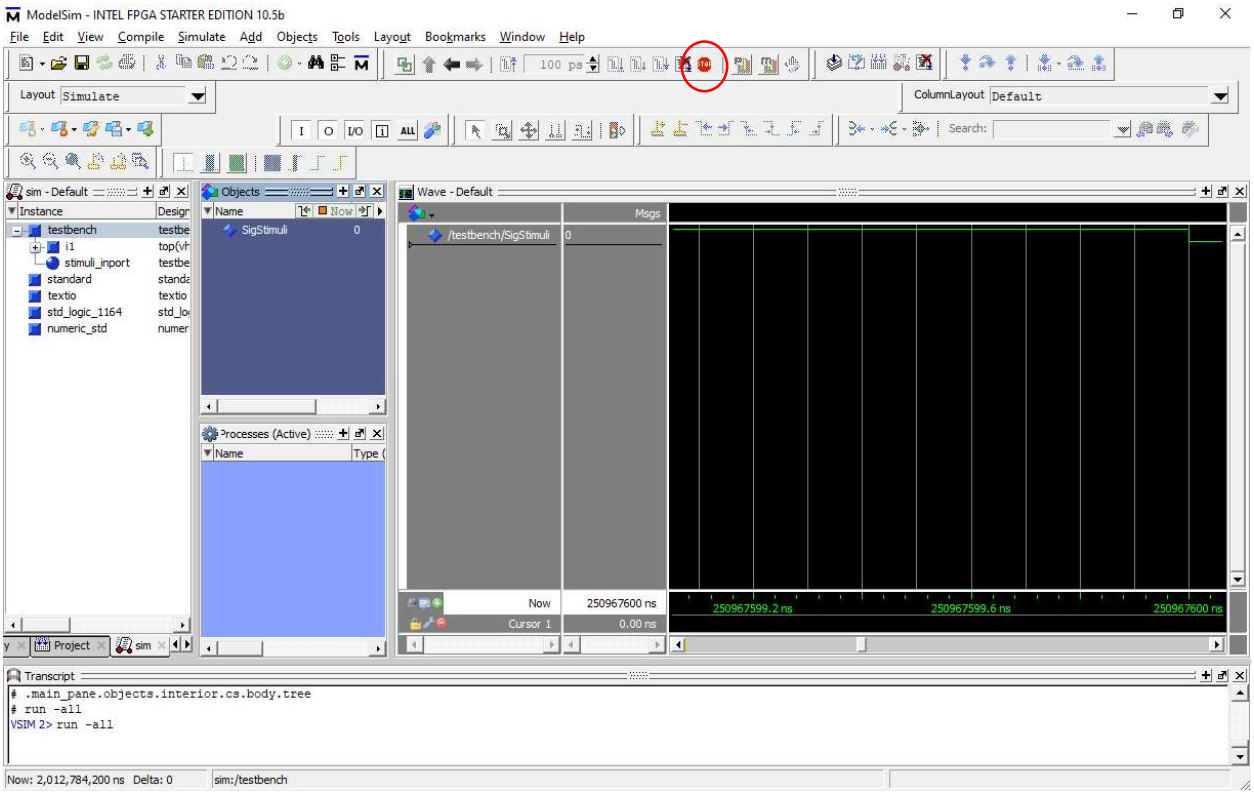
Simulation

Simulation :

Now Quartus is configured to launch the VHDL simulator “ModelSim”.



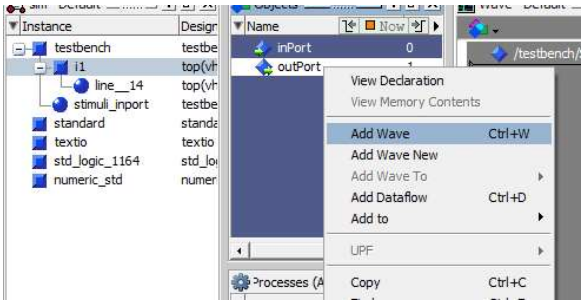
Select “Tools -> Run Simulation Tool -> RTL Simulation”



A new window is opened with ModelSim.

First click on “Stop” because ModelSim is already simulating the design.

In the “Wave” window we only see the “SigStimuli” signal. We have programmed this signal to repeat periodically 10101010… in order to check the behavior of the output. So we have to add the output “outPort” to the “Wave” window.



Select “i1” which is the name of the top instance in the test bench. Remember:

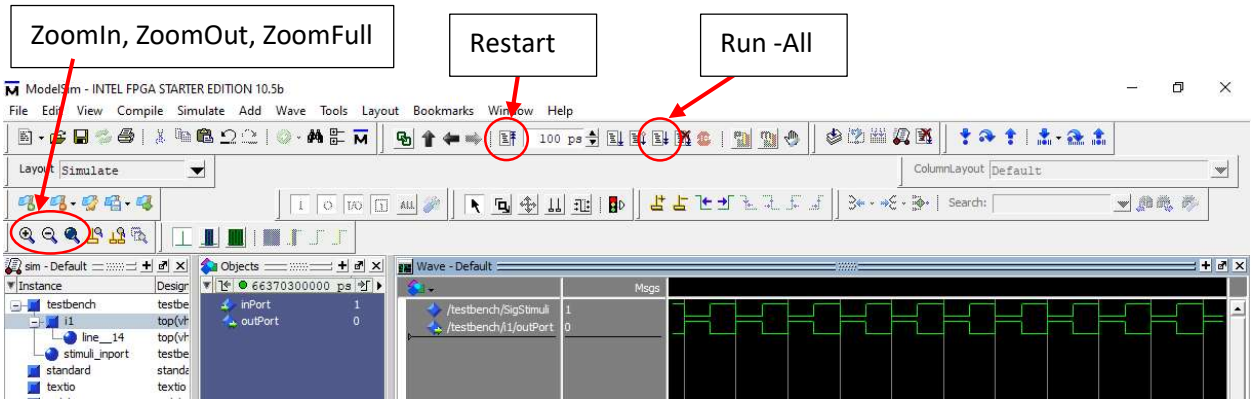
i1 : top port map (inPort => SigStimuli);

It then display the available signals in i1 : “inPort” and “outPort”.

Right click on outPort and select Add Wave.

outPort will be now displayed in the “Wave” window.

We have to restart the simulation with “outPort”.



Click on “Restart” icon. The simulator reset the simulation.

Click on “Run -All” icon . The simulator run the simulation.

Click on “Stop” icon. The simulator stop the simulation.

You should see the output “outPort” in the wave window. The zoom is too strong, you have to zoomout by clicking several times on the ZoomOut icon. Some waves should appear in the “Wave” window. We can now check the behavior of “outPort”.