# Quick Start Quartus

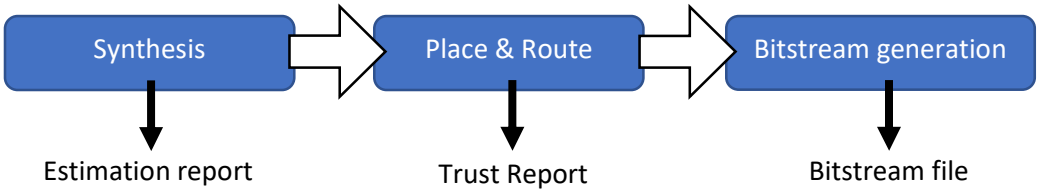
## Synthesis
## Place & Route


### Synthesis :

We have:

- Written our design
- Simulated and validated the behavior of the design
- Set the pin assignment

It's time to compute the configuration of the FPGA. Nothing to do, everything is automatic. Several tools are going to work to find the best configuration for the FPGA to implement your design.

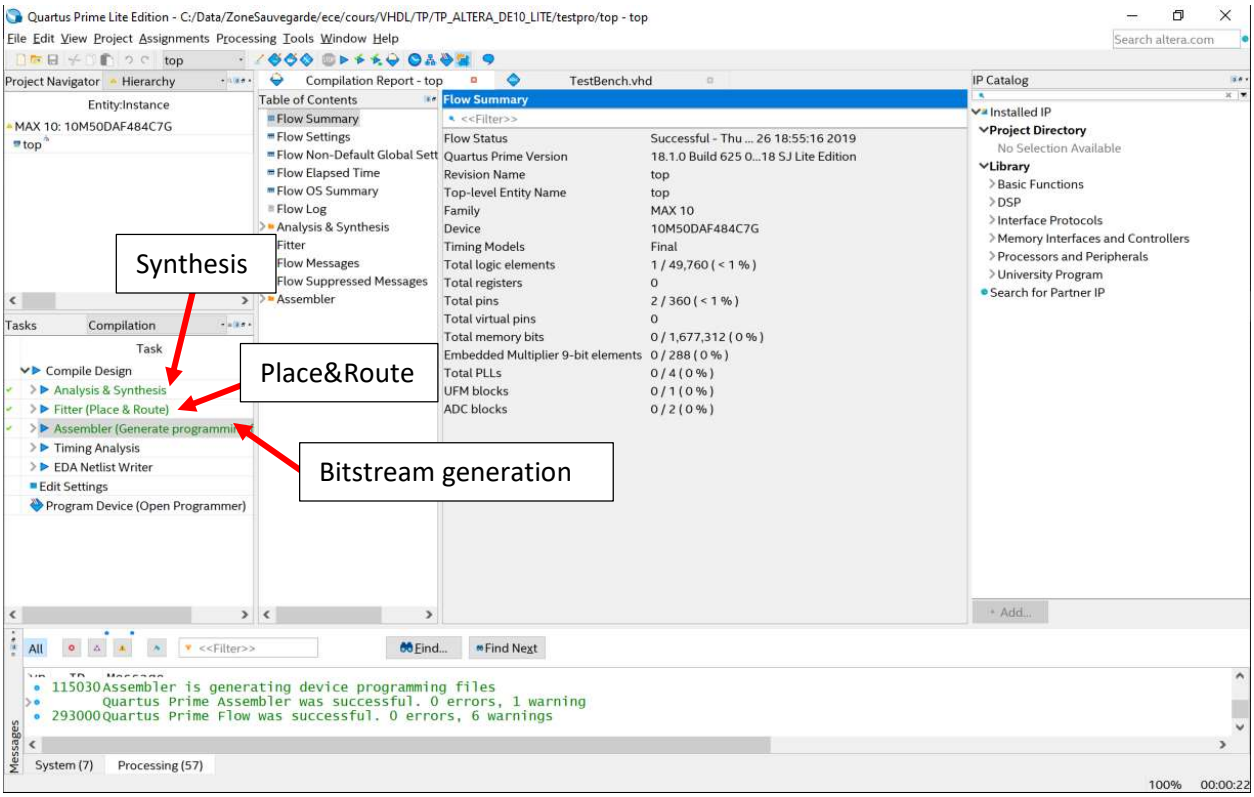



The synthesis will convert your VHDL description into a netlist of logic gates (RTL Level). This step gives a first estimation report which doesn't take into account specific mapping and routing.

The Place&Route Tool will "map" the netlist into the FPGA. "map" means find(place) the programmable logic blocks and route them. This step give a final report. The main features to take care is the occupation: size of your design in the FPGA (100% = FPGA full), and the maximum clock frequency.

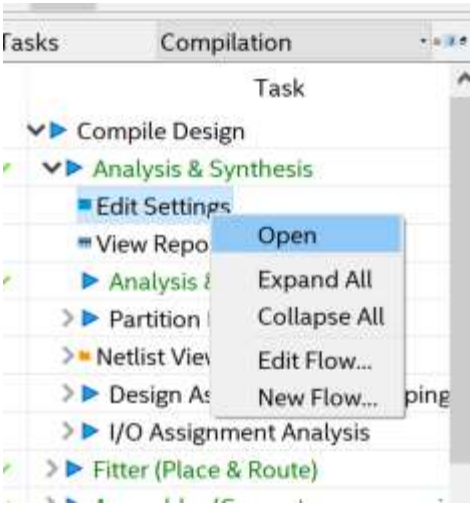
Synthesis and Place&Route steps can take a lot of time.

Bitstream generation is most simple and consist to convert the internal database into an uploadable stream of bit into the FPGA.




Just before launching the Synthesis we must change a parameter of the Synthesis tool.

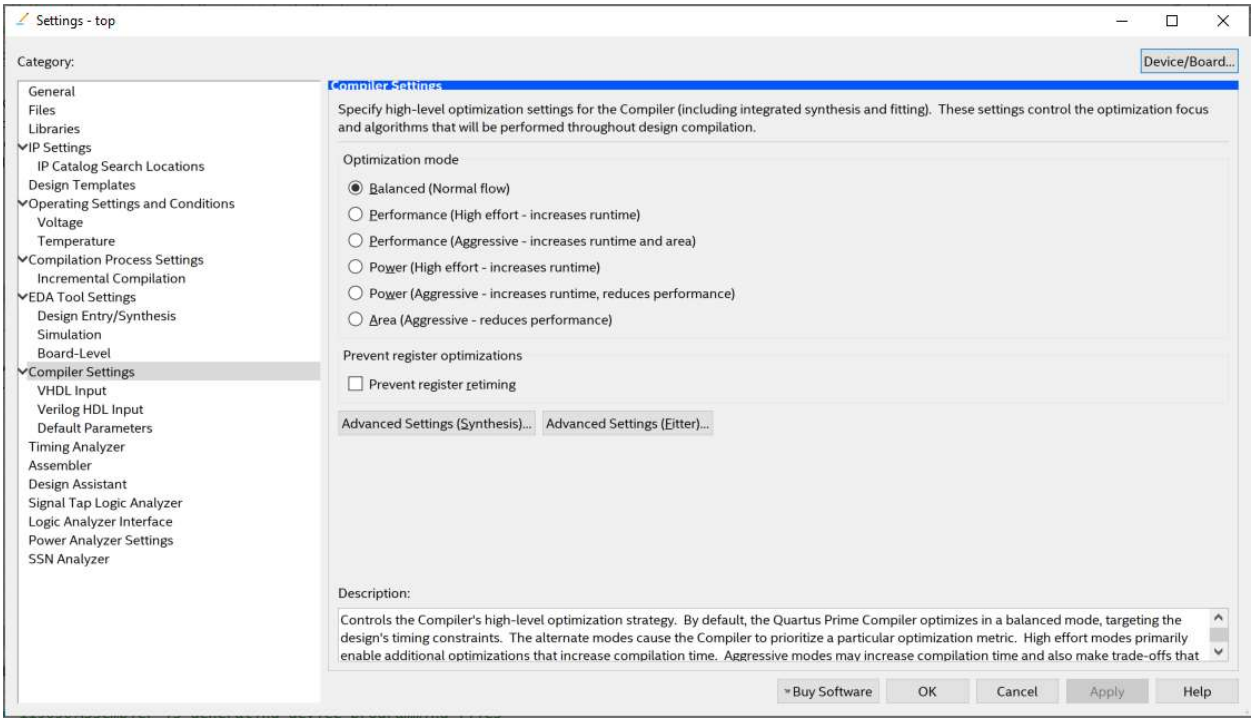
This operation must be done only one time by project.




Open the “Analysis & Synthesis”

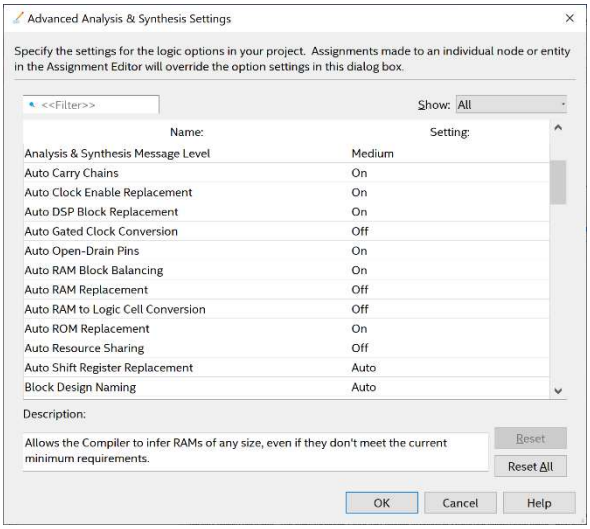
Right click on “Edit settings”

Click “Open”




Select “Compiler Settings”

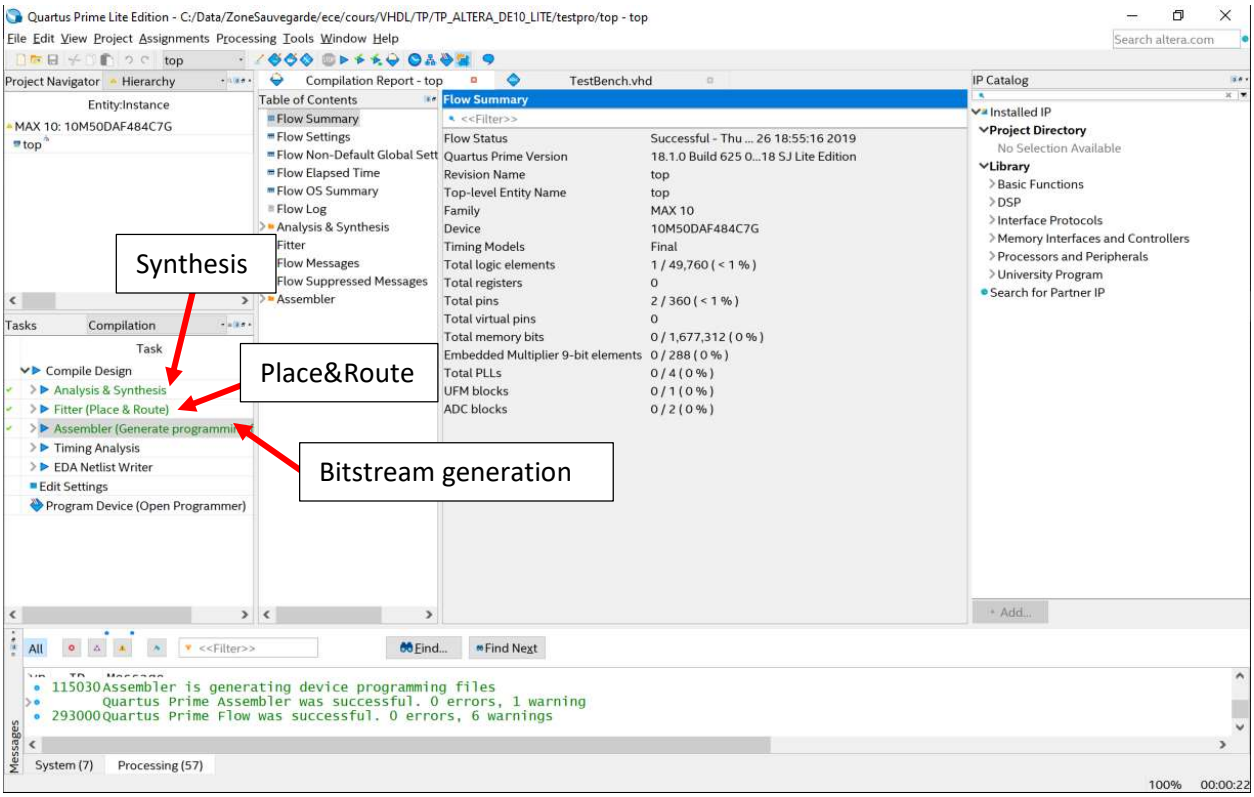
Click on “Advanced Settings (Synthesis)…”




Search the “Auto RAM Replacement” and set it to “Off”

Click “OK”

Click “OK”




Double click on the corresponding tool to run it.

When the Place&Route is finished, a short report is given. In our case we take 1 logic block from 49760 (it remains some place…).

To get the clock frequency : open the “Timing Analysis” tool and double click on view report. Our design is to simple to give a timing report.