CSCE 3953 System Synthesis and Modeling

Project 3: Design and Simulate Combinational Logic in Verilog

Instructor: Dr. Jia Di

Objectives and Tasks

- Objective – design and simulate combinational logic circuits using Verilog

- Solve Problem 14 on textbook Page 139 (old text book Page 141)
  - Count and output the number of 1's in a parallel 8-bit input
- Implement your solution in Verilog
- Either write a testbench or a .DO file
- Simulate the designed circuit in ModelSim for ***ALL*** possible input patterns

Report

- Project objective
- Design methodology / circuit diagram
- Simulation method
- Result (simulation waveform screenshot)
- Analysis and conclusion
- Source code (design file, testbench / .DO file)
- **Include your name in the report file name**
- Due date: September 23 before class, email your report to jdi@uark.edu in either Word or PDF format