CSCE 3953 System Synthesis and Modeling

# Project 6: Finite State Machine

**Instructor: Dr. Jia Di**

# Objective

- Design FSM for a race light controller
- There are three inputs: ***Reset***, ***Start***, and ***Clock***. There are three outputs: ***Red***, ***Yellow***, and ***Green***, which turn on the lights. Only one light can be on at any time. The ***Reset*** signal forces the circuit into a state in which the red light is turned on. When the ***Start*** signal is activated, the red light stays on for at least three clock cycles, then the yellow light is turned on. The yellow light stays on about three clock cycles and then the green light is turned on. The green light stays on for at least three clock cycles and then the red light is turned on and the circuit returns to its reset state.
- Write Verilog code to implement this FSM
- Simulate it in Modelsim using a testbench showing the whole process
- Synthesize the Verilog code in Design Vision
- Simulate the synthesized code in the same manner
- Make your own assumptions

# Report

- Project objective
- Design methodology / STG
- Simulation method
- Result (simulation waveform screenshot)
- Analysis and conclusion
- Source code (design file and testbench)

- Due date: October 19 before class, email your report to jdi@uark.edu in either Word or PDF format