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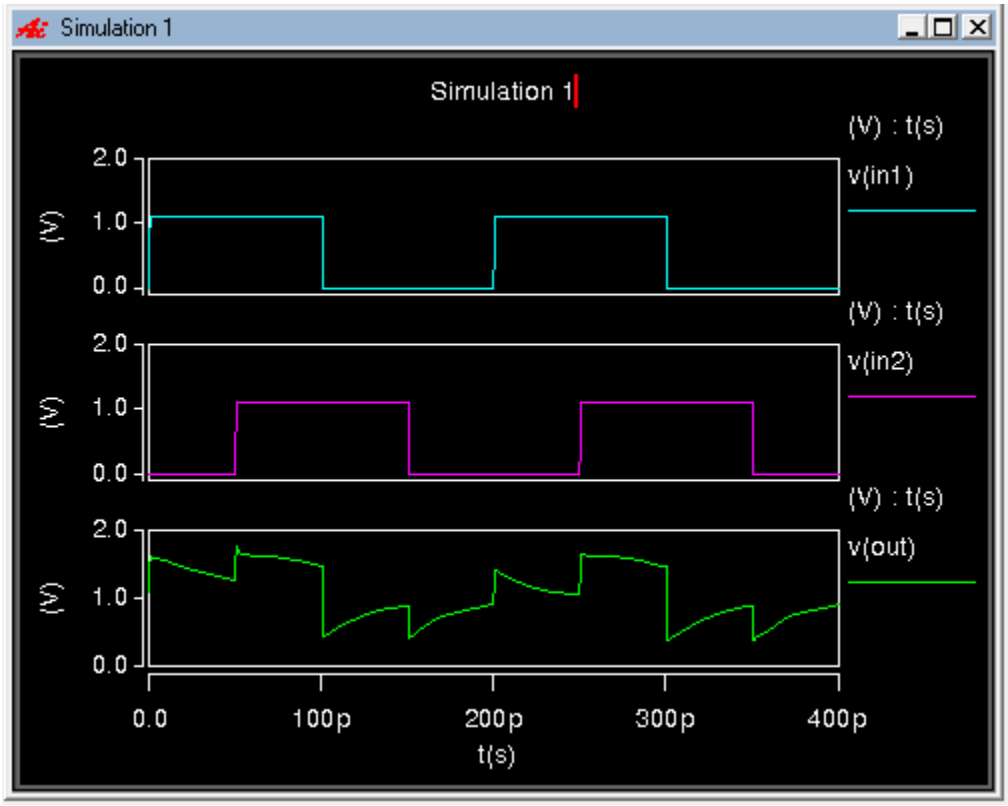
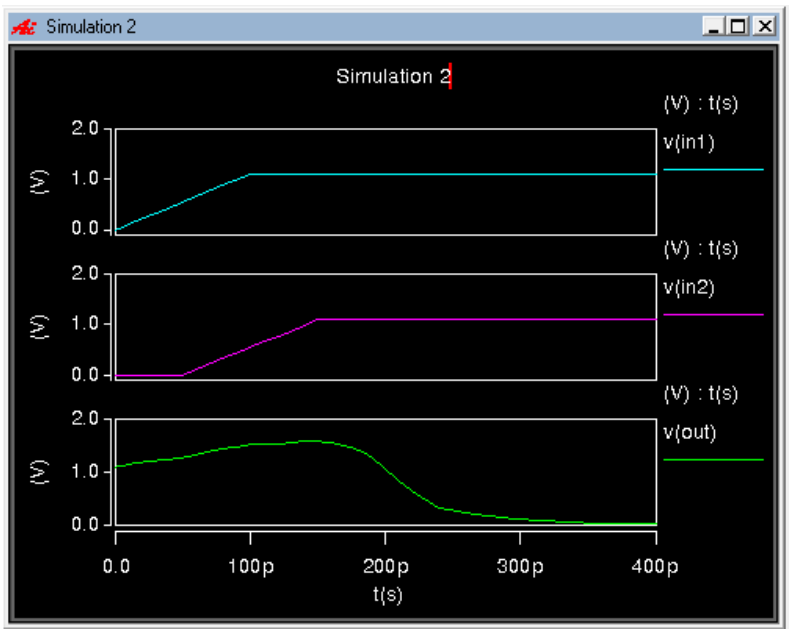
Advanced Digital Design

Lab 1 Report

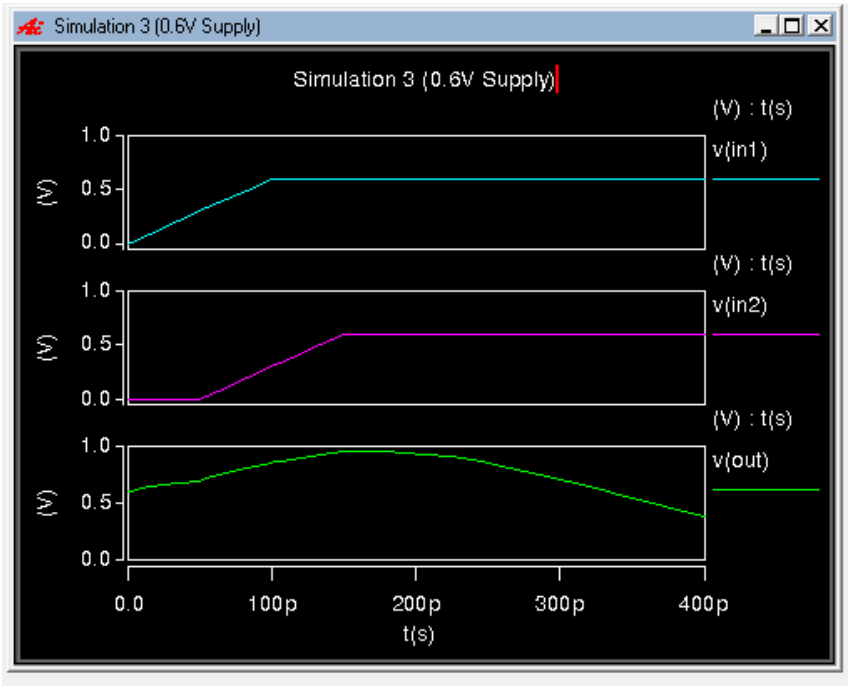
Simulation Waveforms



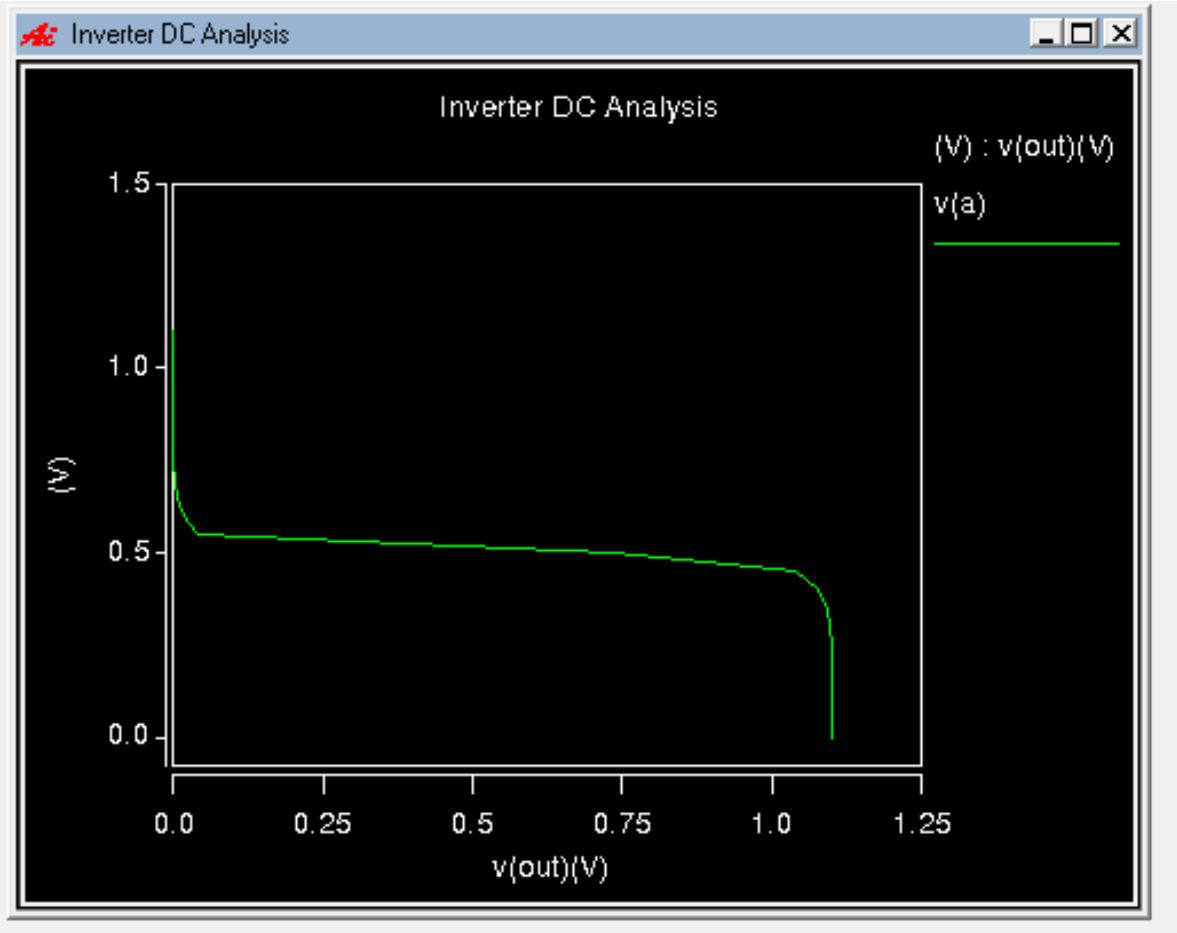
This first simulation waveform is of the NAND2 gate designed in HSPICE. It can be seen that both input signals have a 0ps rise time and a 0ps fall time, creating ideal square wave pulses with 50% duty cycle. The NAND V(out) response to the input patterns can be seen on the bottom graph. As assigned, the simulation shows a total of 400ps of time.



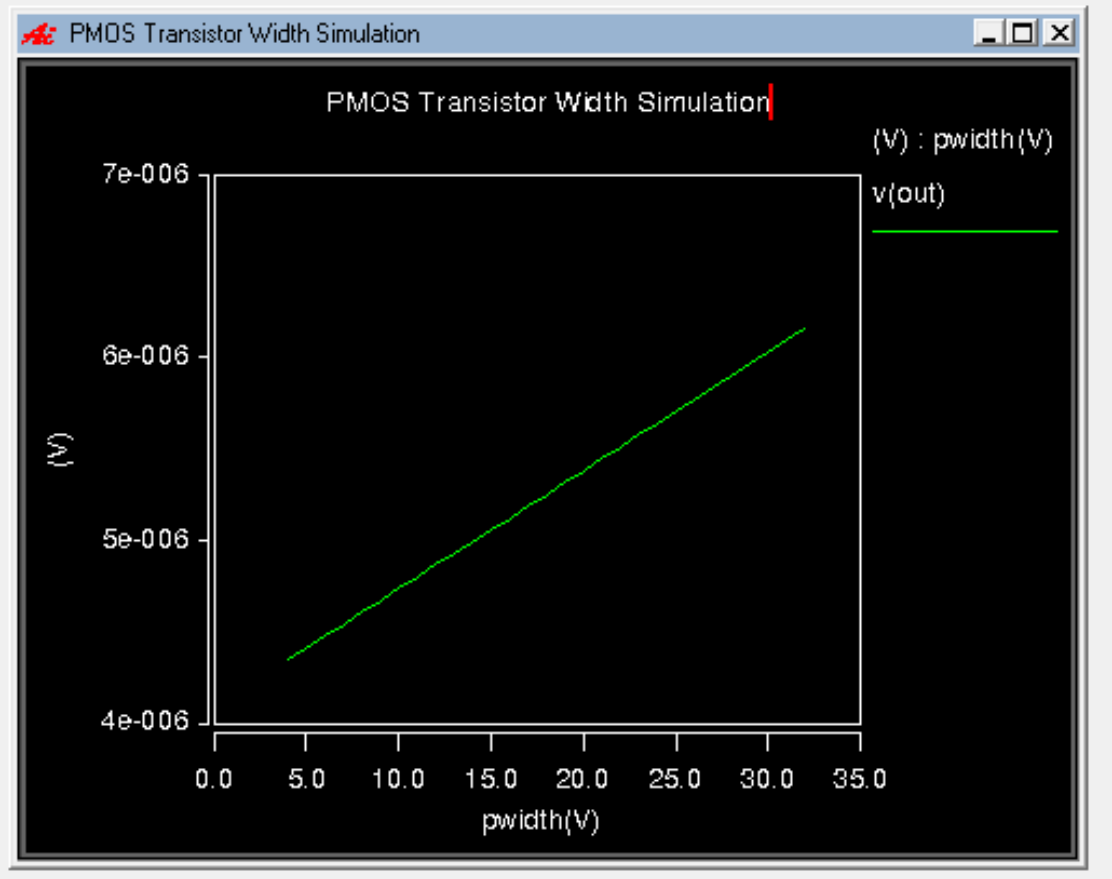
With the second simulation, we were asked to modify the rise and fall times of the signals tow 100ps and change the period of signals to 2000ps. Along with this, I also changed the duty cycle to 1000ps to keep it at 50%. Since there was no instruction to change the total simulation time, I left that at 400ps. With this graph and the next, you can observe with increasing resolution the response of V(out) based on the two inputs.



Here, I have changed the supply voltage to 0.6V, it can be seen that the response of the transistor is now different. Using out knowledge of transistor theory, we know that if the supply voltage is lower, the response time (or speed of the circuit) will be slower.



The following waveform is a DC simulation of a CMOS inverter. The supply voltage is 1.1V and we're sweeping the input from 0 to 1.1 with an increment of 0.05V. It can be seen that the response of the inverter is precisely as expected. Here you can observe the full action of the transistor (cutoff, linear, saturation). As the input voltage goes up, the output voltage goes immediately down to around 0.5 V until the input voltage passes the Vt (threshold) and then the output goes down to 0 V.



In the fifth and final simulation, we show the same inverter circuit from before, but have a steady input voltage at 0.55V (Vdd / 2). Along with that, we fix the NMOS transistor width to 12 and sweep the PMOS width from 4 to 32. We can observe that the amount of leakage increases as transistor width increases (larger transistor, larger capacitance). There is a linear relationship between leakage and PMOS transistor size.