



About Project

Trustable Logic Circuit Design



Policy



- Individual project
- Each student will select a topic on power issues for CMOS digital circuits
- The topic can target any power component at any design level
- Some design work needs to be performed by each student, even for a survey/comparison project
- Any design entry can be used, e.g., VHDL, Verilog, schematic; however, the CAD tool must be able to provide power information
- CAD tools available: Synopsys PrimeTime-PX, Quartus Prime PowerPlay, Xilinx ISE



Project Topic



 The topic could be, but not restricted to, innovative low power design technique / architecture, survey / summary / comparison of a certain topic, an application implementing low power design techniques, analysis of power – performance tradeoffs, power estimation related, etc.

Sample topics:

- Innovative power efficient multiplier design
- Survey and comparison of the existing low power ALU's
- Pipelining and its effect on power dissipation
- High-level power estimation and its error range
- Asynchronous for low power



Some Topics Chosen by Previous Students



- "Clock Gating Techniques Double Gating and Priority Encoding"
- "Low Power Design Techniques for Pipelining"
- "Reducing sub-threshold leakage power"
- "Asynchronous Approach: A Route to Energy-Efficient Computing"
- "Logic Transformation for Low Power"
- "Self-checking and fault tolerant design with respect to lower power design"
- "CMOS Scaling"
- "Clock frequency scaling and GALS"
- "Low power FSMs: an elaboration on orthogonal partitioning"
- "Survey and comparison of the low power flip-flops"
- "Low Power Rank Order Filters"
- "Power Considerations for Calculating xy in FPGAs"
- "Survey and Comparison of Narrow Bus Encoding for Low Power Systems"
- "Low Power Modulo Circuits"
- "Data Gated ALU"
- "The Minimization of Power on a Finite State Machine"
- "FPGA Power Reduction via LUT Optimization and Mapping Technologies"



Report



The report will be double space, single column, #12
 Times New Roman font, no shorter than 10 pages, including figures and tables.

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 The report will contain abstract, introduction, background, theory and application, results and analysis, conclusion and references.



Important Dates



- Topic select deadline: April 2nd (it is strongly recommended that each of you communicates with me to make sure your topic is appropriate <u>way</u> before the deadline)
- Report will due on May 4th midnight



Where to Get Help

Trustable Logic Circuit



- ieeexplore.ieee.org
- Portal.acm.org
- Google
- Interlibrary Loan