CSCE4914 Lab Assignment 2

Due 10/8 11:00PM

Instructions:

1. Unfortunately, linux version of cosmos scope is still down at this point. So for the first part of this assignment, you still need to use the windows version of cosmos scope.
2. Use minimum transistor length L=50nm for all your gate designs.
3. The site of the cells is 0.19(W)*2.47(H). Make sure the cell height (measured from center line of VDD to center line of GND) is 2.47 and the cell width (measured from the left most M1 wire to right most M1 wire, generally is the length of the VDD and GND wire) is a multiple number of 0.19, i.e., your cell size should be 0.19n*2.47, where n is an integer.

Assignment (20% for each task):

1. This task uses Hspice to find out the optimum size of the PMOS to match with NMOS size in an INVx1. First, write an investor SPICE netlist with the smallest NMOS size (W=90nm). Then design a transient simulation to find out the PMOS width such that the t_{pdf} and t_{pdr} of the invertor are equal. Use this width for your INVx1 design. Using Hspice to find out the propagation delay and rise/fall time of this invertor.
2. Standard cell layout design: for this task, you need to design the following gates:
    a. INVx1 (using the NMOS and PMOS size you found in task 1)
    b. INVx4 (multiply NMOS and PMOS sizes of INVx1 by 4)
    c. NAND2x1 (using the NMOS and PMOS size you found in task 1)
    d. NOR2x1 (using the NMOS and PMOS size you found in task 1)

    First, write the SPICE netlist for each gate, then draw the layout using virtuoso. Finally, ensure DRC and LVS are clean using Calibre.

What to turn in:

1. A lab report showing the HSPICE simulation results and the layouts of all gates. Also, show the DRC and LVS report for each gate.
2. HSPICE netlists and output list.
3. Your folder containing virtuoso gates and DRC/LVS report.