CSCE 3953 System Synthesis and Modeling

Project 4: Design and Simulate Sequential Logic in Verilog

Instructor: Dr. Jia Di

Objectives and Tasks

- Objective – design and simulate sequential logic circuits using Verilog

- Solve modified Problem 18 on textbook Page 225 (old book Problem 19 on Page 227)
  - Design and simulate a BCD counter whose initial count is 5
- Make your own assumptions
- Implement your solution in Verilog
- Either write a testbench or a .DO file
- Simulate the designed circuit in ModelSim for ***ALL*** possible output patterns

Report

- Project objective
- Design methodology / circuit diagram / assumptions made
- Simulation method
- Result (simulation waveform screenshot)
- Analysis and conclusion
- Source code (design file, testbench / .DO file)
- **Include your name in the report file name**
- Due date: September 30 before class, email your report to jdi@uark.edu in either Word or PDF format