Digital Design CSCE 2114

Lab 8 Report

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Abstract

The purpose of the final lab was to design and implement an asynchronous active low reset rising edge triggered T-Flip-Flop.

Introduction

The signals of the T-Flip-Flop were outlined in the lab. A Flip Flop is basically a data selector that changes its value based on a certain set of input values.

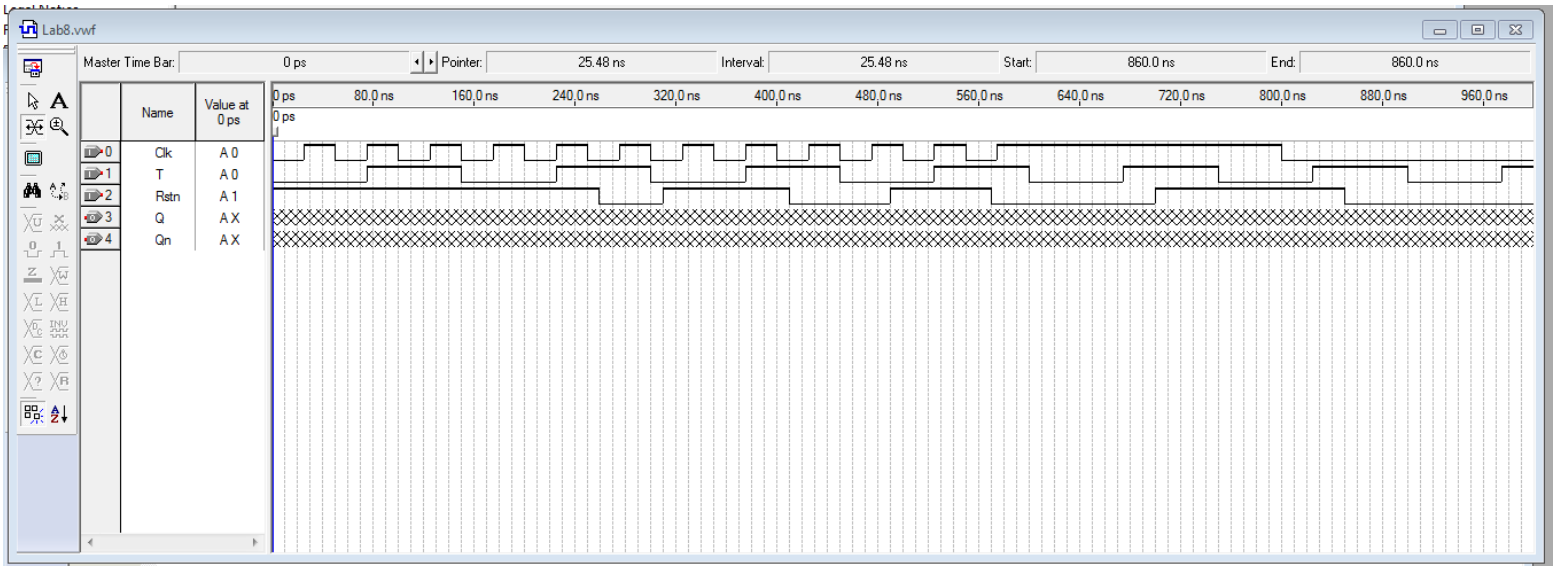
Design and Implementation

The five signals outlined in the lab are as follows. There is the clock input (rising edge triggered), Clk, toggle input, T, the active low asynchronous reset, Rstn, as well as Q and Qn, the output and inverse of the output of the flip-flop. We were to write all the VHDL code for the T-Flip Flop. The following is the VHDL code for the circuit.

Lab8.vhd

```
1  LIBRARY ieee ;
2  USE ieee.std_logic_1164.all ;
3
4  ENTITY Lab8 is
5      PORT ( T, Rstn, Clk     : IN        STD_LOGIC;
6                     Q, Qn    : OUT       STD_LOGIC);
7  END Lab8 ;
8
9  ARCHITECTURE Behavior OF Lab8 is
10     signal Qtemp : std_logic;
11 BEGIN
12     PROCESS (Rstn, Clk)
13     BEGIN
14         IF Rstn = '0' then
15             Qtemp <= '0' ;
16         ELSIF Clk'EVENT AND Clk = '1' and T = '1' then
17             Qtemp <= T XOR Qtemp ;
18         END IF ;
19     END PROCESS ;
20         Q <= Qtemp;
21         Qn <= NOT Qtemp;
22 END Behavior ;
```

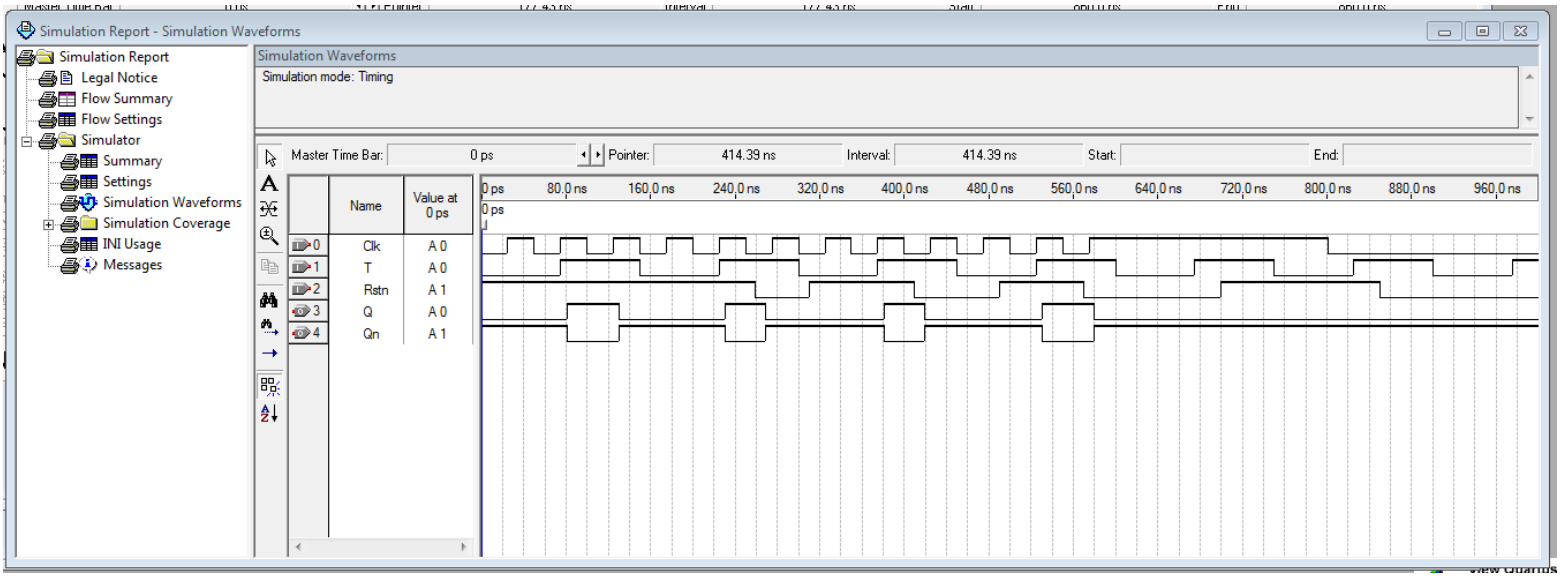
The basic outline of the program is as follows; there is a Qtemp signal that is used as a temporary placeholder signal for the eventual output of the program, since the output itself can't directly be modified. The 'if' statements basically tell the circuit to set to '0' whenever Rstn = '0' and change the value to 'T' whenever T = '1' and Clk = '1.' The following is the waveform diagram I set up for the circuit.



I wanted to create a scenario where the clock alternated, then was high and low for an extended period of time. I did my best to ensure most test cases were included in the eventual output.

Results

The following is the resulting waveform based on the input diagram above.



It can be seen that the output, Q, is high whenever the clock is on a rising edge and T = ‘1.’ This T Flip Flop is an asynchronous reset, meaning the circuit will reset anytime the Rstn signal goes low, not only on a clock edge.

Conclusion

The T flip flop design and implementation was successful.