CSCE 3953 System Synthesis and Modeling

Project 2: First Verilog Design and Simulation

Instructor: Dr. Jia Di

Objectives and Tasks

- Objective – getting familiar with Verilog design and simulation in ModelSim

- Go through the ModelSim tutorial
- Design a 7-to-1 MUX in Verilog (either structural or behavioral)
- Either write a testbench or a .DO file
- Follow the tutorial to simulate the designed MUX

Report

- Project objective
- Design methodology / circuit diagram
- Simulation method
- Result (simulation waveform screenshot)
- Analysis and conclusion
- Source code (design file, testbench / .DO file)
- **Include your name in the report file name**
- Due date: September 21 midnight, email your report to jdi@uark.edu in either Word or PDF format