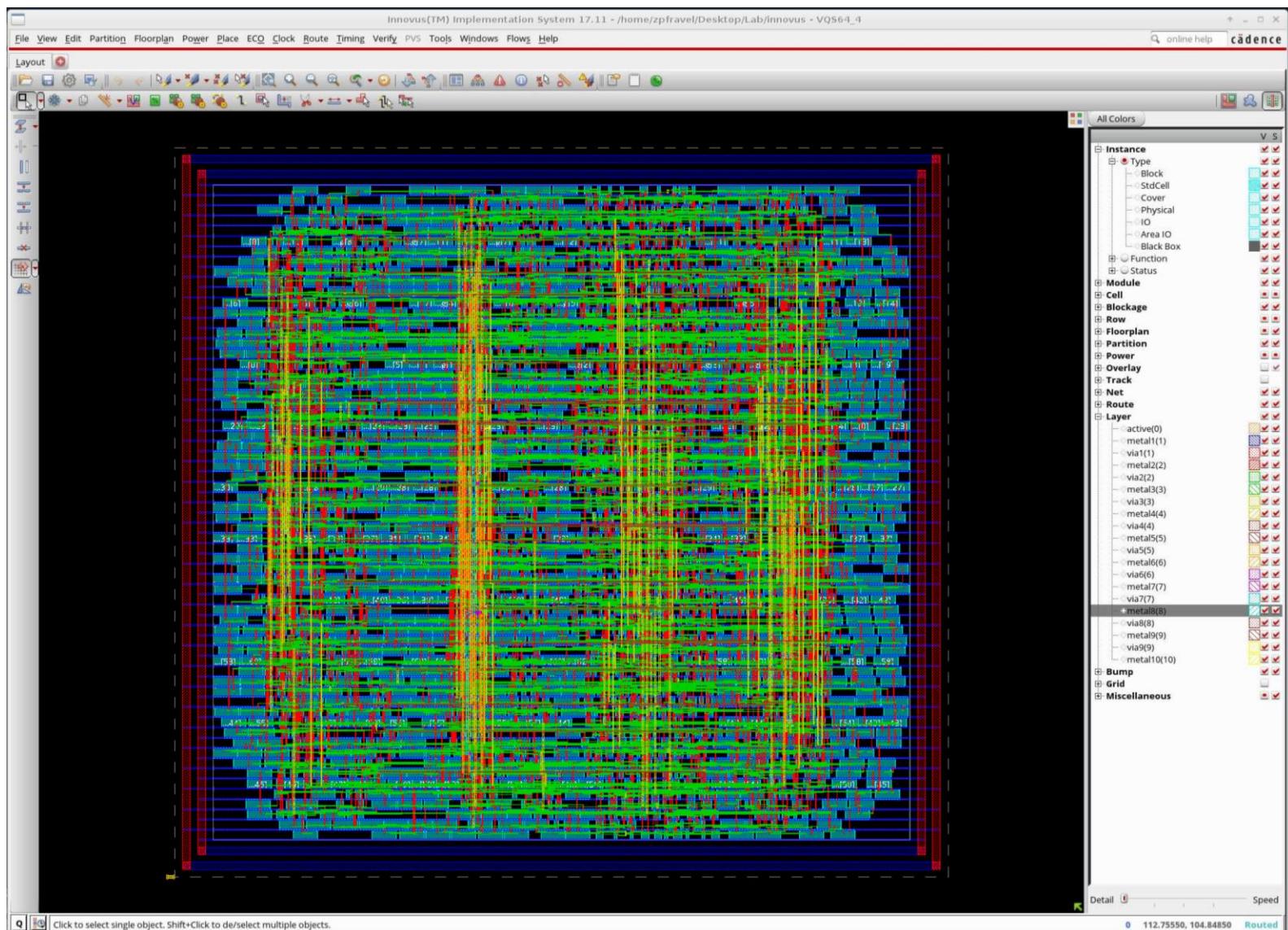


Zack Fravel
CSCE 4914
Lab 5 Report

VQS64_4 Placement and Routing

The following section describes the placement and routing of the VQS64_4 design using 5 metal layers for routing and with a 0.65 core utilization on the floorplan. The first major step in the process is placement of the standard cells. The following images are of the design after placement and the console summary report following placement.



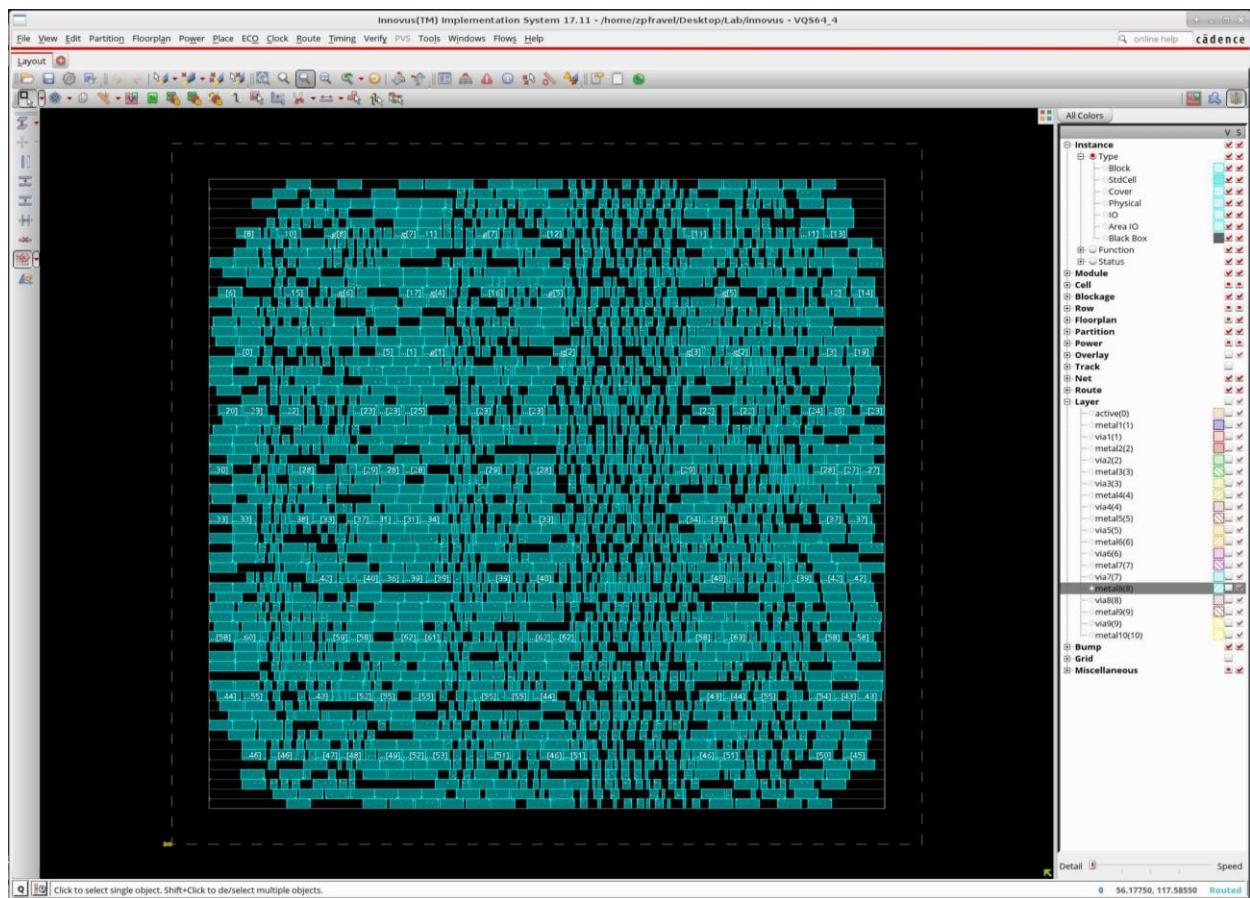
```

Terminal - zpfravel@vlsi:innovus
File Edit View Terminal Tabs Help
*** Free Virtual Timing Model ... (mem=1148.4M)
Starting congestion repair ...
[NR-eGR] honorMsvRouteConstraint: false
[NR-eGR] honorClockSpecNDR : 0
[NR-eGR] minRouteLayer : 2
[NR-eGR] maxRouteLayer : 127
[NR-eGR] numTracksPerClockWire : 0
[NR-eGR] Layer1 has no routable track
[NR-eGR] Layer2 has single uniform track structure
[NR-eGR] Layer3 has single uniform track structure
[NR-eGR] Layer4 has single uniform track structure
[NR-eGR] Layer5 has single uniform track structure
[NR-eGR] Layer6 has single uniform track structure
[NR-eGR] Layer7 has single uniform track structure
[NR-eGR] Layer8 has single uniform track structure
[NR-eGR] Layer9 has single uniform track structure
[NR-eGR] Layer10 has single uniform track structure
[NR-eGR] numRoutingBlks=0 numInstBlks=0 numPGBlocks=142 numBumpBlks=0 numBoundaryFakeBlks=0
[NR-eGR] numPreroutedNet = 0 numPreroutedWires = 0
[NR-eGR] Read numTotalNets=2783 numIgnoredNets=0
[NR-eGR] There are 1 clock nets ( 0 with NDR ).
[NR-eGR] ===== Routing rule table =====
[NR-eGR] Rule id 0. Nets 2783
[NR-eGR] id=0 ndrTrackId=0 ndrViaId=-1 extraSpace=0 numShields=0 maxHorDemand=1 maxVerDemand=1
[NR-eGR] Pitch: L1=270 L2=280 L3=280 L4=560 L5=560 L6=560 L7=1680 L8=1680 L9=3200 L10=336
0
[NR-eGR] =====
[NR-eGR]
[NR-eGR] Layer group 1: route 2783 net(s) in layer range [2, 10]
[NR-eGR] earlyGlobalRoute overflow of layer group 1: 0.00% H + 0.00% V. EstWL: 3.126340e+04um
[NR-eGR]
[NR-eGR] Overflow after earlyGlobalRoute (GR compatible) 0.00% H + 0.00% V
[NR-eGR] Overflow after earlyGlobalRoute 0.00% H + 0.00% V
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00, normalized total congestion
hotspot area = 0.00 (area is in unit of 4 std-cell row bins)
Skipped repairing congestion.
[NR-eGR] -----
[NR-eGR] Layer1(metal1)(F) length: 0.000000e+00um, number of vias: 9106
[NR-eGR] Layer2(metal2)(V) length: 1.313899e+04um, number of vias: 12954
[NR-eGR] Layer3(metal3)(H) length: 1.594768e+04um, number of vias: 444
[NR-eGR] Layer4(metal4)(V) length: 2.369600e+03um, number of vias: 95
[NR-eGR] Layer5(metal5)(H) length: 1.107635e+03um, number of vias: 47
[NR-eGR] Layer6(metal6)(V) length: 4.973995e+02um, number of vias: 5
[NR-eGR] Layer7(metal7)(H) length: 3.080000e+00um, number of vias: 5
[NR-eGR] Layer8(metal8)(V) length: 5.628000e+01um, number of vias: 0
[NR-eGR] Layer9(metal9)(H) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer10(metal10)(V) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Total length: 3.312066e+04um, number of vias: 22656
[NR-eGR] -----
[NR-eGR] Total clock nets wire length: 2.014830e+03um
[NR-eGR] -----
End of congRepair (cpu=0:00:00.1, real=0:00:00.0)
*** Finishing placeDesign default flow ***
***** Total cpu 0:0:10
***** Total real time 0:0:6
**placeDesign ... cpu = 0: 0:10, real = 0: 0: 6, mem = 1096.8M **

*** Summary of all messages that are not suppressed in this session:
Severity ID Count Summary
WARNING IMPDC-1629 1 The default delay limit was set to %d. T...
WARNING IMPSP-9025 1 No scan chain specified/traced.
*** Message Summary: 2 warning(s), 0 error(s)

innovus 2>
innovus 2> saveDesign test_02_pl.enc
#% Begin save design ... (date=11/10 13:02:57, mem=1137.4M)

```



The following is the timing report before pre-CTS optimization.

```

timeDesign Summary

Setup views included:
NG_view_typ

+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns): | -1.546 | 0.045 | -1.546 |
| TNS (ns): | -380.441 | 0.000 | -380.441 |
| Violating Paths: | 254 | 0 | 254 |
| All Paths: | 768 | 512 | 256 |
+-----+-----+-----+

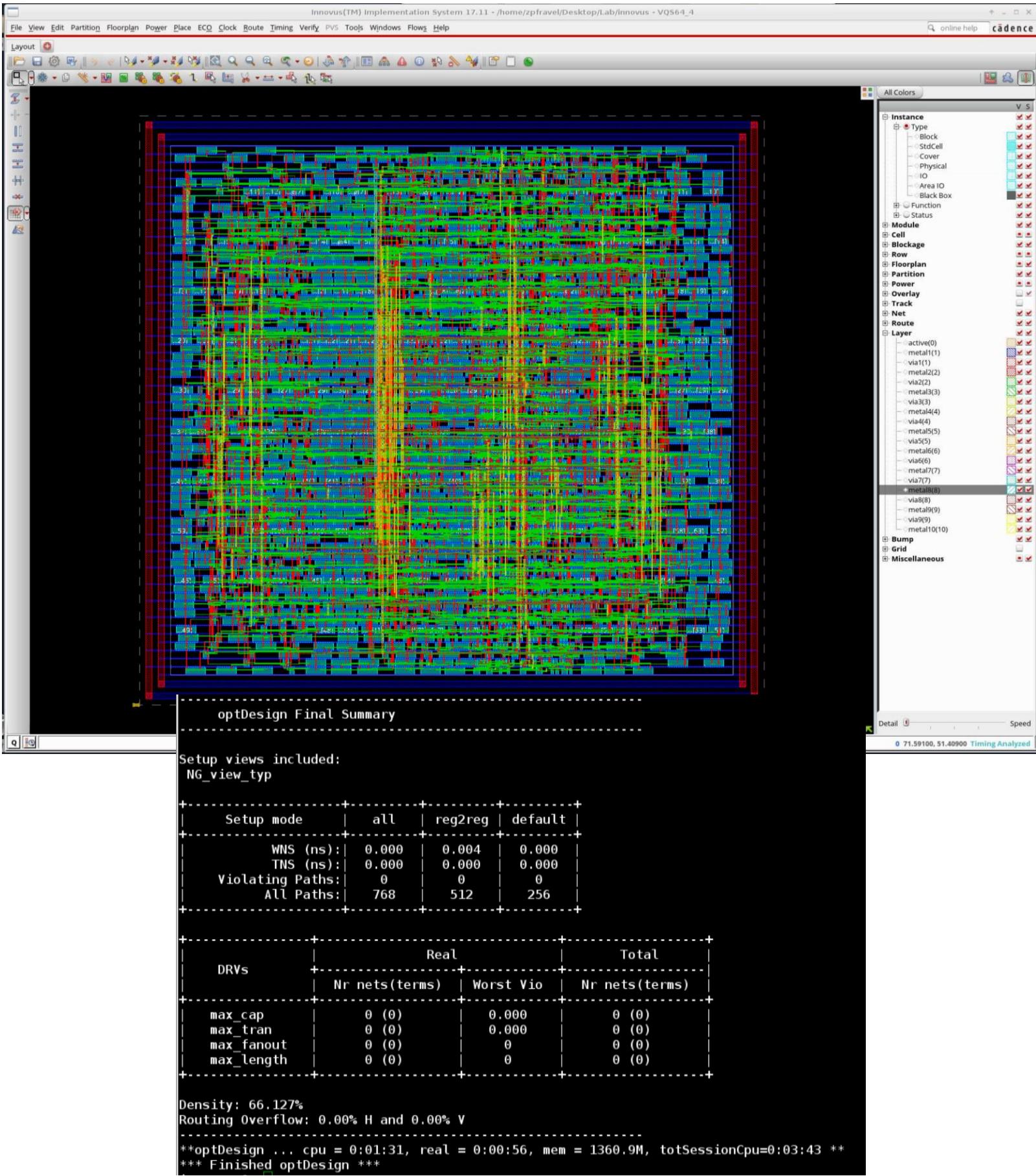
+-----+-----+-----+
| DRVs | Real | Total |
|      | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 1 (1) | -0.002 | 1 (1) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

Density: 64.953%
Routing Overflow: 0.00% H and 0.00% V

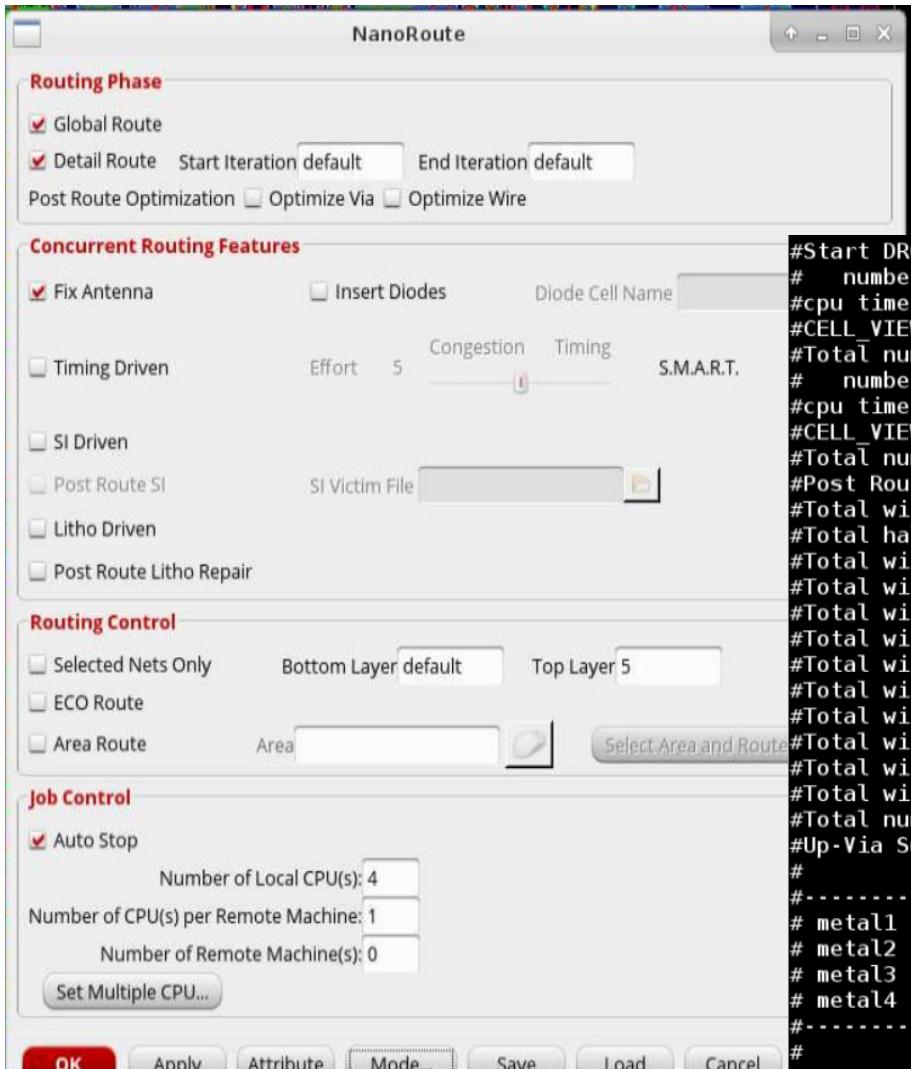
Reported timing to dir ./timingReports
Total CPU time: 1.58 sec
Total Real time: 1.0 sec
Total Memory Usage: 1577.417969 Mbytes

```

And here is a picture of the placement after pre CTS optimization. The following image shows the optimization report generated after the pre-CTS optimization.



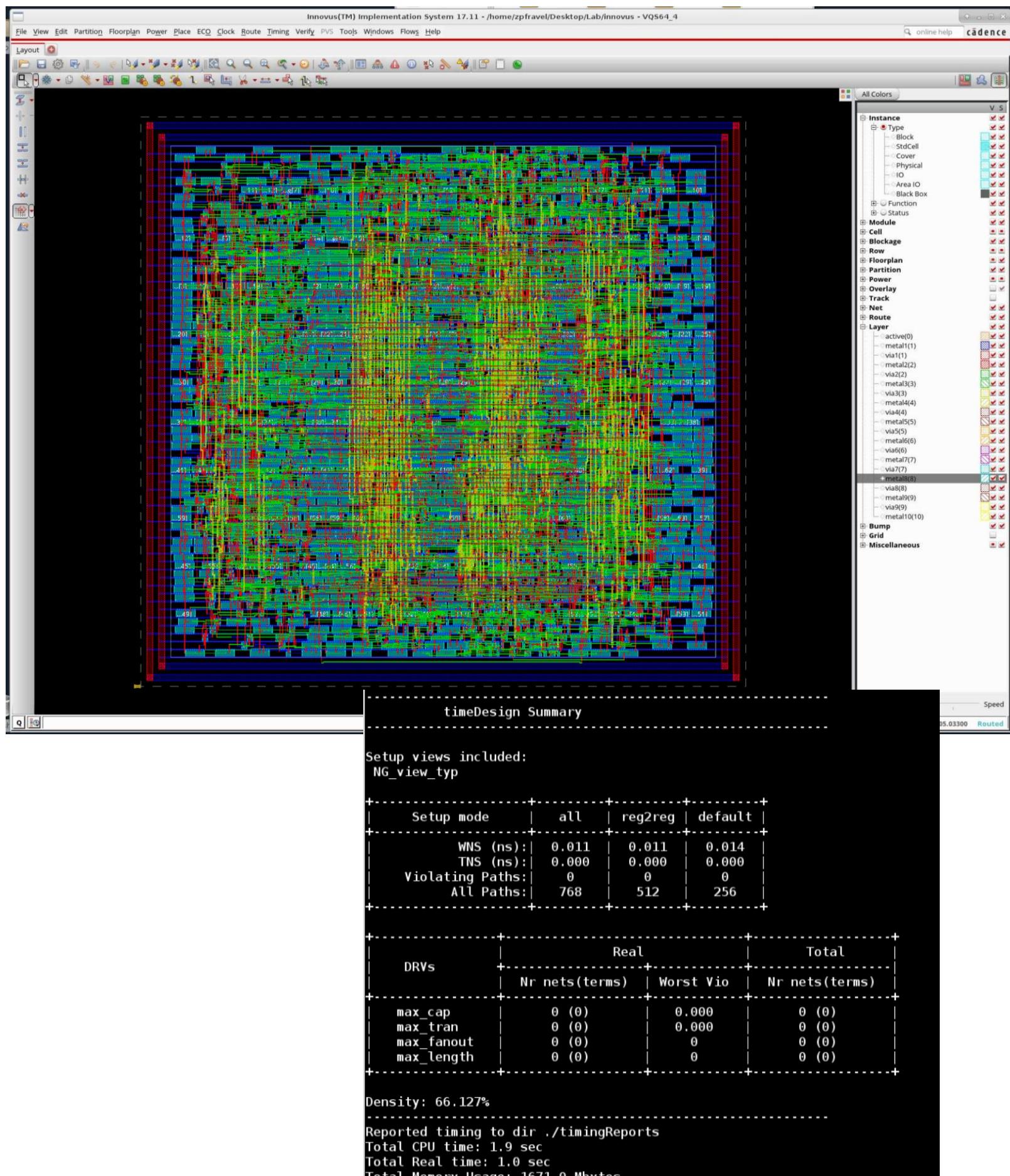
The next step is routing the design. After following the steps provided by the lab slides, I was able to successfully route the design. Below are the routing settings I used and routing summary. As you can see I only used 5 layers for routing, as specified in the instruction. Wire lengths can be observed in the report.



```
#Start DRC checking..
#   number of violations = 0
#cpu time = 00:00:02, elapsed time = 00:00:00, memory = 1435.12 MB
#CELL_VIEW VQS64_4,init has no DRC violation.
#Total number of DRC violations = 0
#   number of violations = 0
#cpu time = 00:00:02, elapsed time = 00:00:01, memory = 1307.86 MB
#CELL_VIEW VQS64_4,init has no DRC violation.
#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 32835 um.
#Total half perimeter of net bounding box = 29080 um.
#Total wire length on LAYER metall1 = 1236 um.
#Total wire length on LAYER metall2 = 11413 um.
#Total wire length on LAYER metall3 = 14206 um.
#Total wire length on LAYER metall4 = 3335 um.
#Total wire length on LAYER metall5 = 2646 um.
#Total wire length on LAYER metall6 = 0 um.
#Total wire length on LAYER metall7 = 0 um.
#Total wire length on LAYER metall8 = 0 um.
#Total wire length on LAYER metall9 = 0 um.
#Total wire length on LAYER metall10 = 0 um.
#Total number of vias = 18557
#Up-Via Summary (total 18557):
#
#-----
# metall1      9664
# metall2      7896
# metall3      867
# metall4      130
#
#                               18557
#
#detailRoute Statistics:
#Cpu time = 00:00:28
#Elapsed time = 00:00:08
#Increased memory = -2.12 (MB)
#Total memory = 1306.64 (MB)
#Peak memory = 1519.66 (MB)
#
#globlalDetailRoute statistics:
#Cpu time = 00:00:30
#Elapsed time = 00:00:09
#Increased memory = -65.55 (MB)
#Total memory = 1298.55 (MB)
#Peak memory = 1519.66 (MB)
#Number of warnings = 60
#Total number of warnings = 61
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Fri Nov 10 13:16:31 2017
#
#routeDesign: cpu time = 00:00:30, elapsed time = 00:00:09, memory = 1306.64 MB

*** Summary of all messages that are not suppressed in this session
Severity ID          Count Summary
WARNING IMPCK-8086      1 The command %s is obsolete and will be removed in a future release.
*** Message Summary: 1 warning(s), 0 error(s)
```

The following is the design after routing with 5 metal layers. Below is the routing timing report.



The final step in the process is to do post route optimization and then metal fill insertion. The following images show the post route optimization report, followed by an image of the metal fill insertion, with the timing report after fill insertion at the end.

```

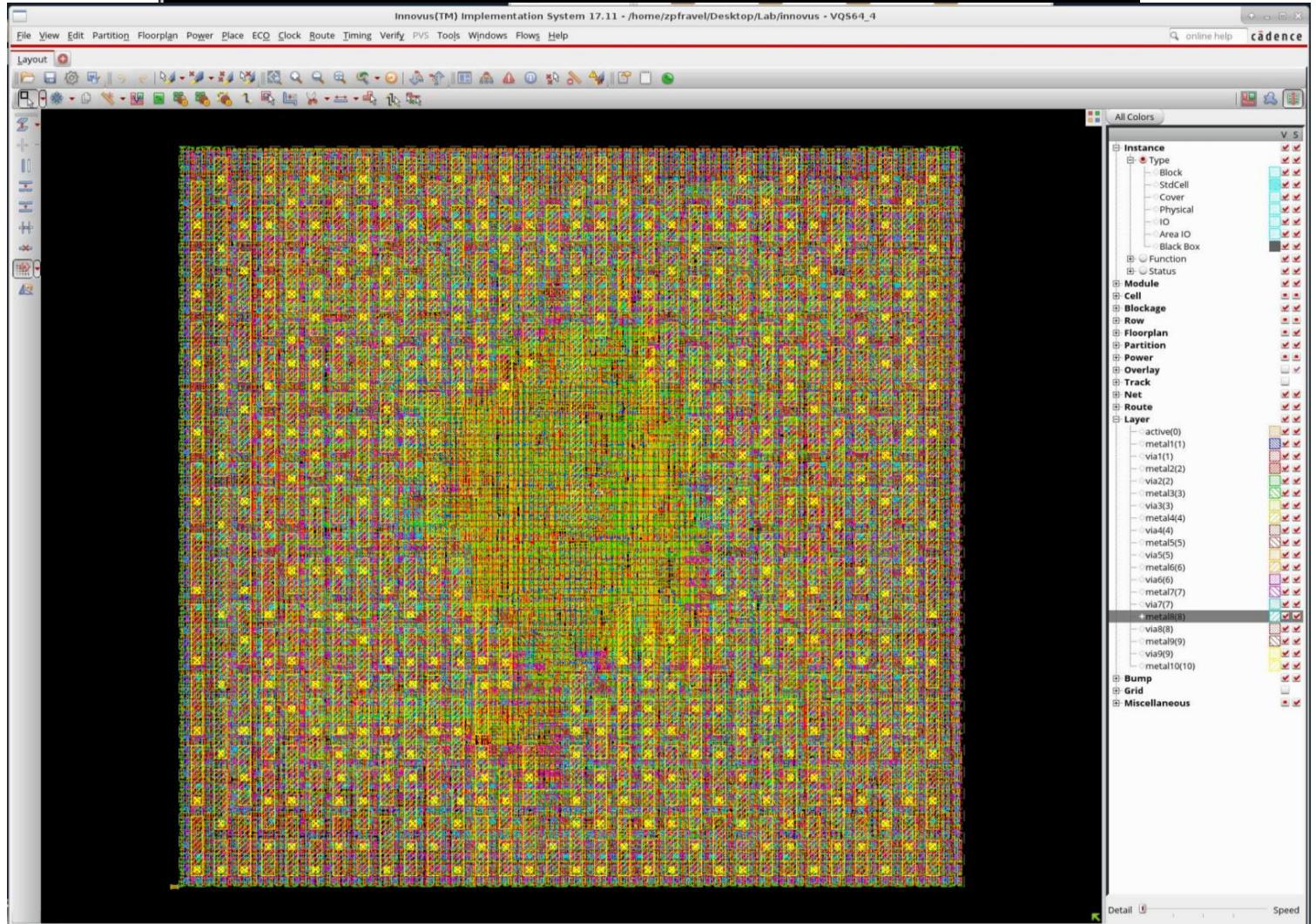
optDesign Final Non-SI Timing Summary

Setup views included:
NG_view_typ

+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns): | 0.012 | 0.012 | 0.014 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 768 | 512 | 256 |
+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
|       | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

```



```

timeDesign Summary

Setup views included:
  NG_view_typ

+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns) : | 0.012 | 0.012 | 0.014 |
| TNS (ns) : | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 768 | 512 | 256 |
+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

Density: 66.127%
-----
Reported timing to dir ./timingReports
Total CPU time: 0.53 sec
Total Real time: 0.0 sec
Total Memory Usage: 1701.945312 Mbytes

```

Final images of each metal layer in the design is included at the appendix at the end. The following table was generated from information in the summary report generated by innovus.

General Design Information

Design Status	Routed
Design Name	VQS64_4
# Instances	2715
# Hard Macros	0
# Std Cells	2715
# Pads	0
# Net	3361
# IO Pins	513

Floorplan/Placement Information

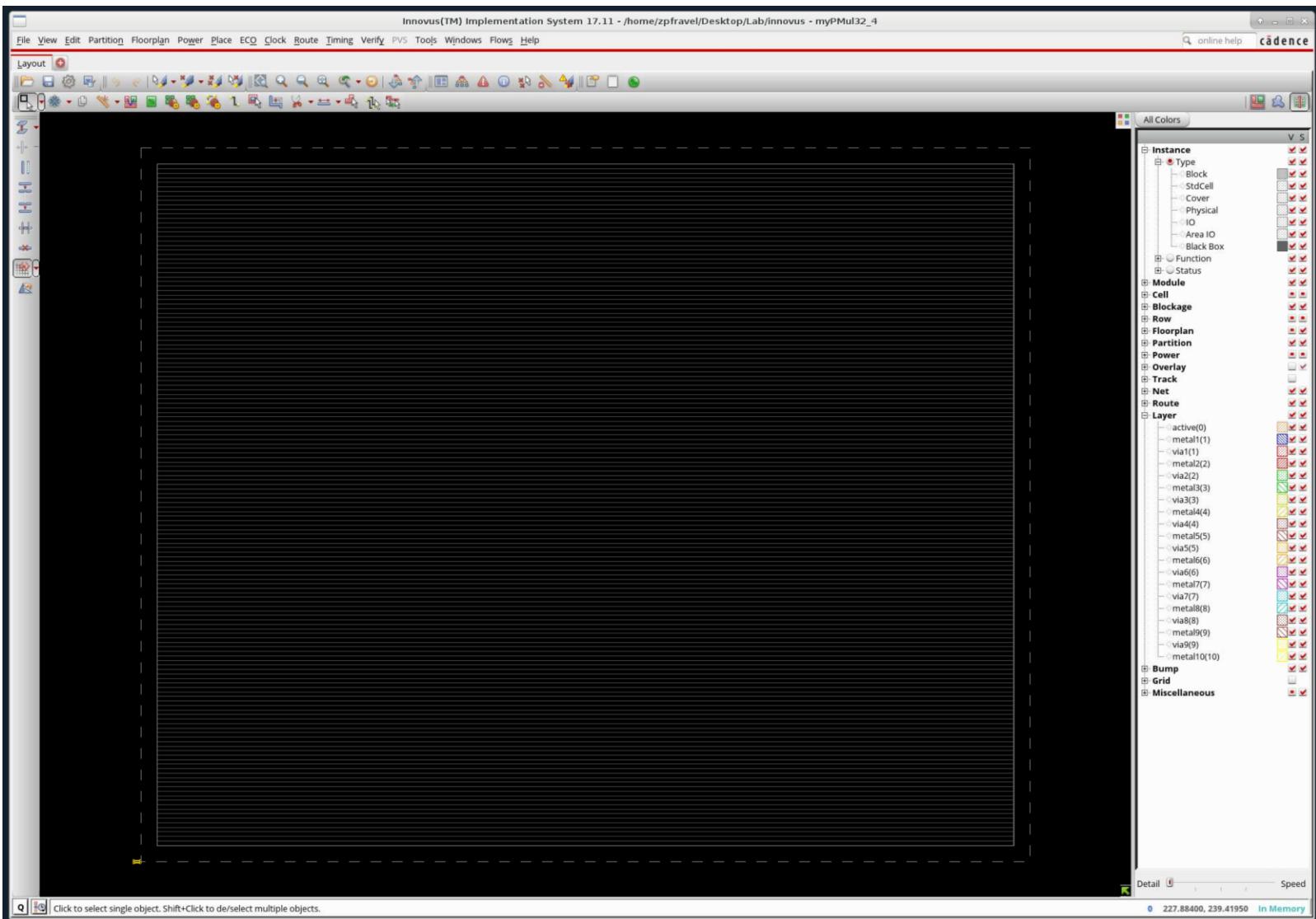
Total area of Standard Cells	5471.088 um^2
Total area of Core	8279.040 um^2
Total area of Chip	10215.206 um^2
Effective Utilization	6.6127 e-01
Number of Cell Rows	64

Wire Length Distribution

Total metal 1 wire length	1235.6650 um
Total metal 2 wire length	11434.1950 um
Total metal 3 wire length	14256.6850 um
Total metal 4 wire length	3341.2400 um
Total metal 5 wire length	2646.8400 um
Total metal 6-10 wire length	0.0000 um
Total wire length	32914.6250 um
Average wire length/net	9.7931 um

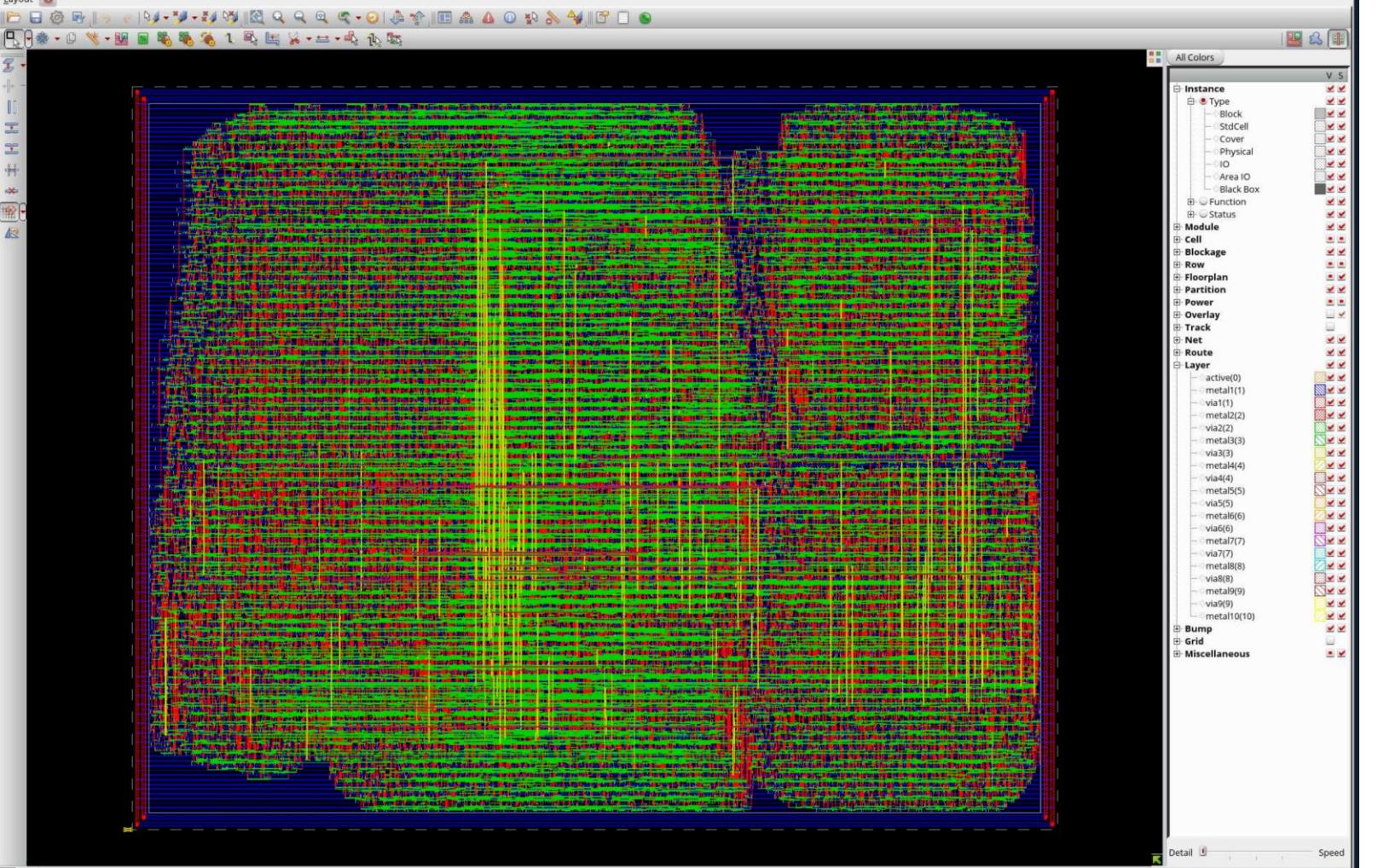
Pmul_32_4 Placement and Routing

The following shows the design process of placement and routing pmul_32_4 design using 6 metal layers for routing and 0.6 core utilization and 0.8 aspect ratio for floorplan placement. The following image is of the floorplan settings before placement and routing.



The pictures on the next page show placement of the pmul32_4 design followed by the summary report of the placement process.

File Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help



Click to select single object. Shift+Click to de-select multiple objects.

Skipped repairing congestion.

[NR-eGR]

```
[NR-eGR] Layer1(metal1) (F) length: 0.000000e+00um, number of vias: 55704
[NR-eGR] Layer2(metal2) (V) length: 9.981329e+04um, number of vias: 76768
[NR-eGR] Layer3(metal3) (H) length: 9.958830e+04um, number of vias: 535
[NR-eGR] Layer4(metal4) (V) length: 5.415520e+03um, number of vias: 42
[NR-eGR] Layer5(metal5) (H) length: 1.870820e+03um, number of vias: 4
[NR-eGR] Layer6(metal6) (V) length: 6.328000e+01um, number of vias: 0
[NR-eGR] Layer7(metal7) (H) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer8(metal8) (V) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer9(metal9) (H) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer10(metal10) (V) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Total length: 2.067512e+05um, number of vias: 133053
[NR-eGR]
```

[NR-eGR] Total clock nets wire length: 2.095640e+03um

[NR-eGR]

End of congRepair (cpu=0:00:00.7, real=0:00:01.0)

*** Finishing placeDesign default flow ***

***** Total cpu 0:0:52

***** Total real time 0:0:29

**placeDesign ... cpu = 0: 0:52, real = 0: 0:29, mem = 1549.1M **

*** Summary of all messages that are not suppressed in this session:

Severity	ID	Count	Summary
----------	----	-------	---------

WARNING	IMPDC-1629	1	The default delay limit was set to %d. T...
---------	------------	---	---

WARNING	IMPSP-9025	1	No scan chain specified/traced.
---------	------------	---	---------------------------------

*** Message Summary: 2 warning(s), 0 error(s)

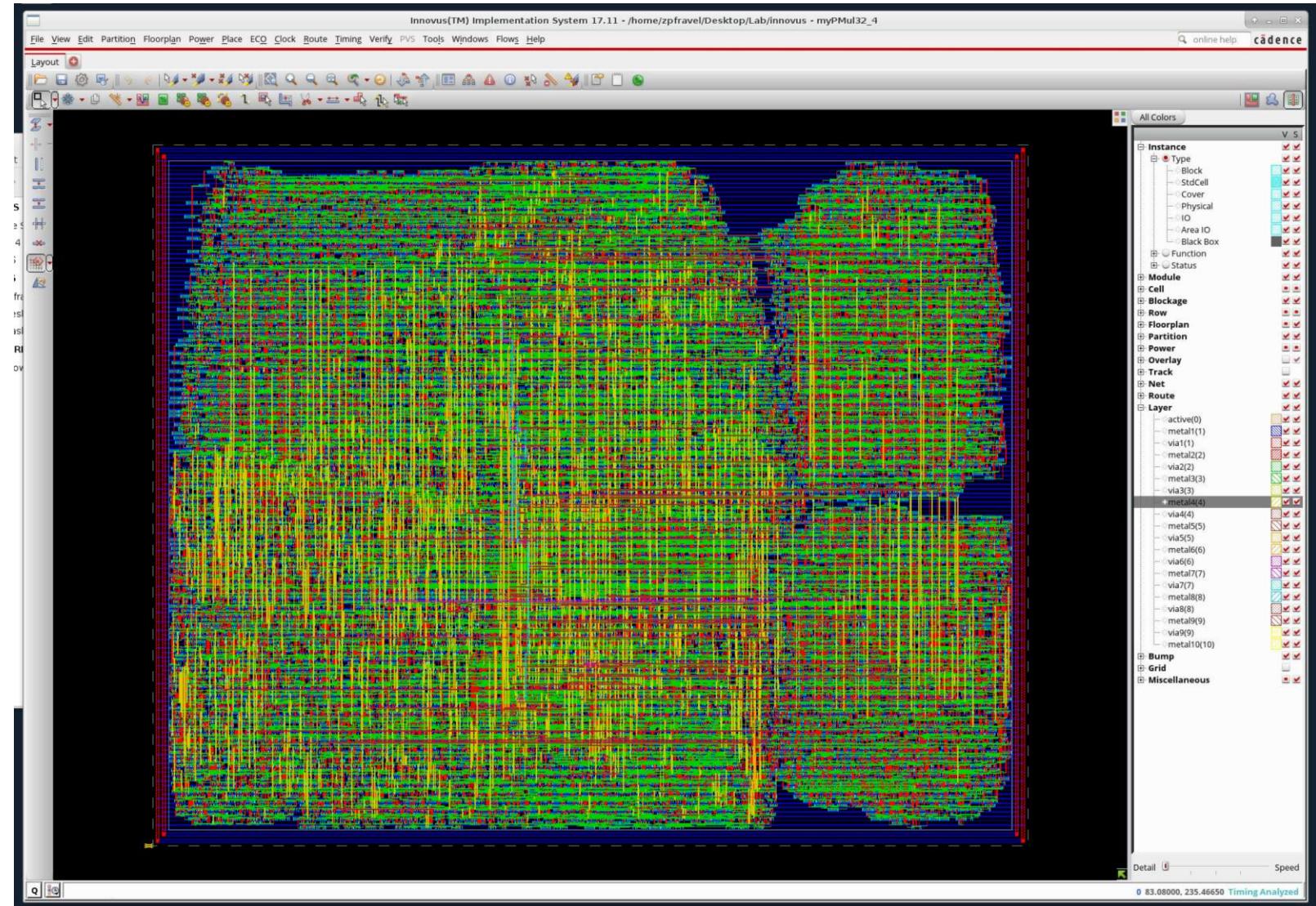
innovus 3> []

Next is the timing report before pre CTS optimization.

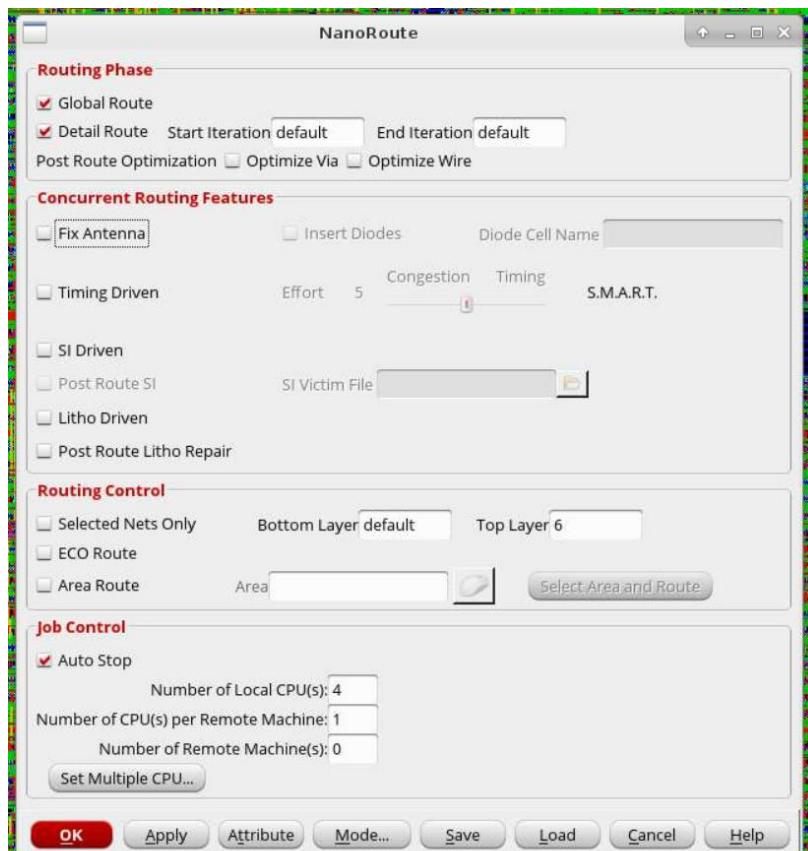
```
-----  
          timeDesign Summary  
-----  
  
Setup views included:  
  NG_view_typ  
  
+-----+-----+-----+-----+  
|   Setup mode |   all | reg2reg | default |  
+-----+-----+-----+-----+  
|       WNS (ns): | -1.653 | -1.653 | 6.362 |  
|       TNS (ns): | -69.729 | -69.729 | 0.000 |  
| Violating Paths: | 69 | 69 | 0 |  
| All Paths: | 384 | 256 | 128 |  
+-----+-----+-----+-----+  
  
+-----+-----+-----+-----+  
|           Real           |           Total           |  
|   DRVs      |-----+-----|-----+-----+  
|           | Nr nets(terms) | Worst Vio | Nr nets(terms)  
+-----+-----+-----+-----+  
| max_cap    | 2 (2) | -0.003 | 2 (2) |  
| max_tran   | 0 (0) | 0.000 | 0 (0) |  
| max_fanout | 0 (0) | 0 | 0 (0) |  
| max_length | 0 (0) | 0 | 0 (0) |  
+-----+-----+-----+-----+  
  
Density: 60.009%  
Routing Overflow: 0.00% H and 0.00% V  
-----  
Reported timing to dir ./timingReports  
Total CPU time: 6.89 sec  
Total Real time: 3.0 sec  
Total Memory Usage: 1600.1875 Mbytes  
innovus 6> innovus 6> █
```

The next step is pre-CTS optimization. The following images show the design placement after pre-CTS optimization and the timing report.

```
-----  
          optDesign Final Summary  
-----  
  
Setup views included:  
  NG_view_typ  
  
+-----+-----+-----+-----+  
|   Setup mode |   all | reg2reg | default |  
+-----+-----+-----+-----+  
|       WNS (ns): | 0.001 | 0.001 | 6.362 |  
|       TNS (ns): | 0.000 | 0.000 | 0.000 |  
| Violating Paths: | 0 | 0 | 0 |  
| All Paths: | 384 | 256 | 128 |  
+-----+-----+-----+-----+  
  
+-----+-----+-----+-----+  
|           Real           |           Total           |  
|   DRVs      |-----+-----|-----+-----+  
|           | Nr nets(terms) | Worst Vio | Nr nets(terms)  
+-----+-----+-----+-----+  
| max_cap    | 0 (0) | 0.000 | 0 (0) |  
| max_tran   | 0 (0) | 0.000 | 0 (0) |  
| max_fanout | 0 (0) | 0 | 0 (0) |  
| max_length | 0 (0) | 0 | 0 (0) |  
+-----+-----+-----+-----+  
  
Density: 75.404%  
Routing Overflow: 0.00% H and 0.00% V  
-----  
**optDesign ... cpu = 0:13:27, real = 0:05:02, mem = 1459.8M, totSessionCpu=0:17:53 **  
*** Finished optDesign ***  
innovus 7> █
```



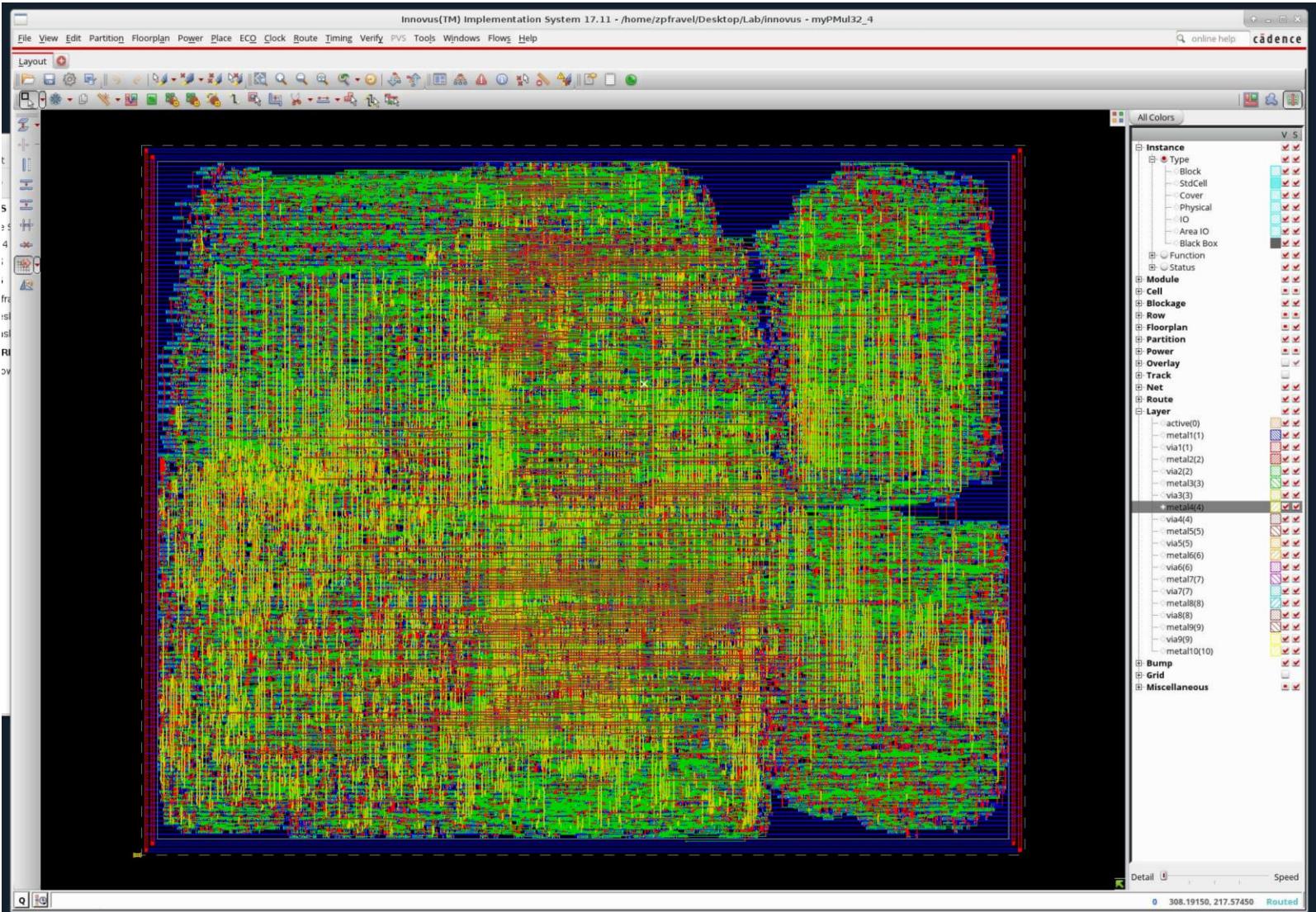
Following pre-CTS optimization, we're ready to route. As stated previously, we are routing using six metal layers.



```

#
# By Layer and Type :
#          Loop   Totals
#    metal1      0      0
#    metal2      1      1
#    Totals      1      1
#cpu time = 00:00:17, elapsed time = 00:00:06, memory = 1455.49 (MB), peak = 1749.59 (MB)
#CELL_VIEW myPMul32_4, init has 1 DRC violations
#Total number of DRC violations = 1
#Total number of violations on LAYER metal1 = 0
#Total number of violations on LAYER metal2 = 1
#Total number of violations on LAYER metal3 = 0
#Total number of violations on LAYER metal4 = 0
#Total number of violations on LAYER metal5 = 0
#Total number of violations on LAYER metal6 = 0
#Total number of violations on LAYER metal7 = 0
#Total number of violations on LAYER metal8 = 0
#Total number of violations on LAYER metal9 = 0
#Total number of violations on LAYER metal10 = 0
#Post Route wire spread is done.
#Total wire length = 234351 um.
#Total half perimeter of net bounding box = 256073 um.
#Total wire length on LAYER metal1 = 7291 um.
#Total wire length on LAYER metal2 = 88072 um.
#Total wire length on LAYER metal3 = 90817 um.
#Total wire length on LAYER metal4 = 33126 um.
#Total wire length on LAYER metal5 = 14774 um.
#Total wire length on LAYER metal6 = 271 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 172024
#Up-Via Summary (total 172024):
#
#-----
# metal1      96429
# metal2      67144
# metal3      7725
# metal4      706
# metal5      20
#-----
#                  172024
#
#detailRoute Statistics:
#Cpu time = 00:03:32
#Elapsed time = 00:00:56
#Increased memory = -20.31 (MB)
#Total memory = 1454.12 (MB)
#Peak memory = 1749.59 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:03:51
#Elapsed time = 00:01:13
#Increased memory = -65.54 (MB)
#Total memory = 1410.58 (MB)
#Peak memory = 1749.59 (MB)
#Number of warnings = 60
#Total number of warnings = 61
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Fri Nov 10 14:39:13 2017
#
#routeDesign: cpu time = 00:03:52, elapsed time = 00:01:14, memory = 1368.18 (MB), peak =
1749.59 (MB)

```



Here is the timing report after routing.

```

timeDesign Summary

Setup views included:
NG_view_typ

+-----+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns): | 0.014 | 0.014 | 6.319 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 384 | 256 | 128 |
+-----+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

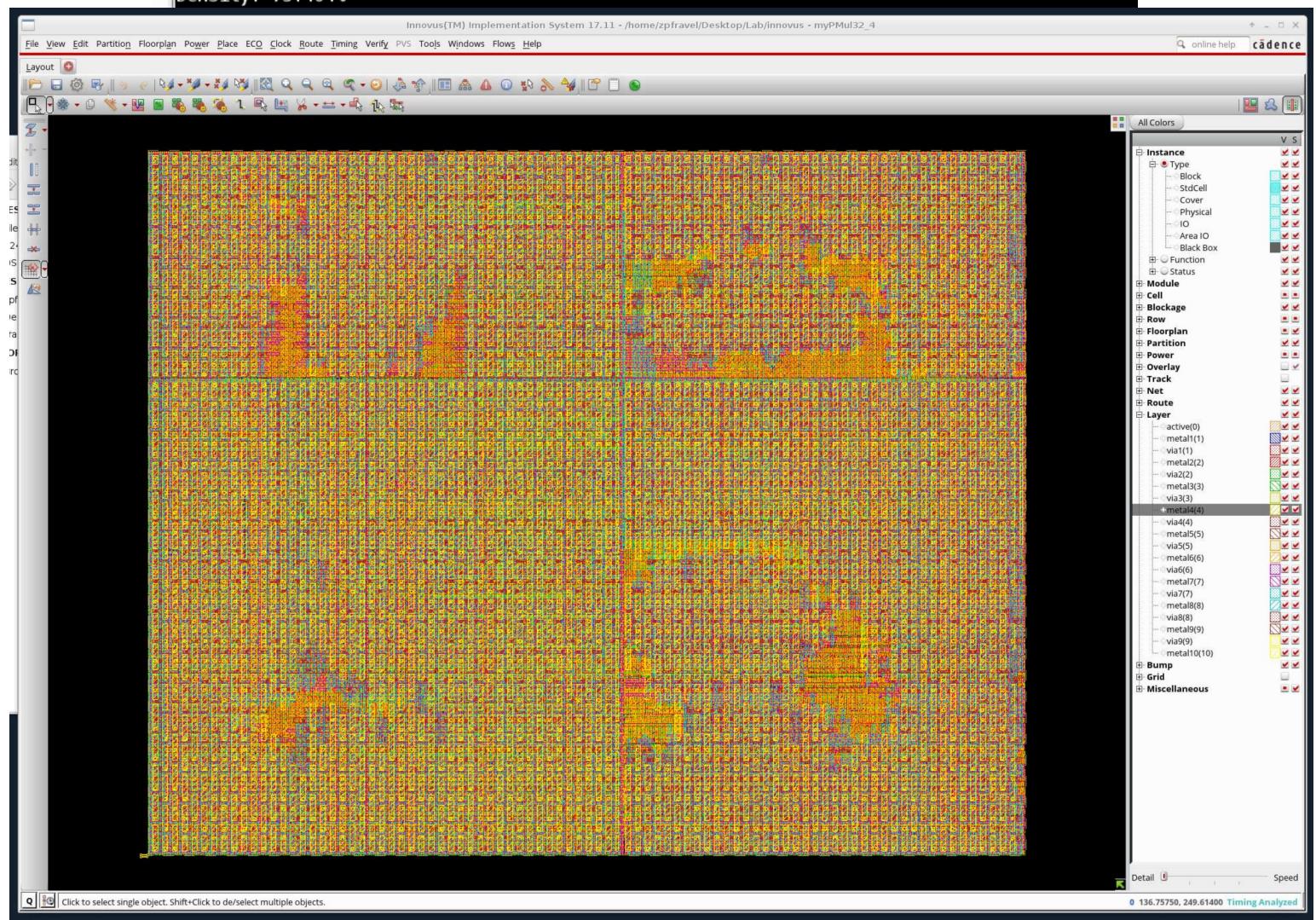
Density: 75.404%

Reported timing to dir ./timingReports
Total CPU time: 13.56 sec
Total Real time: 8.0 sec
Total Memory Usage: 1855.246094 Mbytes
innovus 10> innovus 10>

```

Getting closer to the end now, the next step is to do post route optimization and then metal fill insertion. The pictures are in the following order: post route optimization report, metal fill insertion, and post fill timing report.

optDesign Final Non-SI Timing Summary			
Setup views included:			
NG_view_typ			
Setup mode	all	reg2reg	default
WNS (ns)	0.014	0.014	6.319
TNS (ns)	0.000	0.000	0.000
Violating Paths	0	0	0
All Paths	384	256	128
DRVs		Real	Total
		Nr nets(terms)	Worst Vio
		Nr nets(terms)	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)
Density: 75.40%			



```

timeDesign Summary

Setup views included:
NG_view_typ

+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns): | 0.014 | 0.014 | 6.319 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 384 | 256 | 128 |
+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

Density: 75.404%

Reported timing to dir ./timingReports
Total CPU time: 13.56 sec
Total Real time: 8.0 sec
Total Memory Usage: 1855.246094 Mbytes
innovus 10> innovus 10>

```

Final images of each metal layer in the design is included at the appendix at the end. The following table was generated from information in the summary report generated by innovus.

General Design Information

Design Status	Routed
Design Name	myPmul32_4
# Instances	30722
# Hard Macros	0
# Std Cells	30722
# Pads	0
# Net	35535
# IO Pins	257

Floorplan/Placement Information

Total area of Standard Cells	42401.730 um ²
Total area of Core	56261.996 um ²
Total area of Chip	61177.206 um ²
Effective Utilization	7.5404e-01
Number of Cell Rows	151

Wire Length Distribution

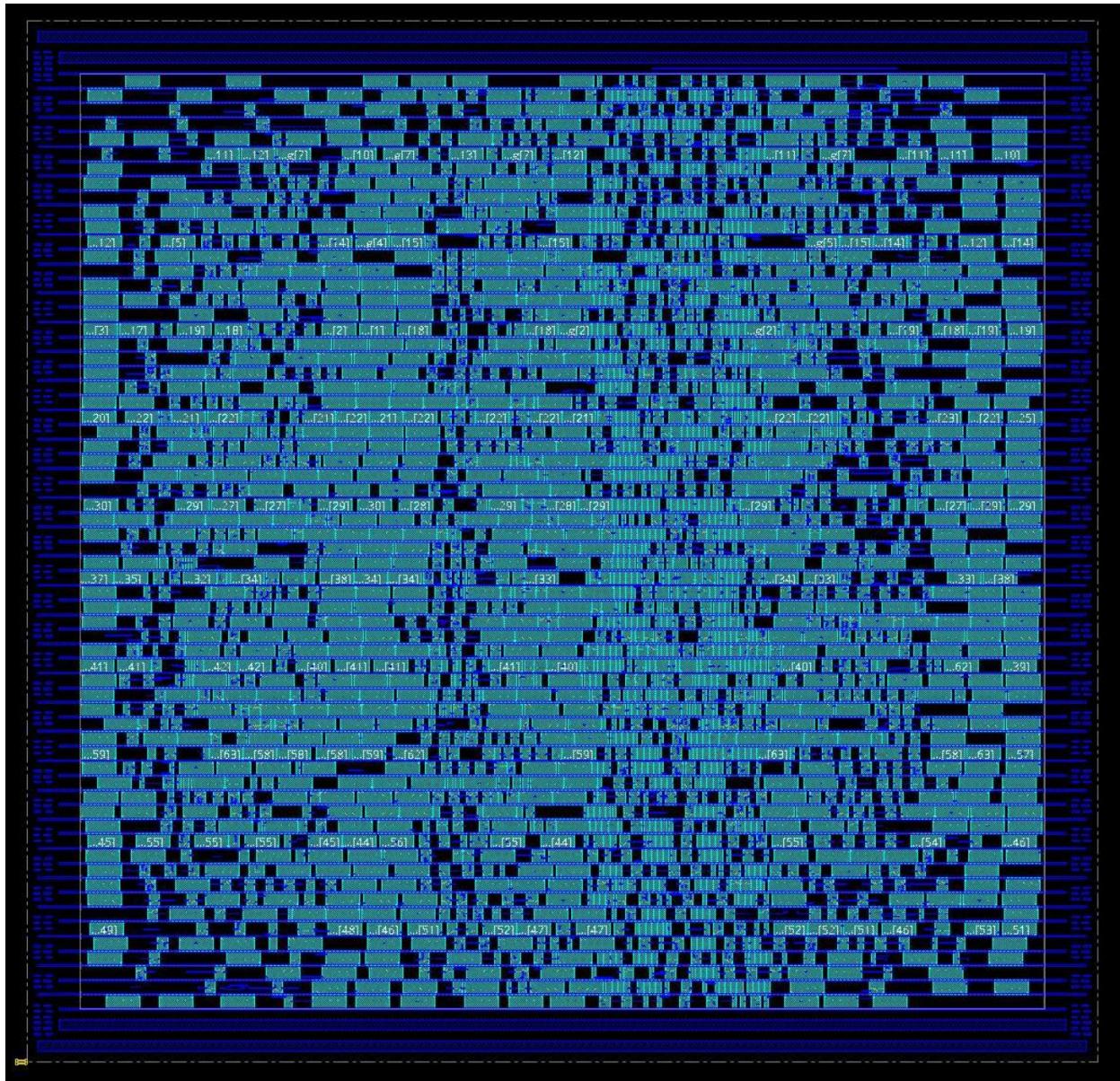
Total metal 1 wire length	7281.9600 um
Total metal 2 wire length	88169.5250 um
Total metal 3 wire length	91135.6450 um
Total metal 4 wire length	33213.1800 um
Total metal 5 wire length	14776.4400 um
Total metal 6 wire length	271.0400 um
Total wire length	234847.7900 um
Average wire length/net	6.6089 um

VQS64_4 Design Images

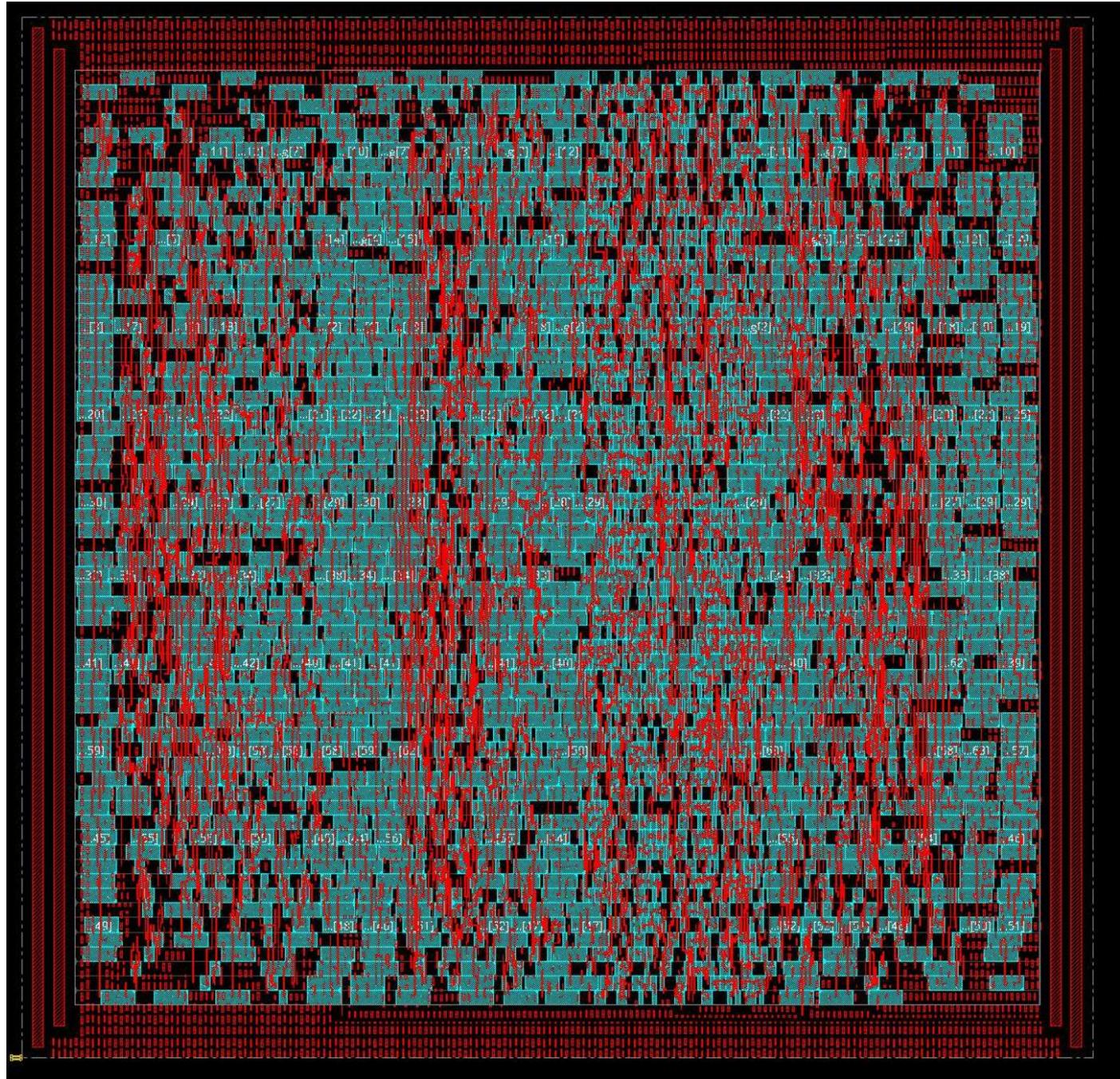
Standard Cells

Shown earlier in report

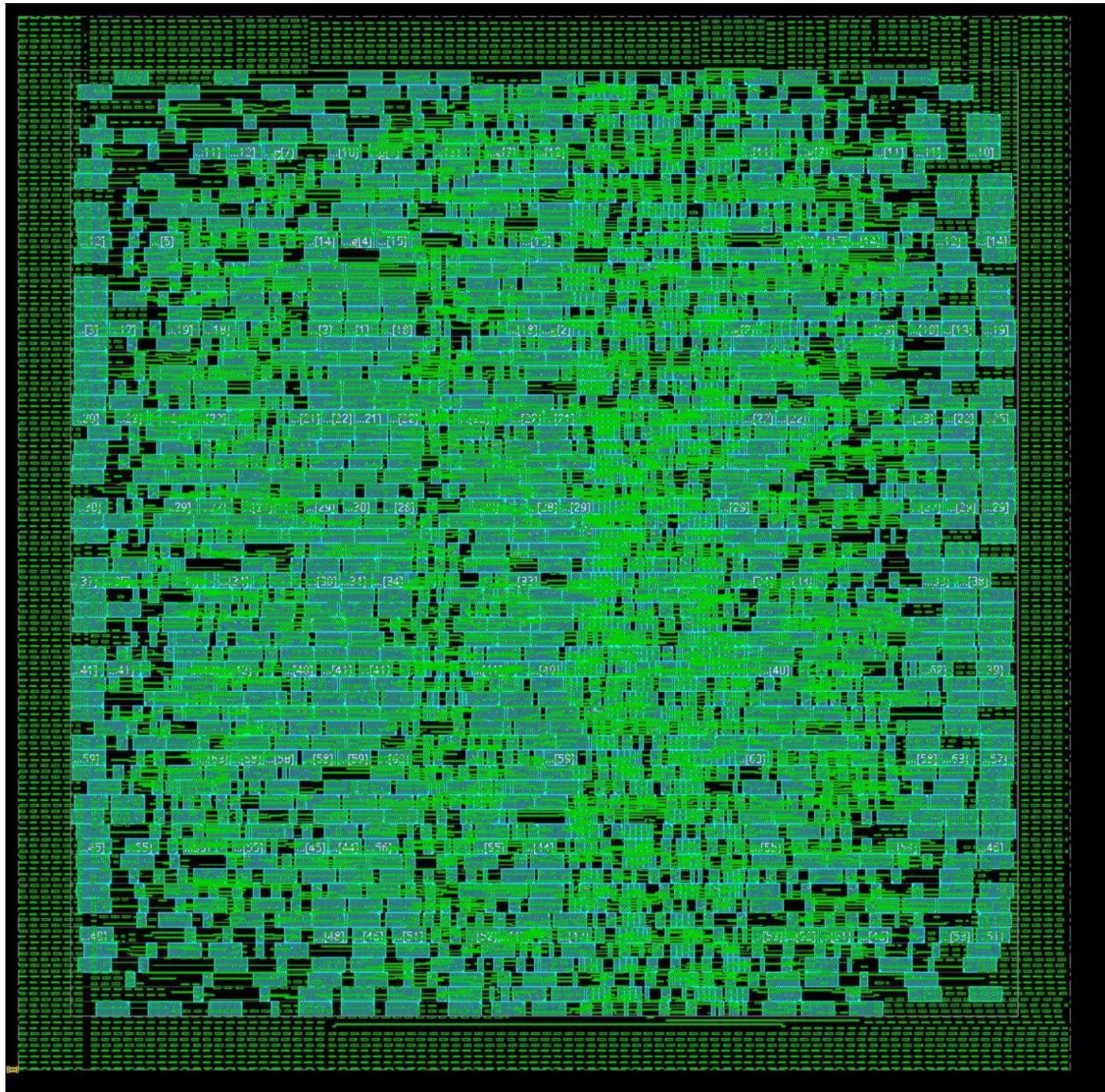
Metal 1



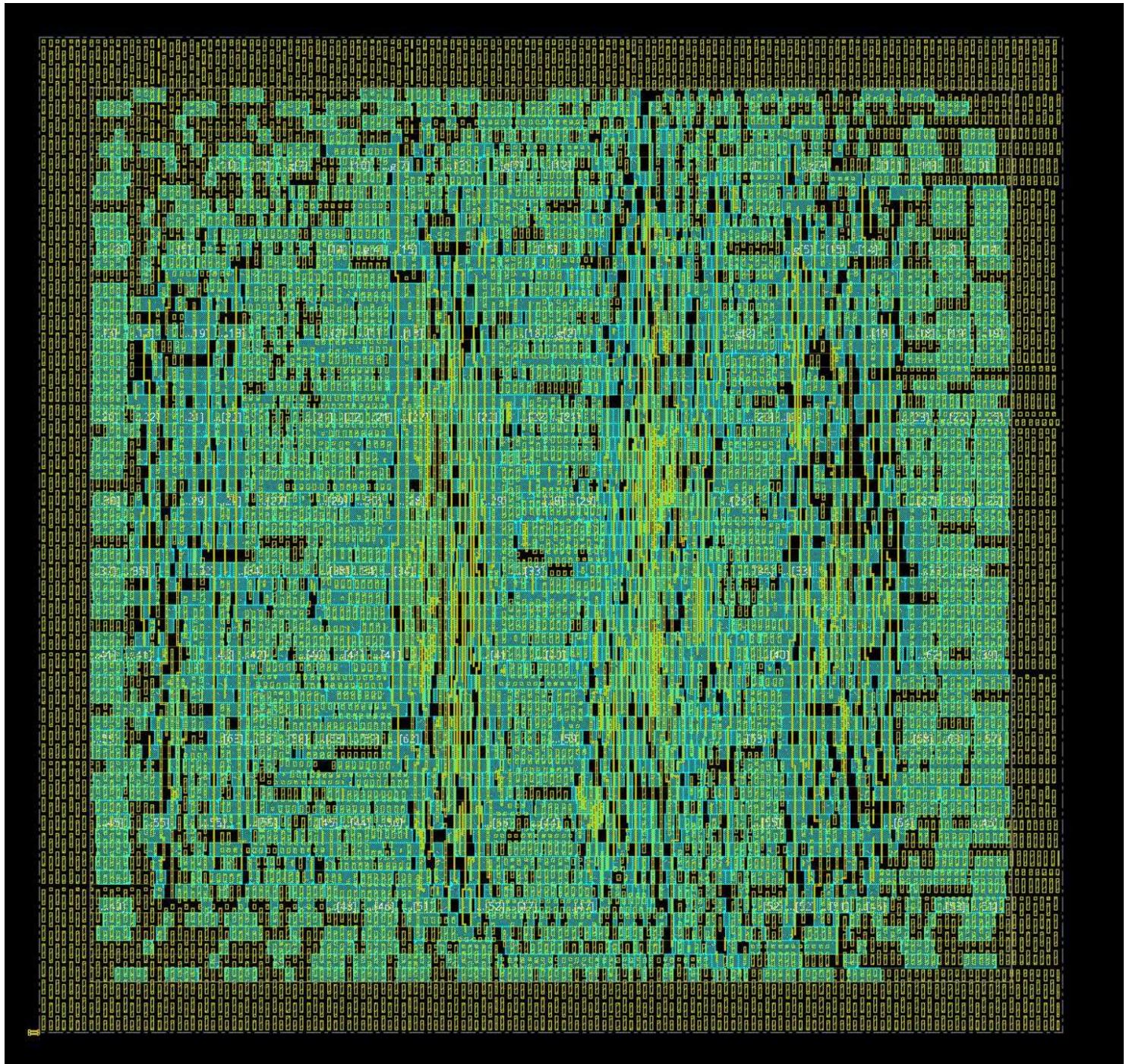
Metal 2



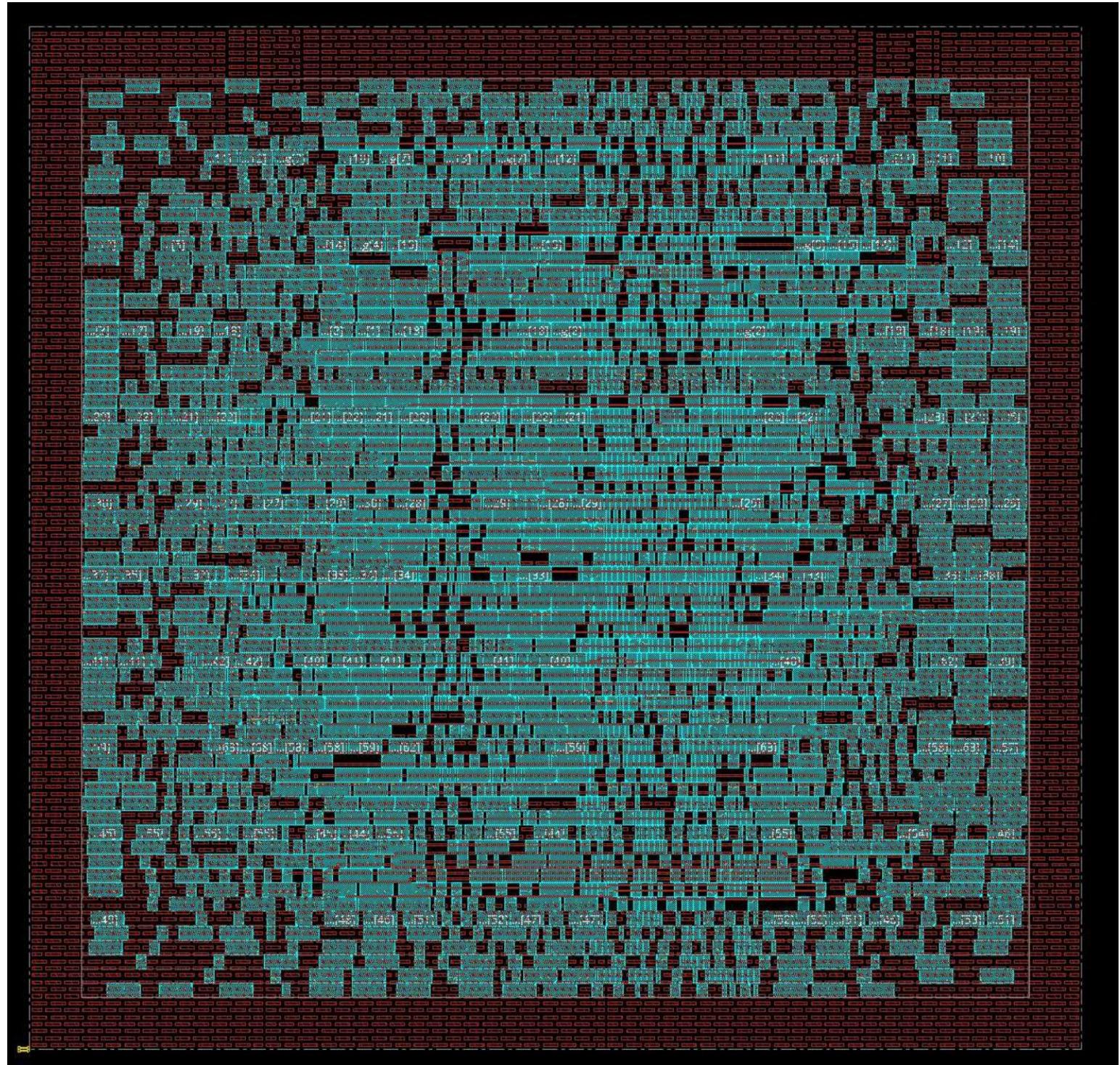
Metal 3



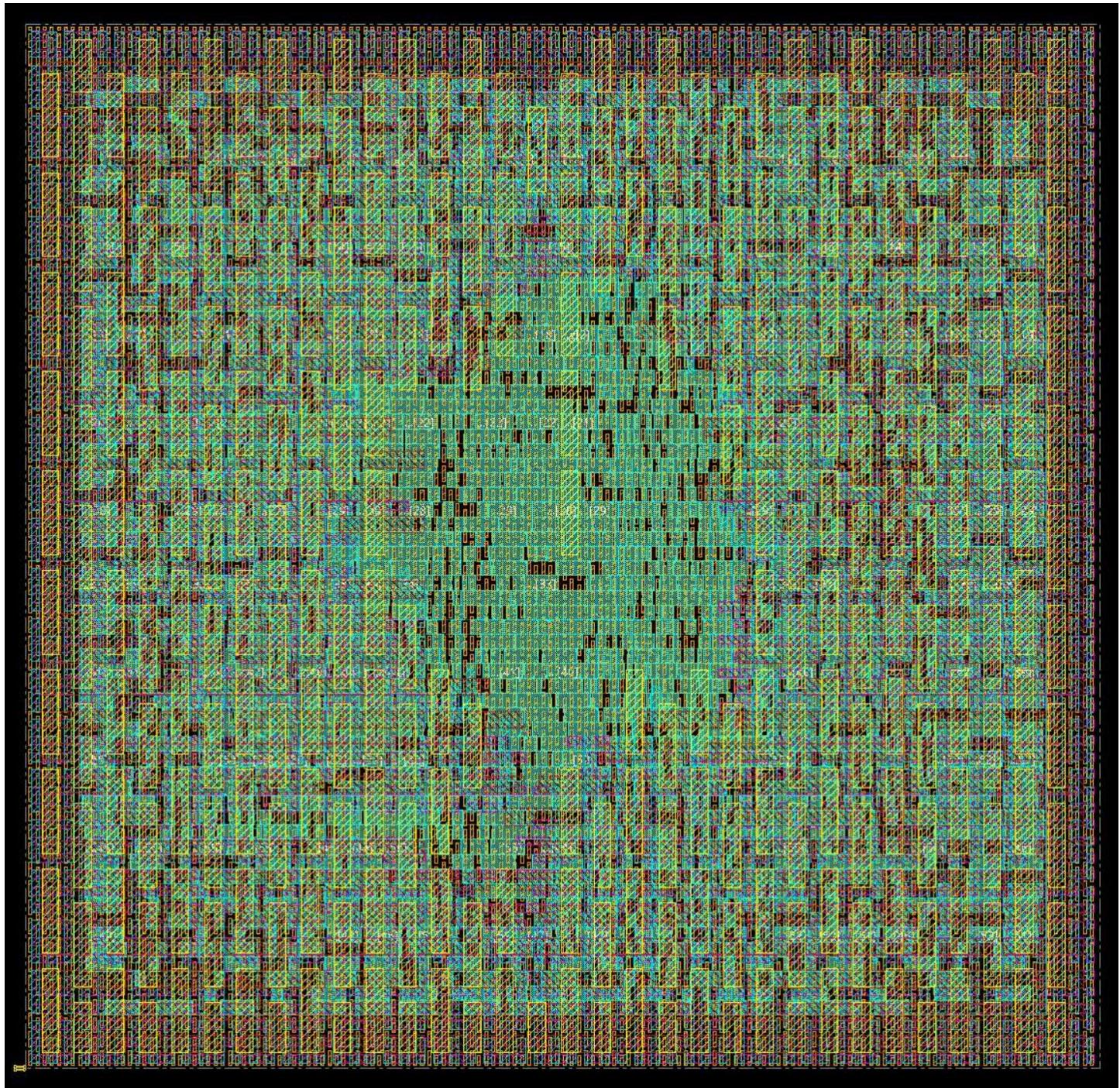
Metal 4



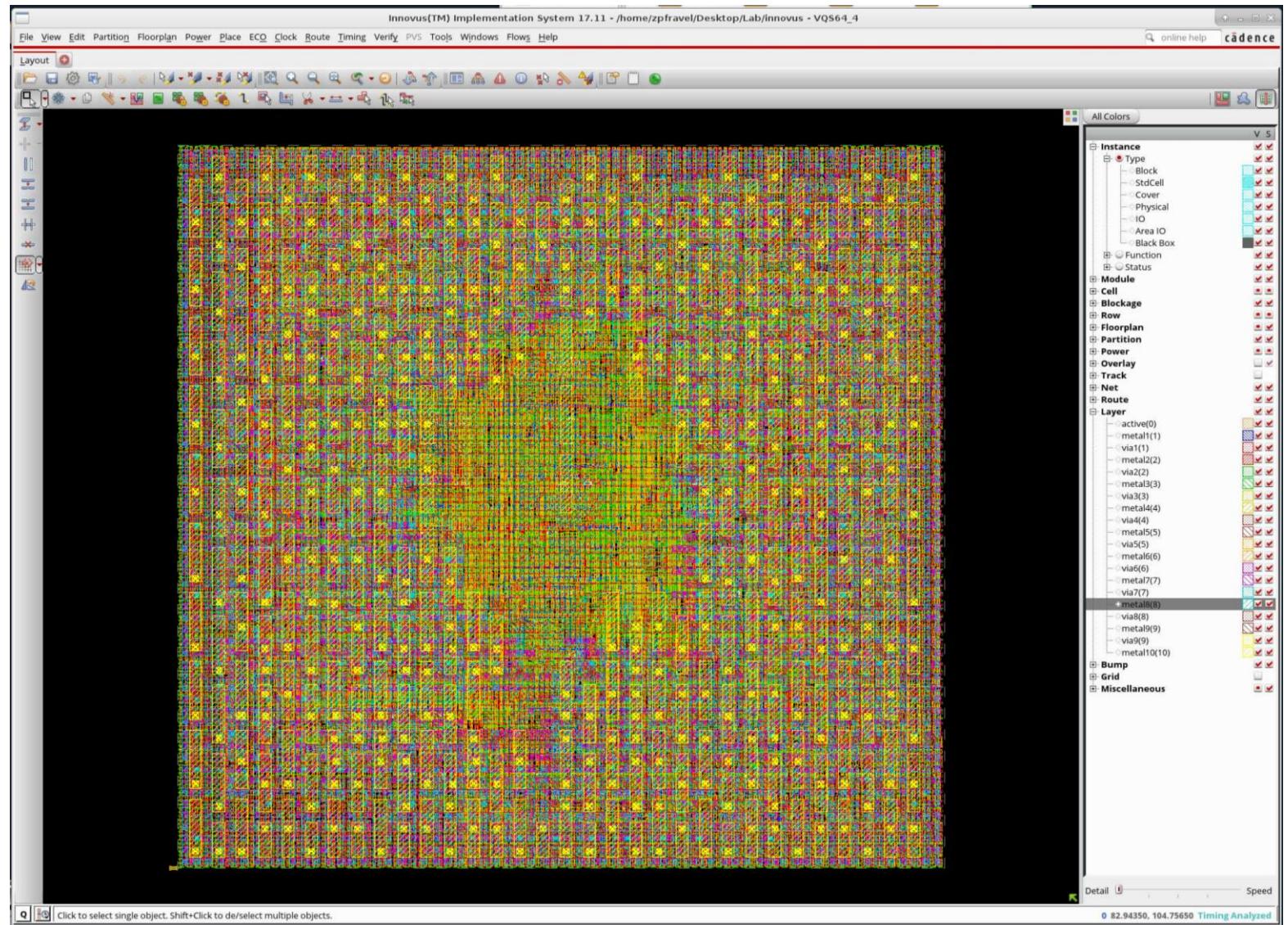
Metal 5



Metal Fill

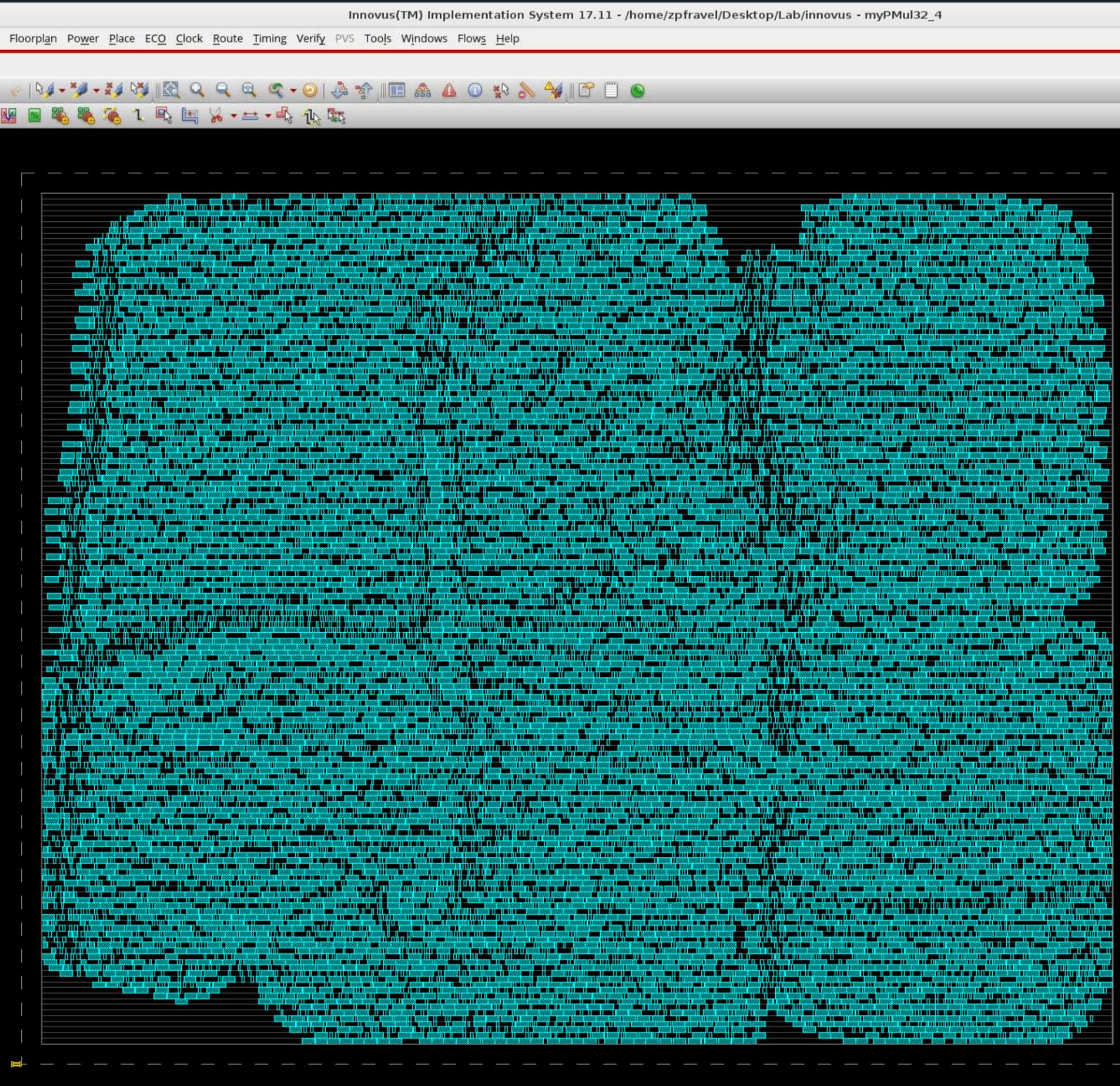


Complete Design



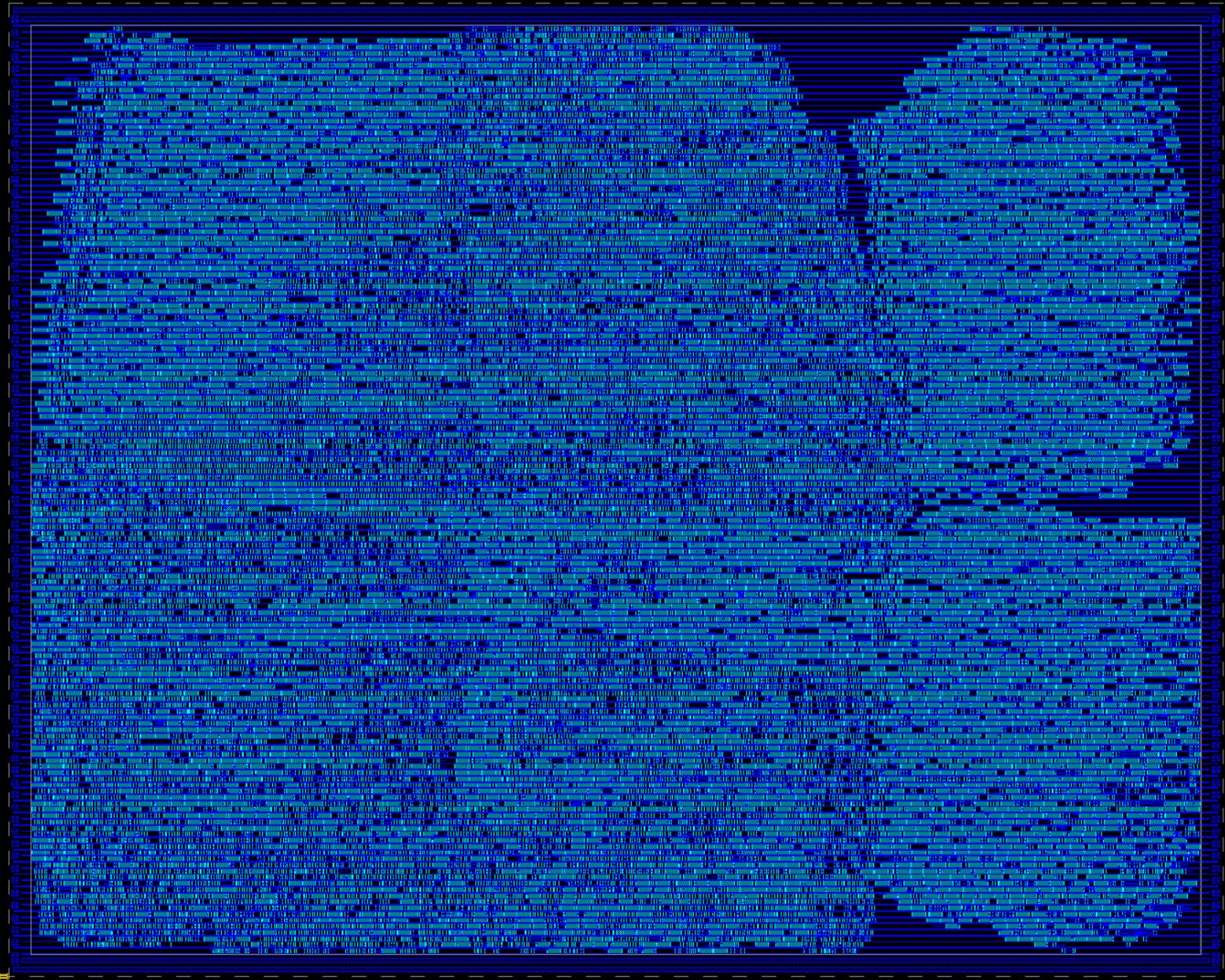
Pmul_32_4 Design Images

Standard Cells

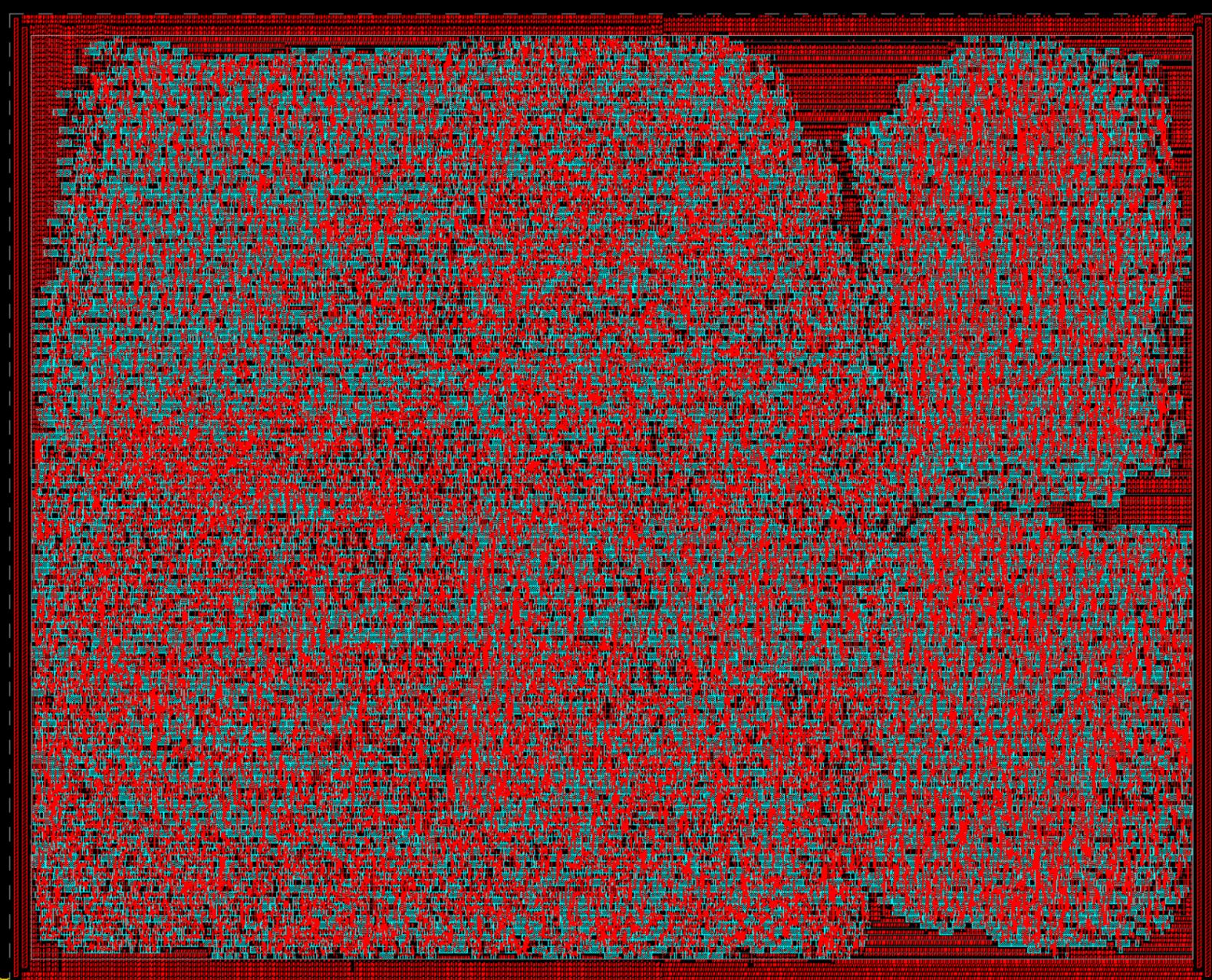


Single object. Shift+Click to de/select multiple objects.

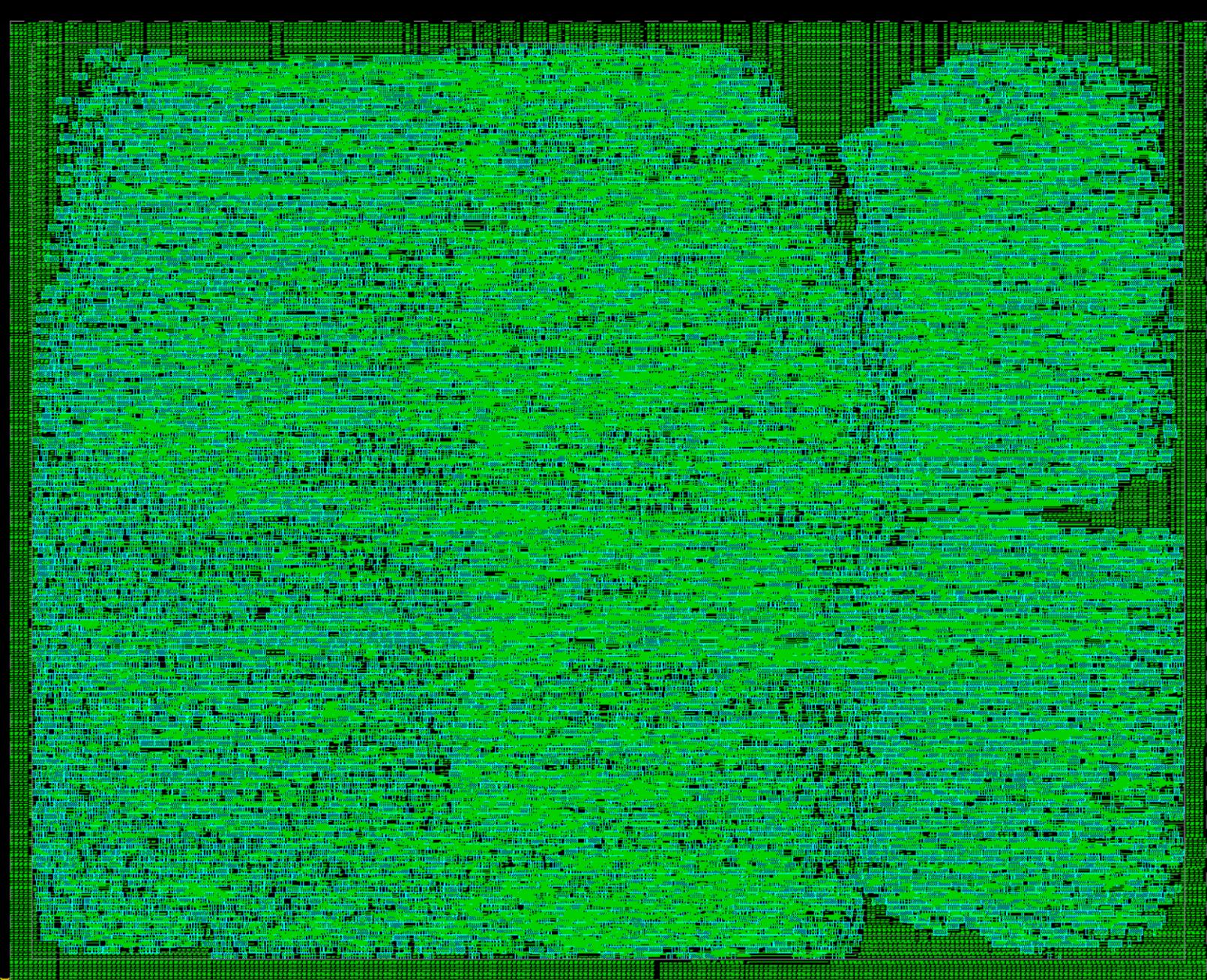
Metal 1



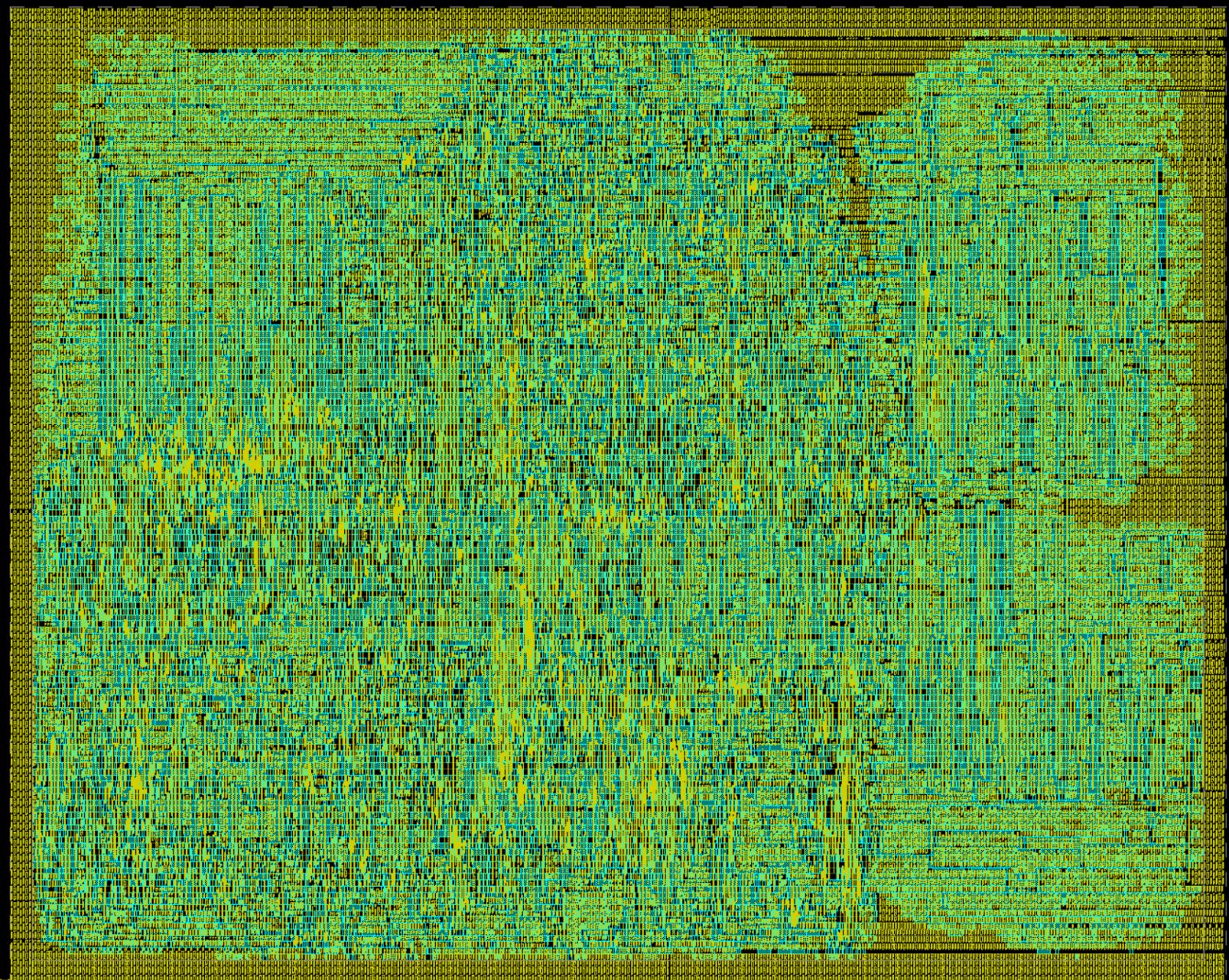
Metal 2



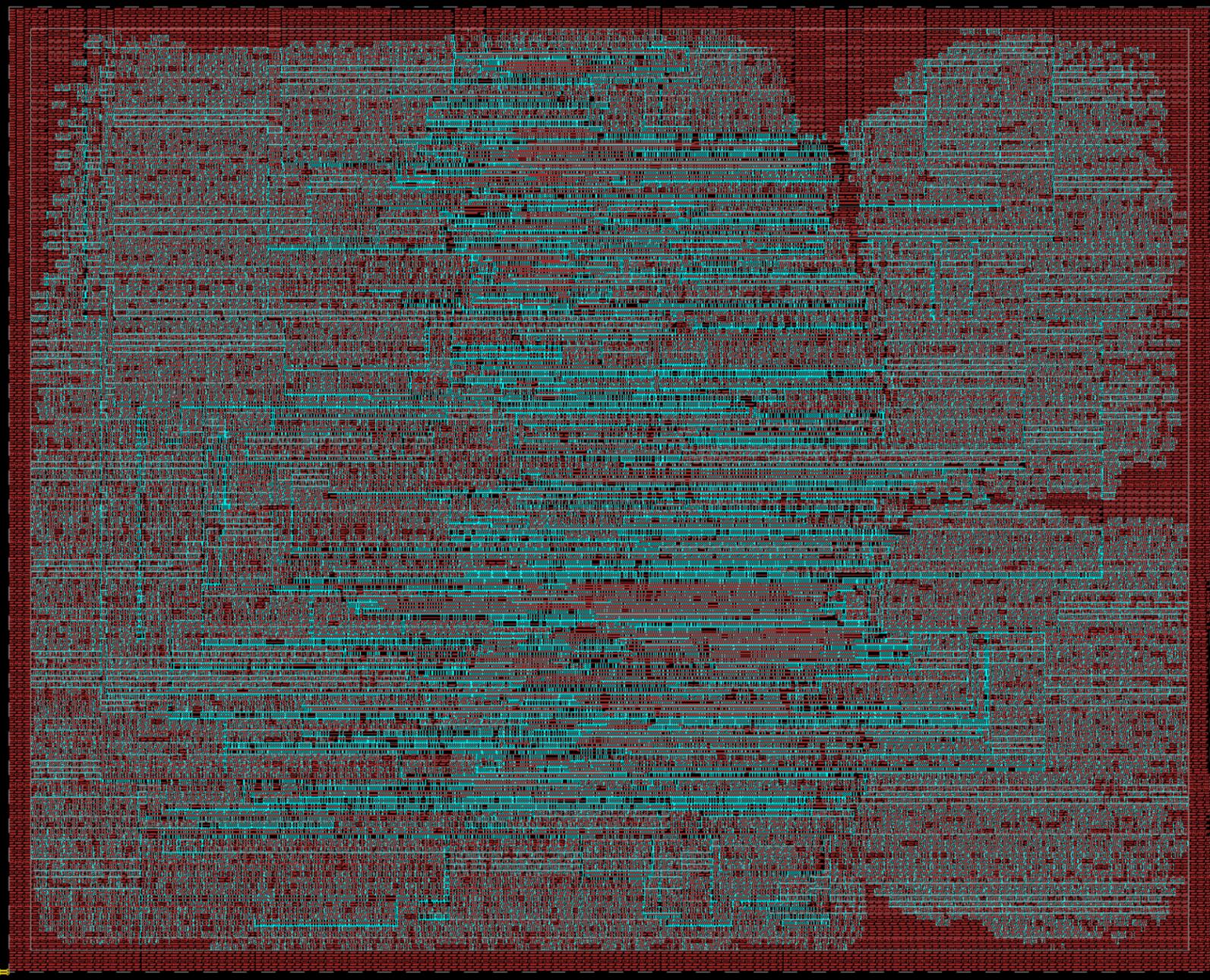
Metal 3



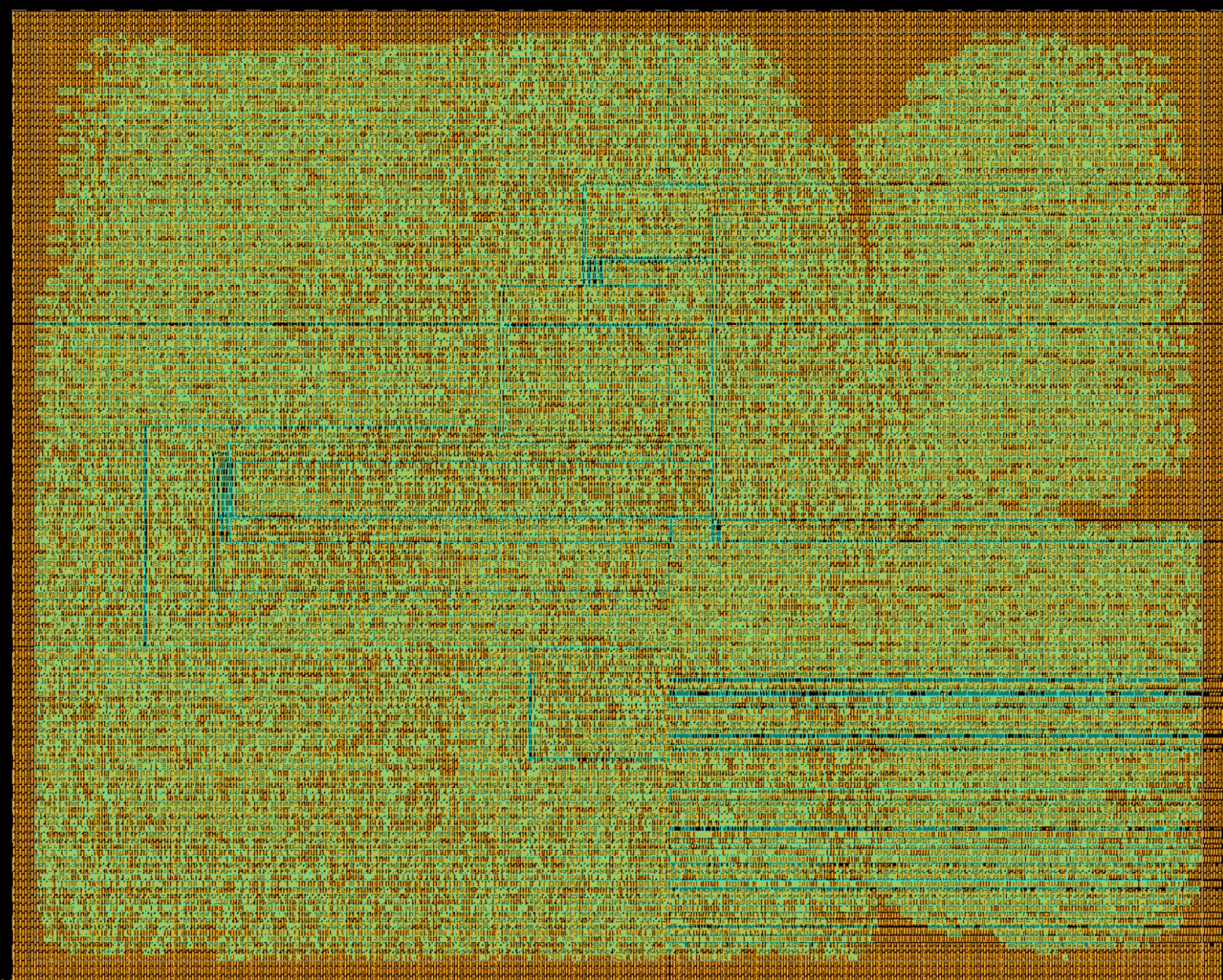
Metal 4



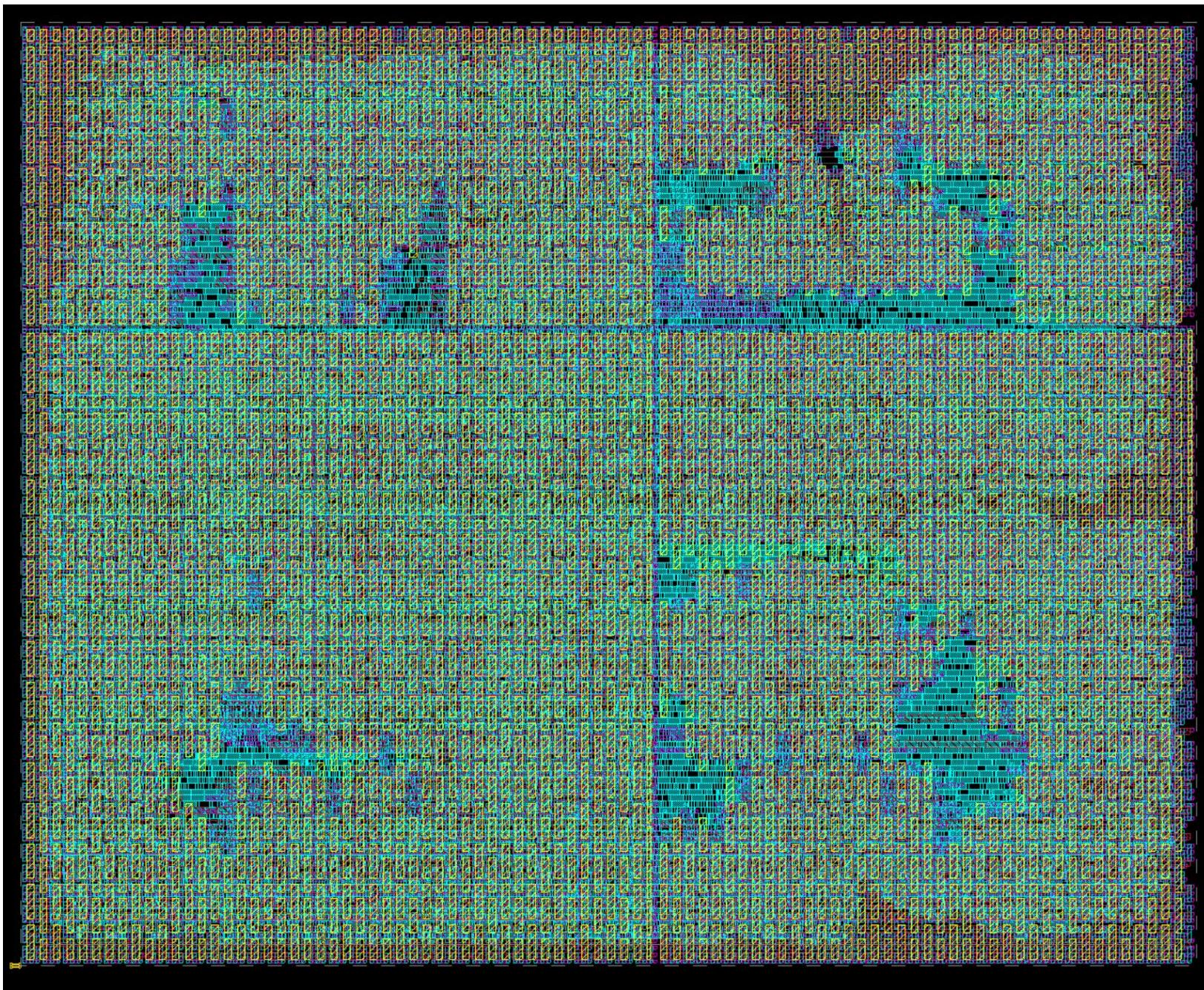
Metal 5



Metal 6



Metal Fill



Complete Design

