CSCE 3953 System Synthesis and Modeling

Project 5: Logic Synthesis and Timing Simulation

Instructor: Dr. Jia Di

Objectives and Tasks

- Objective – synthesize Verilog designs and perform post-synthesis timing simulation

- Synthesize both circuits developed in Project 3 and 4 using Synopsys 90nm library using Design Vision
- Simulate the synthesized circuits in ModelSim using the Synopsys Verilog library for timing following the tutorial
- Bonus – apply constraints to the sequential circuit to determine the fastest clock rate it can operate at, while the output is still correct

Report

- Project objective
- Synthesis process / constraints added
- Simulation method
- Result (simulation waveform screenshot, zoom in to show the delay)
- Analysis and conclusion
- Source code (pre- and post-synthesis file, testbench / .DO file)

- Due date: October 7, email your report to jdi@uark.edu in either Word or PDF format