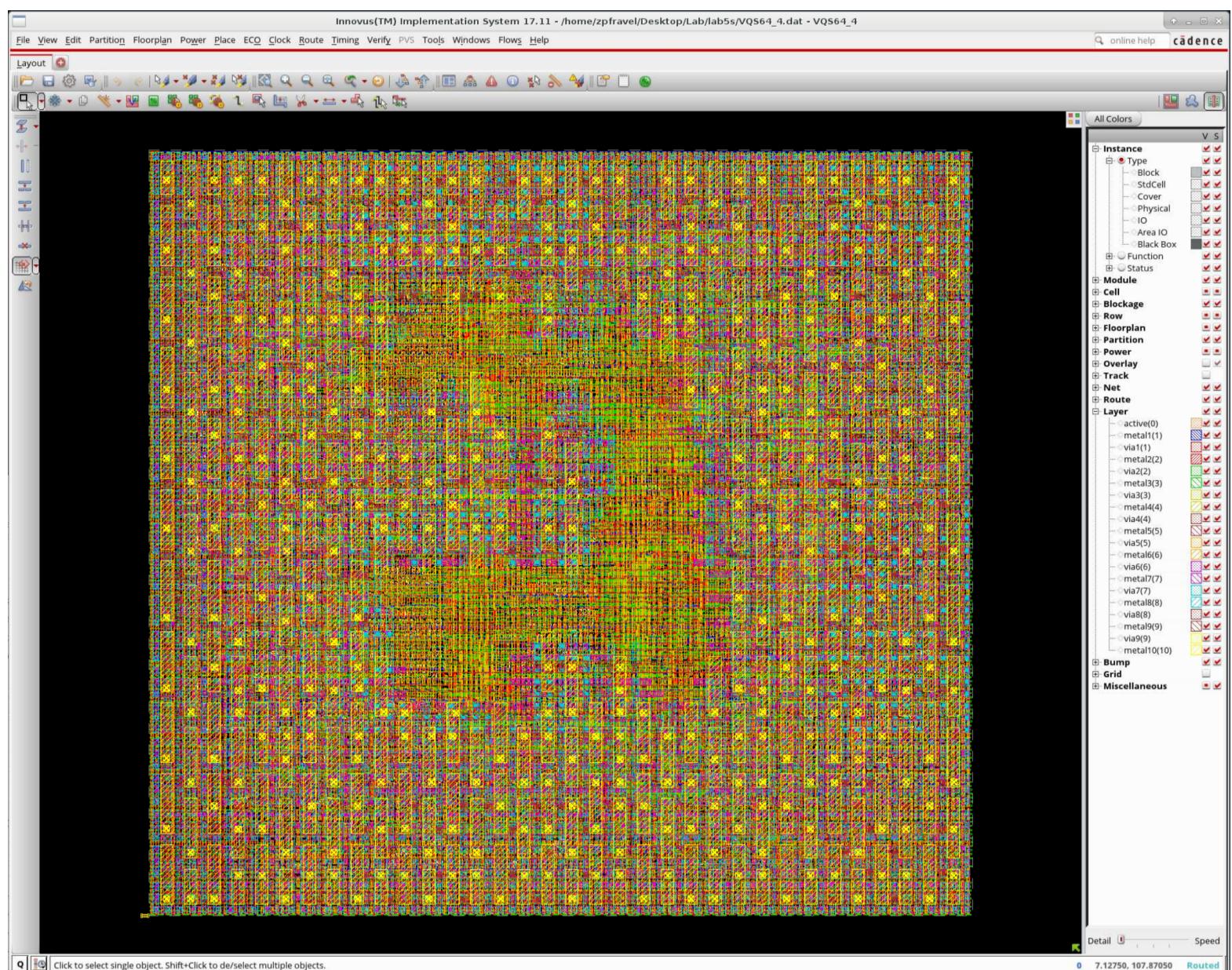
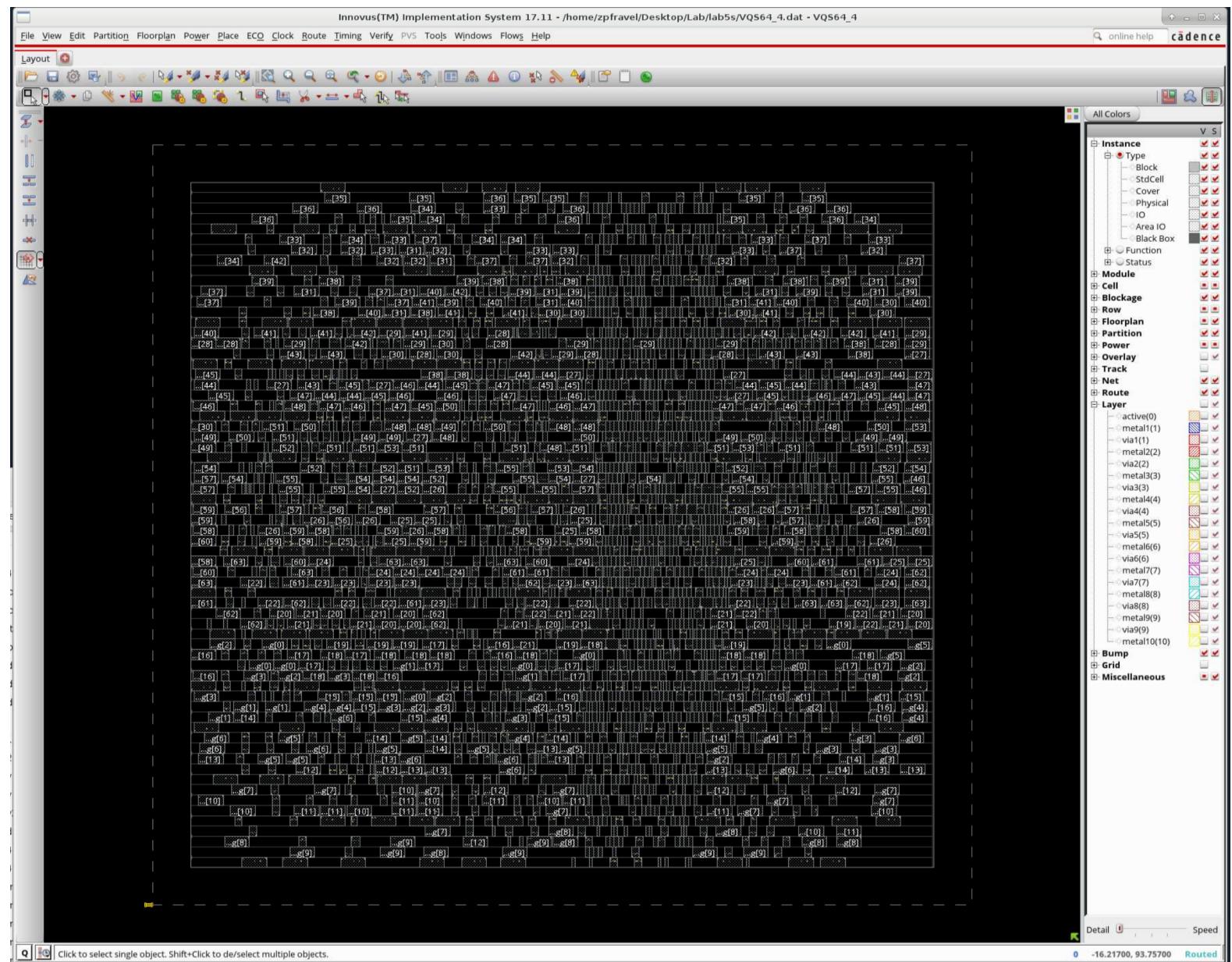


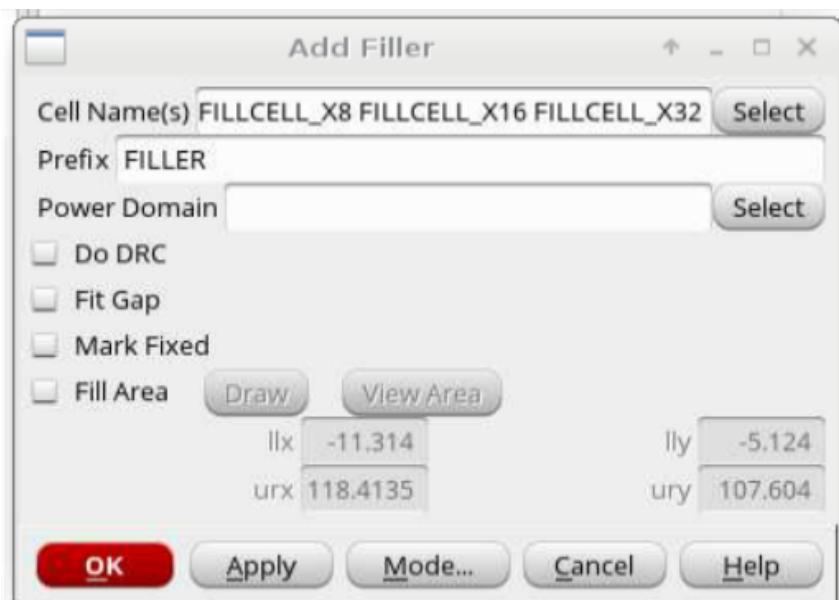
## 1. VQS64\_4

I started the lab by integrating the lab 5 solutions with the primetime libraries. The first step of the lab was to restore the design back into innovus so filler cells can be added. The following screenshots show the physical design before filler cells were added.

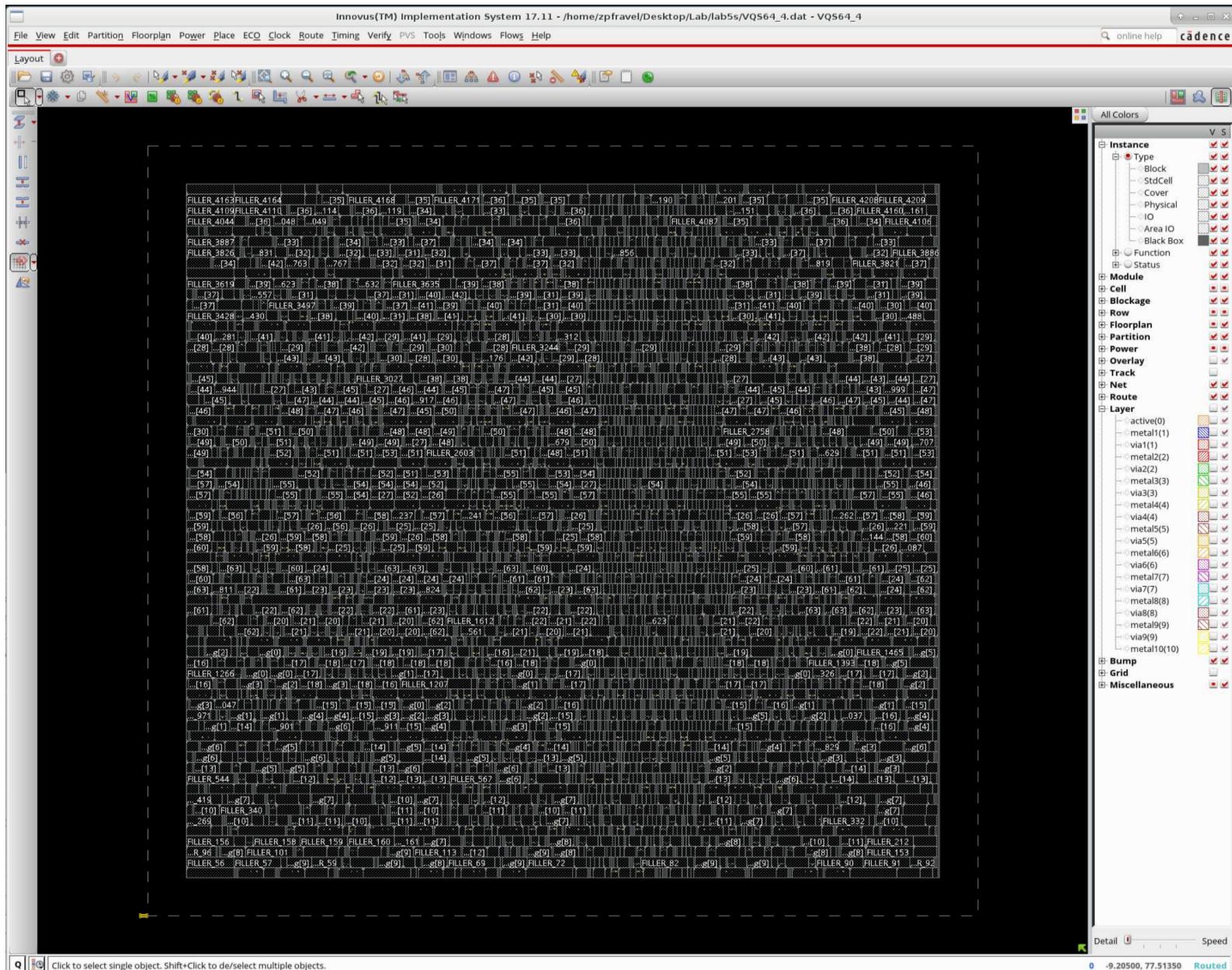




The following dialogue box below shows the filler settings that were used. All filler cell sizes ( $x1$ ,  $x2$ ,  $x4$ ,  $x8$ ,  $x16$ ,  $x32$ ) were utilized.



Here is a shot of the chip after filling, along with a shot of the console information showing the distribution of cells.



```

*INFO: Adding fillers to top-module.
*INFO: Added 68 filler insts (cell FILLCELL_X32 / prefix FILLER).
*INFO: Added 137 filler insts (cell FILLCELL_X16 / prefix FILLER).
*INFO: Added 329 filler insts (cell FILLCELL_X8 / prefix FILLER).
*INFO: Added 781 filler insts (cell FILLCELL_X4 / prefix FILLER).
*INFO: Added 2932 filler insts (cell FILLCELL_X1 / prefix FILLER).
*INFO: Added 0 filler inst (cell FILLCELL_X2 / prefix FILLER).
*INFO: Total 4247 filler insts added - prefix FILLER (CPU: 0:00:00.2).
For 4247 new insts, *** Applied 0 GNC rules (cpu = 0:00:00.0)

```

After filling all the standard cell rows, the next step is to perform parasitic extraction and export to a .spef file that Primetime can compare against.

```

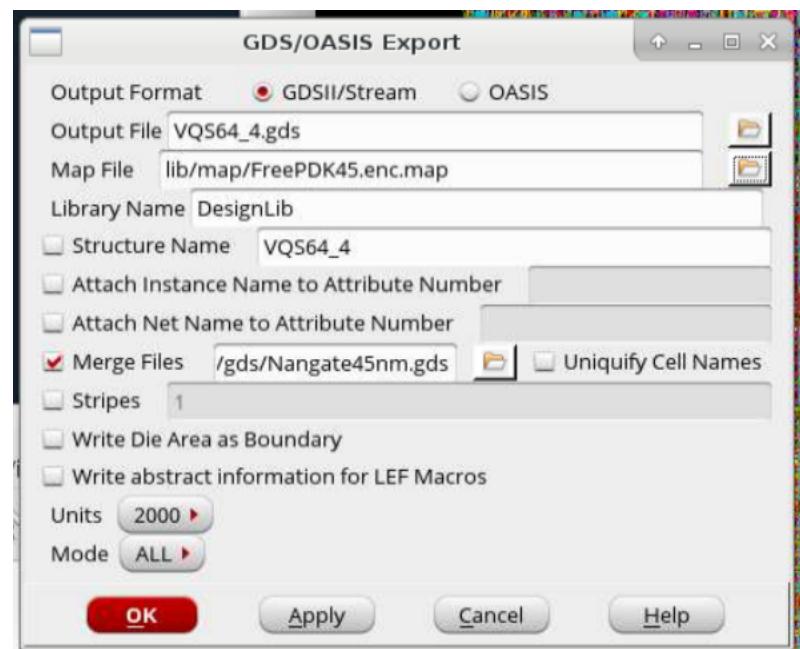
RC Mode: PostRoute -effortLevel low [Extended CapTable, RC Table Resistances]
  RC Corner Indexes          0
Capacitance Scaling Factor : 1.000000
Coupling Cap. Scaling Factor : 1.000000
Resistance Scaling Factor : 1.000000
Clock Cap. Scaling Factor : 1.000000
Clock Res. Scaling Factor : 1.000000
Shrink Factor              : 1.000000
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
Checking LVS Completed (CPU Time= 0:00:00.0  MEM= 1210.9M)
Extracted 10.0039% (CPU Time= 0:00:00.1  MEM= 1281.3M)
Extracted 20.0048% (CPU Time= 0:00:00.1  MEM= 1281.3M)
Extracted 30.0057% (CPU Time= 0:00:00.1  MEM= 1281.3M)
Extracted 40.0036% (CPU Time= 0:00:00.1  MEM= 1281.3M)
Extracted 50.0045% (CPU Time= 0:00:00.1  MEM= 1281.3M)
Extracted 60.0054% (CPU Time= 0:00:00.1  MEM= 1281.3M)
Extracted 70.0063% (CPU Time= 0:00:00.1  MEM= 1282.3M)
Extracted 80.0042% (CPU Time= 0:00:00.2  MEM= 1282.3M)
Extracted 90.0051% (CPU Time= 0:00:00.2  MEM= 1283.3M)
Extracted 100% (CPU Time= 0:00:00.3  MEM= 1284.3M)
Number of Extracted Resistors   : 52350
Number of Extracted Ground Cap. : 54740
Number of Extracted Coupling Cap. : 79788
Filtering XCap in 'relativeOnly' mode using values relative_c_threshold=0.03 and total_c_threshold=5fF.
  CORNER: NG_rc_typ
Checking LVS Completed (CPU Time= 0:00:00.0  MEM= 1268.3M)
PostRoute (effortLevel low) RC Extraction DONE (CPU Time: 0:00:00.5  Real Time: 0:00:01.0  MEM: 1268.297M)
RC Out has the following PVT Info:
  RC:NG_rc_typ, Operating temperature 25 C
Dumping Spef file.....
Printing D_NET...
rc0ut completed:: 100 %
RC Out from RCDB Completed (CPU Time= 0:00:00.1  MEM= 1268.3M)

```



Next we need to move to Calibre to perform a DRC report on the circuit, but before we can do that we must export the GDS layout, making sure to use the FreePDK45 map file and merging with the Nangate45nm.gds.

The next page shows the information generated on the console from the GDS export. Along with exporting to GDS, I also saved the netlist file for use with Primetime later on.

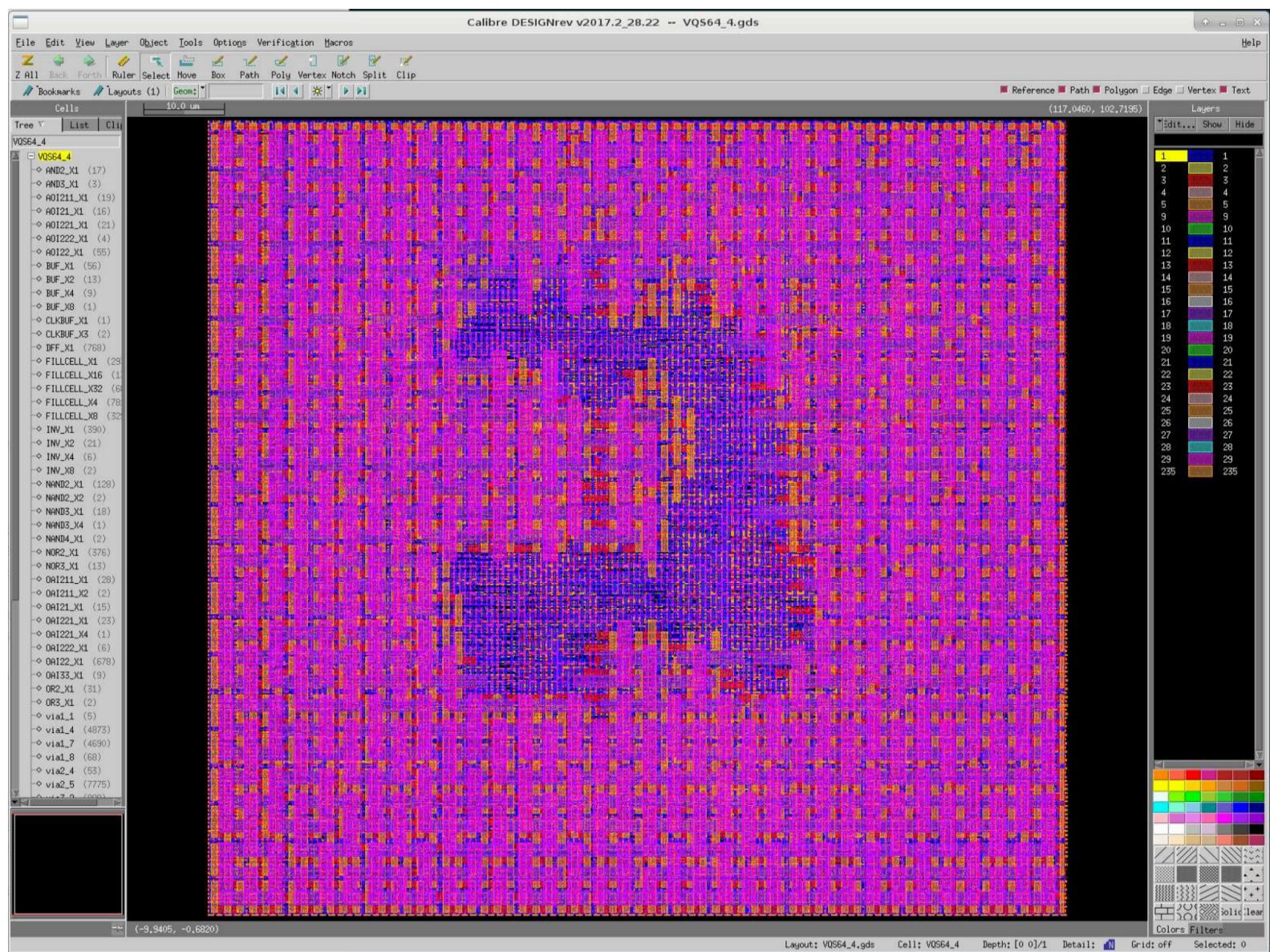


Stream Out Information Processed for GDS version 5:

Units: 2000 DBU

Object	Count	
Instances	6986	
Ports/Pins	0	
Nets	33234	
metal layer metal1	3304	Output for instance
metal layer metal2	17014	Output for bump
metal layer metal3	11625	Output for physical terminals
metal layer metal4	1156	Output for logical terminals
metal layer metal5	135	Output for regular nets
Via Instances	18493	Output for special nets and metal fills Output for via structure generation
Special Nets	209	Statistics for GDS generated (version 5)
metal layer metal1	205	
metal layer metal2	4	
Via Instances	142	
Metal Fills	38532	
metal layer metal1	524	9    poly
metal layer metal2	4842	11     metal1
metal layer metal3	6128	12     vial
metal layer metal4	7465	13     metal2
metal layer metal5	7423	14     via2
metal layer metal6	8949	15     metal3
metal layer metal7	1285	16     via3
metal layer metal8	1286	17     metal4
metal layer metal9	318	18     via4
metal layer metal10	312	19     metal5
Via Instances	29971	20     via5
		21     metal6
		22     via6
Metal FillOPCs	0	23     metal7
Via Instances	0	24     via7
Text	0	25     metal8
		26     via8
Blockages	0	27     metal9
		28     via9
Custom Text	0	29     metal10
Custom Box	0	Stream Out Information Processed for GDS version 5:
Trim Metal	0	Units: 2000 DBU
Merging with GDS libraries		
Scanning GDS file lib/gds/Nangate45nm.gds to register cell name .....		
Merging GDS file lib/gds/Nangate45nm.gds .....		
***** Merge file: lib/gds/Nangate45nm.gds has version number: 5.		
***** Merge file: lib/gds/Nangate45nm.gds has units: 2000 per micron.		
***** unit scaling factor = 1 *****		
#####Streamout is finished!		

Now that the layout is exported, it can be loaded into Calibre to perform the DRC report. The following is a screenshot of the design loaded into Calibre.



The following are screenshots of the successful DRC report generated by Calibre.

Calibre - RVE v2017.2\_28.22 : VQS64\_4.drc.results

File View Highlight Tools **Window** Setup

Show All **No Results Found**

Check / Cell	Results
Check Well.1	0
Check Well.2	0
Check Well.4	0
Check Poly.1	0
Check Poly.2	0
Check Poly.3	0
Check Poly.4	0
Check Poly.5	0
Check Poly.6	0
Check Active.1	0
Check Active.2	0
Check Active.3	0
Check Active.4	0
Check Implant.1	0
Check Implant.2	0

Rule File Pathname: /home/zpfravel/Desktop/Lab/lab5s/\_calibreDRC.rul\_

Nwell and Pwell must not overlap

Check Well.1

DRC Summary Report - VQS64\_4.drc.summary

File Edit Options Windows

```
RULECHECK Metal2.9 .... TOTAL Result Count = 0 (0)
RULECHECK Metal3.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal3.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal3.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal3.8 .... TOTAL Result Count = 0 (0)
RULECHECK Metal3.9 .... TOTAL Result Count = 0 (0)
RULECHECK Metal4.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal4.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal4.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal4.8 .... TOTAL Result Count = 0 (0)
RULECHECK Metal5.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal5.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal5.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal5.8 .... TOTAL Result Count = 0 (0)
RULECHECK Metal6.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal6.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal6.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal6.8 .... TOTAL Result Count = 0 (0)
RULECHECK Metal7.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal7.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal7.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal8.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal8.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal8.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal9.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal9.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal10.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal10.6 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.1 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.2 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.3 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.4 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.5 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.6 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.7 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.8 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.9 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.10 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.11 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.12 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.13 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.14 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.15 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.16 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.17 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.18 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.19 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.20 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.21 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.22 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.23 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.24 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.25 ..... TOTAL Result Count = 0 (0)
RULECHECK Grid.26 ..... TOTAL Result Count = 0 (0)
```

--- RULECHECK RESULTS STATISTICS (BY CELL)

---

--- SUMMARY

---

```
TOTAL CPU Time: 4
TOTAL REAL Time: 4
TOTAL Original Layer Geometries: 73694 (387127)
TOTAL DRC RuleChecks Executed: 156
TOTAL DRC Results Generated: 0 (0)
```

Finally, we're ready to perform power and timing analysis with primetime. Using the pt.tcl script and the updated verilog netlist from innovus, we can run the following command to perform analysis.

```
pt_shell -f pt.tcl
```

Here is a screenshot of the pt.tcl script used for VQS64\_4. We have a 5 ns clock period instantiated with the timing and power reports coming out to two separate files.

```

Open pt.tcl ~Desktop/Lab/lab5s Save
suppress_message "RC-004 RC-008 RC-009 PTE-060"

set target_library "lib/db/NangateOpenCellLibrary_typical_ecsm.db"
set link_library "* lib/db/NangateOpenCellLibrary_typical_ecsm.db"

set topname VQS64_4

set myPeriod_ns 5
set myClk [list mCLK]

read_verilog ${topname}.v
current_design $topname

link

create_clock -period $myPeriod_ns $myClk
set_ideal_network [get_port $myClk]
read_parasitics $topname.spef -keep_capacitive_coupling
complete_net_parasitics -complete_with zero
report_annotated_parasitics -check

set power_enable_analysis TRUE

set_switching_activity -static_probability 0.5 -toggle_rate 0.15 -base_clock $myClk [remove_from_collection [all_inputs] $myClk]
set_switching_activity -static_probability 0.5 -toggle_rate 0.15 -base_clock $myClk -type registers -hierarchy

update_timing
report_timing -group $myClk -capacitance -transition_time > $topname.timing.pt.rpt

update_power
report_power >> $topname.power.pt.rpt

exit

```

Here is the power report generated by Primetime.

\*VQS64\_4.power.pt.rpt - Mousepad

File Edit Search View Document Help

\*\*\*\*\*
Report : Averaged Power
Design : VQS64\_4
Version: M-2017.06-SP1
Date : Sat Nov 18 16:31:48 2017
\*\*\*\*\*

Attributes

-----

Power Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Attrs
clock_network	5.569e-04	0.0000	0.0000	5.569e-04 (39.95%)	i
register	2.295e-04	9.434e-05	6.076e-05	3.846e-04 (27.59%)	
combinational	1.701e-04	2.305e-04	5.202e-05	4.526e-04 (32.47%)	
sequential	0.0000	0.0000	0.0000	0.0000 ( 0.00%)	
memory	0.0000	0.0000	0.0000	0.0000 ( 0.00%)	
io_pad	0.0000	0.0000	0.0000	0.0000 ( 0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000 ( 0.00%)	
Net Switching Power	= 3.248e-04	(23.30%)			
Cell Internal Power	= 9.566e-04	(68.61%)			
Cell Leakage Power	= 1.128e-04	( 8.09%)			
-----					
Total Power	= 1.394e-03	(100.00%)			

1

VQS64\_4.timing.pt.rpt - Mousepad

File Edit Search View Document Help

```
*****
Report : timing
  -path_type full
  -delay_type max
  -max_paths 1
  -group mCLK
  -transition_time
  -capacitance
  -sort_by slack
Design : VQS64_4
Version: M-2017.06-SP1
Date   : Sat Nov 18 16:31:46 2017
*****
```

Startpoint: rC4\_reg[14]  
(rising edge-triggered flip-flop clocked by mCLK)

Endpoint: rC6\_reg[24]  
(rising edge-triggered flip-flop clocked by mCLK)

Path Group: mCLK  
Path Type: max

Point	Cap	Trans	Incr	Path
clock mCLK (rise edge)	0.00	0.00	0.00	
clock network delay (ideal)			0.00	0.00
rC4_reg[14]/CK (DFF_X1)	0.00	0.00	0.00 r	
rC4_reg[14]/Q (DFF_X1)	1.82	0.01	0.09 &	0.09 r
U4491/ZN (OAI22_X1)	3.18	0.01	0.02 &	0.11 f
U4500/ZN (AOI21_X1)	1.86	0.02	0.04 &	0.15 r
U4499/ZN (OAI211_X1)	1.88	0.01	0.03 &	0.18 f
U4345/ZN (INV_X1)	3.60	0.01	0.02 &	0.20 r
U4454/ZN (OAI211_X1)	1.61	0.01	0.03 &	0.23 f
U3219/ZN (OR2_X1)	2.09	0.01	0.05 &	0.28 f
U3221/ZN (NAND3_X1)	2.90	0.01	0.02 &	0.29 r
FE_RC_600_0/ZN (OAI33_X1)	1.65	0.02	0.02 &	0.31 f
U3813/ZN (AOI211_X1)	2.01	0.04	0.07 &	0.38 r
U3126/ZN (AOI21_X1)	1.66	0.01	0.02 &	0.40 f
U3128/ZN (INV_X1)	1.97	0.01	0.02 &	0.42 r
FE_RC_599_0/ZN (AOI221_X1)	4.99	0.02	0.02 &	0.44 f
U4645/ZN (AOI21_X1)	1.83	0.02	0.03 &	0.47 r
U4722/ZN (AOI221_X1)	2.03	0.03	0.02 &	0.49 f
U4721/ZN (AOI222_X1)	2.15	0.05	0.08 &	0.58 r
U3202/ZN (NAND2_X1)	1.60	0.01	0.02 &	0.60 f
U3201/ZN (AND2_X1)	2.26	0.01	0.03 &	0.63 f
U4606/ZN (AOI211_X1)	2.02	0.04	0.04 &	0.67 r
U3142/ZN (NOR2_X1)	1.86	0.01	0.01 &	0.68 f
U4686/ZN (OAI221_X1)	3.80	0.05	0.03 &	0.71 r
U3118/Z (BUF_X2)	8.37	0.01	0.04 &	0.74 r
U4586/ZN (INV_X1)	6.97	0.01	0.02 &	0.76 f
U3110/ZN (INV_X1)	46.73	0.11	0.12 &	0.88 r
U4465/ZN (OAI22_X1)	5.59	0.03	0.05 &	0.93 f
rC6_reg[24]/D (DFF_X1)		0.03	0.00 &	0.93 f
data arrival time				0.93
clock mCLK (rise edge)	0.00	5.00	5.00	
clock network delay (ideal)		0.00	5.00	
clock reconvergence pessimism		0.00	5.00	
rC6_reg[24]/CK (DFF_X1)			5.00 r	
library setup time			-0.05	4.95
data required time				4.95
-----				
data required time				4.95
data arrival time				-0.93
-----				
slack (MET)				4.02

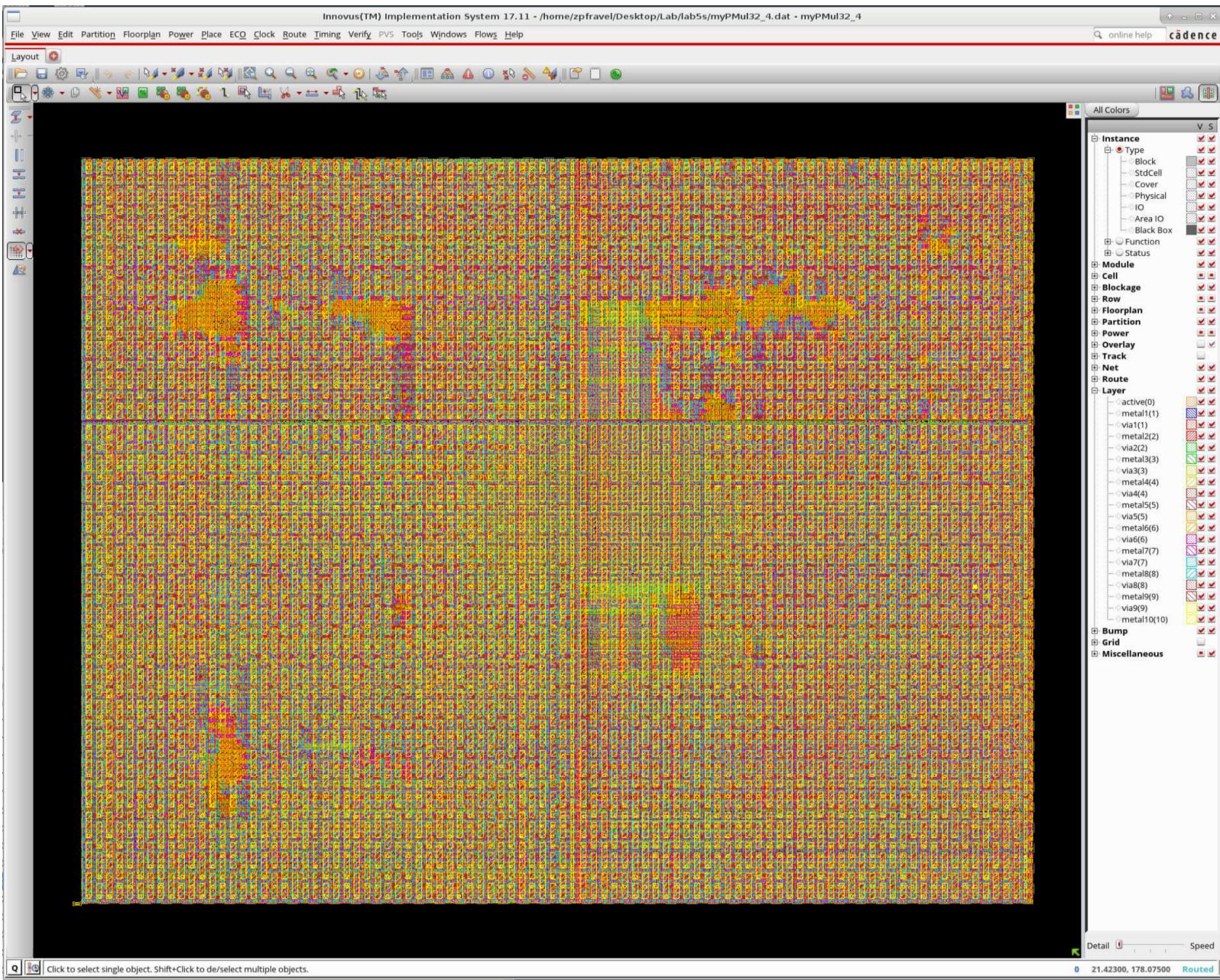
1

Finally, here is the timing report generated by Primetime.

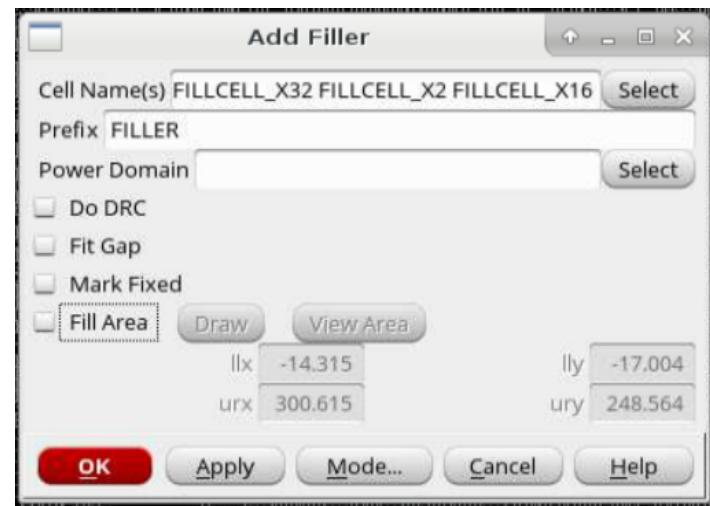


## 2. PMul32\_4

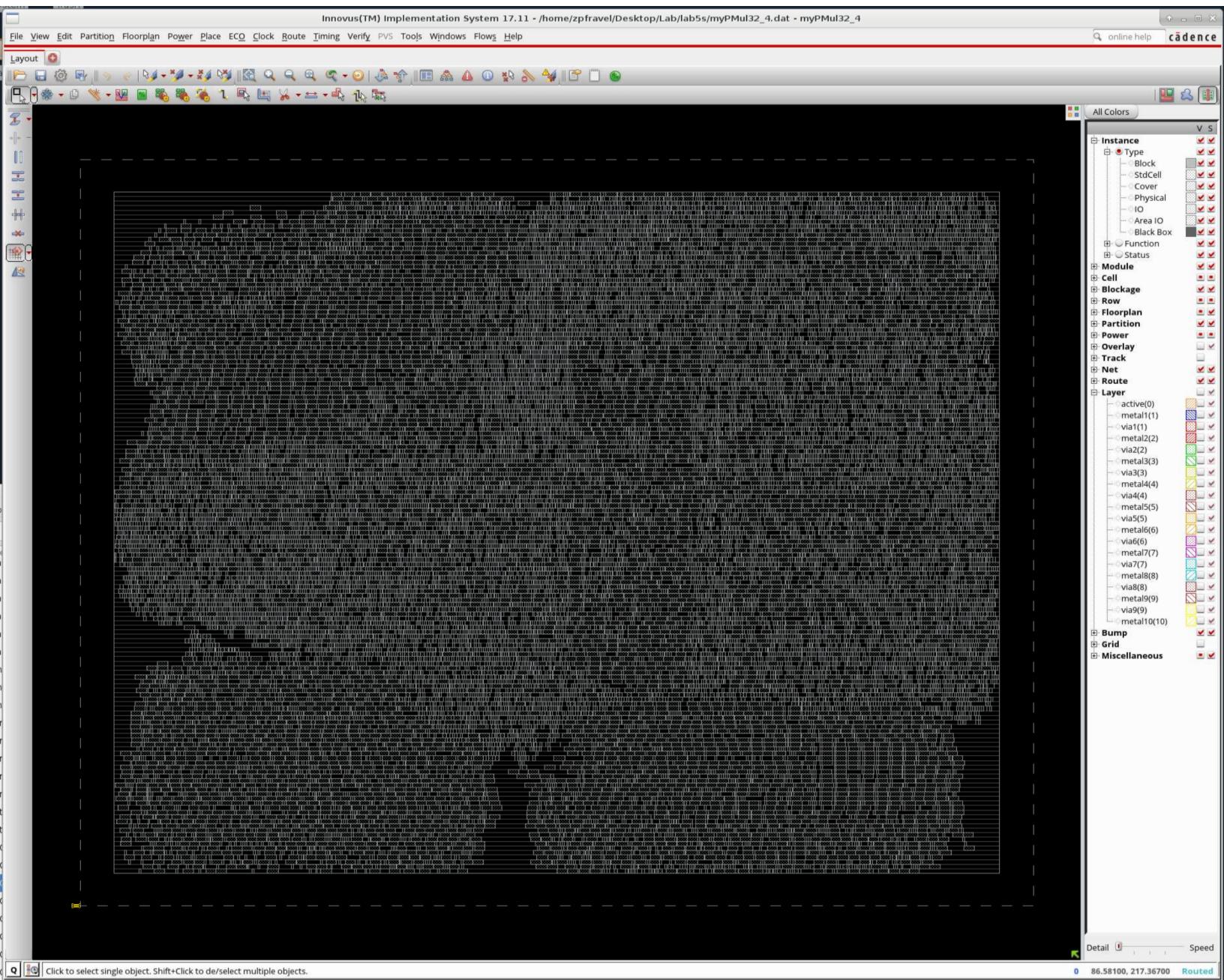
The next part of the lab is to repeat the process all over again for the PMul32\_4 design.



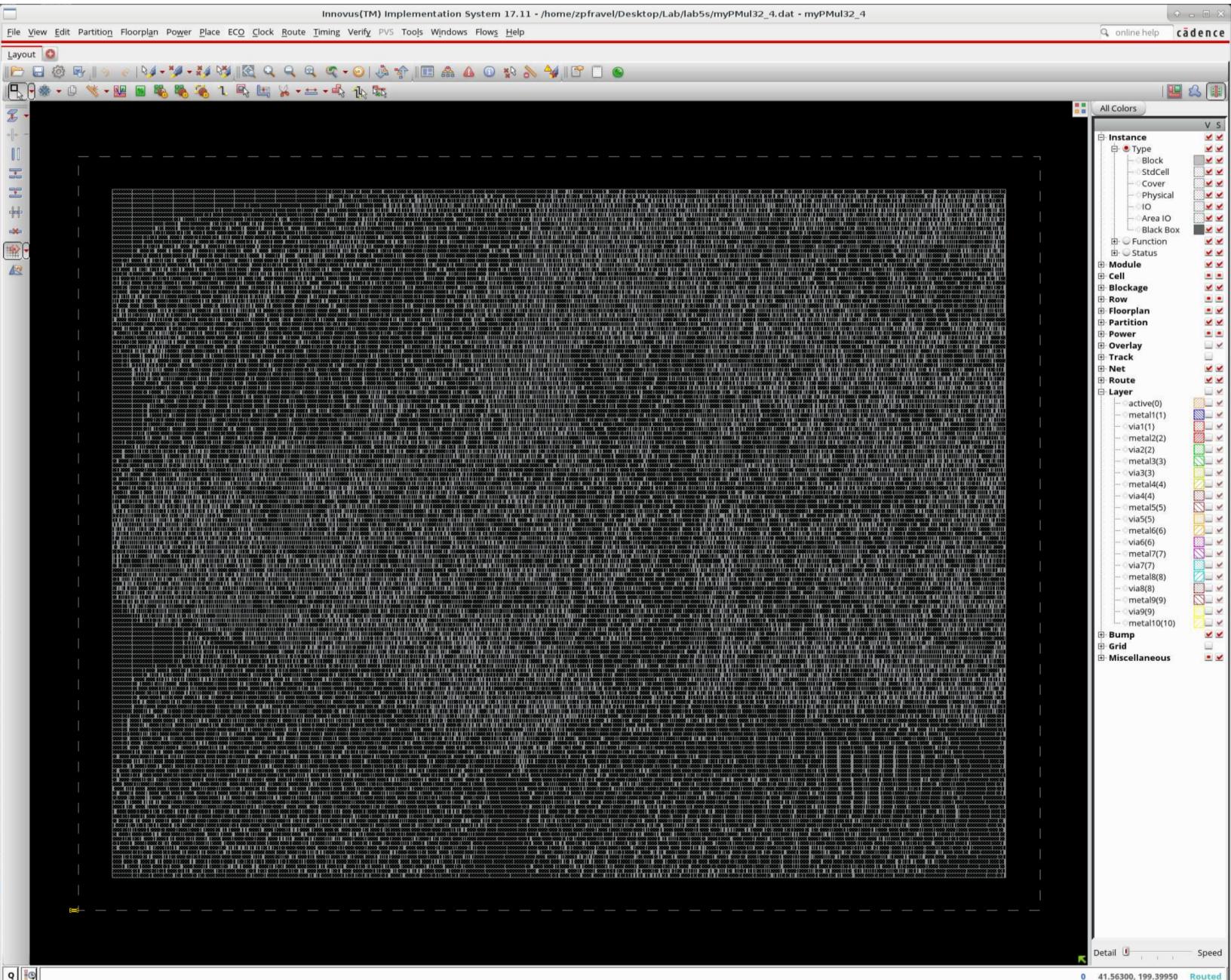
The first step, as before, is to add filler cells to the empty standard cell rows. These filler settings are the same as before with all sizes (x1 - x32) being used. The following screenshots are of the standard cells before and after filling.



Before Filling:



## After Filling:

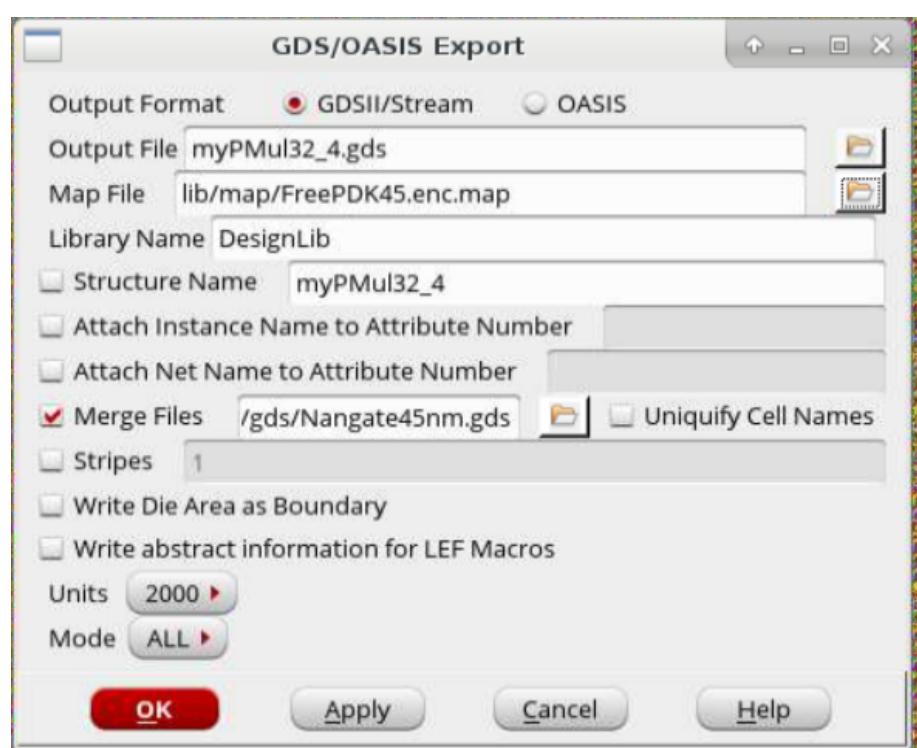


The following console information shows the filler cell distribution.

```
*INFO: Adding fillers to top-module.  
*INFO: Added 244 filler insts (cell FILLCELL_X32 / prefix FILLER).  
*INFO: Added 294 filler insts (cell FILLCELL_X16 / prefix FILLER).  
*INFO: Added 1528 filler insts (cell FILLCELL_X8 / prefix FILLER).  
*INFO: Added 3459 filler insts (cell FILLCELL_X4 / prefix FILLER).  
*INFO: Added 17003 filler insts (cell FILLCELL_X1 / prefix FILLER).  
*INFO: Added 0 filler inst (cell FILLCELL_X2 / prefix FILLER).  
*INFO: Total 22528 filler insts added - prefix FILLER (CPU: 0:00:01.4).  
For 22528 new insts, *** Applied 0 GNC rules (cpu = 0:00:00.0)
```

After filling all the standard cell rows, the next step is to perform parasitic extraction and export to a .spef file that Primetime can compare against.

```
RC Mode: PostRoute -effortLevel low [Extended CapTable, RC Table Resistances]
  RC Corner Indexes          0
Capacitance Scaling Factor : 1.00000
Coupling Cap. Scaling Factor : 1.00000
Resistance Scaling Factor : 1.00000
Clock Cap. Scaling Factor : 1.00000
Clock Res. Scaling Factor : 1.00000
Shrink Factor              : 1.00000
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
Checking LVS Completed (CPU Time= 0:00:00.1  MEM= 1353.6M)
Extracted 10.0007% (CPU Time= 0:00:00.4  MEM= 1438.5M)
Extracted 20.0006% (CPU Time= 0:00:00.6  MEM= 1444.5M)
Extracted 30.0005% (CPU Time= 0:00:00.6  MEM= 1445.5M)
Extracted 40.0005% (CPU Time= 0:00:00.8  MEM= 1450.5M)
Extracted 50.0008% (CPU Time= 0:00:00.9  MEM= 1453.5M)
Extracted 60.0007% (CPU Time= 0:00:01.0  MEM= 1456.5M)
Extracted 70.0006% (CPU Time= 0:00:01.1  MEM= 1459.5M)
Extracted 80.0005% (CPU Time= 0:00:01.4  MEM= 1462.5M)
Extracted 90.0005% (CPU Time= 0:00:01.7  MEM= 1468.5M)
Extracted 100% (CPU Time= 0:00:02.3  MEM= 1472.5M)
Number of Extracted Resistors   : 422483
Number of Extracted Ground Cap. : 455580
Number of Extracted Coupling Cap. : 611072
Filtering XCap in 'relativeOnly' mode using values relative_c_threshold=0.03 and total_c_threshold=0.05
Corner: NG_rc_typ
Checking LVS Completed (CPU Time= 0:00:00.1  MEM= 1456.5M)
PostRoute (effortLevel low) RC Extraction DONE (CPU Time: 0:00:03.4  Real Time: 0:00:03.0  MEM: 1456.488M)
RC Out has the following PVT Info:
  RC:NG_rc_typ, Operating temperature 25 C
Dumping Spef file.....
Printing D_Net...
rcOut completed:: 100 %
RC Out from RCDB Completed (CPU Time= 0:00:00.8  MEM= 1456.5M)
```



As with before, the final step in innovus is to export the layout to a .gds file as well as save the netlist to be used with Primetime later. The next page shows the GDS report generated by the console during the export process.

Object	Count
Instances	51938
Ports/Pins	0
Nets	257269
metal layer metal1	21874
metal layer metal2	143014
metal layer metal3	84213
metal layer metal4	7425
metal layer metal5	743
Via Instances	163303
Special Nets	464
metal layer metal1	460
metal layer metal2	4
Via Instances	312
Metal Fills	207529
metal layer metal1	2338
metal layer metal2	16936
metal layer metal3	26809
metal layer metal4	40407
metal layer metal5	45089
metal layer metal6	54822
metal layer metal7	8381
metal layer metal8	8377
metal layer metal9	2178
metal layer metal10	2192
Via Instances	159333
Metal FillOPCs	0
Via Instances	0
Text	0
Blockages	0
Custom Text	0
Custom Box	0
Trim Metal	0

#### Merging with GDS libraries

Scanning GDS file lib/gds/Nangate45nm.gds to register cell name .....

Merging GDS file lib/gds/Nangate45nm.gds .....

\*\*\*\*\* Merge file: lib/gds/Nangate45nm.gds has version number: 5.

\*\*\*\*\* Merge file: lib/gds/Nangate45nm.gds has units: 2000 per micron.

\*\*\*\*\* unit scaling factor = 1 \*\*\*\*\*

#####Streamout is finished!

Writing GDSII file ...

\*\*\*\*\* db unit per micron = 2000 \*\*\*\*\*  
 \*\*\*\*\* output gds2 file unit per micron = 2000  
 \*\*\*\*\* unit scaling factor = 1 \*\*\*\*\*

Output for instance

Output for bump

Output for physical terminals

Output for logical terminals

Output for regular nets

Output for special nets and metal fills

Output for via structure generation

Statistics for GDS generated (version 5)

----- Stream Out Layer Mapping Information:

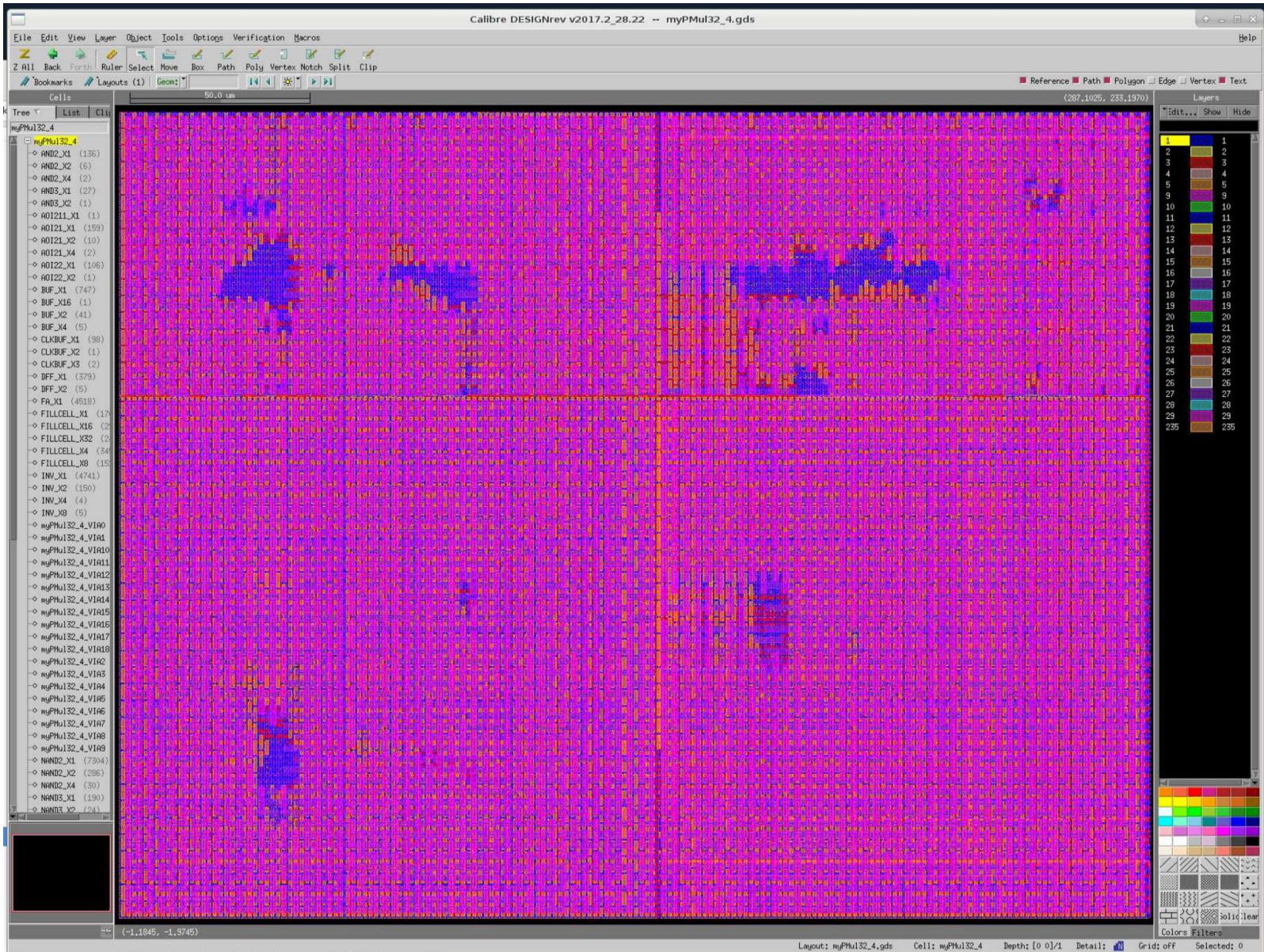
GDS Layer Number	GDS Layer Name
------------------	----------------

9	poly
11	metal1
12	vial
13	metal2
14	via2
15	metal3
16	via3
17	metal4
18	via4
19	metal5
20	via5
21	metal6
22	via6
23	metal7
24	via7
25	metal8
26	via8
27	metal9
28	via9
29	metal10

Stream Out Information Processed for GDS version 5:

Units: 2000 DBU

Now that we have the layout exported to a .gds, we can load it into Calibre to perform DRC analysis. The following is a shot of the design in Calibre.



The following screenshots on the next page show the successful DRC reports generated by Calibre.

The screenshot shows two windows from the Calibre tool. The left window is titled "Calibre - RVE v2017.2\_28.22 : myPMul32\_4.drc.results" and displays a table of DRC results. The right window is titled "DRC Summary Report - myPMul32\_4.drc.summary" and shows a detailed log of rule checks and statistics.

**DRC Summary Report - myPMul32\_4.drc.summary**

```

DRC Summary Report - myPMul32_4.drc.summary
File Edit Options Windows

RULECHECK Metal3.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal3.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal3.8 .... TOTAL Result Count = 0 (0)
RULECHECK Metal3.9 .... TOTAL Result Count = 0 (0)
RULECHECK Metal4.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal4.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal4.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal4.8 .... TOTAL Result Count = 0 (0)
RULECHECK Metal5.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal5.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal5.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal5.8 .... TOTAL Result Count = 0 (0)
RULECHECK Metal6.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal6.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal6.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal6.8 .... TOTAL Result Count = 0 (0)
RULECHECK Metal7.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal7.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal7.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal8.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal8.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal8.7 .... TOTAL Result Count = 0 (0)
RULECHECK Metal9.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal9.6 .... TOTAL Result Count = 0 (0)
RULECHECK Metal10.5 .... TOTAL Result Count = 0 (0)
RULECHECK Metal10.6 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.1 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.2 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.3 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.4 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.5 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.6 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.7 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.8 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.9 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.10 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.11 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.12 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.13 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.14 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.15 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.16 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.17 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.18 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.19 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.20 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.21 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.22 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.23 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.24 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.25 .... TOTAL Result Count = 0 (0)
RULECHECK Grid.26 .... TOTAL Result Count = 0 (0)

--- RULECHECK RESULTS STATISTICS (BY CELL)
---

--- SUMMARY
---
TOTAL CPU Time: 27
TOTAL REAL Time: 28
TOTAL Original Layer Geometries: 468512 (2806054)
TOTAL DRC RuleChecks Executed: 156
TOTAL DRC Results Generated: 0 (0)

```

Finally again, we're ready to perform power and timing analysis with primetime. Using the pt.tcl script and the updated verilog netlist from innovus, we can run the same command from earlier to perform analysis.

```
pt_shell -f pt.tcl
```

Here is a screenshot of the pt.tcl script used for PMul32\_4. I used a 10 ns clock period on this design because a 5 ns clock was too fast, the slack was violated on the timing report. I included the timing report for the 5 ns clock I based this decision on as well on the next page along with the successful report for the 10 ns clock.

```

Open Save pt.tcl
~/Desktop/Lab/lab5s
suppress_message "RC-004 RC-008 RC-009 PTE-060"

set target_library "lib/db/NangateOpenCellLibrary_typical_ecsm.db"
set link_library "* lib/db/NangateOpenCellLibrary_typical_ecsm.db"

set topname myPMul32_4

set myPeriod_ns 10
set myClk [list g_inClk]

read_verilog ${topname}.v
current_design $topname
link

create_clock -period $myPeriod_ns $myClk
set_ideal_network [get_port $myClk]
read_parasitics ${topname}.spef -keep_capacitive_coupling
complete_net_parasitics -complete_with zero
report_annotated_parasitics -check

set power_enable_analysis TRUE

set_switching_activity -static_probability 0.5 -toggle_rate 0.15 -base_clock $myClk [remove_from_collection [all_inputs] $myClk]
set_switching_activity -static_probability 0.5 -toggle_rate 0.15 -base_clock $myClk -type registers -hierarchy

update_timing
report_timing -group $myClk -capacitance -transition_time > ${topname}.timing.pt.rpt

update_power
report_power >> ${topname}.power.pt.rpt

exit

Loading file '/home/zpfravel/Desktop/Lab/lab5s/pt.tcl'...

```

Here is the power report generated from running the script.

**myPMul32\_4.power.pt.rpt - Mousepad**

Report : Averaged Power  
Design : myPMul32\_4  
Version: M-2017.06-SP1  
Date : Sat Nov 18 17:41:38 2017

**Attributes**

i - Including register clock pin internal power  
u - User defined power group

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	( % )	Attrs
clock_network	1.393e-04	0.0000	0.0000	1.393e-04	( 1.74%)	i
register	7.247e-05	7.958e-05	3.054e-05	1.826e-04	( 2.29%)	
combinational	3.433e-03	3.396e-03	8.308e-04	7.660e-03	(95.97%)	
sequential	0.0000	0.0000	0.0000	0.0000	( 0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	( 0.00%)	
io_pad	0.0000	0.0000	0.0000	0.0000	( 0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	( 0.00%)	
Net Switching Power	= 3.476e-03	(43.55%)				
Cell Internal Power	= 3.645e-03	(45.66%)				
Cell Leakage Power	= 8.614e-04	(10.79%)				
Total Power	= 7.982e-03	(100.00%)				

1

myPMul32\_4.timing.pt.rpt - Mousepad

```

File Edit Search View Document Help
*****
Report : timing
  -path_type full
  -delay_type max
  -max_paths 1
  -group g_inClk
  -transition_time
  -capacitance
  -sort_by slack
Design : myPMul32_4
Version: M-2017.06-SP1
Date  : Sat Nov 18 17:36:55 2017
*****
```

Startpoint: reg\_mid\_0\_reg[1]  
                  (rising edge-triggered flip-flop clocked by g\_inClk)  
Endpoint: reg\_out\_reg[122]  
                  (rising edge-triggered flip-flop clocked by g\_inClk)  
Path Group: g\_inClk  
Path Type: max

Point	Cap	Trans	Incr	Path
clock g_inClk (rise edge)	0.00	0.00	0.00	
clock network delay (ideal)			0.00	0.00
reg_mid_0_reg[1]/CK (DFF_X1)		0.00	0.00	0.00 r
reg_mid_0_reg[1]/QN (DFF_X1)	5.24	0.02	0.07 &	0.07 f
U8127/ZN (INV_X1)	7.51	0.02	0.03 &	0.10 r
U15976/ZN (INV_X4)	45.71	0.02	0.02 &	0.12 f
FE_RC_18930/ZN (NAND2_X1)	1.32	0.01	0.01 &	6.43 f
reg_out_reg[122]/D (DFF_X1)		0.01	0.00 &	6.43 f
data arrival time				6.43
clock g_inClk (rise edge)	0.00	5.00	5.00	
clock network delay (ideal)		0.00	5.00	
clock reconvergence pessimism			0.00	5.00
reg_out_reg[122]/CK (DFF_X1)				5.00 r
library setup time			-0.04	4.96
data required time				4.96
data arrival time				-6.43
slack (VIOLATED)				-1.47

1

Here is the timing report for the 5 ns clock period where the slack was violated.

myPMul32\_4.timing.pt.rpt - Mousepad

```

File Edit Search View Document Help
*****
Report : timing
  -path_type full
  -delay_type max
  -max_paths 1
  -group g_inClk
  -transition_time
  -capacitance
  -sort_by slack
Design : myPMul32_4
Version: M-2017.06-SP1
Date  : Sat Nov 18 17:41:34 2017
*****
```

Startpoint: reg\_mid\_0\_reg[1]  
                  (rising edge-triggered flip-flop clocked by g\_inClk)  
Endpoint: reg\_out\_reg[122]  
                  (rising edge-triggered flip-flop clocked by g\_inClk)  
Path Group: g\_inClk  
Path Type: max

Point	Cap	Trans	Incr	Path
clock g_inClk (rise edge)	0.00	0.00	0.00	
clock network delay (ideal)			0.00	0.00
reg_mid_0_reg[1]/CK (DFF_X1)		0.00	0.00	0.00 r
reg_mid_0_reg[1]/QN (DFF_X1)	5.24	0.02	0.07 &	0.07 f
U8127/ZN (INV_X1)	7.51	0.02	0.03 &	0.10 r
U15976/ZN (INV_X4)	45.71	0.02	0.02 &	0.12 f
FE_RC_18930/ZN (NAND2_X1)	1.32	0.01	0.01 &	10.00 f
reg_out_reg[122]/D (DFF_X1)		0.01	0.00 &	10.00 f
data arrival time				10.00
clock g_inClk (rise edge)	0.00	10.00	10.00	
clock network delay (ideal)		0.00	10.00	
clock reconvergence pessimism			0.00	10.00
reg_out_reg[122]/CK (DFF_X1)			-0.04	9.96
library setup time				9.96
data required time				-6.43
data arrival time				3.53
slack (MET)				

1

However, upon slowing down the clock speed to 10 ns, I achieved the following successful timing report.

This concludes the report with success for both VQS64\_4 and PMul32\_4!