Digital Design CSCE 2114

Lab 7 Report

Zack Fravel

December 4th, 2015

zpfravel@uark.edu

Abstract

Lab seven was very similar to previous labs in it asked to design and implement and new simple circuit using Quartus II. This lab had us successfully create a 4 bit up/down counter by using two basic components.

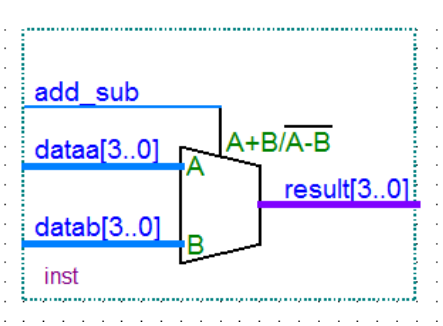
Introduction

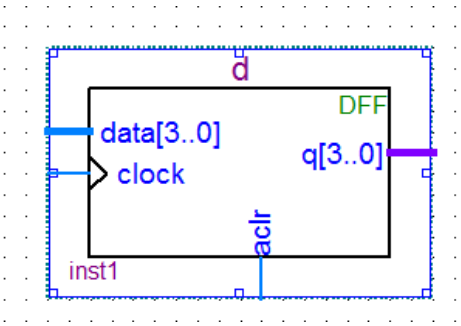
The problem we're trying to solve with this lab is creating a 4-bit up/down counter circuit. As described in the lab itself, the counter we're designing consists of a D-flip-flop and an adder/subtractor. We want the counter to go from 0000 to 1111, therefore the D-flip-flop and the add/sub should be four bits wide. Once we wire the two components together correctly, that should give us our counter.

A quick overview of all the signals we should keep in mind shows we have the Count_value[3..0], Up_down, Clk, Aclr, and Sum[3..0] signals. The Count_value[3..0] is a constant value that determines the increment/decrement step with each rising edge of the clock. The Up_down signal determines which way the counter counts, with '1' representing a count up. Clk, or clock, is the determining factor in when the value of Sum[3..0] is updated. Aclr simply clears all the outputs of the flip flops to '0.' Finally, the Sum[3..0] signal is the current counting value in the circuit, updated with each Clk rising edge.

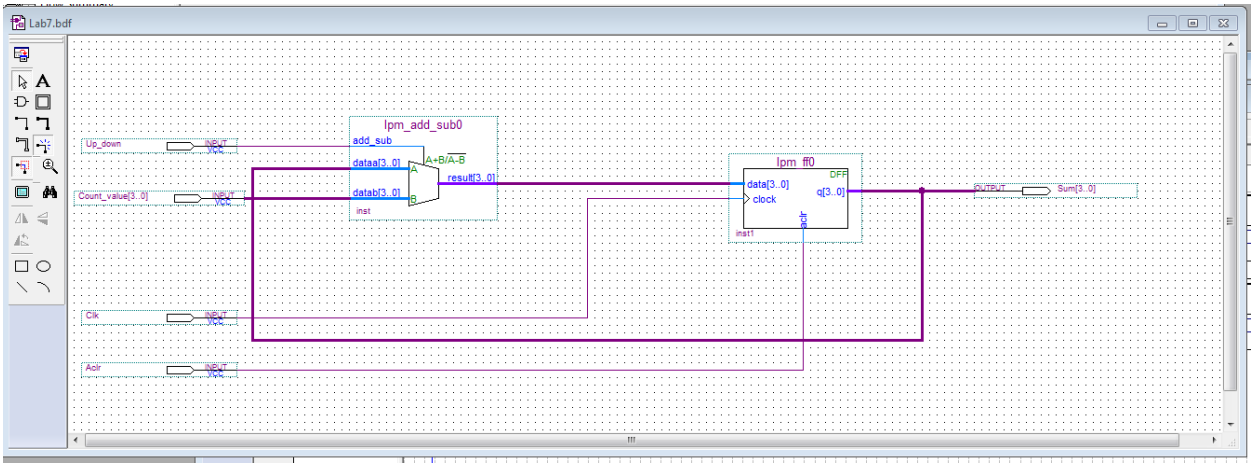
Design and Implementation

The first step in creating the counter was first to configure the adder. An add/sub has 3 inputs, two pieces of data and the add/sub selector, and one output. To connect to the adder, we want a 4-bit flip-flop. This D flip-flop has an asynchronous clear input. The following is a diagram of a 4 bit add/sub and the 4-bit flip-flop found in the megafunctions LPM library.





Once the two components were connected, all that was needed to do is add the input and output ports to the design. The following is the completed counter circuit.

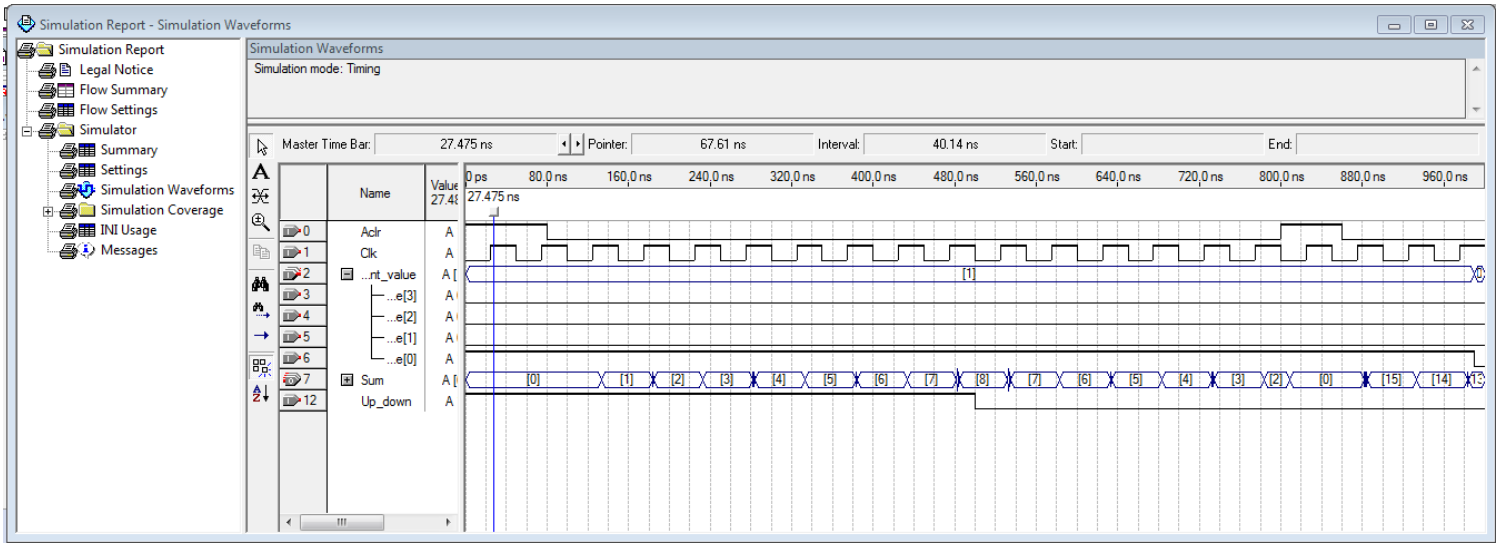


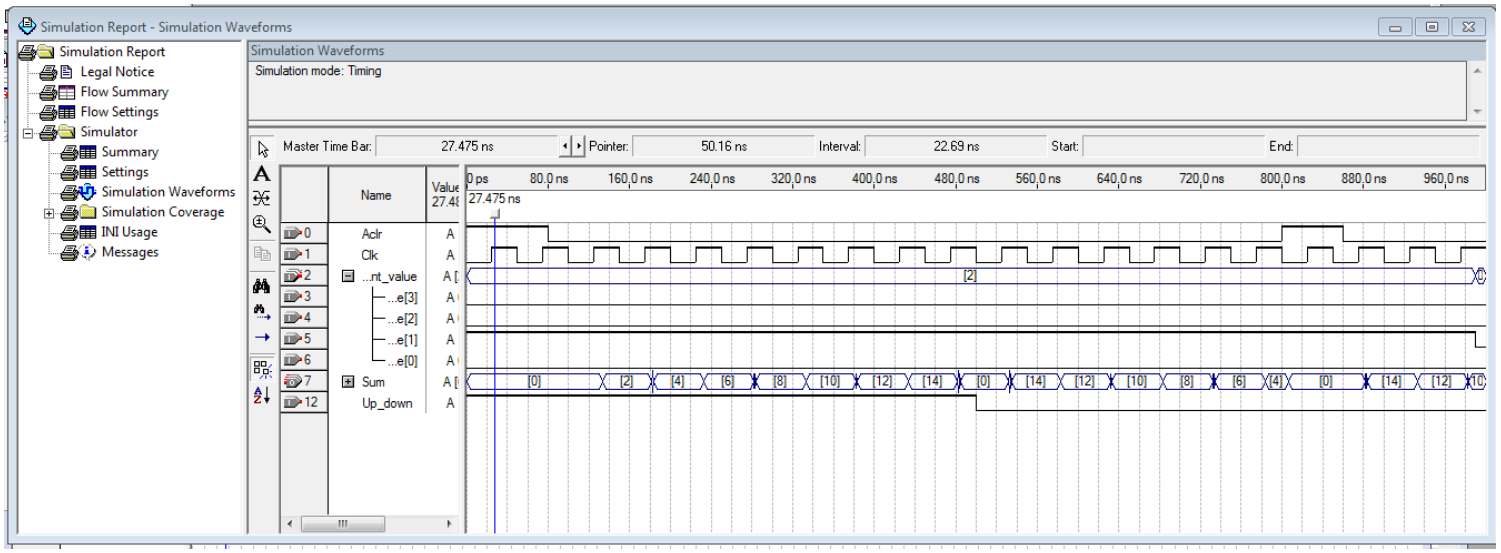
The first data point of the adder is connected to the flip-flop output, while the second point of the adder is connected to the Count_value input, which determines the amount to be added or subtracted. Then there's the Up_down indicator connected to the adder input as well as the clk and aclr inputs that are connected to the flip-flop.

After designing the circuit and compiling it successfully, it was time to set up the waveform diagram. The clk signal was set to periodically change every 50ns from 0 to 1000 ns. The Up_down signal set to '1' from 0 to 500 ns and '0' from 500 to 1000 ns. Aclr was set to '1' from '0' from 800 ns to 860 ns. With these specifications set in place, we were to run two simulations, one with Count_value set to '1' and another set to '2'.

Results

The first waveform represents an up/down counter that increments by one with each step of the clock, the second increments by 2's.





As you can see the circuit successfully counts up until 500 ns and counts down from 500 ns to 1000 ns with each step of the clock.

Conclusion

Using a 4-bit add/sub and a 4-bit flip-flop we were able to successfully design and implement a 4-bit number up/down counter.