CSCE4914 Lab Assignment 1

Due 9/17 11:00PM

Instructions:

1. First, read the prelab instructions on the course website in the lab note section. Make sure you follow each step. Also make sure that you have some basic knowledge of linux commands such as ls, mv, cp, rm (be careful!!!), cd, ln, tar, wget, rsync, source before you begin this lab.
2. To use hspice and cosmos scope, you will need:

   initrc hsp-m

   initrc cscope-m

   Make sure they are run before you use the tools
3. To run hspice simulation, type:

   hspice your_hspice_netlist.sp -o your_hspice_log.lis

   Make sure simulation shows 'job concluded'. For detailed usage, check out the hspice manual, or look up the help output:

   hspice -h
4. To run cosmosscope, simply type:

   cscope &

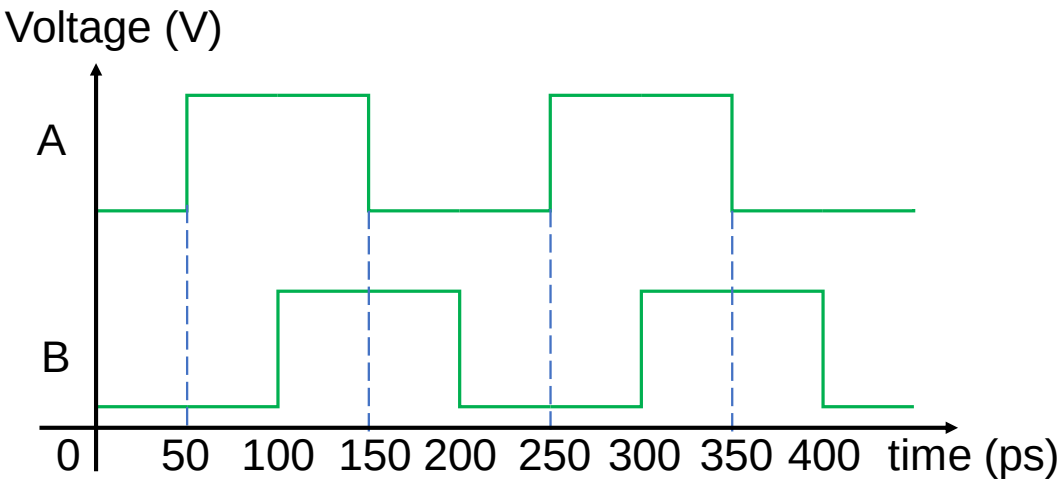
   The & is used so that it runs in the background, leaving you with the command line interface. Cosmos scope usage is the same as in windows.
5. For this simulation, you will need to use a 45nm transistor model card. The feature length (λ) of this 45nm technology is 25nm. You can download the 'hspice.tgz' from the course website in to your work folder using wget, and you can unzip it using atool utility.

```
[746]~/R/3$wget http://e3da.csce.uark.edu/teaching/CSCE4914-17FA/lab/hspice.tgz
--2017-09-10 05:01:59--  http://e3da.csce.uark.edu/teaching/CSCE4914-17FA/lab/hspice.tgz
Resolving e3da.csce.uark.edu (e3da.csce.uark.edu)... 130.184.76.36
Connecting to e3da.csce.uark.edu (e3da.csce.uark.edu)|130.184.76.36|:80... connected.
HTTP request sent, awaiting response... 200 OK
Length: 12796 (12K) [application/x-gzip]
Saving to: 'hspice.tgz'

100%[=======================================================================================

2017-09-10 05:01:59 (247 MB/s) - 'hspice.tgz' saved [12796/12796]

[747]~/R/3$atool -x hspice.tgz
hspice/
hspice/lib/
hspice/lib/tran_models/
hspice/lib/tran_models/models_ss/
hspice/lib/tran_models/models_ss/PMOS_VTH.inc
hspice/lib/tran_models/models_ss/PMOS_THKOX.inc
hspice/lib/tran_models/models_ss/NMOS_VTL.inc
```

6. Unless otherwise specified, use 1.1V as the power supply voltage. Make sure all transistors have a width of 2λ. The NMOS should have a length of 12λ, the PMOS should have a length of 16λ.

Assignment (20% for each task):

1. Perform a transient simulation of a NAND2 gate. Plot the output voltage waveform for 400ps. The input waveform (The voltage is from GND to VDD) is given with a zero rise and fall time:



2. Change the rise and fall time of the input signals to 100ps, and period of all signals to 2000ps. Replot the output waveform.
3. Based on step 2, further change the VDD to 0.6V, replot the output waveform. Compare with the waveform you obtained in step 2, and use transistor theory to explain the difference that you observed from the simulation.
4. Perform a DC simulation of an inverter. Connect the input of the inverter to a DC voltage source and sweep the input voltage from GND to VDD (1.1V) with an increment of 0.05V. Plot the output voltage of the inverter versus the input voltage.
5. Based on step 4, fix the input voltage at VDD/2. While fixing the NMOS width at 12λ, sweep the PMOS width from 4λ to 32λ with an increment of 1λ. Plot the output voltage versus the PMOS width. Explain what you observed using transistor theory.

What to turn in:

1. A lab report with all of your simulation waveforms and your explanations of results.
2. The spice netlist (*.sp) for each simulation and the output log file (*.lis).