Embedded Systems (CSCE 4114)

Lab 1

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Abstract

Lab 1 was intended to introduce us to Quartus 16.0 and familiarize with the controls and tools that are at our disposal, split up into four parts. In the end of the lab we have a simple implementation of combinational logic onto a set of switches and LED's on our development board.

Introduction

Very little actual design work is required for this lab, all of the materials needed are already given to us. The lab was split into four parts; creating a project, simulation, timing constraints and pin assignments, and finally synthesis and implementation. Again, the purpose of the lab is not necessarily learning new VHDL skills, rather familiarization with the development tools and the hardware we'll be using.

In Part I, we're told to create a new project and are given a .vhdl source file that we are asked to compile. This file describes a design with 4 switches, some combinational logic to go along, and 8 LED's, respectfully representing the switches and LED's on the spider's development board. Following we have Part II, III, and IV the lab also walks through how to do the actual pin assignments and upload the design to the board for real time testing.

Design and Implementation

In Part I we are asked a couple of questions about the design we are given, with the first asking to describe the behavior of the module. In a sentence, this design allows us to control the LED's to switch on in different configurations based on the orientations of the 4 switches on the development board. This process is being checked every rising edge of the clock, so it will update based on the clock frequency. The next few questions ask about how the design tool is

actually implementing this circuit. To find this out, we were instructed to do some digging and find out how many registers, pins, and lookup tables (LUTs) were used in the design. There are 8 registers, one corresponding to each of the possible LED output values, and 13 pins (the total number of inputs and outputs including the clock). There are 4 LUT's in this design, representing the four input functions. A 3 to 8 decoder could be used to implement this design with the logic we have, with the 4th switch going to a reset that sets all output bits to '0.'

Results

The next part of the lab walked us through how to build a test bench for our design and how to run a simulation that is suitable. Again, we were given a test bench already and were just asked to load it in and walked through how to set up the simulator. Figure 1 refers to the simulation from the lab.

Simulation Results

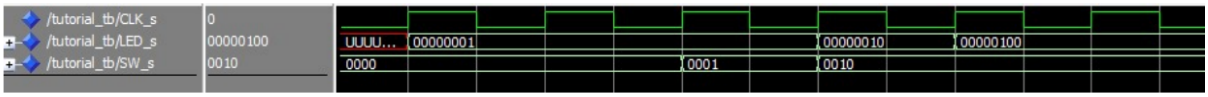

Figure 1

As shown on Figure 1, on the rising edge of the clock (first wave) if there is any change in the behavior of the switch inputs (third wave), the output on the LED's (second wave) gets changed accordingly. This is why the output doesn't follow the input immediately, the process was designed in that way. Whenever we modify the test bench to have SW(3) driven to '1', we have the change on the output wave we expect, '00000000.'

Part III of the lab walked us through how to do pin assignments with the pin planner and gave us the necessary information to assign the correct pins to the correct piece of hardware we

are utilizing. We also in this process give the Quartus tool a goal for optimization of the circuit according to our clock speed with the timing analyzer to create time constraints. Finally, in Part IV we compile the design, select the correct hardware, and are able to plug the device into the computer and hit start. After hitting start, we're able to observe the design we've been working on with our development board and the switches respond correctly to the LED's! Through these four parts this lab successfully walked us through how to create a project, design and implement combinational logic, and synthesize that logic onto a development board following a software simulation.