Zack Fravel

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Skills

2 years experience writing Verilog / VHDL and working with various VLSI design tools.
Strong working familiarity with Python, C/C++, Java, JS, and HTML.
Experienced troubleshooting in time-sensitive, high-volume manufacturing conditions.
Trained in through-hole and SMT electronics assembly.

Work

Manufacturing Technician - Intel
2019 - Present

Currently working full-time at Intel at their Aloha Factory Operations in Oregon as a Die Sort Manufacturing Technician. I am trained to work with a variety of state-of-the-art tools in semiconductor manufacturing, primarily performing error response and recovery as well as preventative maintenance. I also frequently communicate with engineers about potential issues with the tools and help develop solutions that work to increase output.

Electronics Assembly Technician - Moffenzeef Modular and LZX Industries
2018 - 2019

Worked as a contracted assembly technician for two synthesizer startups in Portland. Thoroughly trained in electronics assembly techniques as well as some experience designing analog schematics and creating PCB layouts. I worked in many levels of manufacturing including assembly, QC/rework, delivery, packing, and shipping.

Education

Bachelor of Science in Computer Engineering
University of Arkansas, Fayetteville, AR. Degree earned in 2018.

Project Experience

64-point 8-bit Fast Fourier Transform (FFT) Design Project

Completed work on a semi-custom VLSI design of a 64-point, 8-bit FFT. The project taught me physical design flow using tools from Cadence (Innovus, Virtuoso), Synopsys (Design Compiler, HSpice, Primetime STA), and Mentor Graphics (ModelSim, Calibre).

Low Power Vedic Multiplier Design, Synthesis, and Research Analysis

Performed research designing low power CMOS Multiplier circuits using the Urdhva Tiryagbhyam Algorithm from Vedic Mathematics in order to both minimize computation time and resources by taking advantage of parallelization. I implemented the circuits with structural Verilog and tested their effectiveness by comparing power analysis results with standard shift-add multipliers using Xilinx Design Tools.

Microprocessor Architecture Design and Synthesis Projects

Completed work in designing, simulating, and synthesizing two individual RISC microprocessor architectures. The first was written in VHDL and implemented a MIPS instruction set, the second implemented a SAP-1 architecture and was designed using Verilog. I did RTL Synthesis on the SAP-1 design, along with a gate-level simulation.

Research Course on Contemporary Applications in Graph Theory

Completed a graduate research course in my final semester where I learned the fundamentals of using graph theory for data analysis using Python. I worked on projects in variety of areas including polarization analysis, social networks, and game theory.

References available upon request.

Updated Jul 11, 2019