(501) 519 7667
4725 SE Division St, 109
Portland, OR 97206

Zack Fravel

zackfravel.com
mail@zackfravel.com

Skills

2 years experience writing Verilog / VHDL and working with various VLSI design tools.
Strong working familiarity with Python, C/C++, Java, JS, and HTML.
Fully trained in through-hole and SMT electronics assembly.

Work Experience

Electronics Assembly Technician for Moffenzeef Modular and LZX Industries
July 2018 - Present

Currently working as an assembly technician for two synthesizer manufacturer startups in Southeast Portland. I have been thoroughly trained in through-hole and SMT assembly techniques as well as some experience in creating schematics and designing PCB layouts using DipTrace. I've worked at every level of manufacturing including hand assembly, QC/rework, delivering parts to and from workshops, packing, and shipping.

Products shipped:
LZX Vidiot, LZX Visual Cortex, LZX Cadet Series
Moffenzeef Stargazer, Moffenzeef MSGII, Moffenzeef [Intensifies]

Education

Bachelor of Science in Computer Engineering
University of Arkansas, Fayetteville, AR. GPA: 3.2. Graduated May 2018.

Project Experience

64-point 8-bit Fast Fourier Transform (FFT) Design Project
Completed work on a semi-custom VLSI design of a 64-point, 8-bit FFT. The project taught me physical design flow using tools from Cadence (Innovus, Virtuoso), Synopsys (Design Compiler, HSpice, Primetime STA), and Mentor Graphics (ModelSim, Calibre).

Research Course on Contemporary Applications in Graph Theory
Took a graduate research course in my final semester where I learned the fundamentals of using graph theory for data analysis using Python. I worked on a variety of project areas from measuring political polarization using homophily, to network fragility analysis, to blockchain implementations for measuring consensus, to pitch set theory analysis.

Low Power Vedic Multiplier Design, Synthesis, and Research Analysis
Performed research designing low power CMOS Multiplier circuits using the Urdhva Tiryagbhyam Algorithm found in Vedic Mathematics in order to both minimize computation time and resources by taking advantage of parallelization. I implemented the circuits using structural Verilog and tested their effectiveness by comparing power analysis results with standard shift-add multipliers in Vivado.

Embedded Systems Terasic Spider Robotics Project
Worked with a team on a project implementing behaviors onto an Altera FPGA robot spider. Along with basic behaviors we also learned to implement advanced embedded techniques such as edge detection, debouncing, as well as a wishbone UART controller.

Microprocessor Architecture Design and Synthesis Projects
Completed work in designing, simulating, and synthesizing two individual RISC microprocessor architectures. The first was written in VHDL and implemented a MIPS instruction set, the second implemented a SAP-1 architecture and was designed using Verilog. I did RTL Synthesis on the SAP-1 design, along with a gate-level simulation.