Zack Fravel

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Objective   Internship in Digital Design / Verification.

Highlights   • RTL design and verification experience in Computer Architecture and Embedded Systems
• Proficient in programming and scripting with Python
• 2 years of experience working in electronics manufacturing, from small scale to industrial
• Professional troubleshooter in sensitive, high-volume manufacturing conditions

Skills   • <u>HDLs</u>: SystemVerilog, Verilog, and VHDL
• <u>Design Tools</u>: Synopsys (HSPICE, Design Compiler), Mentor Graphics (Questasim, Calibre),
  Xilinx ISE, and Cadence (Innovus, Virtuoso)
• <u>Programming Languages</u>: Proficient in Python, experienced with C++ and Java

Education   **Master of Science in Electrical & Computer Engineering**   **September 2020 - Present**
Design, Verification, and Validation Program
Portland State University, Portland, OR.

   • <u>Courses (by December 2020)</u>: SystemVerilog, Assertion Based Verification using FPV.

Bachelor of Science in Computer Engineering   **August 2014 - May 2018**
University of Arkansas, Fayetteville, AR. GPA: 3.2

   • <u>Courses</u>: Computer Architecture, Advanced Digital Design, Applications in Graph Theory,

Low

Power Digital Systems, System Synthesis and Modeling, Embedded Systems, Computer
Organization, Programming Paradigms, Software Engineering, Discrete Math, Logic, Ethics.

Work   **Intel**   **May 2019 - April 2020**
Die Sort Manufacturing Technician. Aloha, OR.

Led the night shift maintenance team performing troubleshooting, maintenance tasks and
advanced calibrations on state-of-the-art manufacturing tools. Recommended shift priorities
to my manager while collaborating with engineering teams to implement improved
procedures that emphasized safety while maintaining consistent output.

Contractor   **July 2018 - May 2019**
Electronics Assembly Technician. Portland, OR.

Contributed as an assembly technician for Moffenzeef Modular and LZX Industries by fulfilling
over 200 pre orders for multiple products on time with zero quality escapes.

Experience   **Computer Architecture**
• Designed and simulated a 5-stage pipeline with a reduced MIPS instruction set in VHDL.
• Designed, simulated, and synthesized a custom ISA from the ground-up in Verilog.

Embedded FPGA Design, Synthesis and Programming
 • Traffic light, Vending machine, Wishbone-UART Bus, Terasic spider behaviors

Advanced Digital Design
• Design and synthesis of low power Vedic multiplier.
• Synthesis, routing, and layout of 64-Point 8-bit Fast Fourier Transform

Interests   I spend most of my free time woodworking, playing synthesizers, and cooking authentic BBQ.

Work Samples: https://www.zackfravel.com/