Zack Fravel

135 Hickory Creek Circle
Little Rock, Arkansas, 72212

zackfravel.com
mail@zackfravel.com

Education

Bachelor of Science in Computer Engineering
University of Arkansas, Fayetteville, AR. GPA : 3.2. Earned May 2018.

Overview

2 years experience writing Verilog / VHDL and using a wide range of VLSI design tools.
Strong working familiarity with Python, C/C++, Java, JS, and HTML.
Passionate about psychology, philosophy, and seeking out invigorating creative outlets.

Engineering Coursework

64-point 8-bit Fast Fourier Transform (FFT) Design Project
Completed work on a semi-custom VLSI design of a 64-point, 8-bit FFT. The project taught proper design flow using tools from Cadence (Virtuoso, Innovus), Synopsys (HSpice, Design Compiler, Primetime STA), and Mentor Graphics (ModelSim, Calibre).

Framework for oxDNA Simulation Tools
Worked on a year long project with a team of other computer scientists to wrap oxDNA in a simplified user interface that allows researchers without programming experience to engage with the tools it has to offer. We constructed the backend using a Django Python server, PostgreSQL database, and Celery for running background tasks. The interface itself was built on Angular2 and implemented a 3D renderer using WebGL.

Research Course on Current Applications in Graph Theory
Took a graduate research course in my final semester where all the students performed individual research on a novel subject in the field of graph theory as it relates to computer science. In an attempt to expand my knowledge on music, I created a Python script that implemented graph theoretic analysis on a user-defined pitch class set to calculate parsimonious voice leading on the set's triad and seventh chords.

Low Power Vedic Multiplier Design, Synthesis, and Research Analysis
Performed research designing low power CMOS Multiplier circuits using the Urdhva Tiryagbhyam Algorithm found in Vedic Mathematics. I implemented the circuits using structural Verilog and tested their effectiveness in lowering power consumption through synthesis and comparing power analysis results with shift-add multipliers in Vivado.

Microprocessor Architecture Design and Synthesis Projects
Completed work in designing, simulating, and synthesizing two different RISC microprocessor architectures. The first was written in VHDL and implemented a MIPS instruction set, the second implemented a SAP-1 architecture and was written in Verilog. The SAP-1 computer was synthesized with Synopsys Design Compiler.

Embedded Systems Terasic Spider Robotics Project
Worked with a team on a multi-month project implementing simple behaviors onto an Altera FPGA robot spider. This class was helpful for getting experience with VLSI design tools and FPGAs. Along with that, we also learned advanced embedded design methods developing edge detection, debouncing, and wishbone UART send/receive modules.

Extracurriculars

DIY Electronics and Modular Synthesis
I have learned an enormous amount about electronics and art though performing local music and visual shows with a eurorack modular synthesizer. Along with performing music I have experimented with creating my own instruments using my collective knowledge of music and computer/electrical engineering.

References

Dr. Matthew Patitz	(479) 575 - 5590	patitz@uark.edu
Dr. Christopher Stevens	n / a	cwsteven@uark.edu
Dr. Jia Di	(479) 575 - 5728	jdi@uark.edu

Curriculum

CSCE Courses

Programming Foundations (I, II)
Digital Deisgn
Computer Organization
Programming Paradigms
Software Engineering
Operating Systems
System Synthesis and Modeling
Embedded Systems
Low Power Digital Systems
Advanced Digital Design
Computer Architecture
Computer Graphics
Current Applications in Graph Theory (Graduate research course)
Capstone (I, II)

Notable Electives

Circuits and Electronics
Abnormal Psychology
Cognitive Psychology
Comparative Psychology
Ethics and the Professions
Contemporary Ethical Theory