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## Zack Fravel

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<b>Education</b>	<b>Bachelor of Science in Computer Engineering</b> University of Arkansas, Fayetteville, AR. GPA : 3.2
<b>Overview</b>	2+ years experience writing Verilog / VHDL and using a wide range of VLSI design tools. Strong working familiarity with Python, C/C++, Java, JS, HTML. Passionate about psychology, philosophy, and seeking out invigorating creative outlets.
<b>Engineering Coursework</b>	<b>64-point 8-bit Fast Fourier Transform (FFT) Design Project</b> Completed work on a semi-custom VLSI design of a 64-point, 8-bit FFT. The project taught proper design flow using tools from Cadence (Virtuoso, Innovus), Synopsys (HSpice, Design Compiler, Primetime STA), and Mentor Graphics (ModelSim, Calibre).  <b>Framework for oxDNA Simulation Tools</b> Worked on a year long project with a team of other computer scientists to wrap oxDNA in a simplified user interface that allows researchers without programming experience to engage with the tools it has to offer. We constructed the backend using a Django Python server, PostgreSQL database, and Celery for running background tasks. The interface itself was built on Angular2 and implemented a 3D renderer using WebGL.  <b>Research Course on Current Applications in Graph Theory</b> Took a graduate research course in my final semester where all the students performed individual research on a novel subject in the field of graph theory as it relates to computer science. In an attempt to expand my knowledge on music, I created a Python script that implemented graph theoretic analysis on a user-defined pitch class set to calculate parsimonious voice leading on the set's triad and seventh chords.  <b>Low Power Vedic Multiplier Design, Synthesis, and Research Analysis</b> Performed research designing low power CMOS Multiplier circuits using the Urdhva Tiryagbhyam Algorithm found in Vedic Mathematics. I implemented the circuits using structural Verilog and tested their effectiveness in lowering power consumption through synthesis and comparing power analysis results with shift-add multipliers in Vivado.  <b>Microprocessor Architecture Design and Synthesis Projects</b> Completed work in designing, simulating, and synthesizing two different RISC microprocessor architectures. The first was written in VHDL and implemented a MIPS instruction set, the second implemented a SAP-1 architecture and was written in Verilog. The SAP-1 computer was synthesized with Synopsys Design Compiler.  <b>Embedded Systems Terasic Spider Robotics Project</b> Worked with a team on a multi-month project on implementing simple behaviors onto an Altera FPGA robot spider. This class was helpful for getting experience with VLSI design tools and FPGAs. Along with that, we also learned advanced embedded design methods with edge detection, debouncing, wishbone UART controller modules.
<b>Extracurriculars</b>	<b>DIY Electronics and Modular Synthesis</b> I have learned an enormous amount about electronics and art though performing local music and visual shows with a eurorack modular synthesizer. Along with performing music I have experimented with creating my own instruments using my collective knowledge of music and computer/electrical engineering.

<b>References</b>	Dr. Matthew Patitz	(479) 575 - 5590	patitz@uark.edu
	Dr. Christopher Stevens	(479) 575 - 5728	cwsteven@uark.edu
	Dr. Jia Di	(479) 575 - 5728	jdi@uark.edu

## **Curriculum**

### **CSCE Courses**

Programming Foundations (I, II)  
 Digital Design  
 Computer Organization  
 Programming Paradigms  
 Software Engineering  
 Operating Systems  
 System Synthesis and Modeling  
 Embedded Systems  
 Low Power Digital Systems  
 Advanced Digital Design  
 Computer Architecture  
 Computer Graphics  
 Current Applications in Graph Theory (Graduate research course)  
 Capstone (I, II)

### **Notable Electives**

Circuits and Electronics  
 Abnormal Psychology  
 Cognitive Psychology  
 Comparative Psychology  
 Ethics and the Professions  
 Contemporary Ethical Theory