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Zack Fravel

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Education

Bachelor of Science in Computer Engineering GPA : 3.112 **I** Major GPA : 3.250
University of Arkansas, Fayetteville, AR. Graduation : May 2018

Overview

2+ years experience working with VLSI design tools, VHDL, Verilog, and MIPS Assembly. Programming experience working in Git with Python, C/C++, Java, JS, and HTML. Passionate about psychology, philosophy, and seeking out invigorating creative outlets.

Engineering Work

Framework for oxDNA Simulation Tools
Currently working with a team to develop a user friendly, web based front end for oxDNA, a widely used molecular self assembly simulation software. The website is intended to open up these powerful simulation and visualization tools to researchers who lack a computer science background.

64-point 8-bit Fast Fourier Transform (FFT) Design Project
Worked on a semi-custom VLSI design of a 64-point, 8-bit FFT. The project involved using VLSI design tools from Cadence (Virtuoso, Innovus), Synopsys (HSpice, Design Compiler, Primetime STA), and Mentor Graphics (ModelSim, Calibre) in order to synthesize, place, and route the design followed by analysis on timing, area, and power.

Low Power Vedic Multiplier Research
Performed research on designing low power CMOS Multiplier circuits using the Urdhva Tiryagbhyam Algorithm found in Vedic Mathematics. I implemented the circuits using structural Verilog and tested their effectiveness in lowering power consumption by synthesizing and comparing power analysis results with shift-add multipliers in Vivado.

Microprocessor Architecture Simulation and Synthesis Projects
Worked on two independent projects simulating RISC microprocessors. The first project was a behavioral simulation of a pipelined MIPS architecture in VHDL while the second implemented a bus architecture with custom instructions. The latter was designed using Verilog and fully synthesized with the Synopsys Design Compiler using a 90nm process.

Embedded Systems Terasic Spider Robotics Project
Worked with a team on a multi-month project revolving around an Altera FPGA Spider robot. This class was helpful for getting experience with VLSI design tools and FPGAs, designing modules like edge detectors, debouncers, and a Wishbone UART controller.

Android Client/Server Mobile App Software Development
Lead user interface developer in a group project dedicated to the design of a mobile app using Android for a cashier service with integrated SQL databases and shopping cart.

Extracurriculars

Modular Synthesist
I have learned an enormous amount about electronics and art though performing local music and visual shows with a eurorack modular synthesizer. My experience with modular synthesizers in a lot of ways opened up my creativity and gave me new insights into the relationship between engineering and the creative process.

KXUA Radio DJ
University of Arkansas, Fayetteville (2014 - 2016)

References

Dr. Matthew Patitz	(479) 575-5590	patitz@uark.edu
Dr. Jia Di	(479) 575-5728	jdi@uark.edu

Curriculum

CSCE Courses

Programming Foundations (I, II)
Digital Deisgn
Computer Organization
Programming Paradigms
Software Engineering
Operating Systems
System Synthesis and Modeling
Embedded Systems
Low Power Digital Systems
Advanced Digital Design
Computer Architecture
Computer Graphics
Current Applications in Graph Theory (Graduate research course)
Capstone (I, II)

Notable Electives

Circuits and Electronics
Abnormal Psychology
Cognitive Psychology
Comparative Psychology
Ethics and the Professions
Contemporary Ethical Theory