

# Zack Fravel

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<b>Career Profile</b>	I'm a computer engineering graduate with 4 years of academic experience designing circuits and programming. I also have 2 years of experience working in electronics manufacturing. I'm currently enrolled in the Design Verification and Validation program at Portland State.	
<b>Highlights</b>	<ul style="list-style-type: none"><li>• 2 years of hardware design experience with Verilog, VHDL, and industry standard tools.</li><li>• Proficient in fundamental programming paradigms and scripting with Python.</li><li>• Experienced troubleshooter in time-sensitive, high-volume manufacturing conditions.</li></ul>	
<b>Education</b>	<b>Master of Science in Electrical &amp; Computer Engineering</b> Portland State University, Portland, OR.	<b>September 2020 - Present</b>
	<b>Bachelor of Science in Computer Engineering</b> University of Arkansas, Fayetteville, AR.	<b>August 2014 - May 2018</b>
<b>Work</b>	<b>Intel</b> Aloha, OR <i>Die Sort Manufacturing Technician</i>  Worked full-time on the night shift at Intel performing troubleshooting, preventative maintenance tasks and advanced calibrations on state-of-the-art manufacturing tools. As shift maintenance team coordinator, I frequently collaborated with engineering teams to implement improved procedures for a safer, more efficient sort floor.	<b>May 2019 - April 2020</b>
	<b>Electronics Assembly Technician</b> Portland, OR  Contributed as an assembly technician for two modular synthesizer startups in Portland. I am trained in through hole and SMT soldering and have experience in electronics manufacturing from PCB design, assembly, QC and rework, to shipping.	<b>July 2018 - May 2019</b>
<b>Experience</b>	<b>System Synthesis and Modeling: Reduced MIPS and Custom ISA Synthesis Projects</b> Designed and tested two microprocessor architectures in VHDL and Verilog respectively. The first design I completed was a Pipelined MIPS Datapath capable of handling branch, jmp, memory, and arithmetic functions. The second project was more complex as it was written in Verilog, synthesized using Synopsys Design Compiler, and was a more custom design.	
	<b>Embedded Systems: FPGA Design and Synthesis</b> Completed a wide variety of FPGA design projects that taught me the importance and potential of rapid prototyping. I gained a solid understanding of the fundamentals of FPGA architecture and prototyping with simple FSM designs like traffic lights and vending machines to more complex designs like a Wishbone-UART Rx/Tx Bus.	
	<b>Digital Design, Synthesis, and Layout</b> Gained about a year of experience with industry standard digital design tools from Synopsys (HSPICE, Design Compiler), Cadence (Innovus, Virtuoso), and Mentor Graphics (Modelsim, Calibre) learning the fundamentals of design synthesis, placement, and routing techniques.	
	<b>Low Power Digital Systems Design: Vedic Multiplier</b> Spent a semester studying the fundamentals of low power digital design from circuit-level power reduction techniques all the way up to algorithm and system-level low power methodologies. The semester culminated in a project where I used an algorithm from Vedic mathematics to design a low-power multiplier.	