Zack Fravel

Mailing Address:
4607 SE Taylor St
Portland, OR 97215

Email: mail@zackfravel.com
Phone: (501) 519 7667

Skills

2 years experience writing Verilog / VHDL and working with VLSI design tools.
Working familiarity with Python, C/C++, Java, JS, and HTML.
Experienced troubleshooting in time-sensitive, high-volume manufacturing conditions.

Work

Intel
Manufacturing Technician
May 2019 - Present

Currently working at Intel's Aloha Factory Operations in Oregon as a Die Sort Manufacturing Technician. I primarily work on hands-on tasks that range from repairing down tools to preventative maintenance. In the few months I've been at Intel, I have been able to gain enough skill to start leading our maintenance team as well as work with engineering to discuss issues with the tools and potential routes for troubleshooting.

Moffenzeef Modular, LZX Industries, and Barefoot Sound
Electronics Assembly Technician
August 2018 - May 2019

Worked as a contracted assembly technician for two synthesizer startups and a professional studio monitor manufacturer in Portland. Thoroughly trained in electronics assembly techniques, I have experience in almost every level of small parts electronics manufacturing from design to assembly, QC/rework, packing, and shipping.

Education

Bachelor of Science in Computer Engineering
University of Arkansas, Fayetteville, AR. GPA: 3.2. Graduated May 2018.

Project Experience

64-point 8-bit Fast Fourier Transform (FFT) Design Project
The project taught me some of the fundamentals of physical design flow using tools from Cadence (Innovus, Virtuoso), Synopsys (Design Compiler, HSpice, Primetime STA), and Mentor Graphics (ModelSim, Calibre).

Low Power Vedic Multiplier Design, Synthesis, and Research Analysis
Performed research designing low power CMOS Multiplier circuits using the Urdhva Tiryagbhyam Algorithm from Vedic Mathematics in order to both minimize computation time and resources by taking advantage of parallelization. I implemented the circuits with structural Verilog and tested their effectiveness by comparing power analysis results with standard shift-add multipliers using Xilinx Design Tools.

Microprocessor Architecture Design and Synthesis Projects
Completed work in designing, simulating, and synthesizing two individual RISC microprocessor architectures. The first was written in VHDL and implemented a MIPS instruction set, the second implemented a SAP-1 architecture and was designed using Verilog. I did RTL Synthesis on the SAP-1 design, along with a gate-level simulation.

Research Course on Contemporary Applications in Graph Theory
Completed a graduate research course where I learned the how to take advantage of graph theory for data analytics using Python. I worked on projects in variety of areas including political polarization analysis, social network analysis, and game theory.

References available upon request.

Updated Nov 7, 2019