EE 330 FINAL DESIGN REPORT

Digital Potentiometer, Amplifier, and DAC Design

Abstract

A report on the design of an integrated circuit implementing a digital potentiometer, amplifier, and digital-to-analog converter

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Project Design Requirements

For our EE 330 final project, we were instructed to design an integrated circuit with four modes, each allowing the circuit to behave like a different type of component. The user should be able to select the operating mode of the circuit by setting the logic values of two input lines, A_0 and A_1, and to be able to further modify the behavior of the circuit by changing the logic values of four additional lines, C_0, C_1, C_2, and C_3. For the remainder of this document, the C_n lines will be referred to as the characteristic input since these lines modify the characteristics of each mode. Each of the circuit's four modes is discussed in more detail in the following paragraphs.

The first mode of the circuit occurs when A_0 and A_1 are set to $(0,0)$, respectively. In this mode, per the project description, the circuit behaves as a noninverting finite gain amplifier, wherein the gain of the amplifier is programmable through the circuit's C_n inputs. Because of restraints emplaced on the values of V_{DD} and V_{SS}, the output of the amplifier is limited to values between $\pm 0.9V$. Additionally, because of the lack of discussion of op-amp design in EE 330, the op-amp does not feature internal compensation. Thus, the user must provide external compensation.

The second mode of the circuit occurs when A_0 and A_1 are set to $(0,1)$, respectively. In this mode, the circuit behaves as a programmable inverting finite gain amplifier where, once again, the gain is programmable through the C_n inputs. As with the programmable noninverting mode, the output of the op-amp is limited to values between $\pm 0.9V$. Further, once again, the user must provide external compensation for the op-amp.

When A_0 and A_1 are set to $(1,0)$, respectively, the circuit enters its third mode of operation. In this mode, the circuit behaves as a 4-bit DAC where the user selects the output voltage level using the C_n characteristic inputs. The user may select up to 16 different voltage levels, which scale linearly from 0 to $\frac{15}{16}V_H$ in increments of $\frac{1}{16}V_H$. The output voltage is dependent on a V_{REF}, in our case V_H, which is in reference to GND.

In the fourth mode of the circuit, which occurs when A_0 and A_1 are set to $(1,1)$, the circuit behaves independently as a potentiometer and operational amplifier. In this mode, the user is given complete control over these two components; thus, care must be taken so that the input voltages are set appropriately to avoid forward biasing the parasitic diodes found in the MOSFETs

Global Design Choices

Due to the mixed-signal nature of this circuit, it is necessary to establish global logic-high and logic-low voltage levels. For all sub-circuits, except for the independent potentiometer found in the fourth mode of operation, logic-high is considered to be V_{DD} and logic-low is considered to be V_{SS}. Thus, for the user to control the circuit, the A_n and C_n lines must be driven to $\pm 0.9V$.

Design Breakdown

At a high level, the circuit is grouped into four sub-circuits, each of which implements one of the circuit's four modes. Each sub-circuit is always active and always outputting a signal. A 4-to-1 multiplexer is used

to allow the user to select which sub-circuit to output, thus allowing the user to switch between modes. The 4-to-1 multiplexer's select lines are tied to the circuit's A_0 and A_1 lines. Figure 1, below, shows the circuit's compartmentalized design.

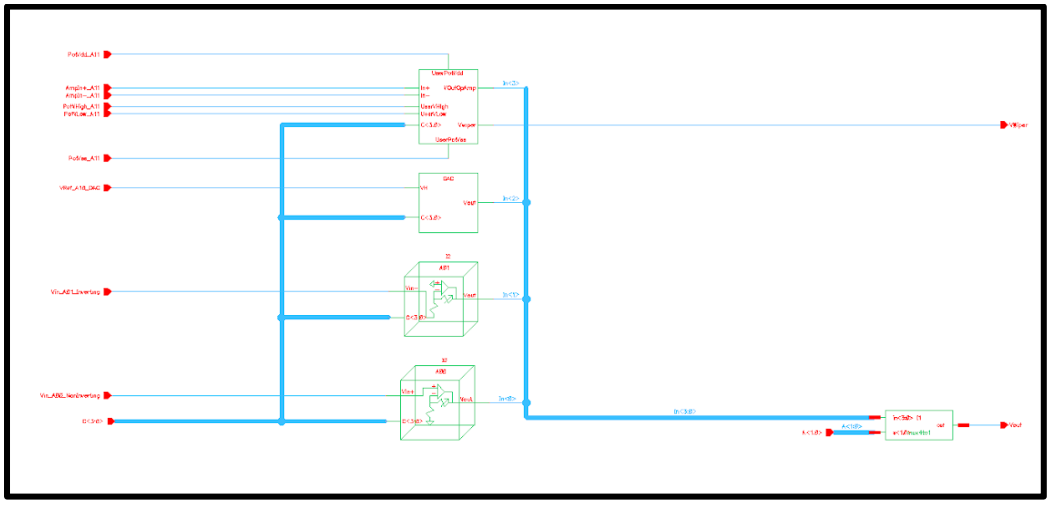

Figure 1: Overall Circuit Design

Notice that the circuit has two outputs available to the user; one which comes from the 4-to-1 multiplexer, and one which comes from the independent digital potentiometer (Mode 4). It was necessary to make the circuit have two outputs instead of one because a multiplexer is unable to output two signals at once. As a result of this, the user is always able to access the circuit's independent potentiometer even when A_0 and A_1 are not set to $(1,1)$.

Building Blocks

Just as the overall circuit can be broken down into a set of four sub-circuits, each sub-circuit can be broken down into a set of smaller components, termed "building blocks." These building blocks include a transmission gate, a 4-to-1 multiplexer, an operational amplifier, a resistor array, and a 3-to-8 decoder. Each building block is discussed in further detail below.

Transmission Gate

Due to the analog nature of this project, there are several locations in the circuit where current must be able to flow bi-directionally through switches. NMOS and PMOS switches are not suitable for these locations because of their unidirectional nature. Because of this, it was necessary to design a transmission gate, which is simply a circuit consisting of an NMOS and PMOS tied together with complementary inputs. The schematic for the transmission gate used in the final circuit can be seen in Figure 2, below.

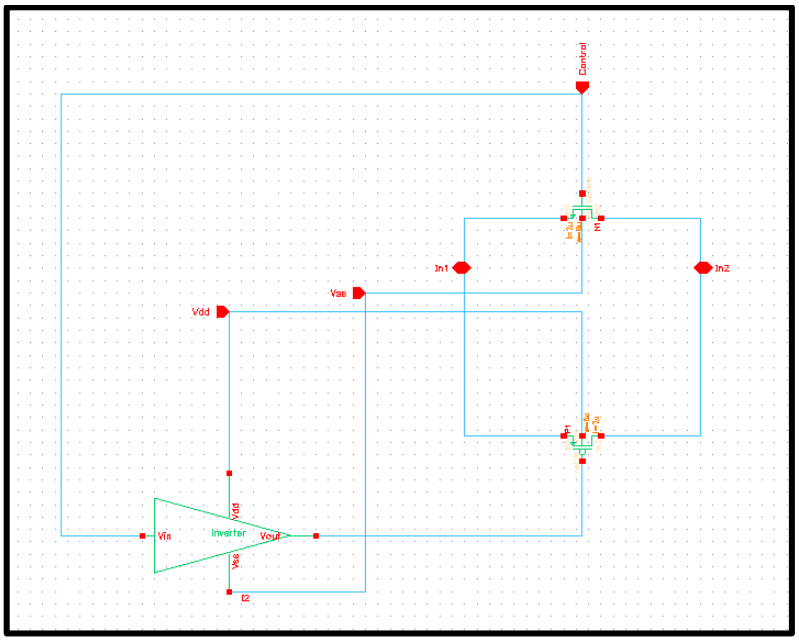

Figure 2: Transmission Gate Schematic

Of primary importance in this schematic is that the drains and sources of the NMOS and PMOS transistors are tied together and that the gates of the transistors are complementary. As a result of this, when the $Control$ input is low, both transistors are forced into the cutoff region of operation, thus meaning that current is unable to flow between $In1$ and $In2$. However, when the $Control$ input is high, both transistors are enabled and are allowed to operate in the triode and saturation regions, depending on the voltage present at the transistors' drains and sources. When operating like this, current can flow from $In1$ to $In2$ by passing through the PMOS transistor, and current can flow from $In2$ to $In1$ by passing through the NMOS transistor. Table 1, below, describes the expected operation of the transmission gate.

	$Control = 1$	$Control = 0$
Flow from $In1$ to $In2$	Possible	Not Possible
Flow from $In2$ to $In1$	Possible	Not Possible

Table 1 Transmission Gate Expected Behavior

To test the transmission gate, the testbench circuit seen in Figure 3, below, was created. In this testbench, the transmission gate's V_{DD} and V_{SS} were set to $\pm 0.9V$, respectively, and V_{in} was set to be a sinusoidal waveform with an amplitude of $0.9V$ and a frequency of $2.5kHz$. V_{cont} was set to be a square wave with a period of $500\mu s$ which went from logic-high (V_{DD}) to logic-low (V_{SS}) in $1ns$. The transmission gate load, R_0, was arbitrarily selected to be a $5k\Omega$.

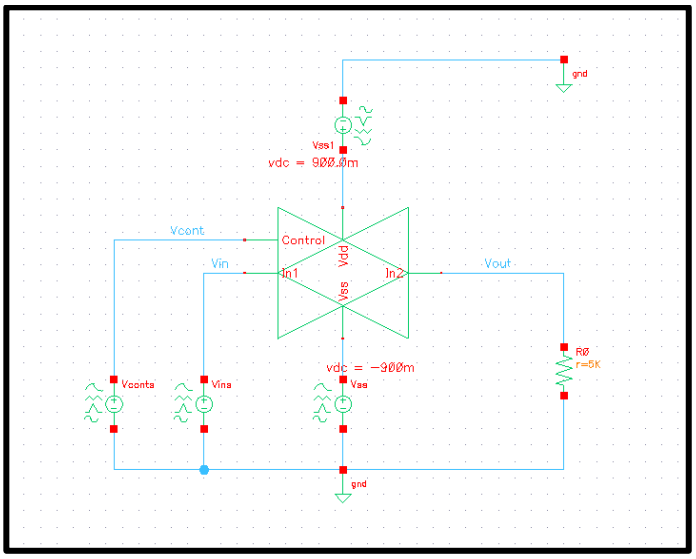

Figure 3: Transmission Gate Testbench Circuit Schematic

A transient analysis was run for $2ms$, allowing for the waveform in Figure 4, below, to be obtained.

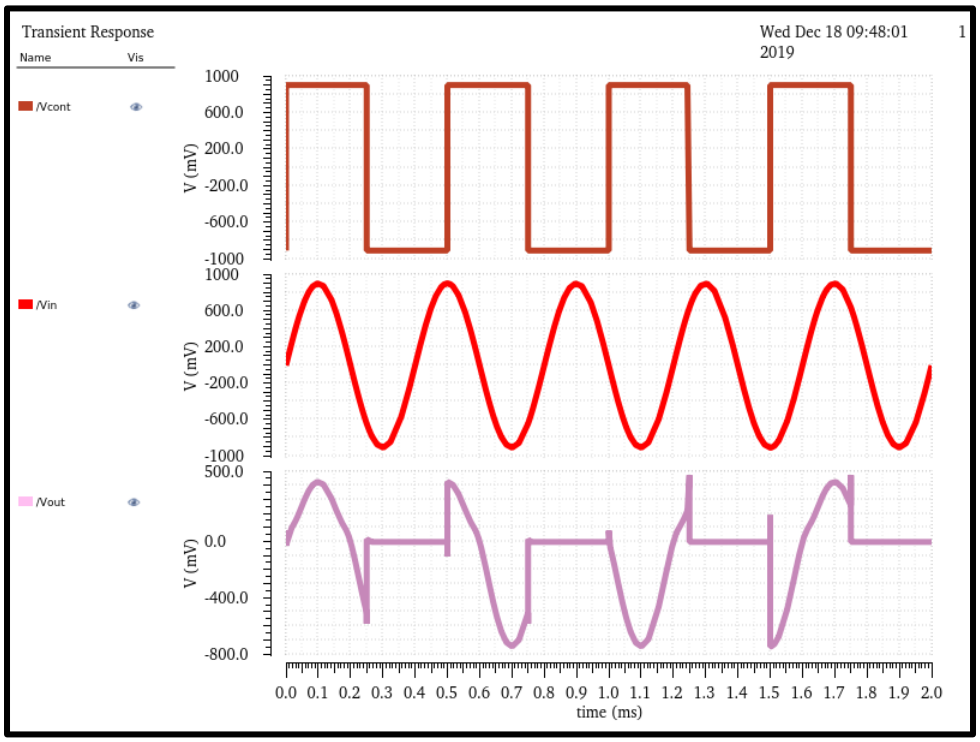

Figure 4: Transmission Gate Testbench Results. $V_{cont} = Brown, V_{in} = Red, and\ V_{out} = Pink.$

As can be seen from these results, V_{out} (pink) follows the V_{in} (red) waveform whenever V_{cont} (brown) is high. This is true even when V_{in} is negative, thus indicating that the transmission gate is capable of allowing current to flow bidirectionally.

It should be noted that V_{out} is not an exact duplicate of V_{in}. Rather, the amplitude of V_{out} is approximately $0.45V$ less than the amplitude of V_{in}. This is because V_{cont} is a constant value and V_{in} is

not. As a result, as V_{in} increases, V_{GS} approaches V_T. When this happens, the current through the MOSFETs in the transmission gate decreases, causing V_{out} to never approach V_{in}.

Once the circuit had been tested and was confirmed to be functioning correctly, a layout was created for the transmission gate. This layout can be seen in Figure 5, below.

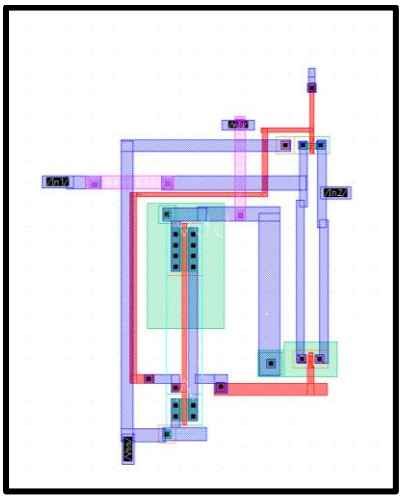

Figure 5: Transmission Gate Layout

To ensure the validity of this layout, a DRC and LVS check was performed. Results from both checks can be seen in Figure 6, below.

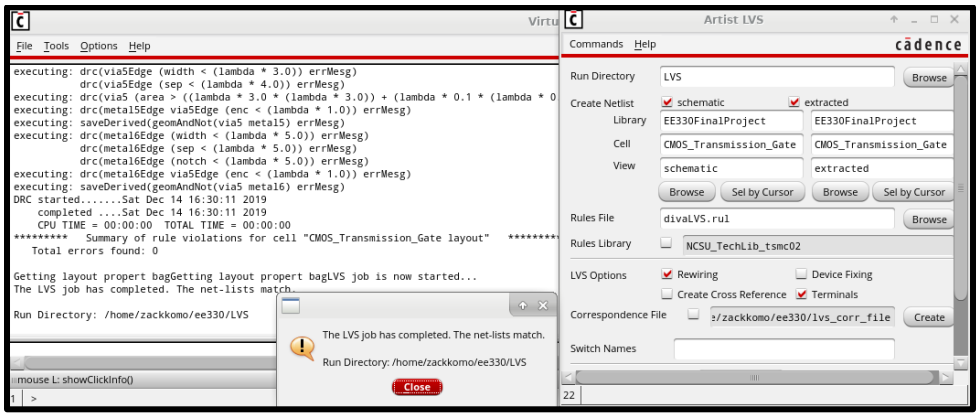

Figure 6: Transmission Gate DRC and LVS Results

Note that both checks state that no errors were found and that all net-lists match. This indicates that the transmission gate layout is correct and matches the transmission gate schematic.

4-to-1 Multiplexer

Because of how it was decided to handle mode-selection (that is, by having four sub-circuits always on and using a multiplexer to choose which output is seen by the user), it was necessary to design a 4-to-1 multiplexer. Because an analog multiplexer is simply a digital multiplexer which is capable of passing

analog signals, designing a 4-to-1 analog multiplexer was a simple task. The schematic for the 4-to-1 multiplexer used in the final circuit can be seen in Figure 7, below.

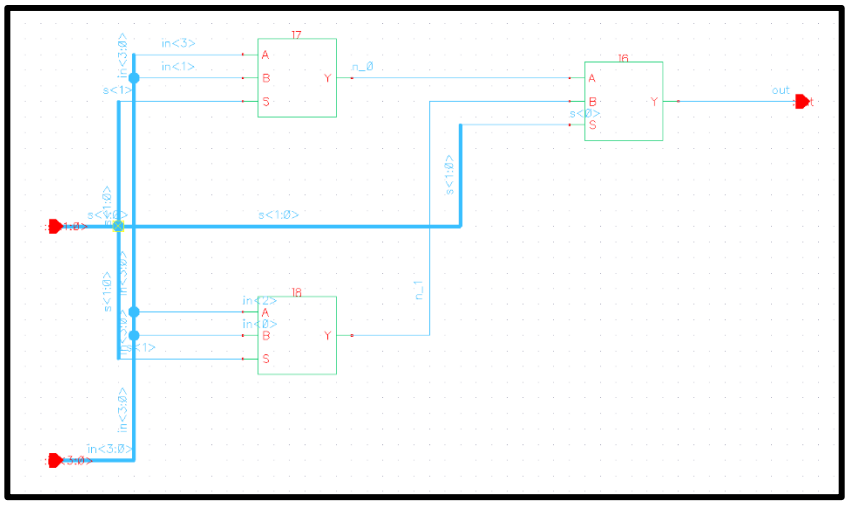

Figure 7: 4-to-1 Analog Multiplexer Schematic

As can be seen from this schematic, the 4-to-1 analog multiplexer is a set of three 2-to-1 analog multiplexers. The schematic for each 2-to-1 multiplexer can be seen in Figure 8, below.

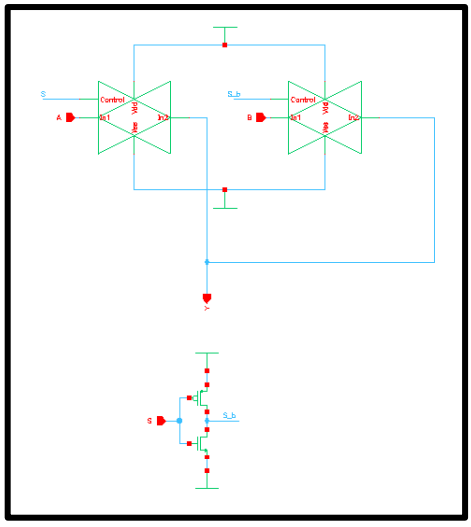

Figure 8: 2-to-1 Analog Multiplexer Schematic

Note that this schematic utilizes two transmission gates to implements the multiplexer's logic instead of two MOSFETs, thus allowing the multiplexer to handle bi-directional current flow. This is what allows the multiplexer to be an analog multiplexer instead of a standard digital multiplexer.

Because they can be easily tested during the construction of the overall circuit, special testbenches were not created for the 4-to-1 and 2-to-1 multiplexers. Their operation will be confirmed to be working later in this report when they are integrated into the final circuit schematic.

A layout for the 2-to-1 multiplexer was created to make that of the 4-to-1 multiplexer more modular. The aforementioned layout can be found in Figure 9, below.

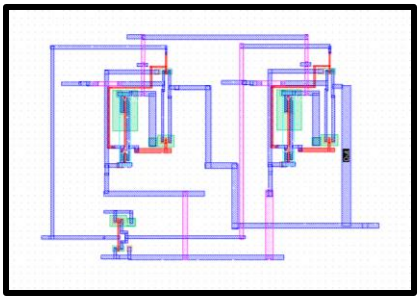

Figure 9: 2-to-1 Analog Multiplexer Layout

To ensure the validity of this layout, a DRC and LVS check was performed. Results from both checks can be seen in Figure 10, below.

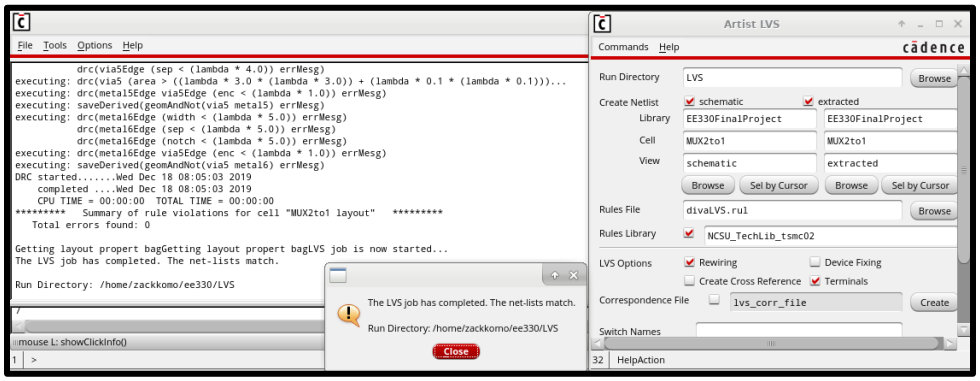

Figure 10:2-to-1 MUX DRC and LVS Results

After the layout for the 2-to-1 multiplexer, a layout for the 4-to-1 multiplexer was created. This can be seen in Figure 11, below.

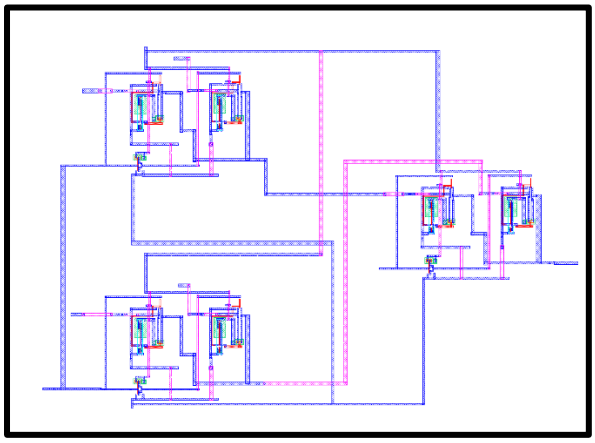

Figure 11: 4-to-1 Analog Multiplexer Layout

Once again, to make sure the layout was done correctly, a DRC and LVS check were performed. The results of these checks can be seen in Figure 12, below.

Figure 12: 4-to-1 Analog Multiplexer DRC and LVS Results

Operational Amplifier

In addition to a transmission gate and 4-to-1 multiplexer, it was also necessary to design an operational amplifier for use in each sub-circuit. Per the project document's recommendations, a standard two-stage, externally compensated op-amp was created. The schematic for this amplifier can be seen below, in Figure 13.

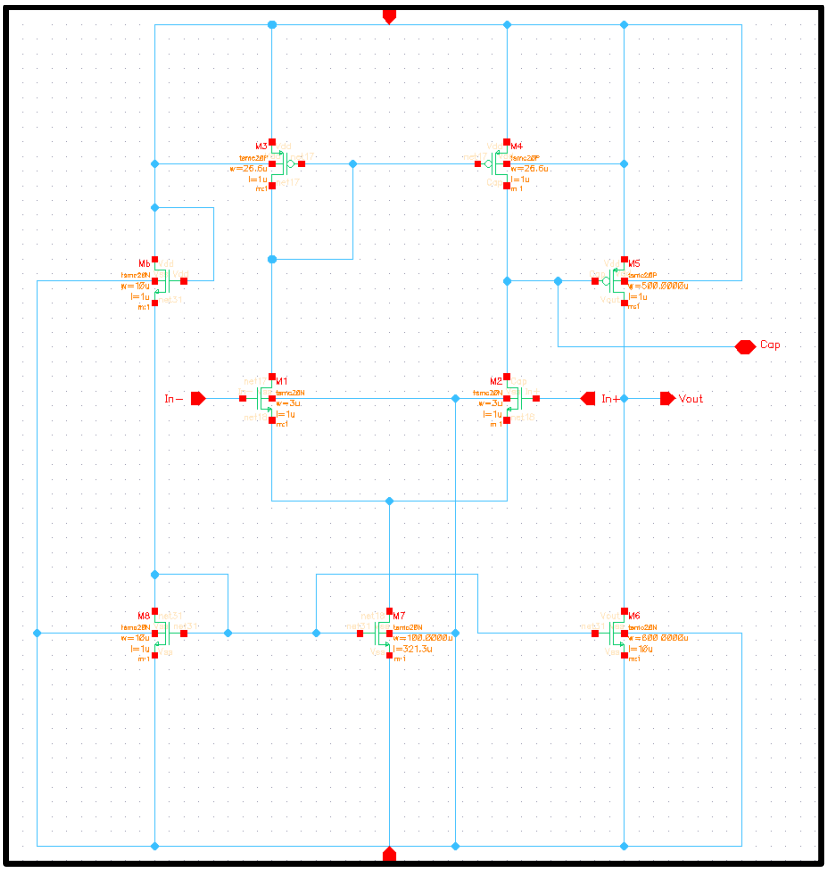

Figure 13: Operational Amplifier Schematic

Wherein M_1, M_2, M_3, and M_4 form the first stage of the amplifier, M_5 forms the second stage of the amplifier, and all other MOSFETs are used for biasing purposes. When originally designed, the amplifier was designed with the external compensation being located inside the amplifier. That is, there was not a

pin that allowed the user to use their compensation capacitor. The value of the internal compensation was $10pF$, thus meaning that all of the math used in the amplifier was based on a $10pF$ capacitor. While the amplifier does work for other compensation values, it performs best when $10pF$ is used.

When designing the amplifier, it was necessary to choose values for some of the amplifier's characteristics, such as slew rate (which influences how much current M_7 must be able to sink) and the amplifier's $40dB$ frequency (which influences the sizing of M_5). Because EE 330 did not discuss amplifier design, many characteristics were based on the LMC 660 amplifier, which is what is used in lab. These characteristics can be seen below:

Characteristic	**Desired Value**
Slew Rate	$\frac{1.1V}{\mu s}$
DC Offset Voltage	$0V$
$V_{out-max}$	V_{DD}
$V_{out-min}$	V_{SS}
$40dB$-Frequency	$> 100kHz$

Table 2: Op-Amp Desired Characteristics

To test the functionality of the designed op-amp, the testbench seen below was created. In this testbench, the op-amp is set up in a unity-gain configuration where V_{out} is tied directly to the op-amp's In_- port. The amplifier's V_{DD} and V_{SS} are connected to $0.9V$ and $-0.9V$, respectively, and the op-amp's In_+ port is connected to a sinusoidal source with an amplitude of $100mV$ and a frequency of $100kHz$.

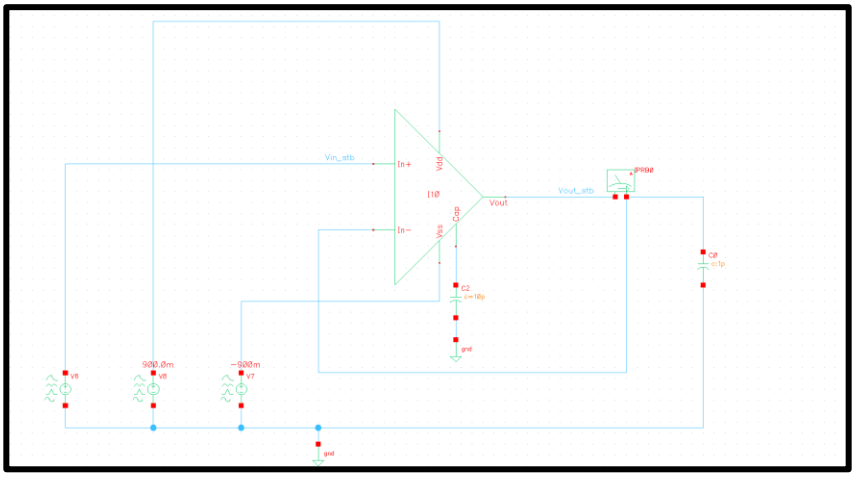

Table 3: Op-Amp STB TB Setup

An STB analysis was run on the testbench circuit, allowing for the amplifier's gain and phase to be plotted versus frequency. These graphs can be seen in the figure below.

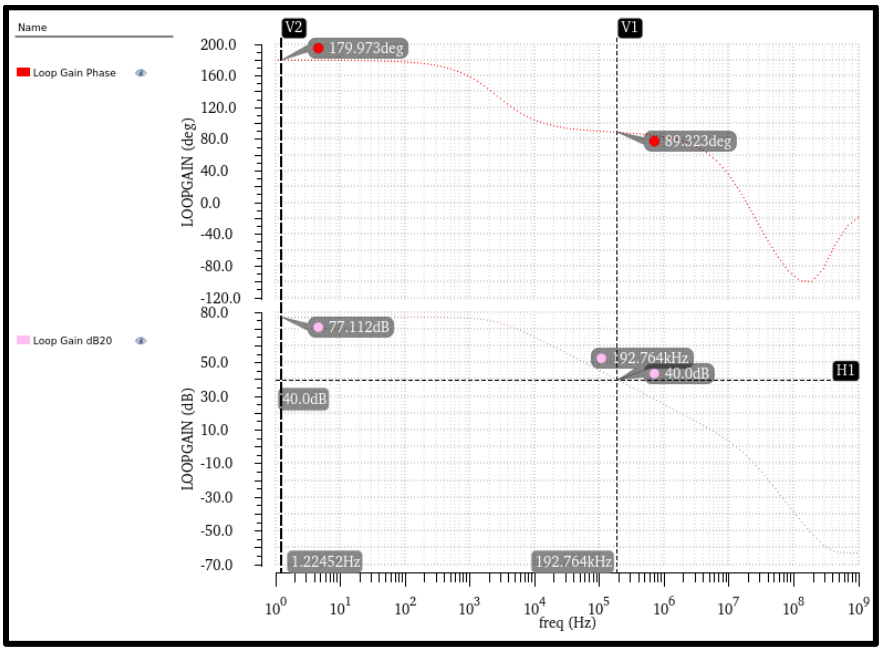

Figure 14: Op-Amp Loop Gain and Loop Phase Plots

An additional testbench was also created to identify the amplifier's maximum output, minimum output, and slew rate. These testbenches worked by setting the op-amp in an inverting configuration and by setting the amplifier's input to a large square-wave signal which transitions from high to low, and low to high, in $1ns$. The data collected from these testbenches are shown in the table below.

	Actual Values	**Desired Values**
Low-Frequency Gain	$77.1dB$	∞
$40dB$ Frequency	$192.7kHz$	$> 100kHz$
Low-Frequency Phase	$179.9°$	$180°$
$40dB$ Phase	$89.3°$	$90°$
Slew Rate	$\frac{3.26V}{\mu s}$	$\frac{1.1V}{\mu s}$
DC Offset Voltage	$3.5mV$	$0V$
$V_{out-max}$	$824.3mV$	V_{DD}
$V_{out-min}$	$-833.9mV$	V_{SS}

Figure 15: Measured and Ideal Amplifier Characteristics

As can be seen from this table, the amplifier performs reasonably well, although it fails to reach several of the characteristics which were desired. For example, it does not have an infinite low-frequency gain and it does not have a slew rate of $1.1V$ per microsecond. The amplifier's lack of infinite low-frequency gain can be attributed to the fact that a physical amplifier can't have an infinite gain. In EE 230, it was stated that a good amplifier should have a gain of approximately $10k$, or $80dB$. $77.1dB$ $(7.161k)$ is less than $80dB$ but is also reasonable given how the amplifier will be used in this circuit.

The difference between the expected slew rate and the measured slew rate is most likely the result of experimentally modifying transistor width-length ratios after the initial math. In the original design, the amplifier was unable to provide a satisfactory gain; instead of amplifying the input signal, it attenuated it. It was difficult to determine why this was occurring mathematically, however, the problem was able

to be fixed by changing the width-length ratios of several of the transistors used in the second stage. It seems likely that the difference between the expected and measured slew rates is the result of these changes.

Resistor Array

Because a digital potentiometer is necessary for all four modes of the circuit, a resistor array building block was also designed. The resistor array design used in the final circuit is based on Dallas Semiconductor's Maxim DS 1666 resistor array and can be seen in the figure below.

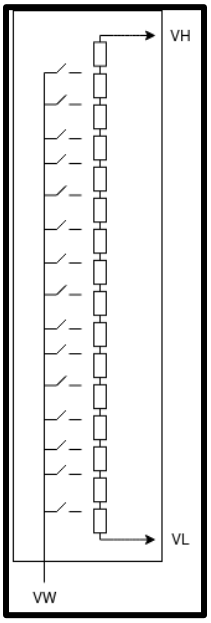

Figure 16: Resistor Array Schematic

Wherein each resistor in the design is a $5k\Omega$ resistor, V_H is the high side of the resistor, and V_L is the low side of the resistor. A 16-bit, one-hot encoded input controls which switch in the resistor is closed, thus allowing for the resistance between V_H and V_W to be adjusted linearly. In the array's schematic, each switch is substituted with a transmission gate, thus allowing the resistor array to handle bi-directional current flow. This can be seen in the figure below.

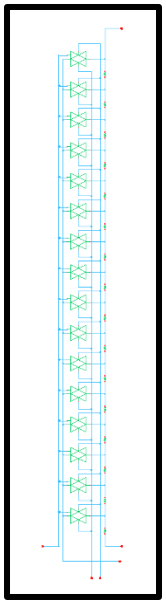

Figure 17: Schematic for Digital Potentiometer

A zoomed-in image of the resistor array, which makes it easier to see connections between the transmission gates, is provided below.

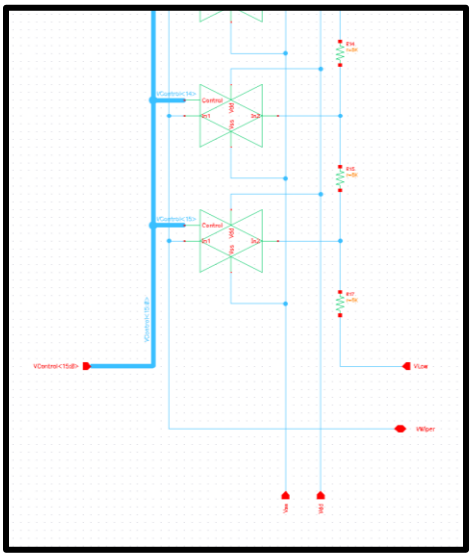

Figure 18: Zoomed in view of Digital Potentiometer

Similar to the 4-to-1 multiplexer, testbench results will not be provided in this section of the document since the functionality of the resistor array can be easily gauged by observing the noninverting amplifier testbench results, which will be presented later in this document.

Once designed, a layout for the digital potentiometer was created. This layout can be seen below.

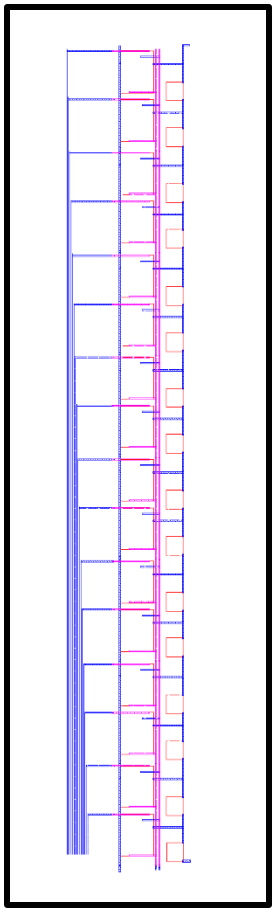

Figure 19: Layout for the Resistor Array

Once complete, a DRC and LVS check were performed. The results from these checks can be seen below. Because both checks passed, it can be concluded that the resistor array's layout matches the array's schematic.

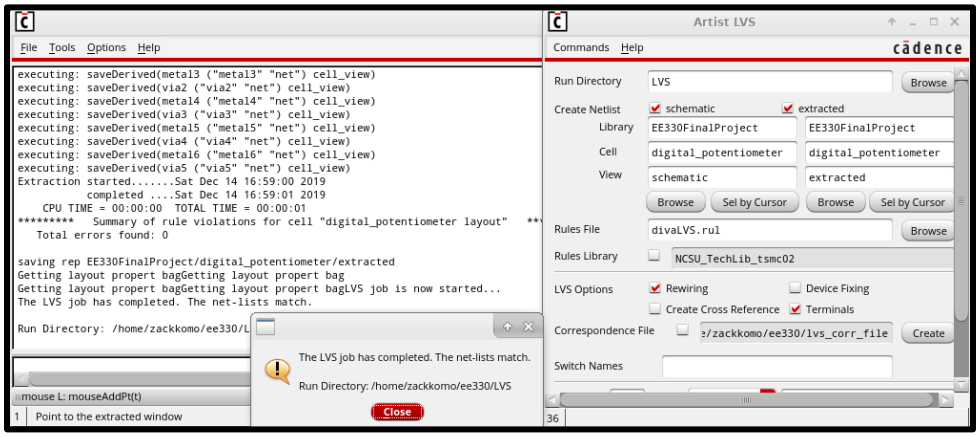

Figure 20: Test results for DRC and LVS

4-to-16 Decoder

To be able to convert the 4-bit C_n input lines into a 16-bit data bus, a 4-to-16 decoder was necessary. The 4-to-16 decoder was initially created and tested in Verilog, as can be seen in the figure below.

```
module decoder4to16 (
binary_in   , //  4 bit binary input
decoder_out , //  16-bit  out
 );

 input [3:0] binary_in  ;
 output [15:0] decoder_out;
 reg [15:0] decoder_out ;

always @ (binary_in)
begin
  decoder_out = 0;
    case (binary_in)
      4'h0 : decoder_out = 16'h0001;
      4'h1 : decoder_out = 16'h0002;
      4'h2 : decoder_out = 16'h0004;
      4'h3 : decoder_out = 16'h0008;
      4'h4 : decoder_out = 16'h0010;
      4'h5 : decoder_out = 16'h0020;
      4'h6 : decoder_out = 16'h0040;
      4'h7 : decoder_out = 16'h0080;
      4'h8 : decoder_out = 16'h0100;
      4'h9 : decoder_out = 16'h0200;
      4'hA : decoder_out = 16'h0400;
      4'hB : decoder_out = 16'h0800;
      4'hC : decoder_out = 16'h1000;
      4'hD : decoder_out = 16'h2000;
      4'hE : decoder_out = 16'h4000;
      4'hF : decoder_out = 16'h8000;
       endcase
  end
  endmodule
```

Figure 21: 4-to-2 Digital Multiplexer Verilog Code

To test the decoder, a simple Verilog testbench which runs through all possible values of the input was created. This code, along with the results of this code, can be seen in the following two figures.

```
module decoder_TB();
reg [3:0] A;
wire [15:0] B;

initial  A = 4'b0;

decoder4to16 test(.binary_in(A), .decoder_out(B));

always
begin
#10;
assign A = A+1;
end
endmodule
```

Figure 22: Test bench code for 4-to-16 Decoder

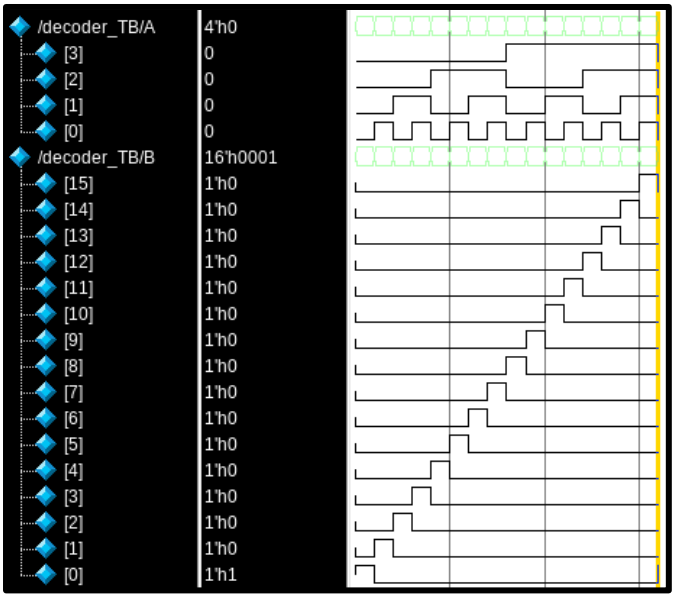

Figure 23: Results of testbench for the 4-to-16 decoder

Of key importance in the testbench results is that only one of the sixteen possible outputs are active for a given combination of the input, A. This is expected behavior for a 4-to-16 decoder.

Once designed and tested, Genus was used to synthesize the decoder's Verilog code into a Cadence schematic. The synthesized schematic can be seen below.

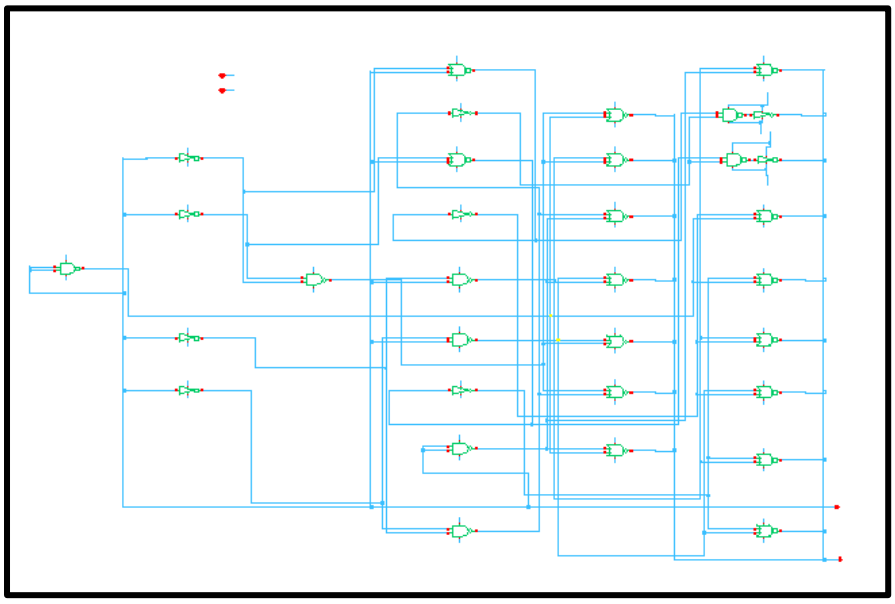

Figure 24: Schematic for 4-to-16 decoder

It is important to note that, when synthesized, Genus assumed that logic-high should be V_{DD} and that logic-low should be GND, or $0V$. To correct this, it was necessary to modify the OSU cells so that the gates' V_{DD} and V_{SS} could be passed in as inputs instead of being global values. Additionally, it was necessary to connect the bulks of the NMOS and PMOS transistors to V_{SS} and V_{DD}, respectively.

To ensure that no mistakes were made while modifying the synthesized logic, a simple testbench (seen in the below figure) was created. This testbench passes in $0.9V$ and $-0.9V$ for the decoder to use as V_{DD} and V_{SS} and is set up such that every combination of four 1-bit inputs is simulated. The result of this testbench is similar to the one seen in ModelSim, indicating that the schematic was synthesized and modified successfully.

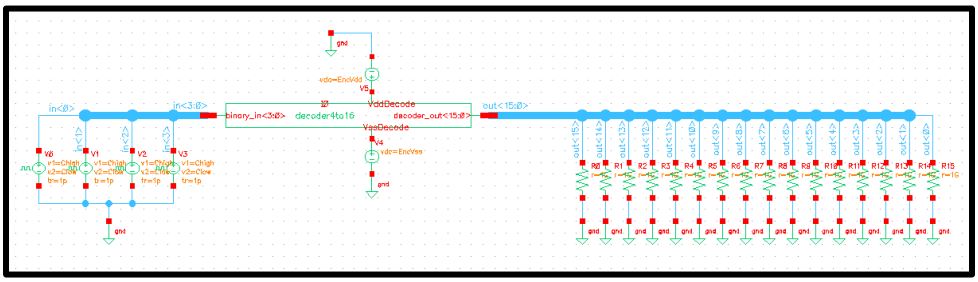

Figure 25: Cadence testbench for the 4-to-16 decoder

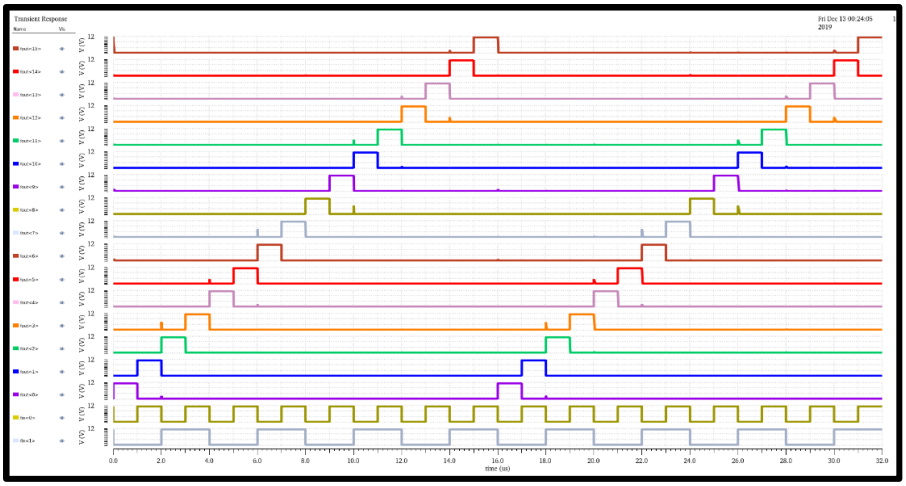

Figure 26: Results from cadence testbench for the 4-to-16 decoder

After confirming that the schematic had been synthesized and modified correctly, a layout was generated using Innovus. The generated layout can be seen below.

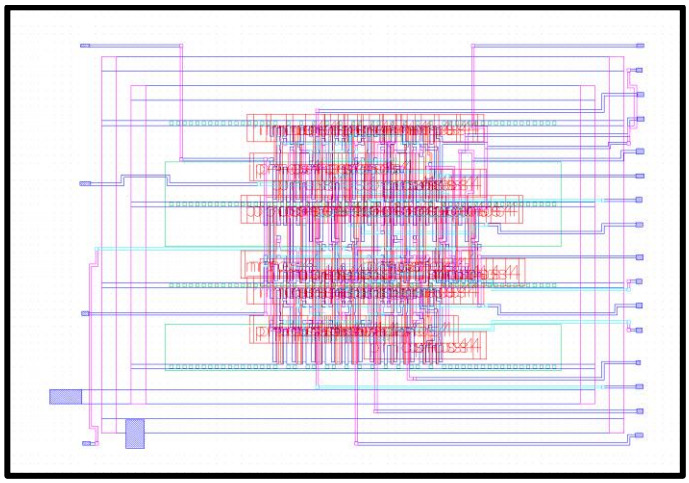

Figure 27: Layout for the 4-to-16 decoder

A note about the above layout is that the changes made in the schematic did not transfer to the layout. Thus, it was necessary to adjust the decoder's input pins and bulk connections on the layout. The results of the DRC and LVS checks can be seen below.

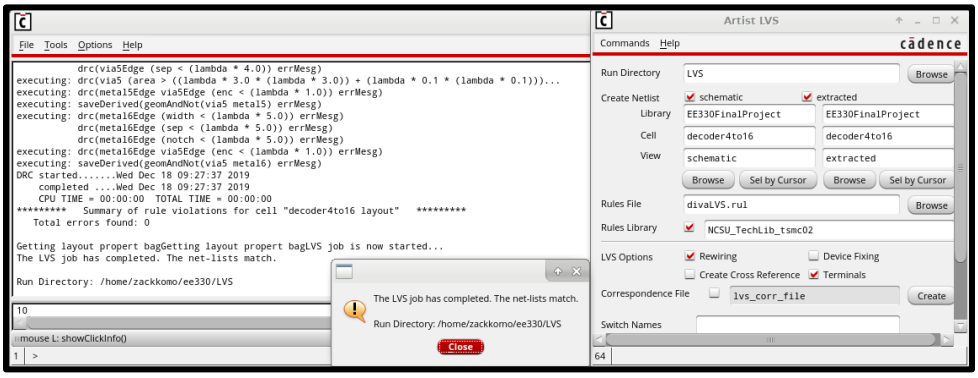

Figure 28: Results of DRC and LVS test for the 4-to-16 decoder

Implementation

To implement each of the four previously discussed sub-circuits, the five building blocks were connected in different configurations. The design of each sub-circuit can be seen below.

$(A_0, A_1) = (0,0)$: Programmable Noninverting Amplifier

To create a programmable noninverting amplifier, an op-amp and resistor array were connected such that one end of the resistor array was connected to GND, one end of the resistor array was connected to the amplifier's output, and the resistor array's wiper was connected to the op-amp's positive input terminal. This configuration can be seen in the figure below.

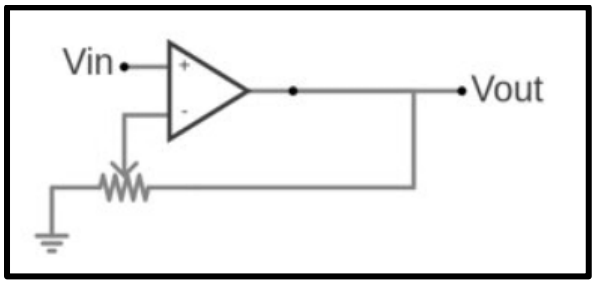

Figure 29: Programmable Noninverting Amplifier Configuration

Wherein the wiper location can be adjusted through the C_n input lines, which is padded through a 4-to-16 decoder. The amplifier's schematic can be seen below.

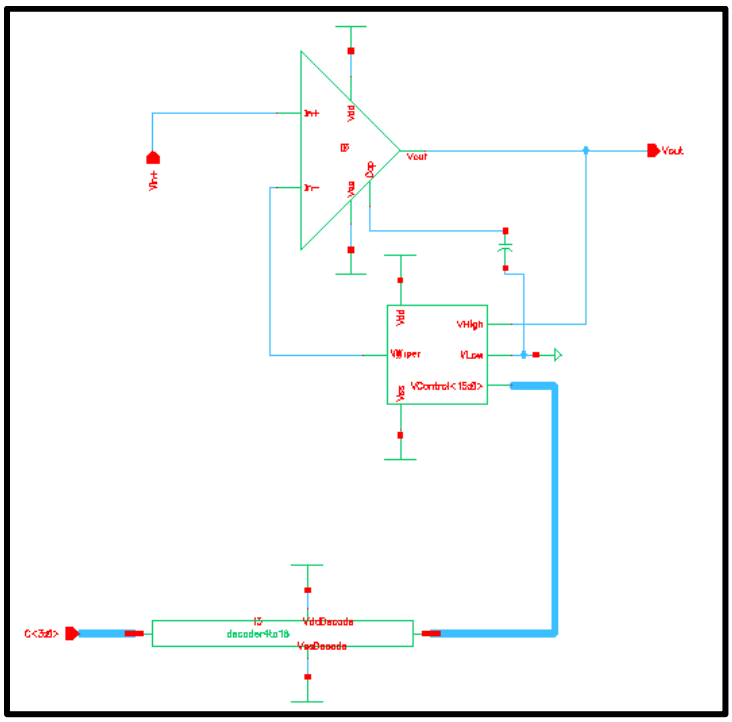

Figure 30: Programmable Noninverting Amplifier Schematic

To test this circuit, the following testbench circuit was created. Global V_{DD} was set to $0.9V$, global V_{SS} was set to -0.9V, and each of the input C_n lines was set to be a square wave that went from $-0.9V$ to $0.9V$. The amplifier's input was connected to a sinusoidal source with an amplitude of $56.25mV$ and a frequency of $2kHz$.

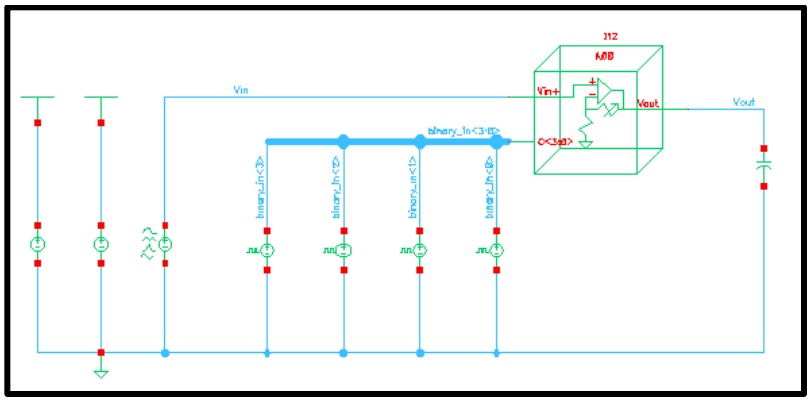

Figure 31: Programmable Noninverting Amplifier Testbench Circuit

A transient analysis was run for $8ms$, allowing the waveforms below to be obtained.

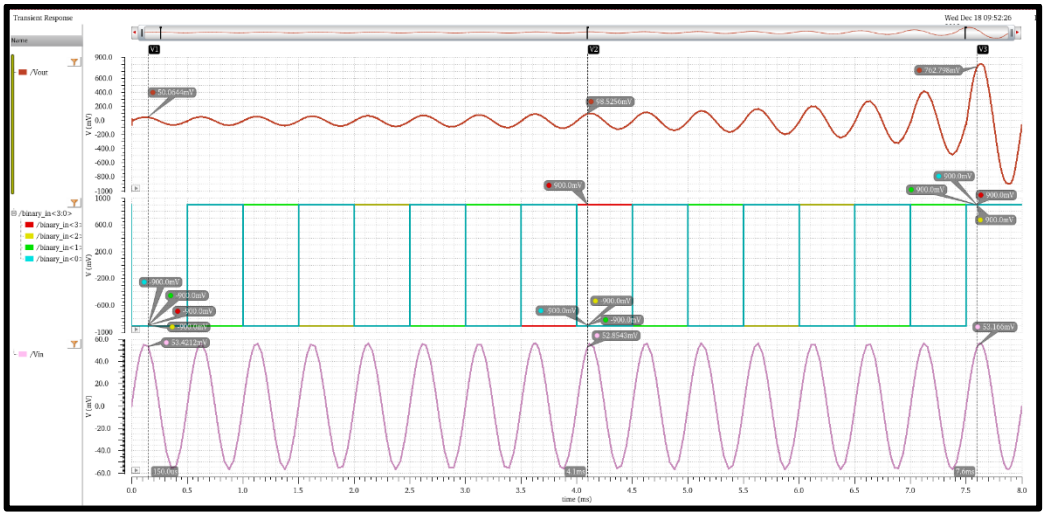

Figure 32: Programmable Noninverting Amplifier Testbench Results

Mathematically, the output of the programmable noninverting amplifier should follow the equation shown below, wherein C is the decimal value of the C_n binary input lines.

$$G = \frac{C}{16 - C} + 1$$

To verify the functionality of the circuit, the output was probed at various points and compared with the expected output, obtained from the previously mentioned equation.

4-Bit Select	Predicted	Simulated
0000	$56.25mV$	$50.0644mV$
1000	$84.375mV$	$98.526mV$
1111	$900mV$	$762.796mV$

Table 4: Programmable Noninverting Amplifier Actual vs. Ideal Outputs

As can be seen from these results, the schematic output closely correlates to the expected outputs. The greatest error exists when C is 15 (1111). This is primarily the result of the op-amp not being capable of rail-to-rail outputs.

$(A_0, A_1) = (0,1)$: Programmable Inverting Amplifier

To create a programmable inverting amplifier, an op-amp and resistor array were connected such that one end of the resistor array was connected to V_{In}, one end of the resistor array was connected to the amplifier's output, and the resistor array's wiper was connected to the op-amp's negative input terminal. A simplified view of this setup can be seen below.

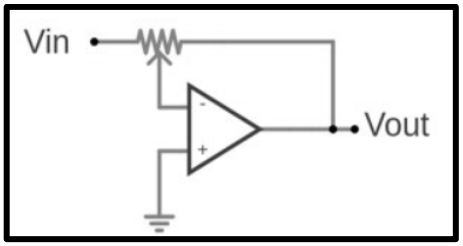

Figure 33: Programmable Inverting Amplifier Configuration

Where, once again, the wiper location can be adjusted through the C_n lines. The schematic used in the final circuit can be seen in the figure below.

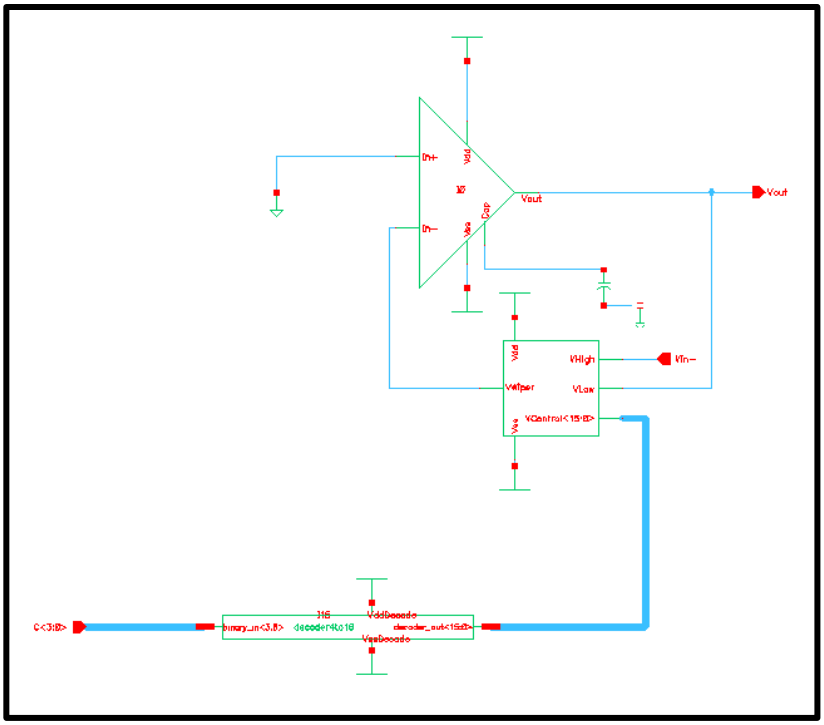

Figure 34: Programmable Inverting Amplifier Schematic

To test this circuit, the following testbench circuit was created. As with the noninverting amplifier, V_{DD} was set to $0.9V$, global V_{SS} was set to -0.9V, and each of the input C_n lines were set to be a square wave which went from $-0.9V$ to $0.9V$. The amplifier's input was connected to a sinusoidal source with an amplitude of $56.25mV$ and a frequency of $2kHz$.

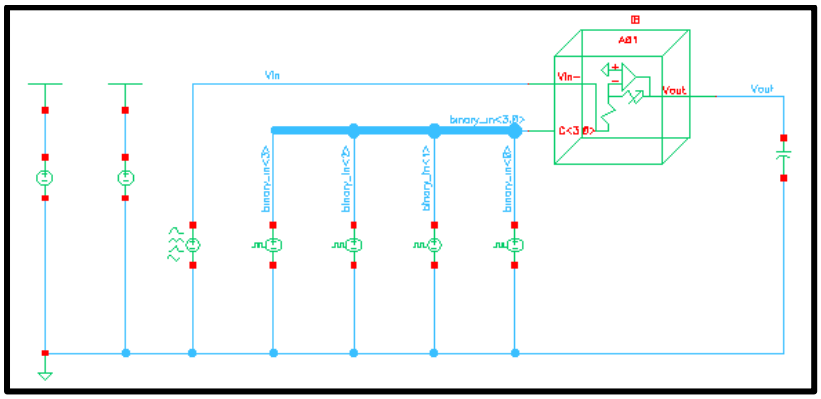

Figure 35: Programmable Inverting Amplifier Testbench Circuit

A transient analysis was run for $8ms$, allowing the below waveforms to be obtained.

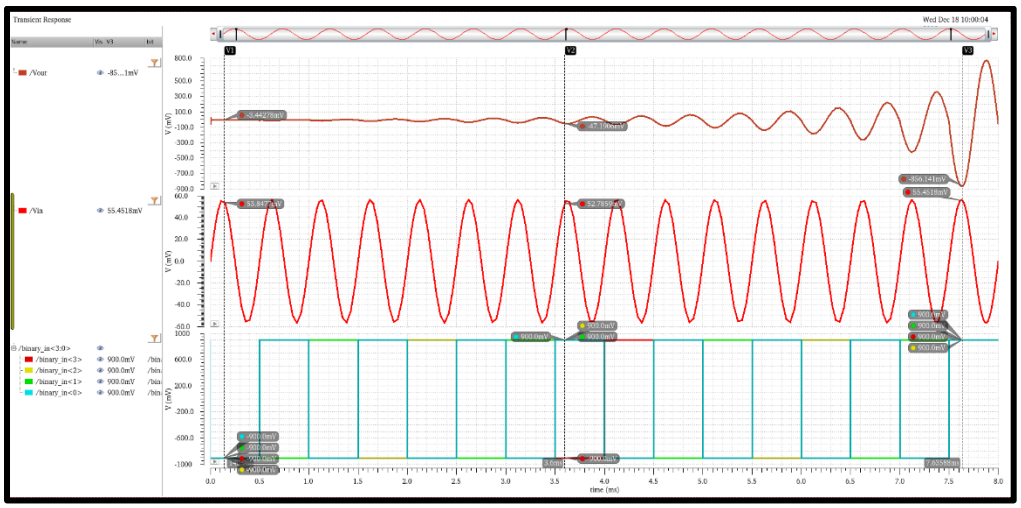

Figure 36: Programmable Inverting Amplifier Testbench Results

An analysis of the circuit schematic shows that the output of the programmable inverting amplifier should follow the equation shown below.

$$G = -\frac{C}{16 - C}$$

To verify the functionality of the circuit, the output was probed at various points and compared with the expected output, obtained from the previously mentioned equation.

4-Bit Select	Predicted	Simulated
0000	$0mV$	$-3.44278mV$
0111	$-43.75mV$	-47.1906
1111	$-843.75mV$	$-856.141mV$

Table 5: Programmable Inverting Amplifier Actual vs. Ideal Outputs

Once again, the schematic output closely correlates to the expected outputs. Although error still exists, the error is noticeably less than the error seen in the programmable noninverting amplifier. This is because the op-amp's negative rail is closer to V_{SS} than the positive rail is to V_{DD}.

$(A_0, A_1) = (1,0)$: 4-Bit DAC

To implement the 4-bit DAC sub-circuit, a resistor array, op-amp, and decoder were once again used. The low side of the resistor array, V_{REF}, was grounded and the other end of the resistor array was given to the user. The resistor array's control lines were connected to the output of the 4-to-16 decoder, which accepts the circuit's C_n lines as an input. The resistor array's wiper was connected to the positive input node of the op-amp, which was set up in a unity-gain configuration. This can be seen in the figure below.

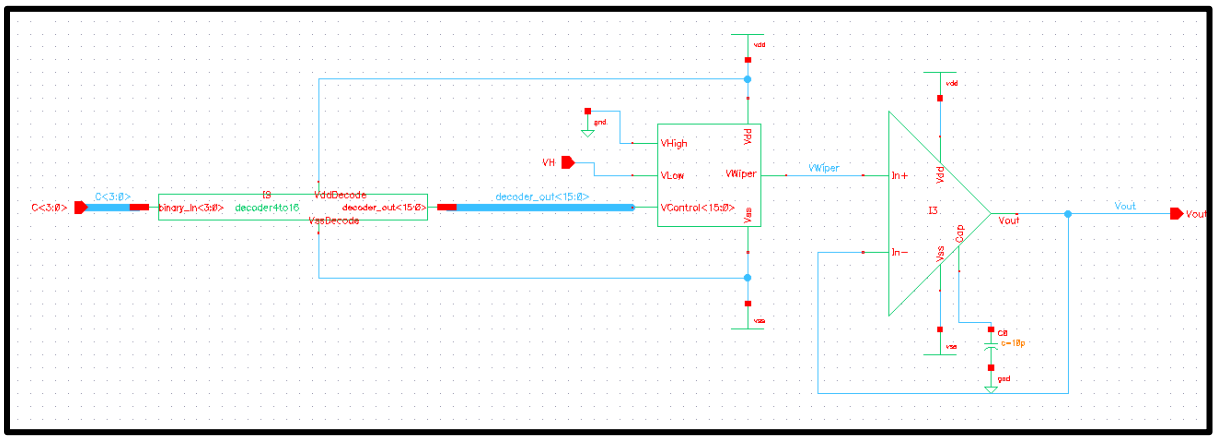

Figure 37: A10 Schematic, 4-bit DAC

This configuration works because, as the user's 4-bit input changes, the voltage seen at the resistor's wiper changes as well. The op-amp sees this change at its In_+ port and, because of its unity-gain configuration, replicates the voltage level at its output. The output of the 4-bit DAC can be modeled using the equation below, wherein C is the decimal value of the binary C_n input lines.

$$V_{out} = \frac{C}{16} V_{in}$$

Due to the use of the op-amp as a unity-gain buffer, this equation is only valid while V_{out} is between $\pm 0.9V$, which are the op-amp's voltage limits. If the equation predicts a value whose magnitude is greater or less than $0.9V$, then the actual output will be the amplifier's positive or negative rail.

To test this sub-circuit, the testbench circuit seen below was created. In this circuit, global V_{DD} and global V_{SS} are set to $\pm 0.9V$, respectively, and the DAC's input voltage is set to be a square wave with an amplitude of $100mV$ and a period of $16ms$. The DAC's control inputs are also connected to square wave sources with amplitudes of $0.9V$ and periods of $1ms$, $2ms$, $4ms$, and $8ms$. This combination of input periods means that this testbench will fully test the DAC for both positive and negative voltages.

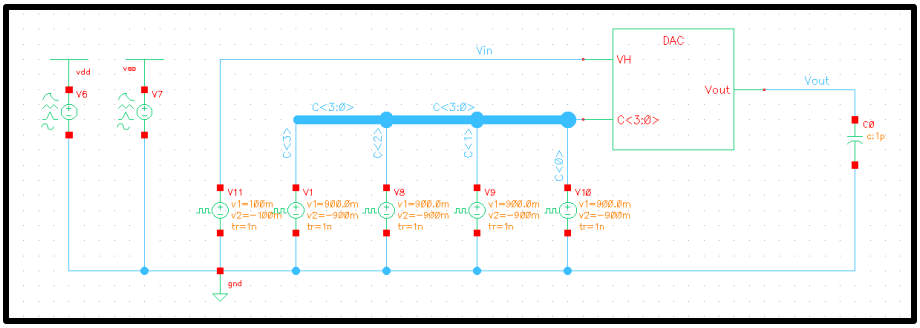

Figure 38: Testbench for A10, the DAC

The results of running a transient analysis can be seen below. Of primary importance in these results is that, while the input voltage is negative, the output waveform, V_{out} (pink), starts at nearly $0V$ and decreases by steps of $\frac{1}{16}$ until reaching approximately fifteen-sixteenths of the input voltage. When the input voltage is positive, V_{out} starts at nearly $0V$ and increases by steps of $\frac{1}{16}$ until again reaching approximately fifteen-sixteenths of the input voltage. This "stepping" behavior is exactly what is expected from the 4-bit DAC.

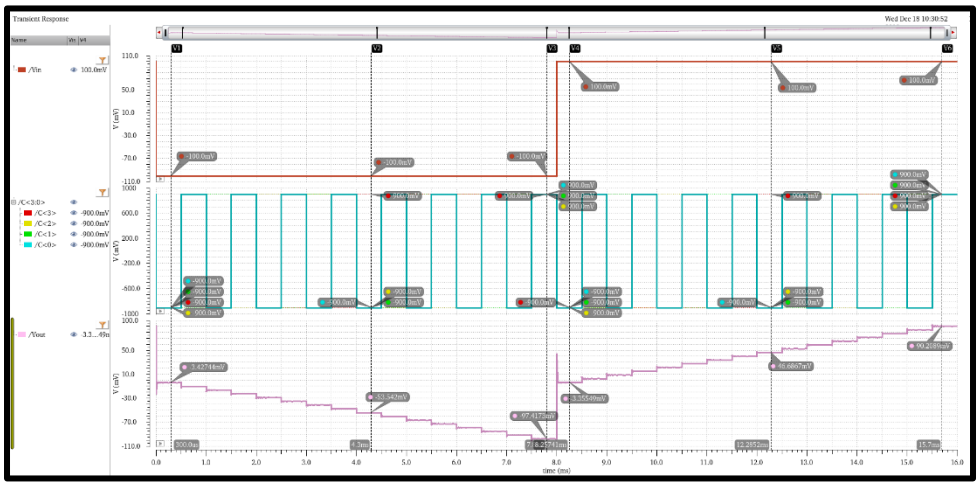

Figure 39: Results from testing the DAC

The output of the DAC was probed at several locations. These measured values, along with the output values predicted by the equation provided previously, can be seen in the table below.

4-Bit Select	Predicted	Simulated
0000	$0mV$	$-3.42744mV$
1000	$-50mV$	$-53.542mV$
1111	$-93.75mV$	$-97.4173mV$
0000	$0mV$	$-3.35549mV$
1000	$50mV$	$46.6867mV$
1111	$93.75mV$	$90.2089mV$

Table 6: 4-Bit DAC Measured vs. Predicted Values

Overall, the predicted and measured values closely align, with there being a constant difference of about $3.5mV$ between the predicted and measured values. This difference is the result of the amplifier's DC offset voltage, which was previously identified to be approximately $3.5mV$, and is considered to be acceptable under most operating cases. However, the user should be aware that this means that the DAC should not be used for small input voltages; instead, a precision DAC should be used.

$(A_0, A_1) = (1,1)$: Potentiometer and Operational Amplifier

To implement the fourth sub-circuit, an independent potentiometer and operational amplifier, a resistor array, op-amp, and decoder were once again used. The amplifier was set up such that the user had access to all of the amplifier's pins, including the external capacitor pin, but not its V_{DD} and V_{SS} pins. These pins were connected to the circuit's global V_{DD} and V_{SS}, where are required to be $\pm 0.9V$. For the potentiometer portion of this sub-circuit, the user was given access to the resistor array's V_H, V_L, and V_{Wiper} pins, thus allowing them to connect the resistor array in any configuration that they desired. The user was also given access to the decoder's 4-bit input, thus allowing them to directly control the resistor array's resistance ratio, and to the decoder's specific V_{DD} and V_{SS} pins. Because the user has access to the decoder's V_{DD} and V_{SS} pins, the user can use the potentiometer with voltages exceeding $\pm 0.9V$, so long as they ensure that their control inputs use V_{DD} and V_{SS} as their logic-high and logic-low values. Further, the user should ensure that their voltages will not burn the MOS devices. Signals up to $5V$ were tested in Cadence, but this does not mean that it possible for the user to input $5V$ signals. The limitations of what the user can input should be determined from the physical limitations of the MOS devices.

The output of the potentiometer can be expressed as a simple voltage divider equation, wherein C is the decimal value of the binary inputs:

$$(\mathrm{V_H} - \mathrm{V_L}) * \frac{16 - \mathrm{C}}{16} - V_L$$

The final schematic for this sub-circuit can be seen below. Notice that the operational amplifier and digital potentiometer circuits are independent of each other.

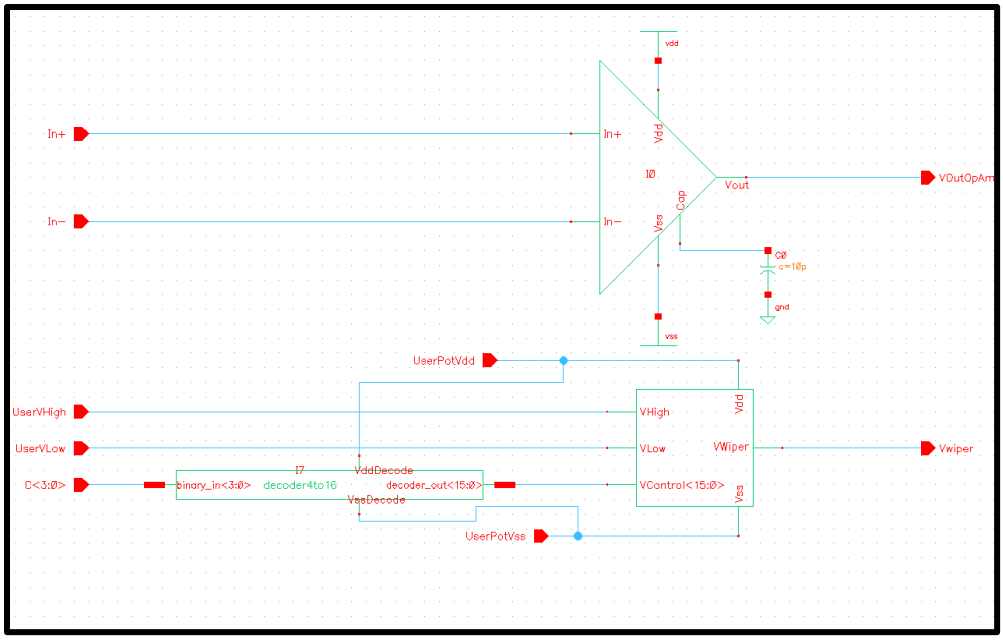

Figure 40: Schematic for A11, Digital Potentiometer and Operational Amplifier

To ensure the validity of this setup, a testbench circuit was created. This testbench places the op-amp in a non-inverting configuration with a gain of three and places the potentiometer in a setup where it has $5V$ across it. The potentiometer's control lines are set up to increment through all possible wiper voltages, and the op-amp's input is a sinusoidal signal with a frequency of $2kHz$ and an amplitude of $56.25mV$. To avoid clipping, the user-defined V_{DD} and V_{SS} for the decoder are set to $\pm 5V$.

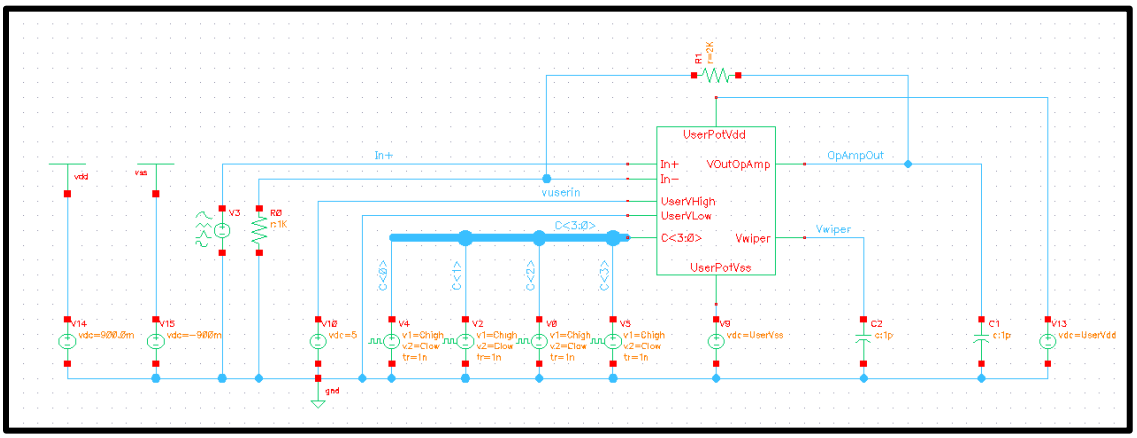

Figure 41: Testbench for A11

A transient analysis was run on this circuit for $8ms$. The output of this analysis can be seen in the figure below.

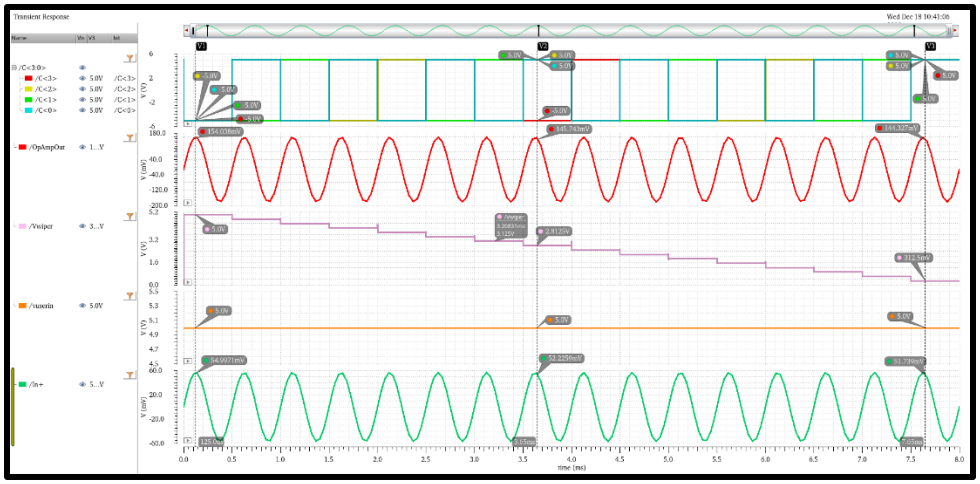

Figure 42: Results of testbench for A11. From top to bottom: 4-bit input C, Op Amp output, Potentiometer Output, User VH, User Vin for Op Amp positive pin

The waveform was probed at a variety of locations. The results of these probes can be seen in the table below, along with expected values.

4-Bit Control	Predicted Potentiometer Output	Simulated Potentiometer Output	Predicted Op-Amp Gain	Simulated Op-Amp Gain
0000	$5V$	$5V$	3	2.8
0111	$2.8125V$	$2.8125V$	3	2.79
1111	$0.3125V$	$0.3125V$	3	2.78

Table 7: Measured vs. Predicted Testbench Values

As can be seen from this table, the potentiometer output perfectly matches the equation provided previously, indicating that it is working as expected. The op-amp's gain closely matches with the expected gain, although it is off slightly and appears to fluctuate a small amount. However, the magnitude of the fluctuation appears to be minimal, and the gain offset is likely the result of the op-amp's DC offset.

Final Result

To test the overall circuit schematic, which was presented in the "Design Breakdown" section of this document, the following testbench circuit was created. In this testbench, the A_0 and A_1 lines are set up to increment through all four of the circuit's modes. For each mode, the C_n lines are run through all possible input combinations, thus meaning that each mode of the circuit is tested with all valid user inputs. The input voltages used by Mode 1 and Mode 2 are connected to a DC source outputting a constant value $56.25mV$, and the input voltage used by Mode 3 is set to a DC source outputting a constant $0.9V$. The op-amp in Mode 4 is set up to act as a comparator which C_1 as an input, and the potentiometer is set up to have a voltage of $0.9V$ across it.

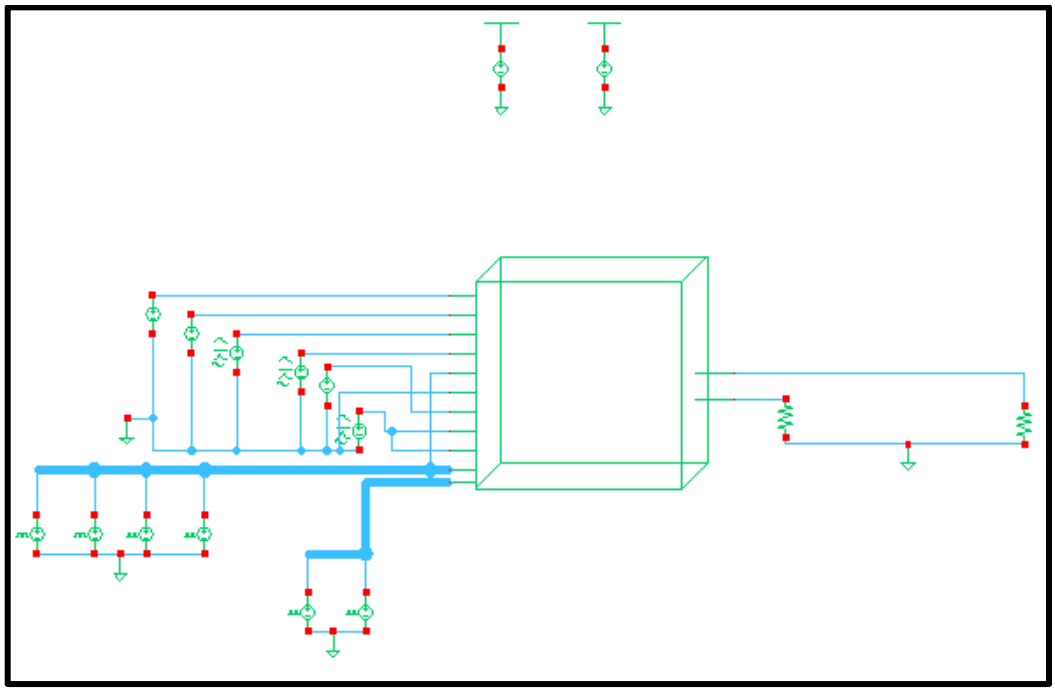

Figure 43: Final Circuit Testbench (The pin names for the symbol are not present in the image due to the software being too zoomed out to capture them)

A transient analysis of this circuit was run for $65ms$. Because most sub-circuits were tested and verified before being integrated into the final circuit, it is not necessary to perform measurements on the output of each mode. Not only would this yield redundant information, but it would also be a very cluttered and inefficient way of testing the circuit. Instead, to confirm that the overall circuit is functional, it is sufficient to look at the waveform and check if the output appears to go through four modes and that each mode appears to behave as expected. The output of this testbench can be seen below.

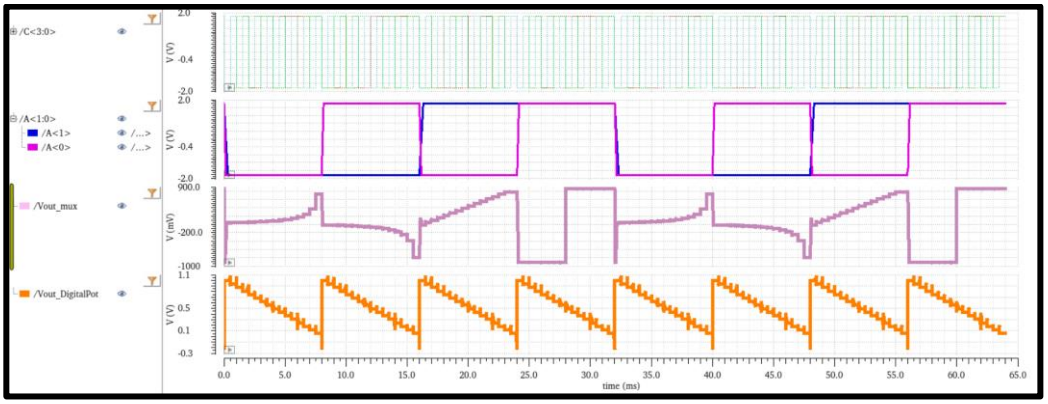

Figure 44: Overall Circuit Testbench Results

By looking at the multiplexer output (purple), it can be seen that the circuit appears to go through four unique modes, each lasting $8ms$. In the first $8ms$ period, the multiplexer output appears to increase from $0V$ to a value which is very close to, but not exactly, $0.9V$. This increase occurs at a nonlinear rate. This matches the expected output of the circuit's first mode. In the second $8ms$ period, this again occurs, however, the output of the multiplexer appears to be negative. This matches the expected

behavior of the circuit's second mode. In the third $8ms$ period, the multiplexer's output appears to increase linearly from $0V$ to $0.9V$ in 15 steps, which matches with the expected behavior of the 4-bit DAC (Mode 3). In the fourth $8ms$ period, the multiplexer output appears to be a square wave which has a duty cycle of 50% and a period of $8ms$. Considering that the op-amp in Mode 4 is set up to operate as a comparator that uses C_1 as input, this output appears correct. Though all modes, the $V_{out-DigitalPot}$ waveform appears to linearly go from $0.9V$ to $0V$ every $8ms$. This matches the expected output of the potentiometer from Mode 4, which is always active and always outputting. Because the output waveform appears to have four distinct output sections, each one matching the expected behavior of each mode, it can be concluded that the overall circuit design functions as intended.

Areas for Improvement

As with all projects, the first revision is never perfect and always has room for improvement. One major way that this circuit could be improved would be to add an enable line to each sub-circuit which is connected to the A_0 and A_1 lines. Adding an enable line would allow for sub-circuits to be deactivated when not in use, making the overall circuit far more energy-efficient. As it is currently designed, all sub-circuits are always active, meaning that the overall circuit draws a significant amount of power. This makes the circuit impractical for actual use.

Because little emphasis is placed on op-amp design in EE 330, no thought was given as to how the op-amp's size could be minimized. As a result of this, the MOS transistors used in the op-amp are very large (one, for example, is $500\mu m$ in width). While technically valid, this design would never be accepted in industry. Thus, another major way that this circuit could be improved would be by re-designing the operational amplifier to account not only for performance but also for size. However, this may not be possible to due until EE 435, in which op-amp design will be discussed.