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EE 330 Final Design Project

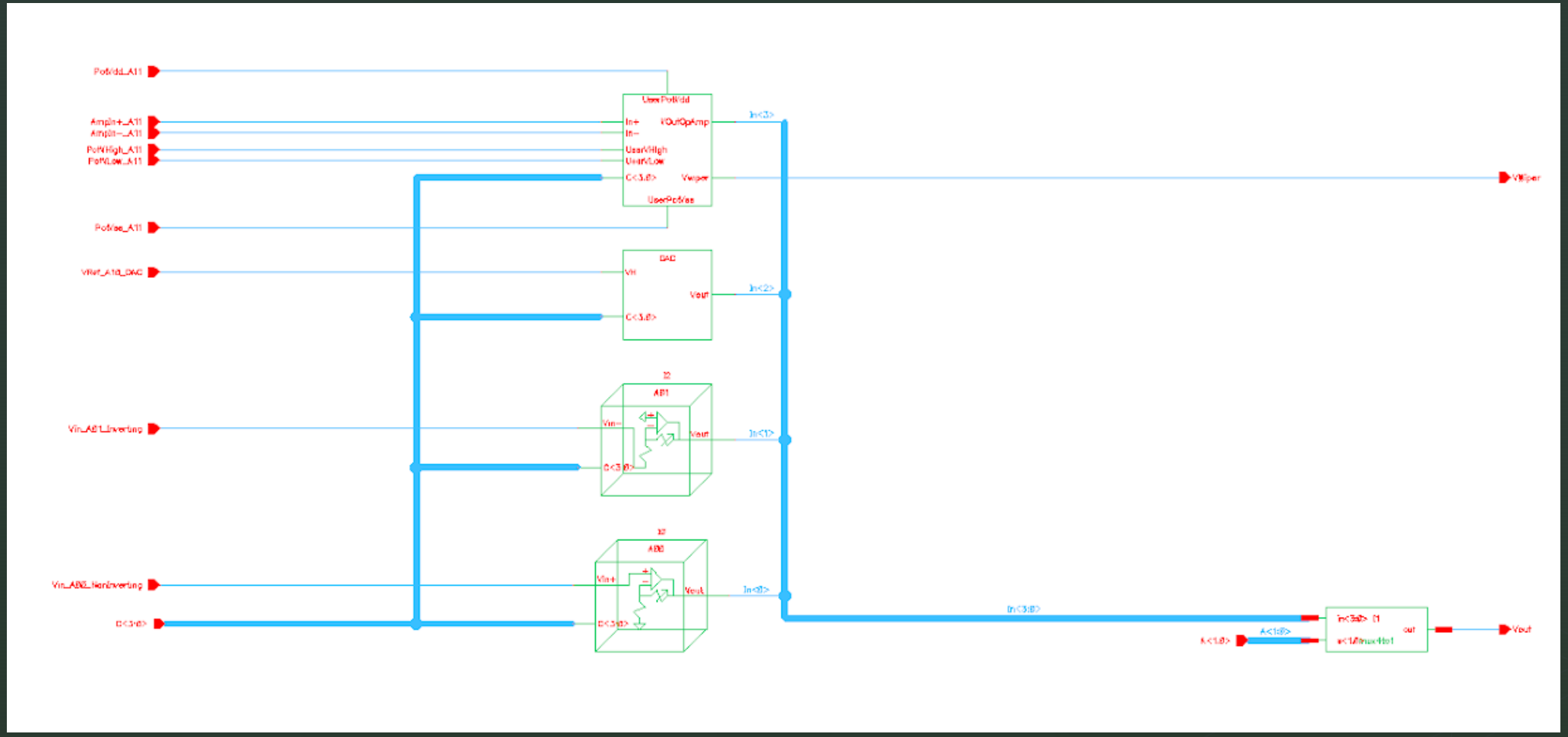
Summary

- Design an integrated circuit with four modes. The state of the circuit is controlled through two digital inputs, A_0 and A_1:
  - $(A_0, A_1) = (0,0)$: Circuit behaves as a programmable noninverting amplifier
  - $(A_0, A_1) = (0,1)$: Circuit behaves as a programmable inverting amplifier
  - $(A_0, A_1) = (1,0)$: Circuit behaves as a 4-bit DAC
  - $(A_0, A_1) = (1,1)$: Circuit is to behave independently as a digital potentiometer and an operational amplifier.

Summary (Cont.)

- To implement these modes, it was necessary to build four additional “building blocks,” which could be interconnected together:
  - 4-to-16 Decoder: For decoding the user’s 4-bit characteristic-control signal, C
  - Operational Amplifier: For amplifying an arbitrary input signal
  - Resistor Array: For creating a variable resistance ranging from $5k\Omega$ to $80k\Omega$, in increments of $5k\Omega$
  - 4-to-1 Multiplexer: For selecting the mode corresponding to the A_0 and A_1 inputs.

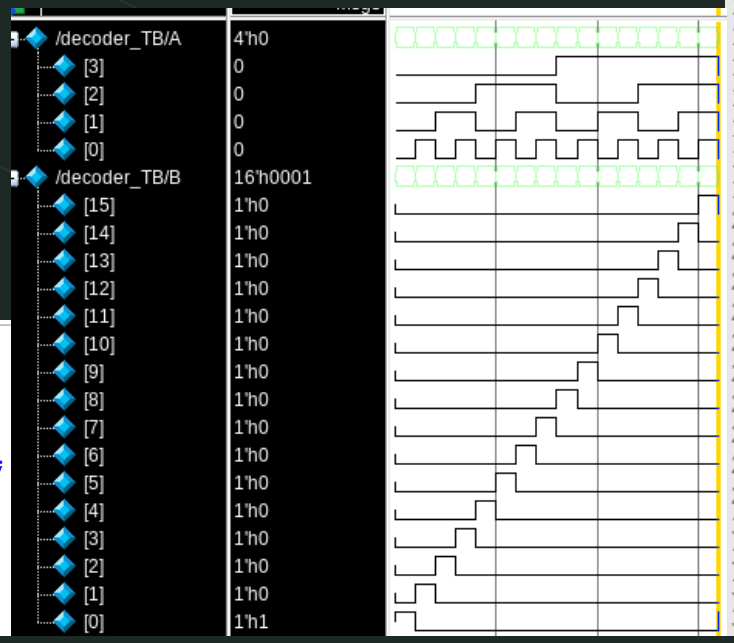
Master Schematic



4-to-16 Decoder

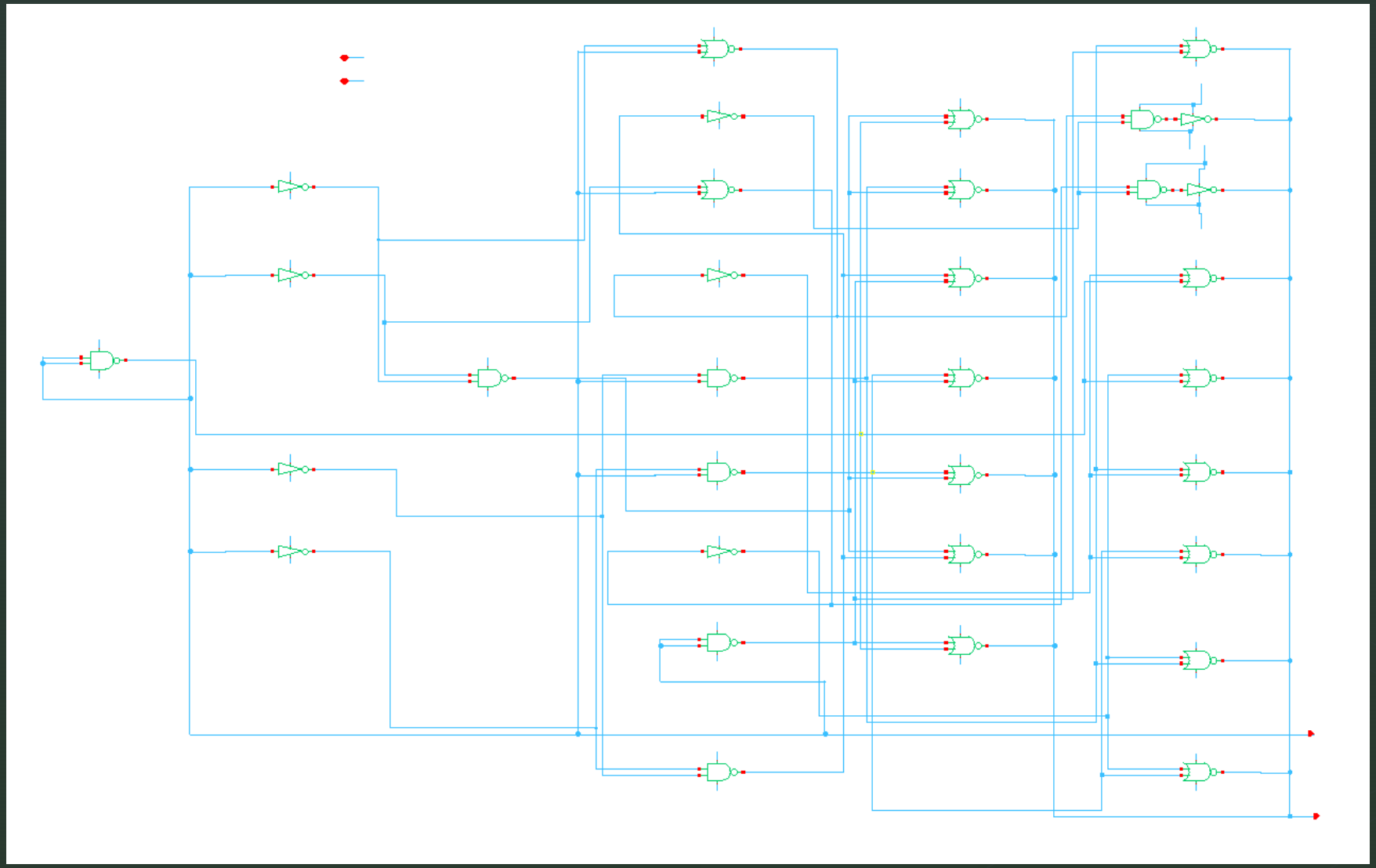
- Decoder and testbench were designed with Verilog in ModelSim
- To reduce routing efforts, all inputs and outputs were set to be registers, later interpreted as busses in Cadence.

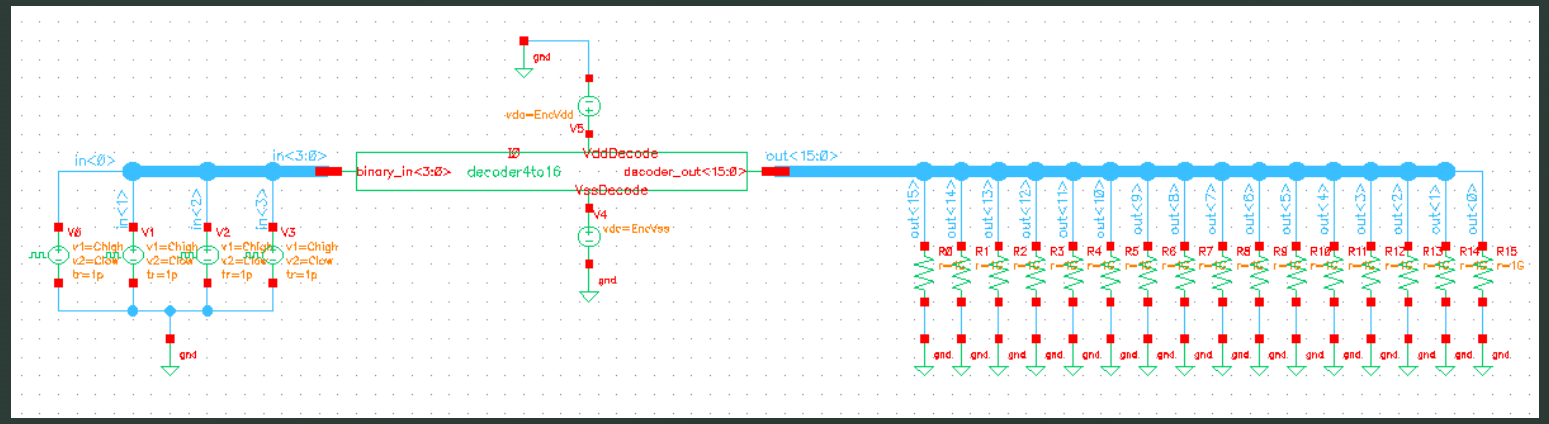
```verilog
module decoder4to16 (
binary_in   , //  4 bit binary input
decoder_out , //  16-bit  out
 );

 input [3:0] binary_in  ;
 output [15:0] decoder_out;
 reg [15:0] decoder_out ;

always @ (binary_in)
begin
  decoder_out = 0;
    case (binary_in)
      4'h0 : decoder_out = 16'h0001;
      4'h1 : decoder_out = 16'h0002;
      4'h2 : decoder_out = 16'h0004;
      4'h3 : decoder_out = 16'h0008;
      4'h4 : decoder_out = 16'h0010;
      4'h5 : decoder_out = 16'h0020;
      4'h6 : decoder_out = 16'h0040;
      4'h7 : decoder_out = 16'h0080;
      4'h8 : decoder_out = 16'h0100;
      4'h9 : decoder_out = 16'h0200;
      4'hA : decoder_out = 16'h0400;
      4'hB : decoder_out = 16'h0800;
      4'hC : decoder_out = 16'h1000;
      4'hD : decoder_out = 16'h2000;
      4'hE : decoder_out = 16'h4000;
      4'hF : decoder_out = 16'h8000;
     endcase
  end
  endmodule
```

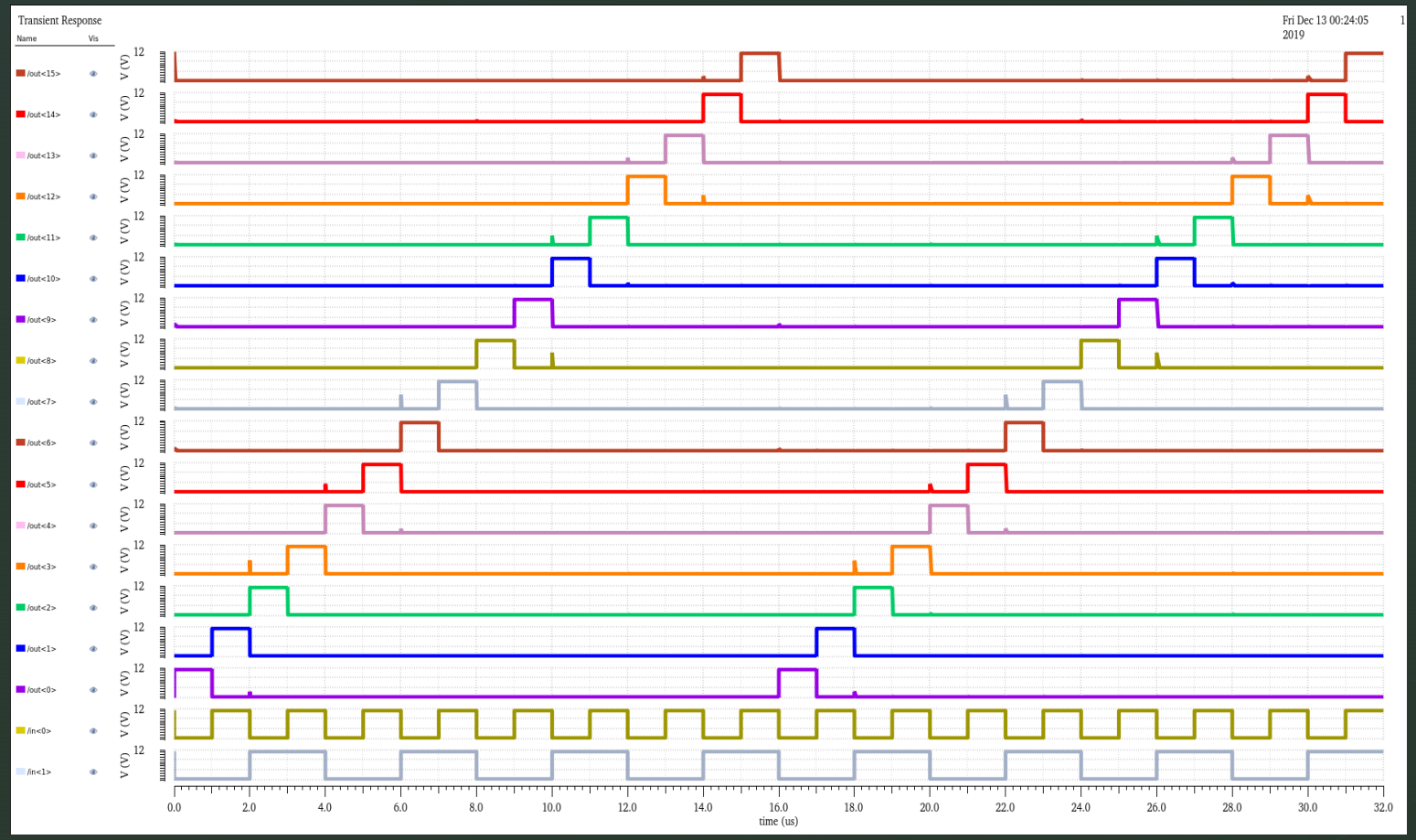



```verilog
module decoder_TB();
reg [3:0] A;
wire [15:0] B;

initial  A = 4'b0;

decoder4to16 test(.binary_in(A), .decoder_out(B));

always
begin
#10;
assign A = A+1;
end
endmodule
```

The Verilog design was synthesized using Genus. During synthesis, all gate V_{DD}'s and V_{SS}'s were set to global nets and all bulk connections were set to the source of each PMOS or NMOS. The gates were edited after synthesis to allow for V_{DD} and V_{SS} to be non-global and for the bulk connections to be connected to V_{DD} and V_{SS}.

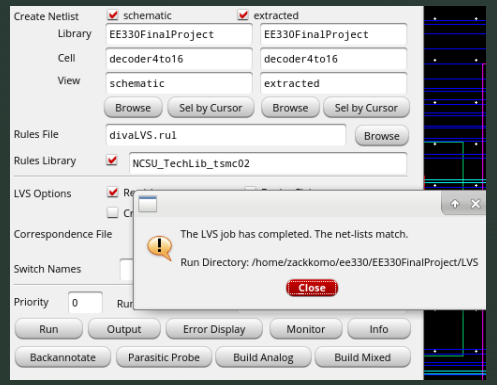




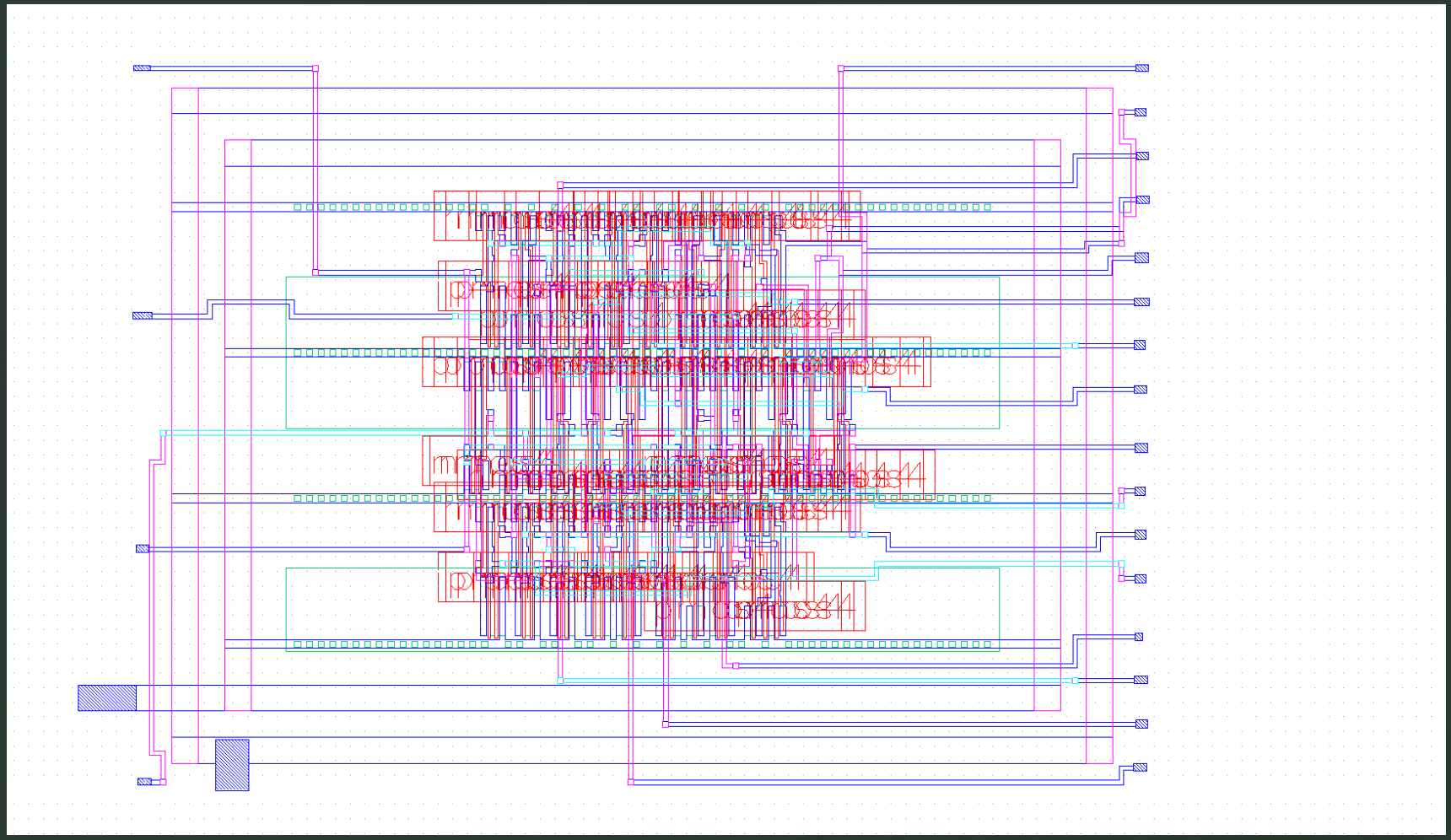


A testbench was created for the circuit in Cadence (left). The testbench results can be seen on the bottom left.

```
*********   Summary of rule violations for cell "decoder4to16 layout"   *********
   Total errors found: 0

DRC started at Fri Dec 13 00:42:02 2019

Validating hierarchy instantiation for:
library: EE330FinalProject
cell:    decoder4to16
view:    layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Fri Dec 13 00:42:02 2019
    completed ....Fri Dec 13 00:42:02 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "decoder4to16 layout"   *********
   Total errors found: 0
```



Using Innovus, a layout was generated. The layout passed both DRC and LVS checks, seen to the left.



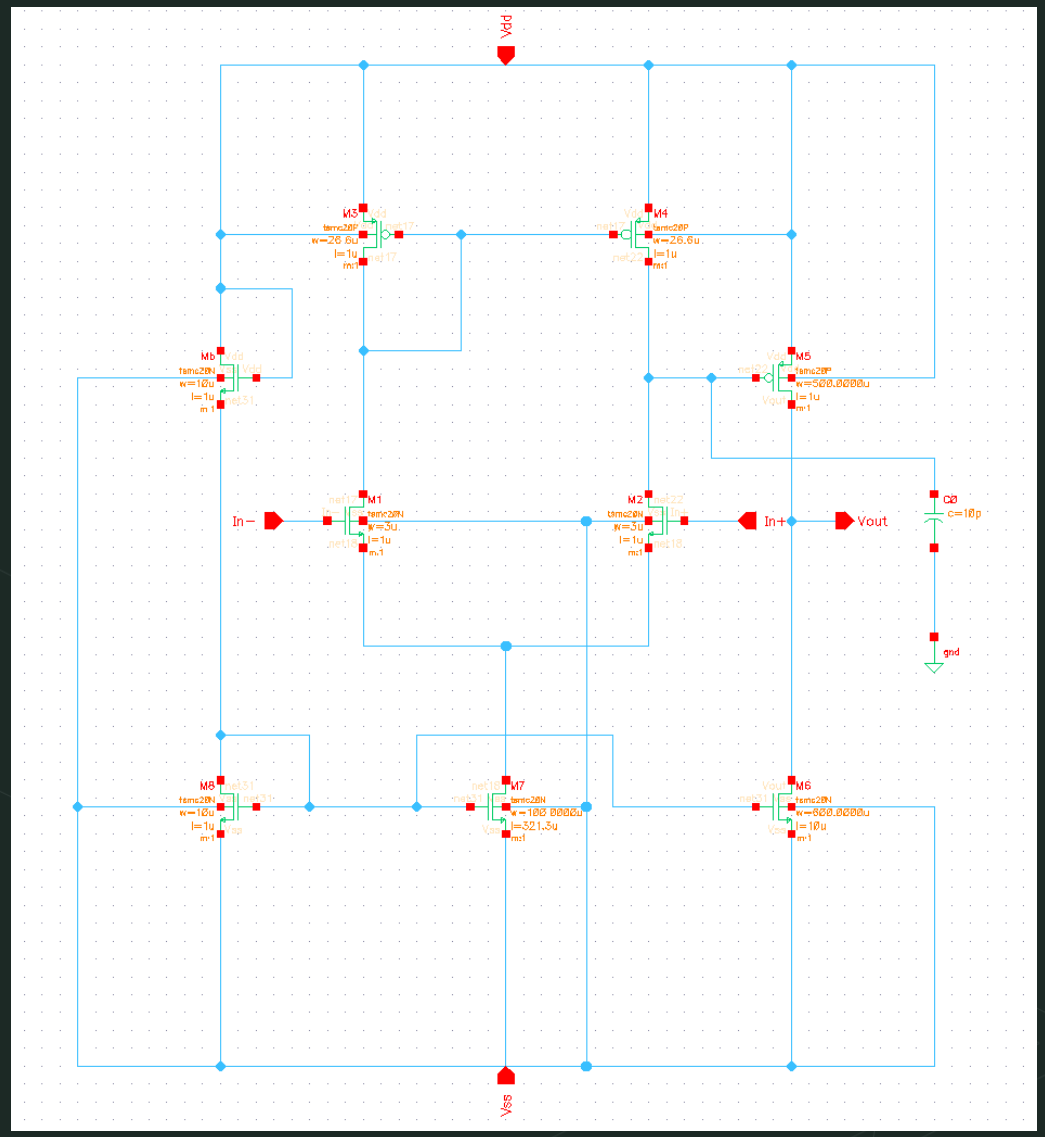
Operational Amplifier

Ideal Characteristics

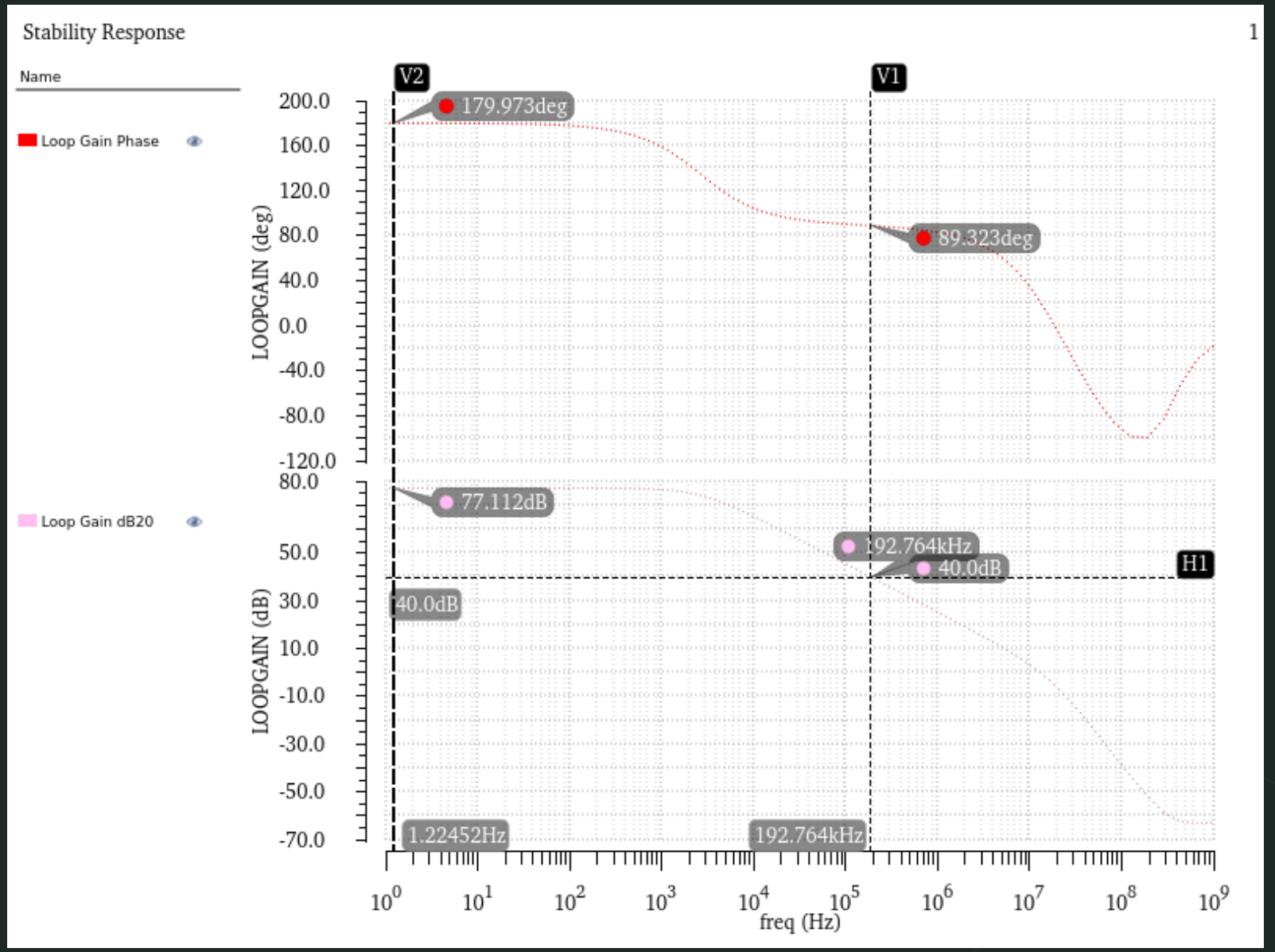
- $Slew\ Rate = \frac{1.1V}{\mu s}$
- $DC\ Offset = 0V$
- $V_{OutMax} = V_{DD}$
- $V_{OutMin} = V_{SS}$

Actual Characteristics

- $Slew\ Rate \approx \frac{3.26V}{\mu s}$
- $DC\ Offset = 3.5mV$
- $V_{OutMax} = 824.34mV$
- $V_{OutMin} = -833.952mV$



Bode Plot

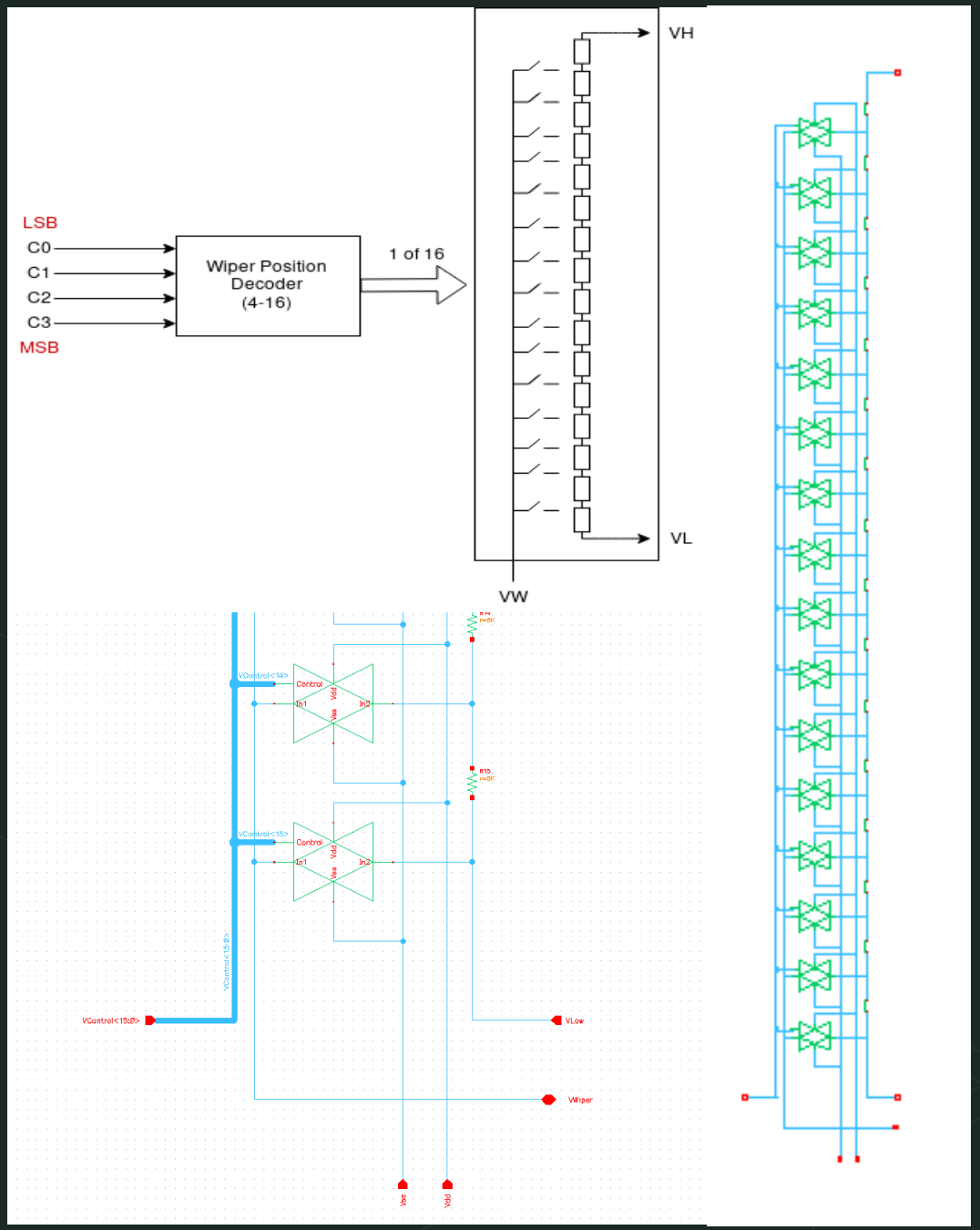

Stability Response
1
Name
Loop Gain Phase
Loop Gain dB20
V2
V1
H1
179.973deg
89.323deg
77.112dB
192.764kHz
40.0dB
40.0dB
1.22452Hz
192.764kHz
LOOPGAIN (deg)
200.0
160.0
120.0
80.0
40.0
0.0
-40.0
-80.0
-120.0
LOOPGAIN (dB)
80.0
50.0
30.0
10.0
-10.0
-30.0
-50.0
-70.0
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9
freq (Hz)

Resistor Array

The resistor array will operate like the image to the right. The decoder will drive the individual switches which will be one-hot encoded (only one on at a time). That way the wiper can “move” from top to bottom in steps of 5kΩ.

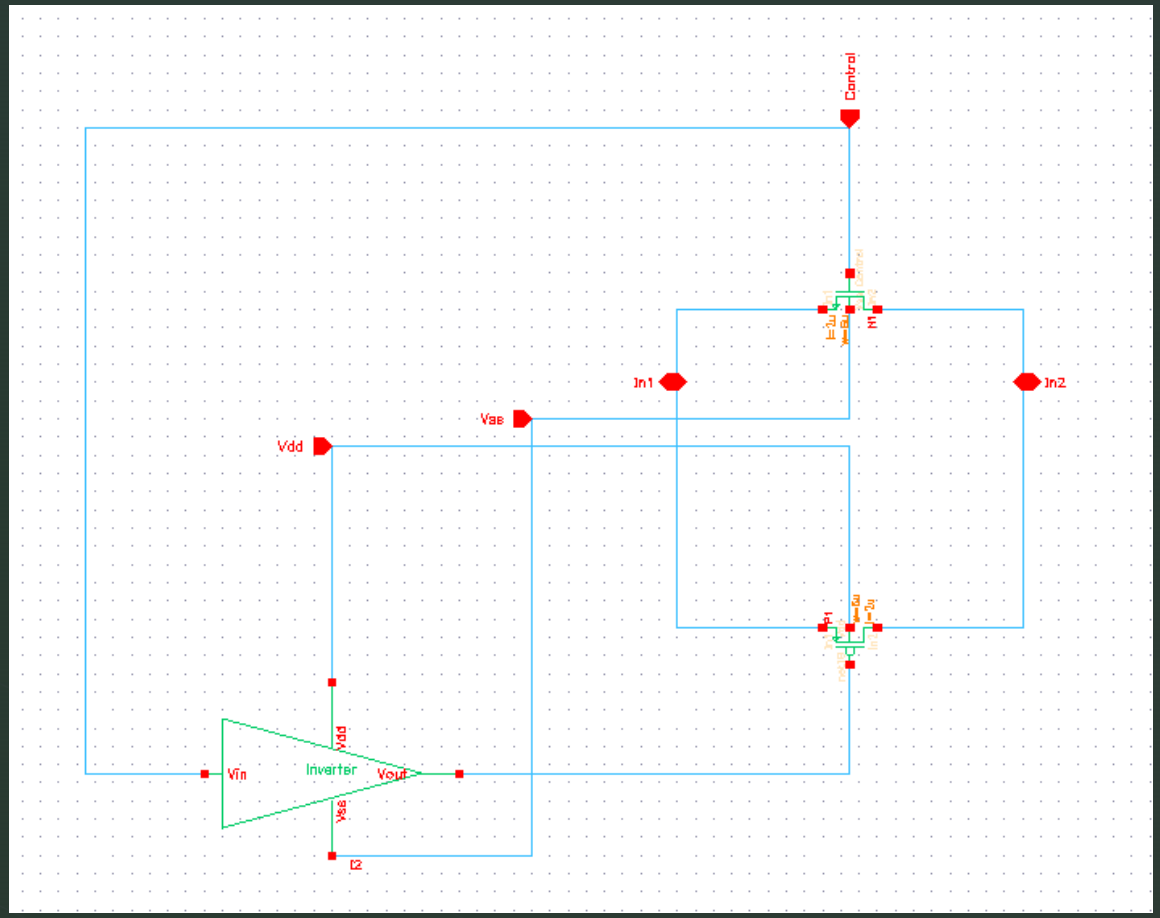
We made 15 such switches, each connecting between the 5kΩ segments, the control from the decoder and V_{DD}, V_{SS}, as well as the wiper pin.

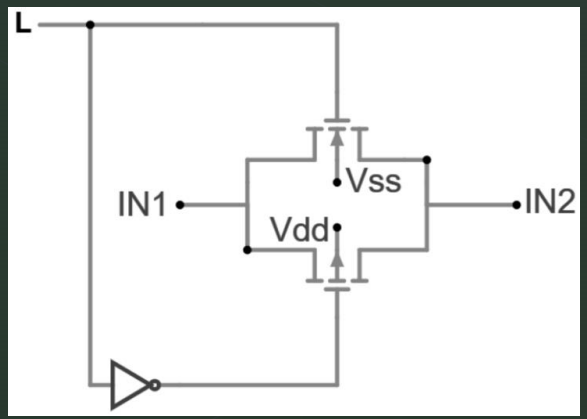
The main part of the array is the Transmission Gate



Transmission Gate

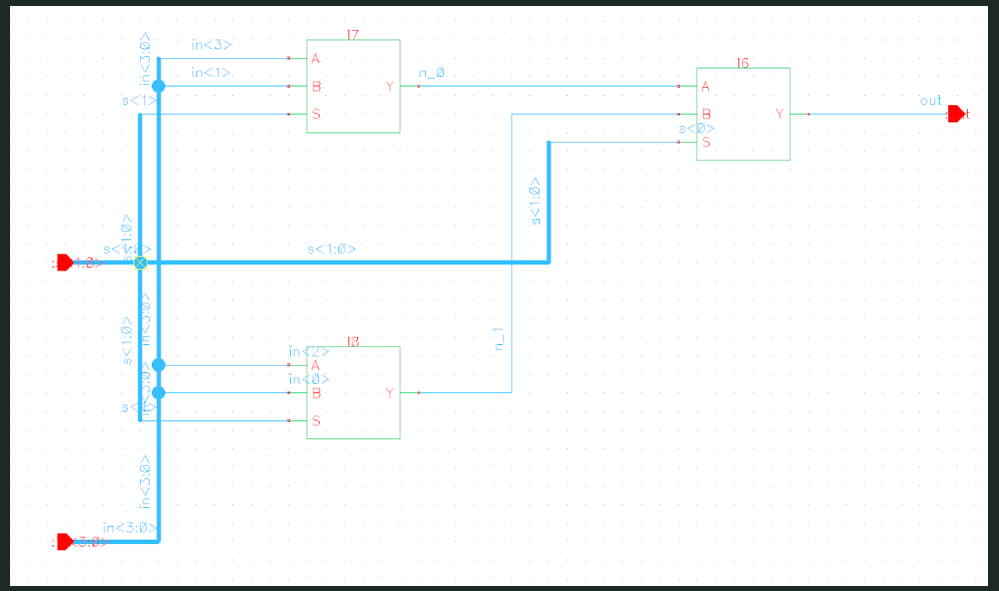
- Essentially this part is an NMOS and PMOS whose two drains are connected, and two sources are connected.
- Their bulks are connected to V_{SS} and V_{DD} respectively.
- The NMOS is driven directly from the control pin (from decoder) and the PMOS from an inverted control pin signal.
- Allows for AC signals (bidirectional)

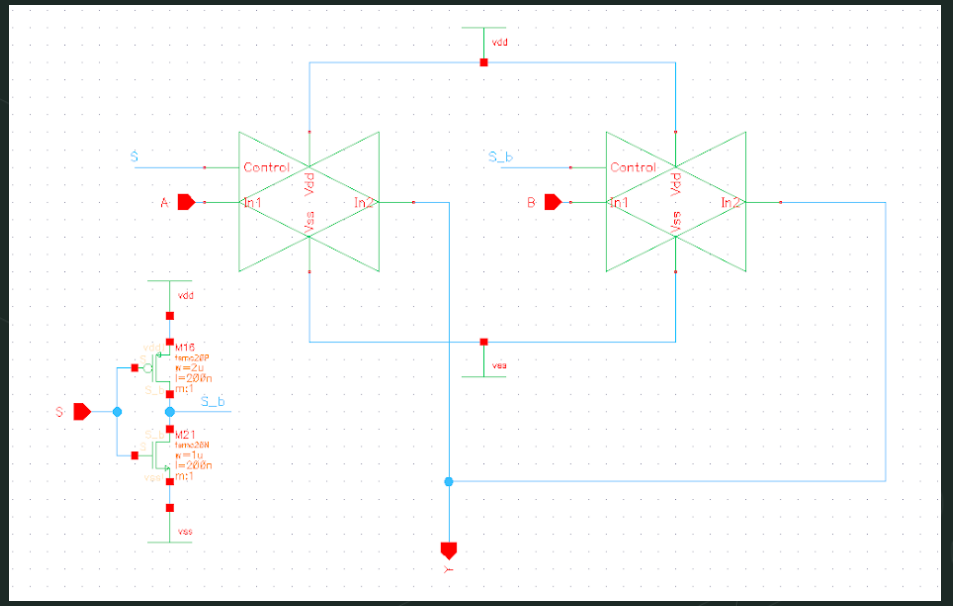




$4\ to\ 1\ MUX$

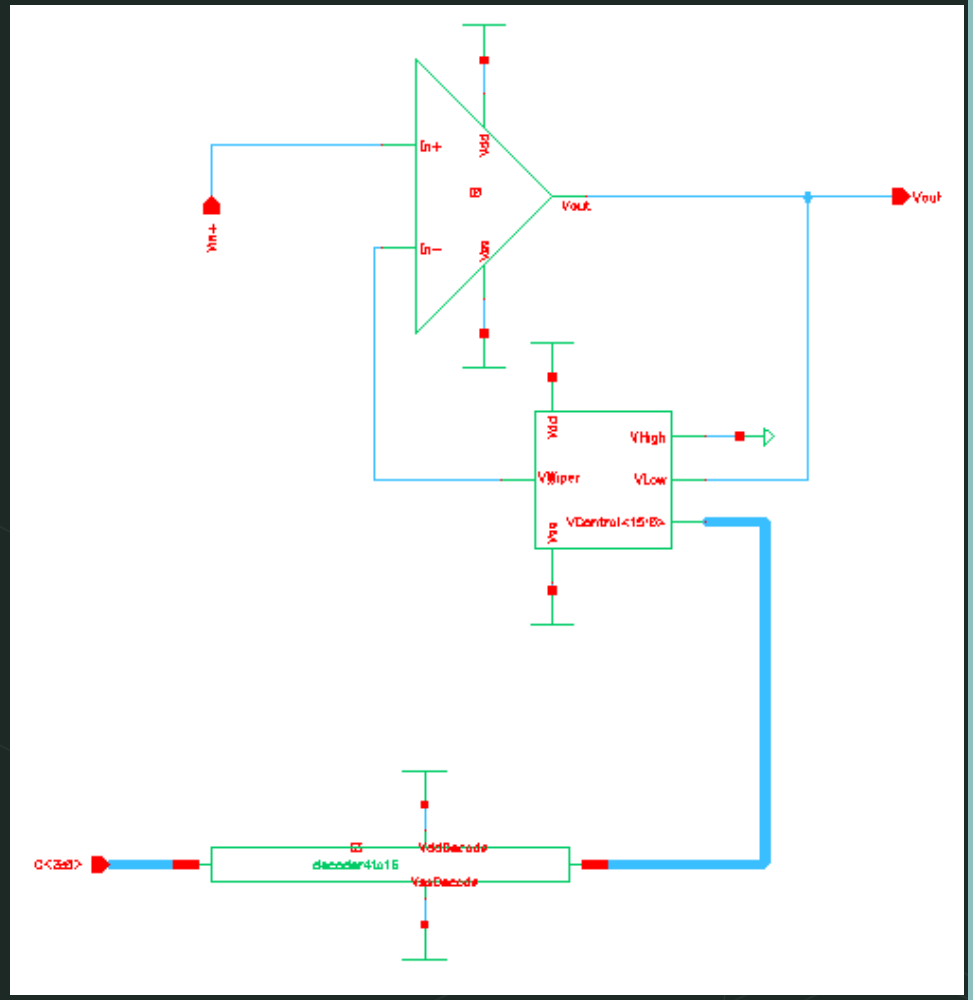
- Basic configuration of 3 2-1 MUXes where one selects between option 01 and 11, while the other between 00 and 10 and the third selects between the output of the previous two
- The 2-1 MUXes were made using the transmission gate mentioned earlier since they had to handle AC signals as well (analog MUXes)

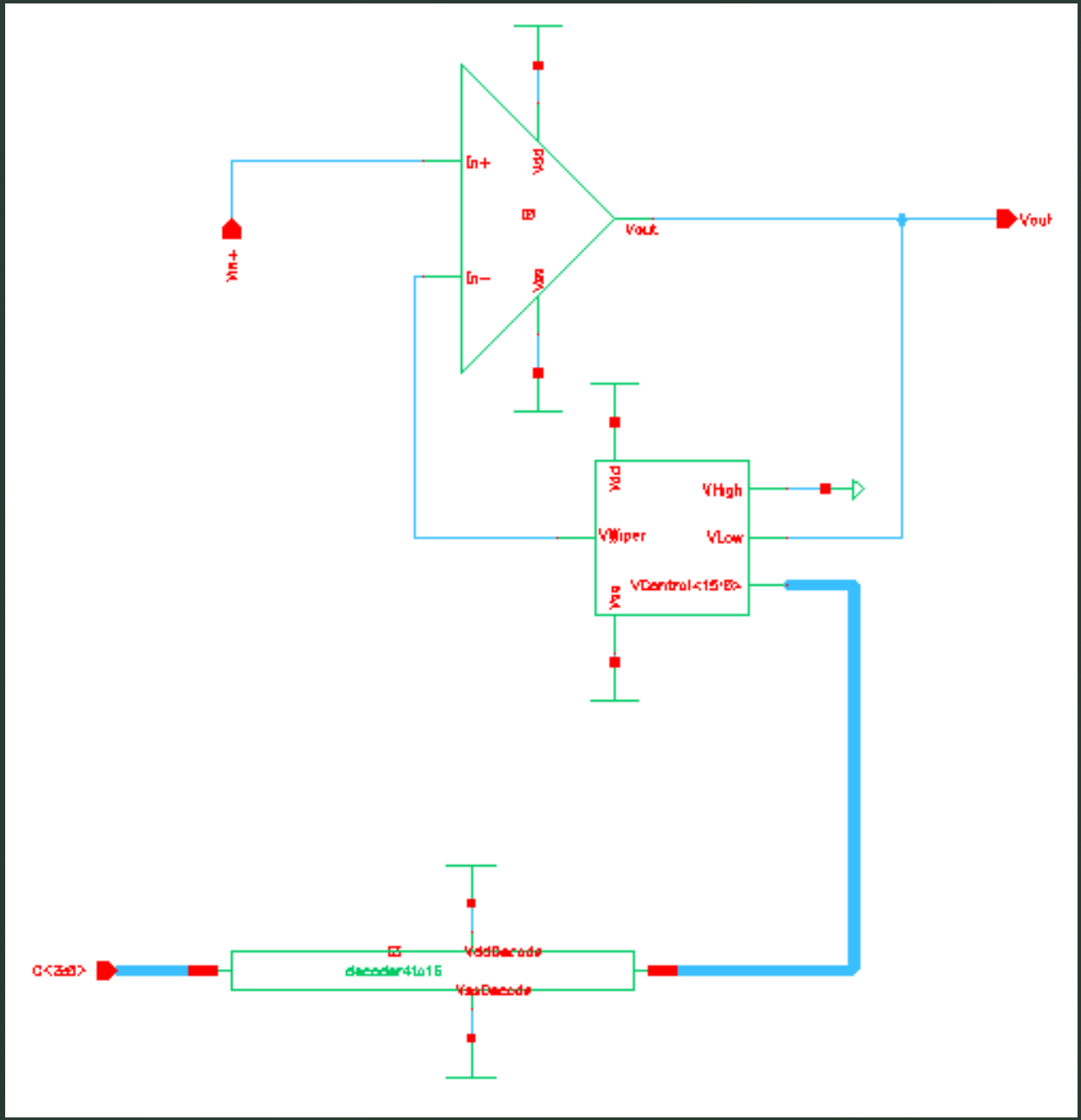




$(A_0, A_1) = (0,0)$: Programmable Noninverting Amp

- Uses a digital potentiometer to control a gain between 2 and 17, depending on a 4-bit input, C.
- Inputs:
  - V_{IN}: The signal to be amplified by the op-amp
  - $C = (C_3, C_2, C_1, C_0)$: 4-bit digital input for selecting gain.
- Outputs:
  - V_{Out}: The op-amp's output signal, given by the expression $V_{Out} = \left[1 + \frac{15-C}{1+C}\right] V_{IN}$
- Constraints:
  - C must be a logic high signal $(0.9V)$ or a logic low voltage $(-0.9V)$.
  - V_{Out} is constrained to values between $0.9V$ and $-0.9V$



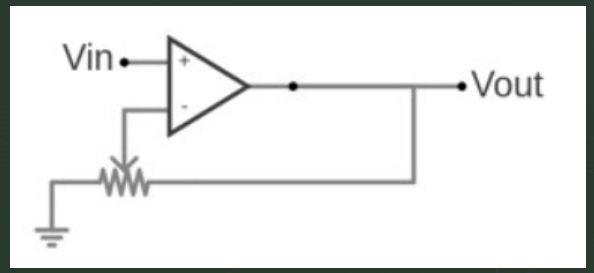


Components Used:

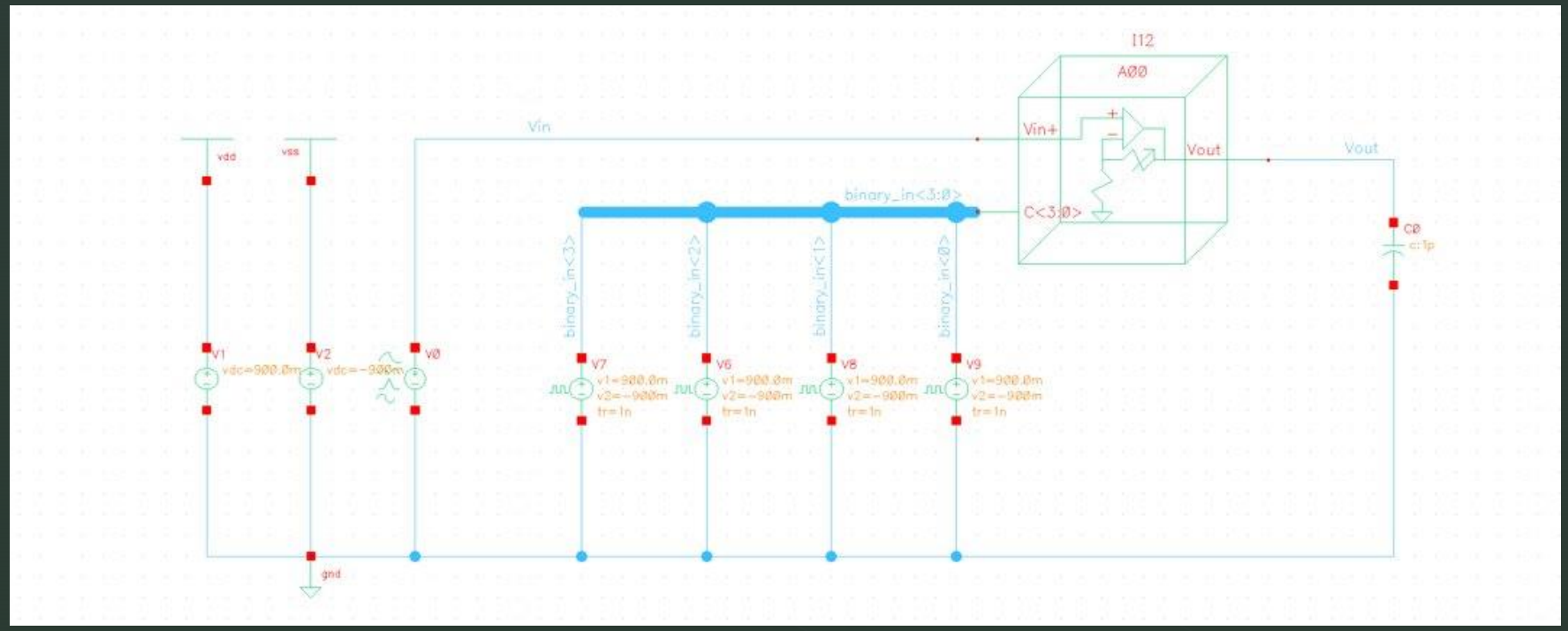
- 4-to-16 Decoder
- Operational Amplifier
- Resistor Array

Description:

The decoder programs the potentiometer to split the resistance accordingly GND and V_{Out}, thus forming a generic non-inverting op amp whose $\frac{R_2}{R_1}$ ratio is determined by the Digital Select C.

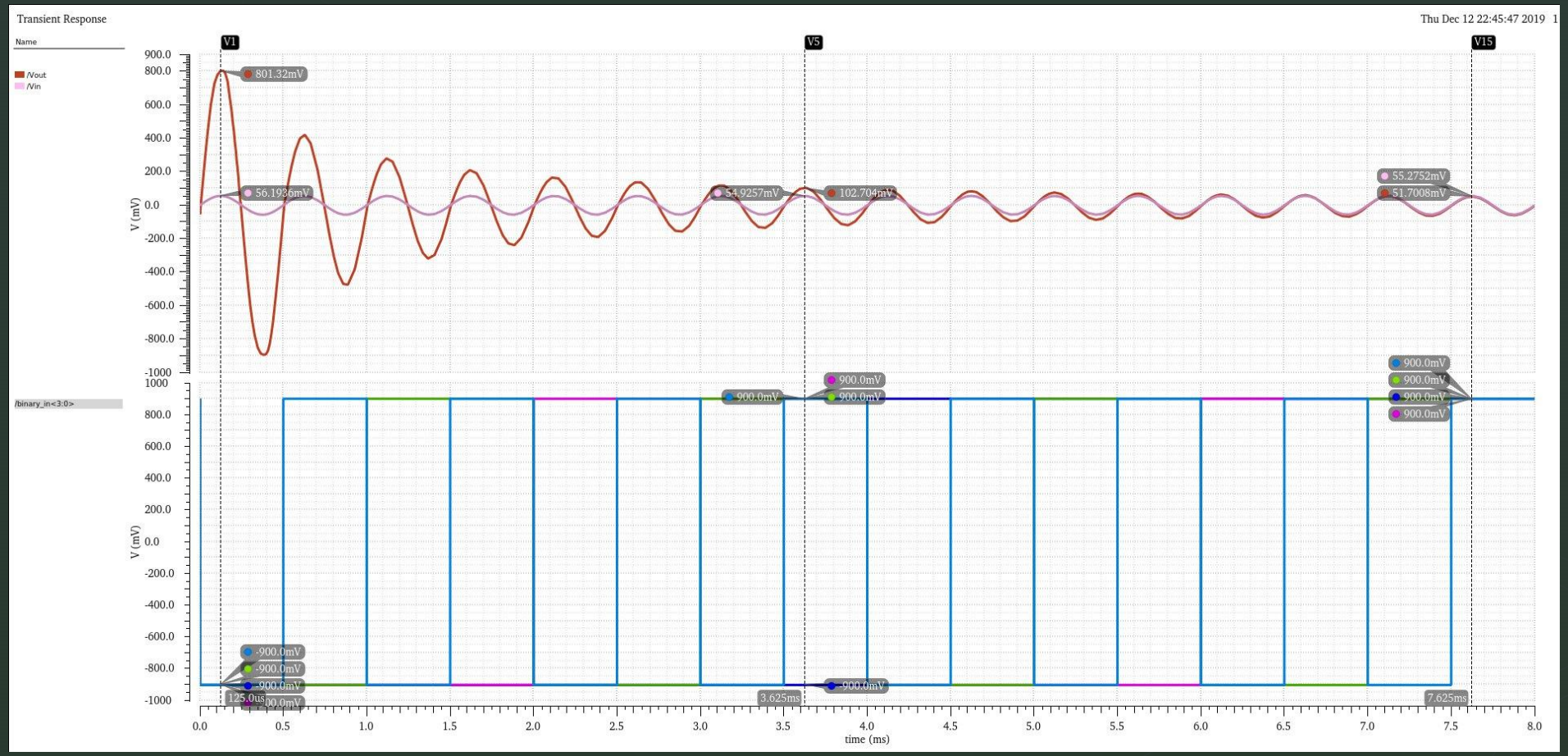


Testbench for A00



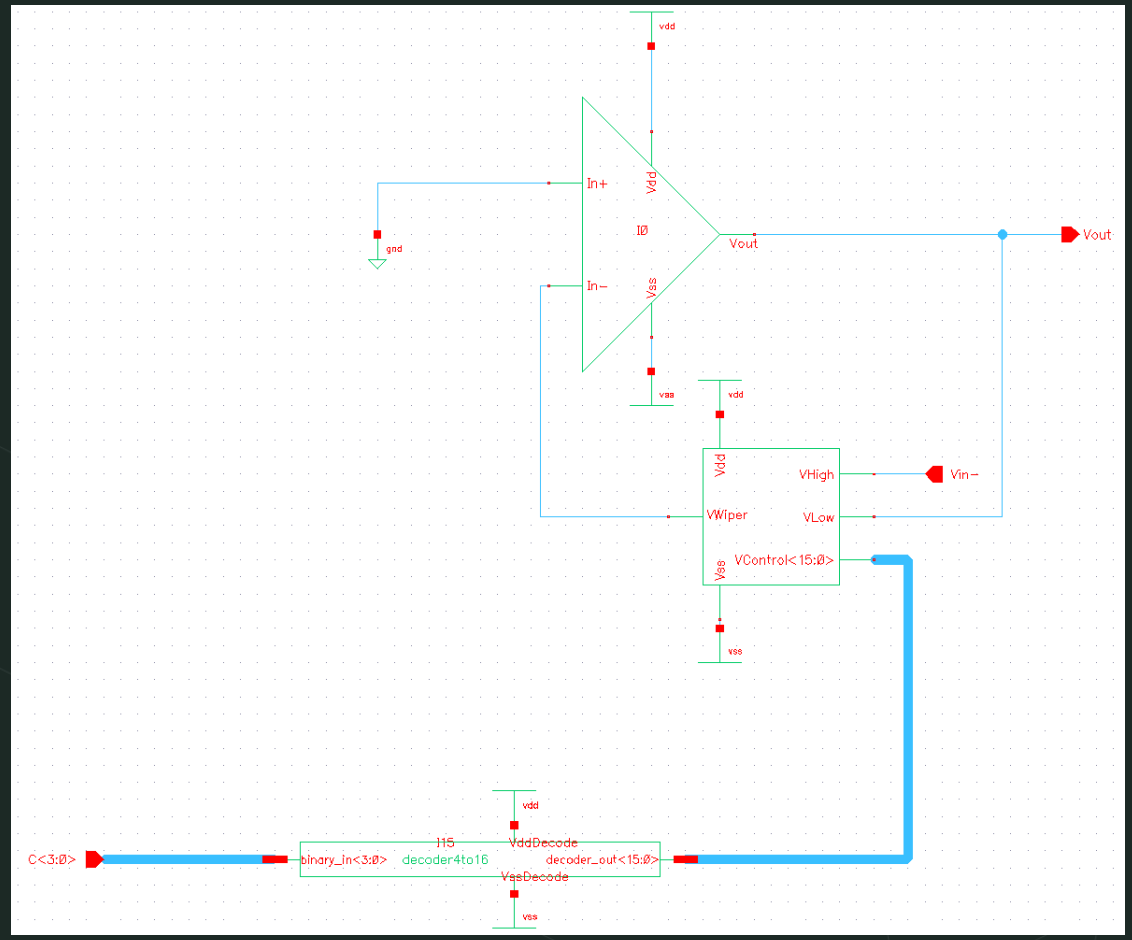
- V_{IN+} is a sinusoidal signal with magnitude $56.25mA$ and frequency of $2kHz$. V_{IN+} completes one period for every state of C.
- C is a 4-bit binary number which counts from 0000 to 1111Resistor Array

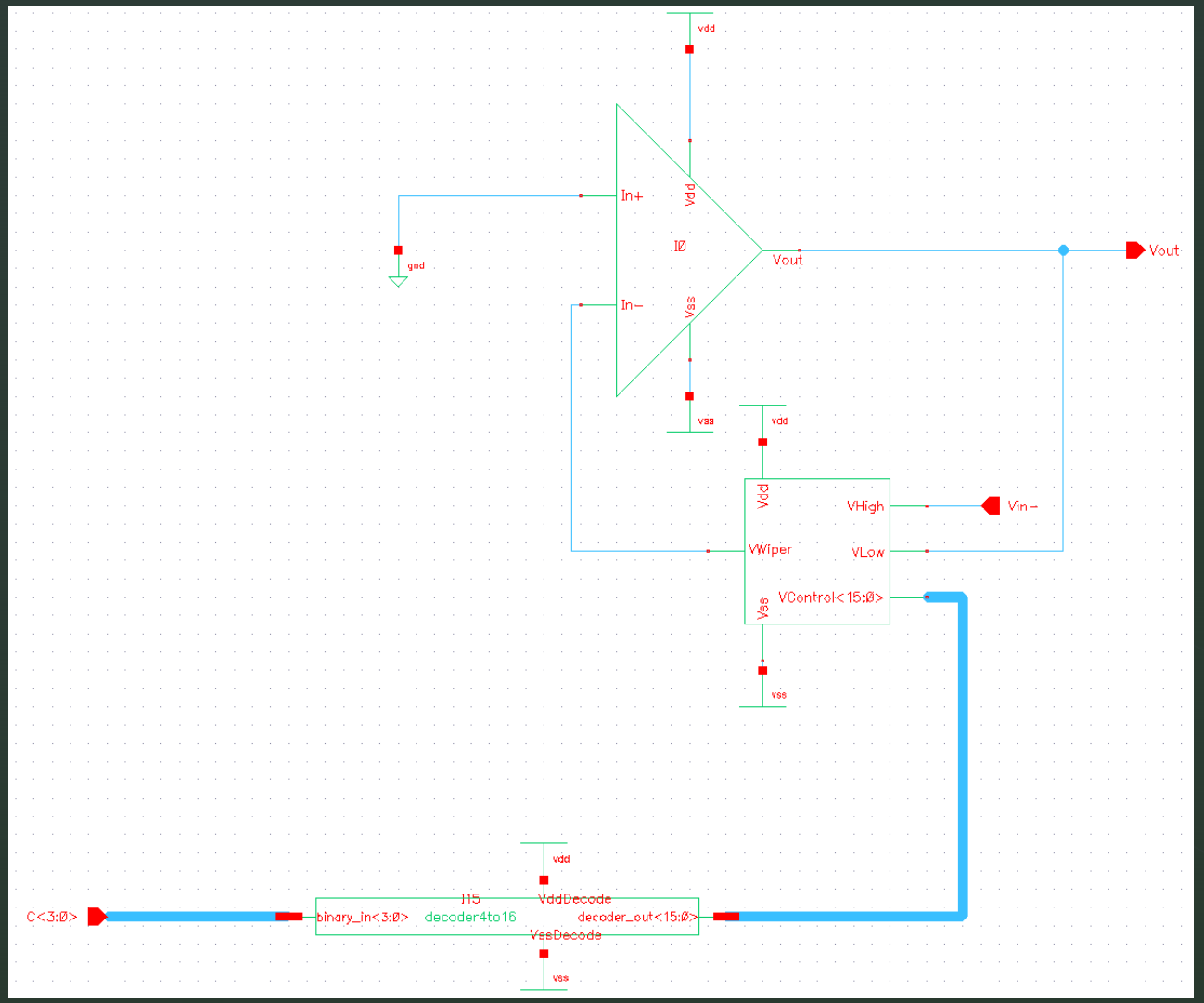
Output at Select C	Expected	Simulated
C = 0000	900mV	801.32mV
C = 0111	112.5mV	102.704mV
C = 1111	56.25mV	51.708mV



$(A_0, A_1) = (0,1)$: Programmable Inverting Amp

- Uses a digital potentiometer to control a gain between $-\frac{1}{16}$ to -16, depending on a 4-bit input, C.
- Inputs:
  - V_{IN}: The signal to be amplified by the op-amp
  - $C = (C_3, C_2, C_1, C_0)$: 4-bit digital input for selecting gain
- Outputs:
  - V_{Out}: The op-amp's output signal, given by the expression $V_{Out} = -\left[\frac{15-C}{1+C}\right] V_{IN}$
- Constraints:
  - C must be a logic high signal $(0.9V)$ or a logic low voltage $(-0.9V)$.
  - V_{Out} is constrained to values between $0.9V$ and $-0.9V$



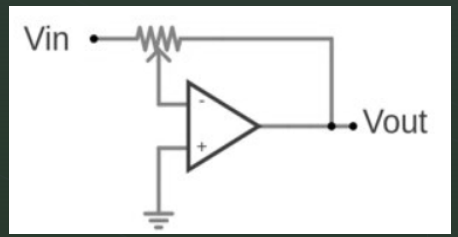


Components Used:

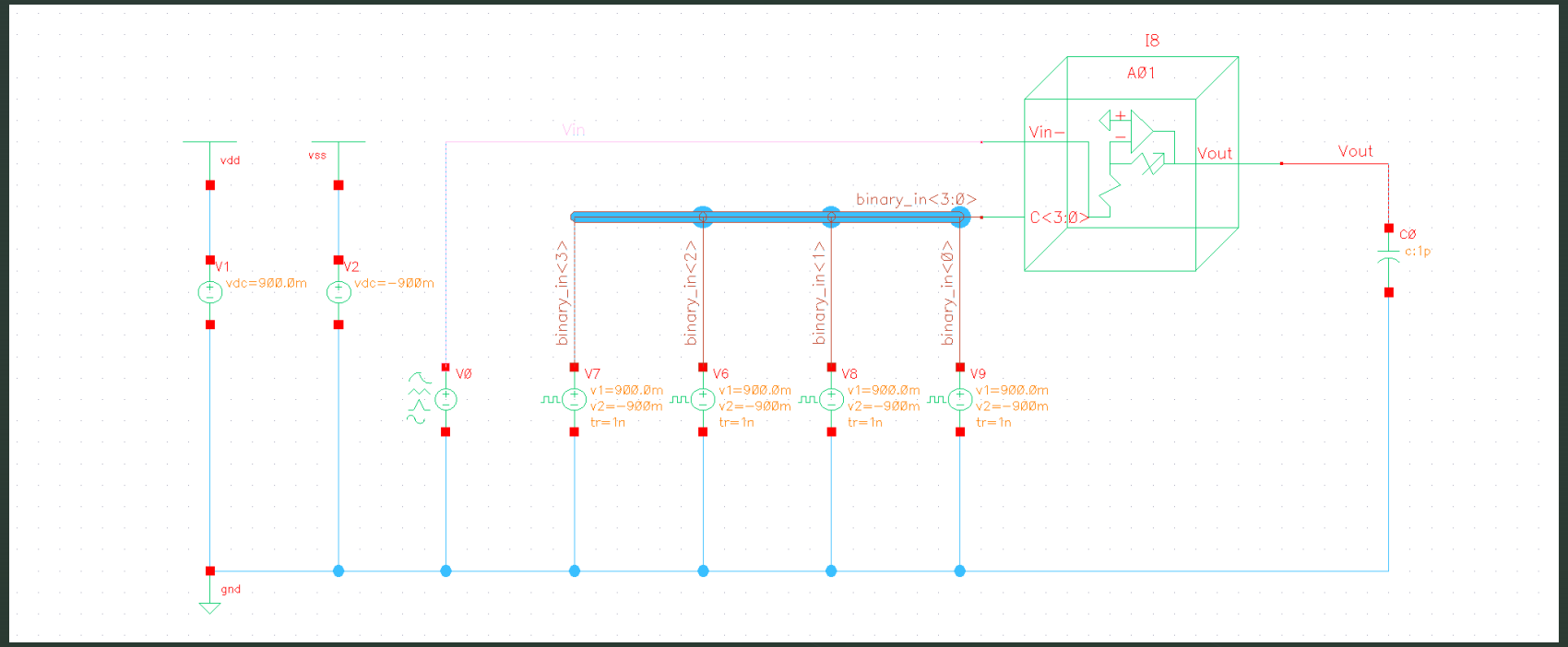
- 4-to-16 Decoder
- Operational Amplifier
- Resistor Array

Description:

The decoder programs the potentiometer to split the resistance accordingly GND and V_{Out}, thus forming a generic non-inverting op amp whose $\left[\frac{R_2}{R_1} + 1\right]$ ratio is determined by the Digital Select C.

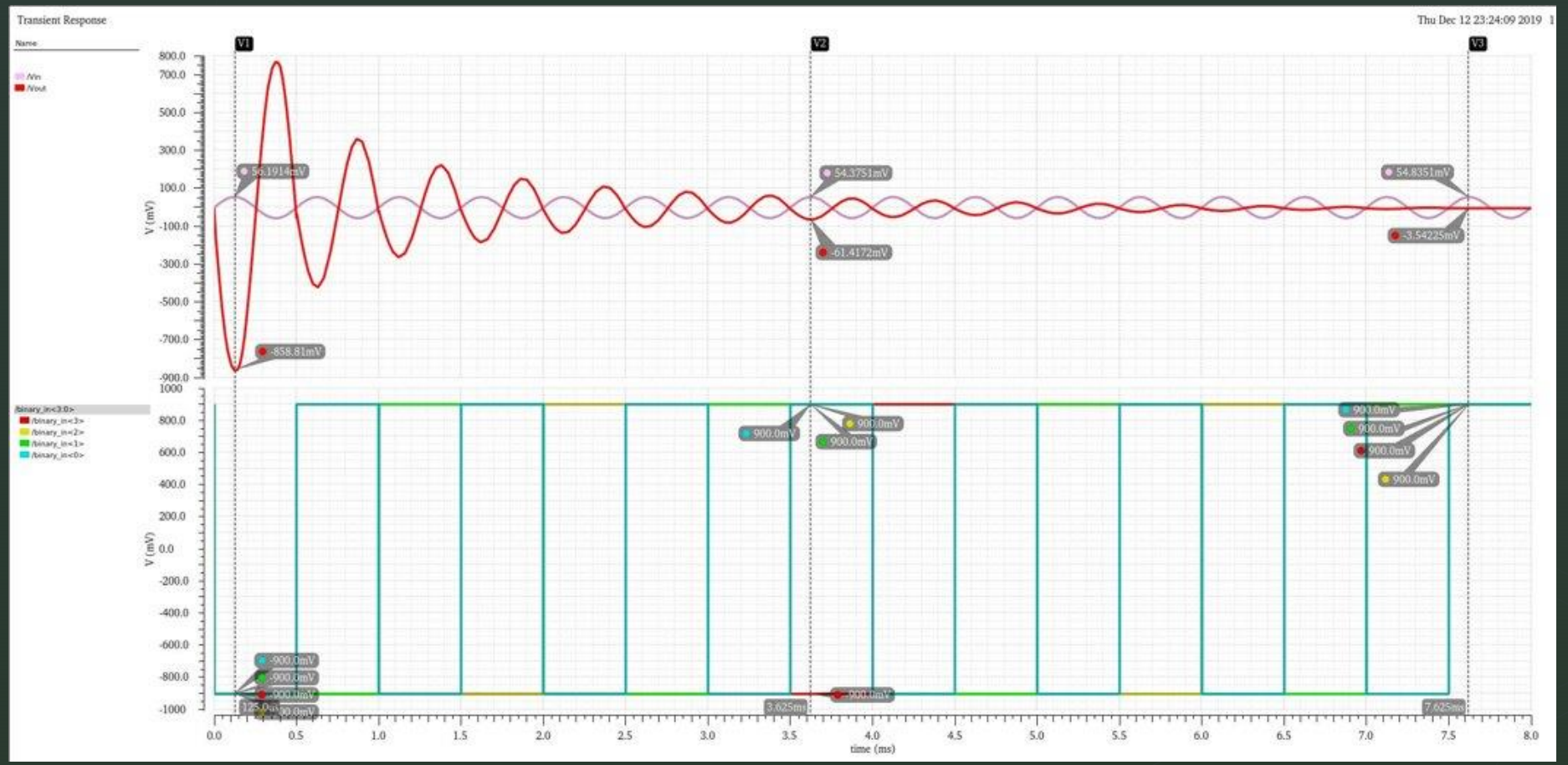


Testbench for A01



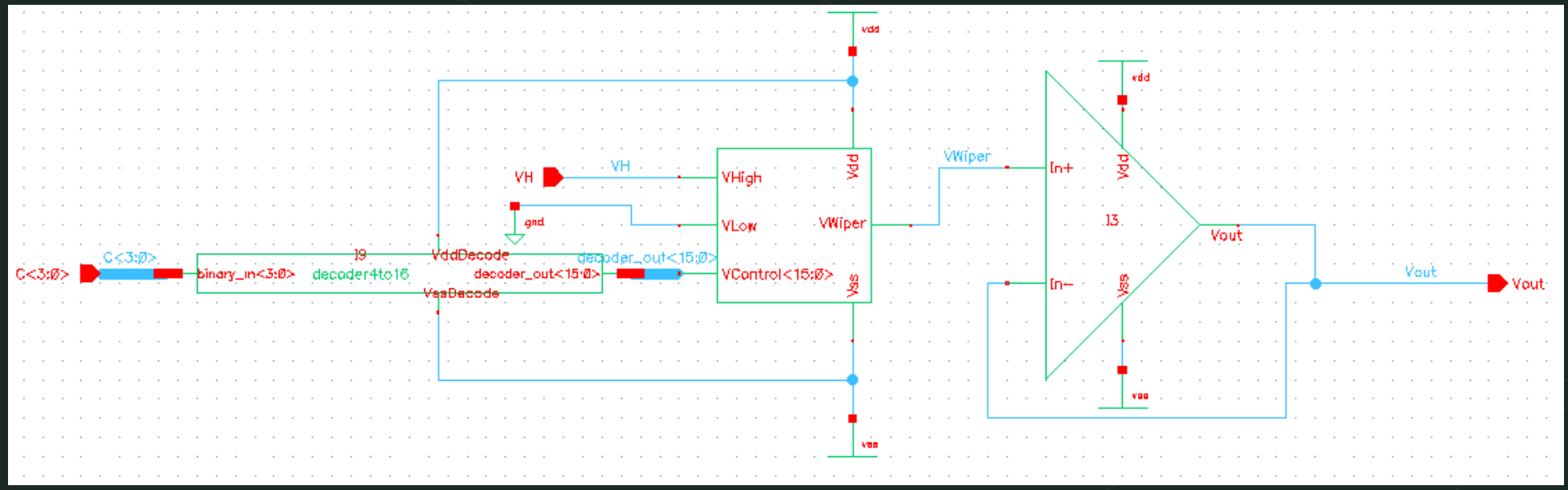
- V_{IN+} is a sinusoidal signal with magnitude $56.25mA$ and frequency of $2kHz$. V_{IN+} completes one period for every state of C.
- C is a 4-bit binary number which counts from 0000 to 1111Resistor Array

Output at Select C	Expected	Simulated
C = 0000	-843.75mV	-858.81mV
C = 0111	-56.25mV	-61.417mV
C = 1111	0mV	-3.542mV

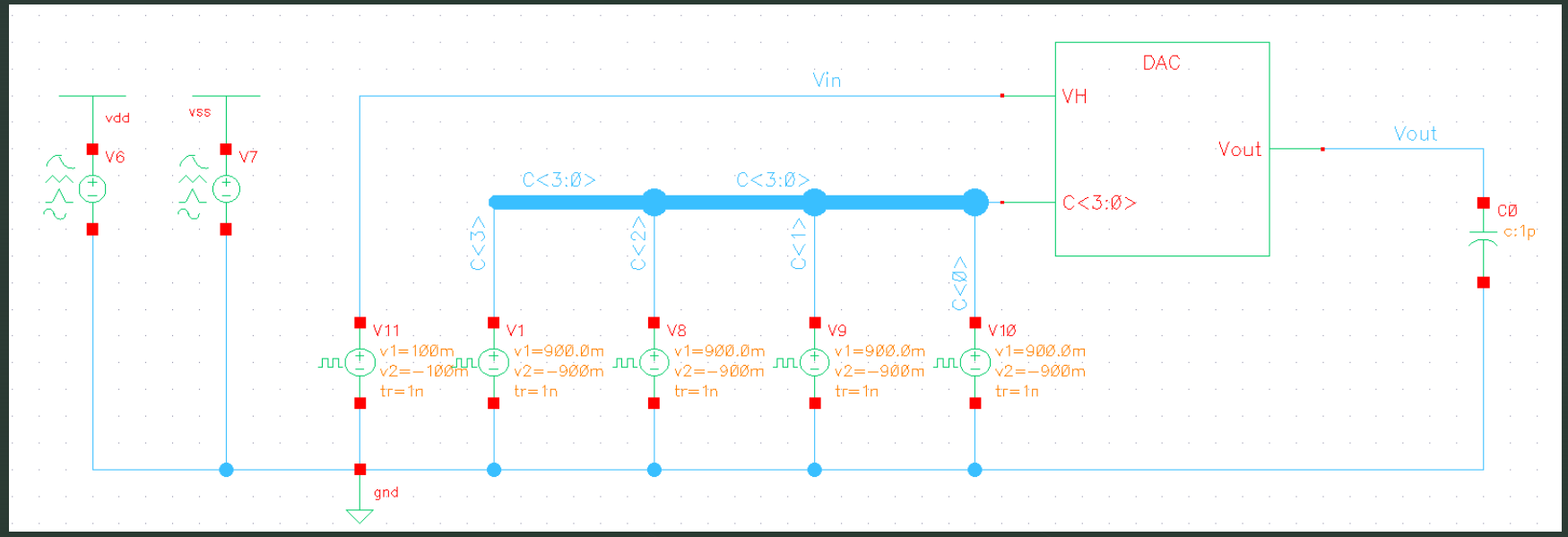


$(A_0, A_1) = (1,0)$: 4-Bit DAC

- 4-bit DAC w herein the DAC output is determined by the control settings on the potentiometer. The DAC input, often termed “VREF”, is connected to one end of the resistor array and the other end is grounded.
- Inputs:
  - V_H: The reference voltage, V_{REF}, for the DAC.
  - $C = (C_3, C_2, C_1, C_0)$: 4-bit digital input for selecting output ratio
- Output:
  - V_{Out}: The DAC’s analog output signal, given by the expression $\mathrm{V_{Out}} = \frac{15-C}{16} V_H$
- Constraints:
  - C must be a logic high signal $(0.9V)$ or a logic low signal $(-0.9V)$.
  - V_{Out} is constrained to values betw een $0.9V$ and $-0.9V$

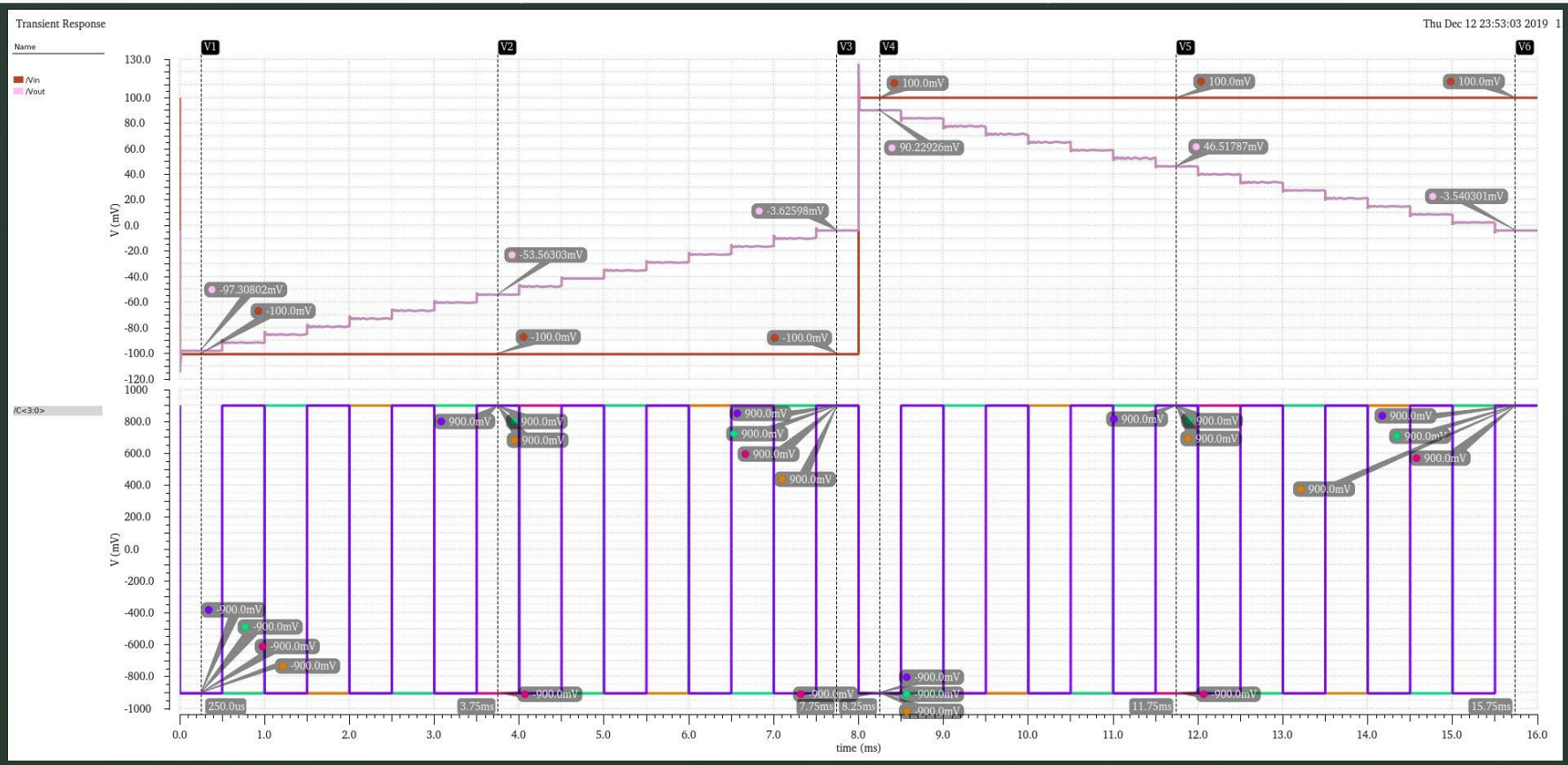


Testbench for A10



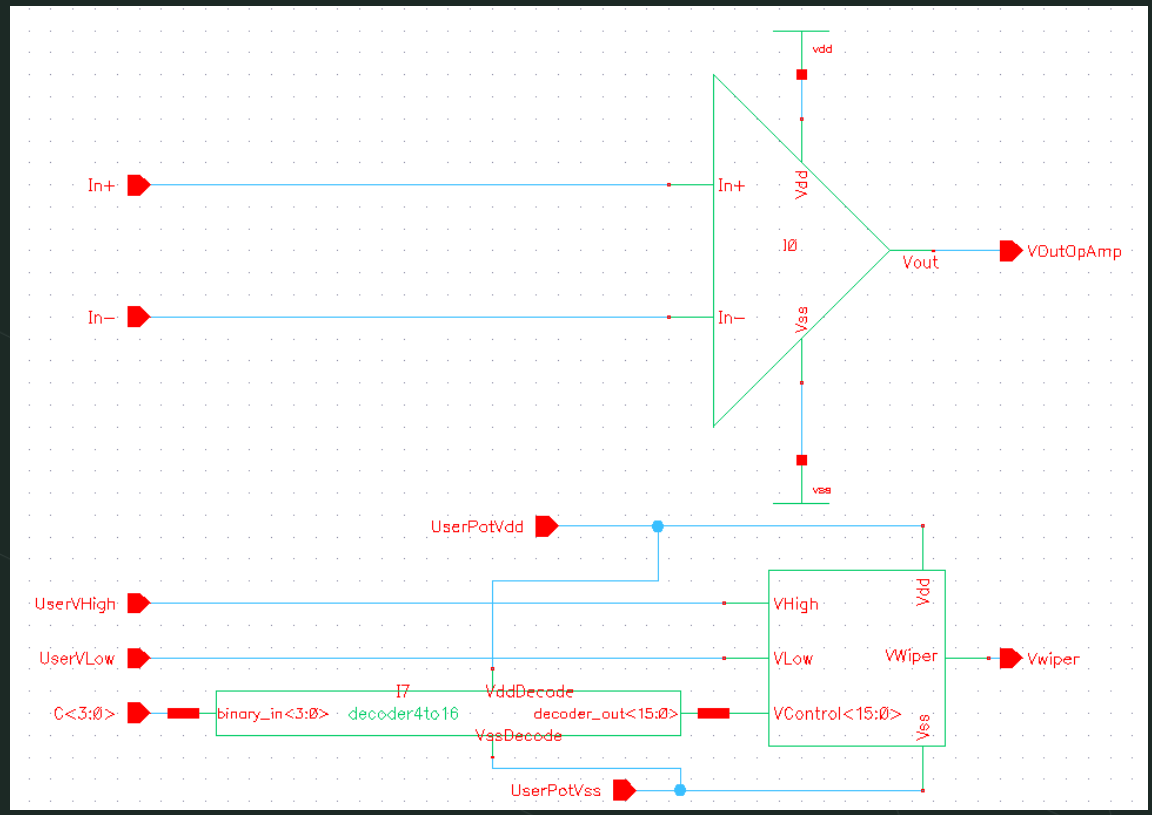
- V_{IN+} is a pulse signal with magnitude $100mA$.
- C is a 4-bit binary number which counts from 0000 to 1111. C completes two full counts; one for each state of V_{IN+}

Output at Select C	Expected	Simulated
C = 0000 (V_H negative)	-93.75mV	-97.3mV
C = 0111	-50mV	53.563mV
C = 1111	0mV	-3.542mV
C = 0000 (V_H positive)	93.75mV	90.229mV
C = 0111	50mV	46.518mV
C = 1111	0mV	-3.542mV

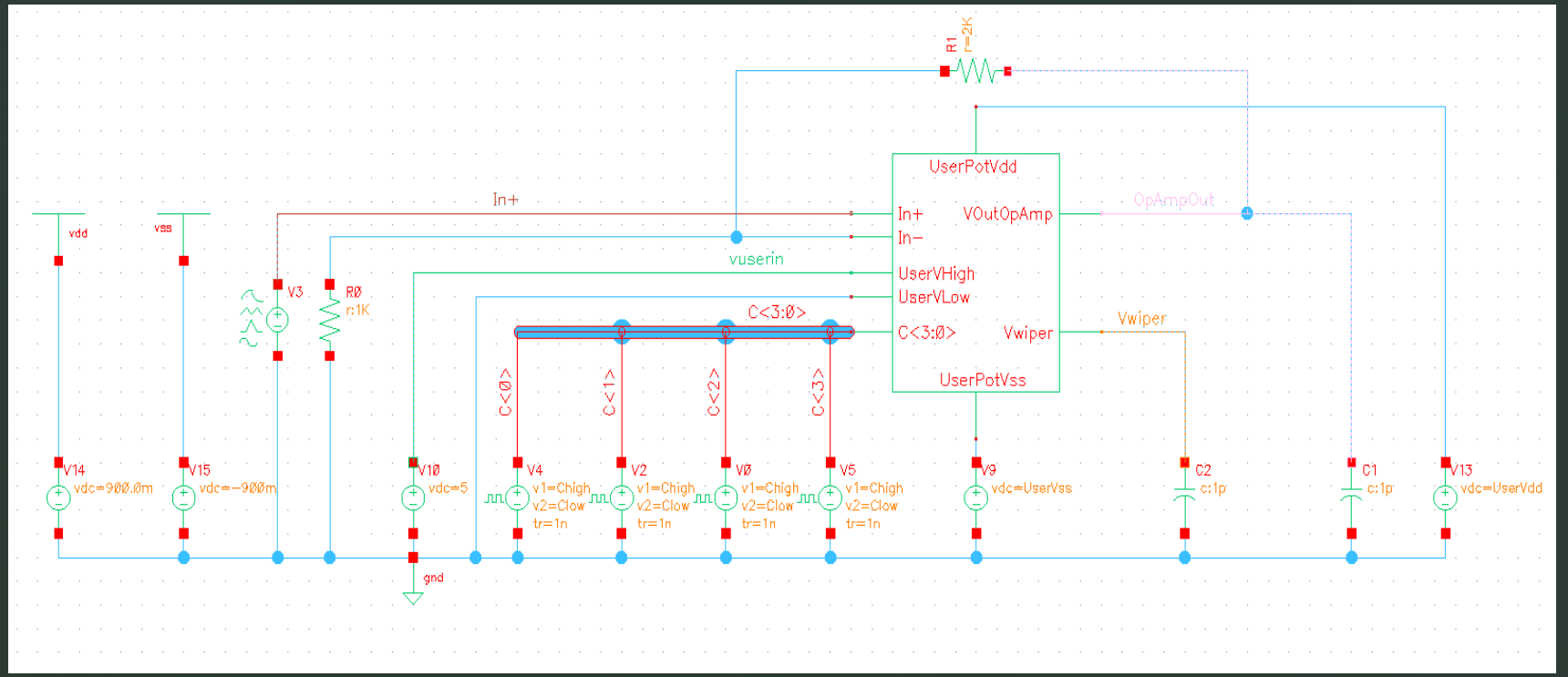


$(A_0, A_1) = (1,1)$: Potentiometer and Op-Amp

- Allows the user to use the potentiometer and op-amp in whatever configuration they want. The digital potentiometer has 16 taps, each with a nominal impedance of $5k\Omega$
- Inputs:
  - In_+ and $In\_$: The op-amp's input signals.
  - $UserVHigh$ and $UserVLow$: The high and low ends of the potentiometer.
  - $C = (C_3, C_2, C_1, C_0)$: 4-bit digital input for selecting potentiometer state
- Outputs:
  - V_{Wiper}: The voltage at the potentiometer's wiper, given by the expression $V_{Wiper} = \left((UserVHigh - UserVLow) * \frac{15-C}{16}\right) - UserVLow$. In other words, a voltage divider where C is the digital select.
- Constraints:
  - C must be a logic high signal equal to $UserVHigh$ or a logic low signal equal to $UserVLow$.
  - V_{Out} is constrained to values between $0.9V$ and $-0.9V$

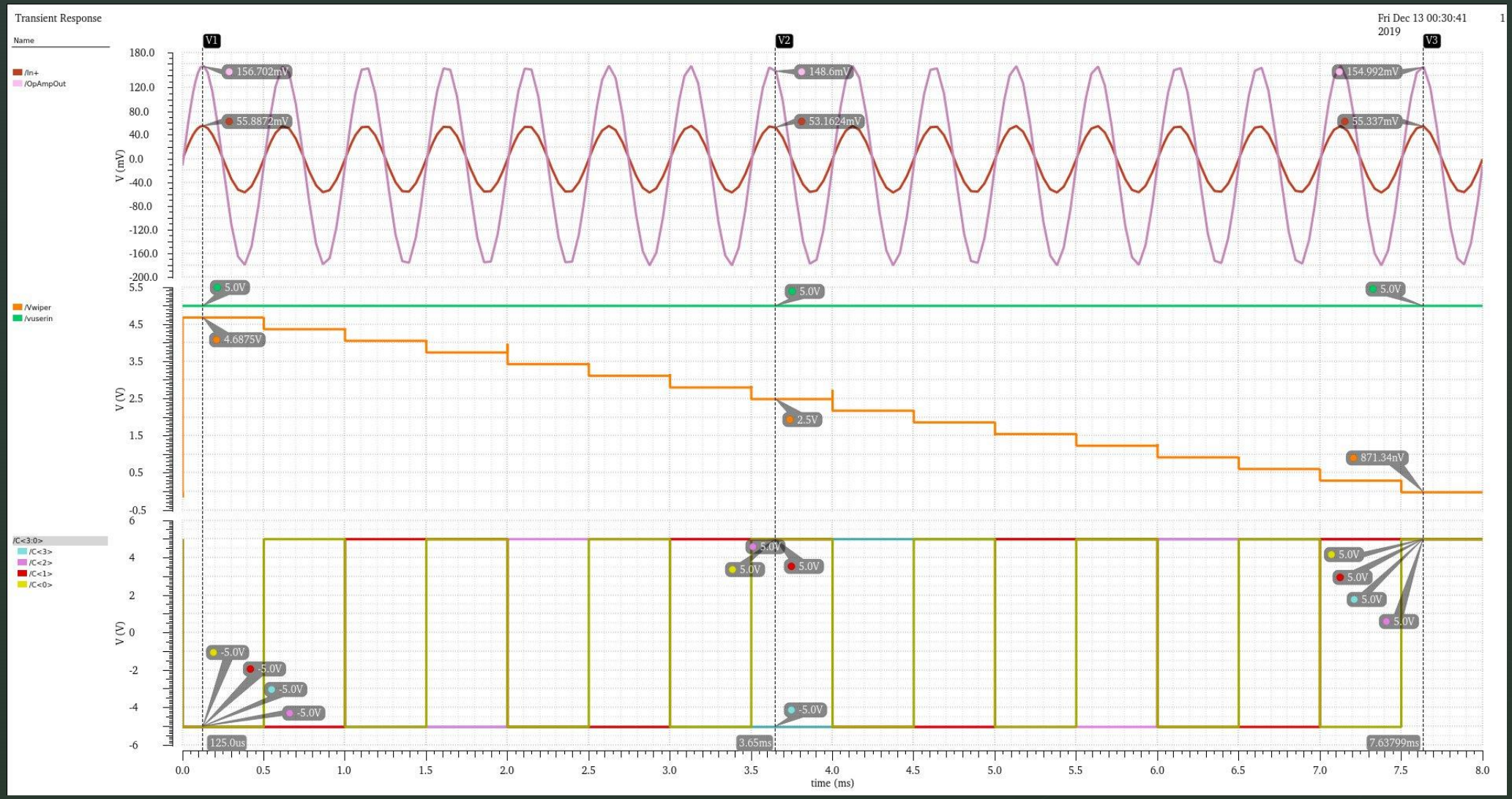


Testbench for A11



- V_{IN+} is a sinusoidal signal with magnitude $56.25mA$ and frequency of $2kHz$.
- $UserVHigh = UserPotVdd = UserPotVss$ is a DC signal with voltage of $5V$.
- C is a 4-bit binary number which counts from 0000 to 1111.

- The op-amp was had a gain of 2.8, which is similar to the expected gain of 3.
- The digital potentiometer had an output signal which matched the expression $V_{Wiper} = \left((V_H - V_L) * \frac{15-C}{16}\right) - V_L$ with a high accuracy.



Questions?