## Final Exam

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## 1 Introduction

This project consisted of running the  $\mu\text{C}/\text{OS-II}^{\text{TM}}$  operating system with three tasks. The first task blinks a green LED. The second task posts a semaphore that is unlocked by a button ISR, upon unlocking the task then increments a 7 segment display. The third task displays a user menu to a terminal with various options that are discussed in further detail in the proceeding sections of this document. Included with the submission of this document are two videos, one video is of the button, 7 segment display, and the two LEDs, the second video is a capture of the putty terminal when running the EEPROM, DMA, and SDRAM options (I found it difficult to take video with my phone that was watchable while attempting to hold it steady for 3+ minutes for the SDRAM test to complete).

# 2 System Design

This system uses i2c communications to read and write to an EEPROM device on the board. The options for telling the OS what to do are selected by a user by using the menu displayed in the terminal, the terminal menu also includes options to run a DMA test and a SDRAM test. The system includes the Nios II processor, an I2C controller, on-chip memory (RAM), a SDRAM controller, a DMA controller, and four peripherals a red LED, a green LED, a seven segment display, and a button. The button is set up to interrupt when pressed and release a Semaphore that allows the seven segment display increment code to execute. The code for turning the green LED on and off is put in the highest priority task and it toggles the LED every 500ms (making it flash every 1 second). The rest of the pieces to this project are accessed through a terminal that runs through a COM port, the terminal will display six options Write EEPROM, Read EEPROM, Turn on Red LED, Turn off Red LED, DMA Test, and SDRAM Test. A block diagram of the system can be seen below in Figure 1

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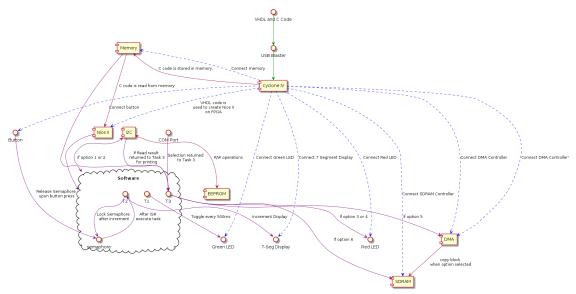


Figure (1) Embedded System Block Diagram

## 3 Theory of Operation

This system runs the  $\mu$ C/OS-II<sup>TM</sup> operating system with three tasks. The first task toggles the green LED on and off every 500ms, this task was given the highest priority since it does not require interaction from the user and can run on its own. Making it the highest priority prevents other tasks from blocking it while waiting on input. The second task increments the seven segment display upon a button press. When the program initializes the button registers an ISR with the operating system so that when the button is pressed it triggers the button's ISR. The button ISR releases a Semaphore that is locked in the second task which calls the increment display method. The semaphore once locked waits until it is unlocked to continue executing the code below it, in this case that code is the  $increment\_display()$  method. After the ISR is executed and the display is incremented the code loops back to locking the semaphore until the button ISR is triggered again.

The final task in this system contains all of the menu options that are displayed in the terminal. The first and second options are Write EEPROM and Read EEPROM respectively. Write EEPROM will prompt the user for an address followed by a prompt for data, once the values are given the I2C controller will write the given data to the EEPROM at the address provided. The read EEPROM function will prompt the user for an address and the I2C controller will return the value at that address in the EEPROM. The next two options are fairly straight forward, they are Turn on Red LED and Turn off Red LED, the first will set the value of the value of the LED to 0x01 (on) and the second will set it to 0x00 (off). The final to options in the menu are DMA Test and SDRAM Test. The first will initialize a 1MB block of the SDRAM starting at the base address 0x10000000 to 0x000A0000 (NOTE: this value was arbitrarily chosen to avoid false positives that could result from using all ones or zeros, since they

could just be left over from running a SDRAM test). Once the 1MB block is initialized the DMA Test then copies the 1MB block from the base address to another 1MB section starting at 0x10100000, finally it is run once more copying the block to the next 1MB chunk of memory starting at 0x10200000. The last step of each copy checks the 1MB block to ensure that the values were copied correctly. The final option on the menu is the SDRAM test, which conducts a test by writing all ones to the SDRAM, writing all zeros to the SDRAM, and writing incrementing values to the SDRAM. After each step the SDRAM is checked to ensure that the values were written properly.

#### 4 Results

The EEPROM, Red LED, and the Green LED functioned normally like in the last homework assignment (the code was the base I started this project from) and the results can be seen in Figure 2 below as well as in the video submitted with this document. The new additions to this project were the incrementing of the 7 segment display using a semaphore that is unlocked in the button ISR. I was able to get this to work without much issue, though I did figure out that it needed to be the second highest priority behind the blinking LED because if it was the highest it would stop the LED from blinking if the conditions are right. The SDRAM test is fairly simple write ones, then zeros, then incrementing values each time. When testing the SDRAM as you can see in Figure 3 the process of writing to and reading from the SDRAM takes about 35 seconds each (meaning 35sec to read and 35sec to write), so directly writing to the SDRAM is rather slow. The DMA copy turned out to be much faster, so fast that I couldn't really get a good time estimate because the copy seemed to happen within a single clock tick, I still dont really see how this happened since I am assuming it should take multiple clock ticks to write but I guess it is only 1MB so maybe not, because of this issue where the copy was starting and finishing on the same clock tick I decided to pick a random value to write to the block so that I could ensure that my copy was actually copying something. Turns out that it was and the value was properly written to the block of SDRAM as you can see in the terminal output in Figure 4.

```
Options:
1) Write EEPROM
Read EEPROM
3) Turn on Red LED
4) Turn off Red LED
You chose option 1
Enter Address: 10
Enter Data: 45
Options:
1) Write EEPROM
2) Read EEPROM
3) Turn on Red LED
4) Turn off Red LED
You chose option 2
Enter Address:
Value at address 10 is 45
```

Figure (2) EEPROM Output

```
Options:
1) Write EEPROM
2) Read EEPROM
3) Turn on Red LED
4) Turn off Red LED
5) DMA Test
6) SDRAM Test
You chose option 6
Writing ones to SDRAM...done.
Process took 32 seconds
Verifying ones...done.
Process took 37 seconds
Memory Test PASSED
Writing zeros to SDRAM...done.
Process took 30 seconds
Verifying zeros...done.
Process took 35 seconds
Memory Test PASSED
Writing incrementing values to SDRAM...done.
Process took 33 seconds
Verifying incremented values...
```

Figure (3) SDRAM Output

```
1) Write EEPROM
Read EEPROM
Turn on Red LED
Turn off Red LED
5) DMA Test
6) SDRAM Test
You chose option 5
Initializing 1MB block to 0x000A0000.
Copying 1MB block to 0x10100000...Process took 0.00000
Verifying DMA Copy...done.
Process took 0.33 seconds
DMA Copy Successful.
Copying 1MB block to 0x10200000...Process took 0.00000
Verifying DMA Copy...done.
Process took 0.32 seconds
DMA Copy Successful.
```

Figure (4) DMA Output

### 5 Conclusion

I found was able to complete the majority of this project without much trouble. The only portion that really gave me any issues was the DMA copy, I am not sure if it is just so fast that the 100MHz clock isn't fast enough to read it or what, but as I said in the results section I verified the copies each time and the data was there. I attempted to debug the timing quite a few times and every time I saw that the start and stop times I used to clock the functions were the same value every time when it came time to print them. I attempted to find a better way to clock the functions to no avail, most of the HighRes timing stuff is in C++ and this project is basically limited by the 100MHz clock when it comes to timing.

#### $\mathbf{A}$

#### VHDL Code

```
-- ECE532 Final Exam
-- Zackary McClamma
-- 11-DEC-2019
library ieee;
  use ieee.std logic 1164.all;
entity final exam is
  port
  (
                 : \mathbf{in} \quad \mathbf{std} \, \_ \, \mathsf{logic} \ := \ \ \mathbf{'X'}; \ -\!\!\!\!- \ \mathit{rxd}
      i uart rxd
                        : out std logic;
                                                   --txd
      o uart txd
                        : inout std_logic;
: inout std_logic;
      b\,\_\,i\,2\,c\,\_\,s\,c\,l
      b_i2c_sda
green_led
                        : out std_logic;
                        : out std_logic;
      red_led
                                               std_logic_vector(12 downto 0);
                 o_sdram_addr
                                     : out
-- a d d r
                 o sdram ba
                                               std_logic_vector(1 downto 0);
                                      : out
-- b a
                  o_sdram_cas_n
                                      : out
                                              std_logic;
-- cas_n
                                              std logic;
                  o sdram cke
                                      : out
-- cke
                  o sdram cs n
                                              std logic;
                                      : out
--cs_n
                 b sdram dq
                                      : inout std logic vector (31 downto 0) := (oth)
                 o\_sdram\_dqm
                                              std logic vector (3 downto 0);
                                      : out
-- dqm
                                      : out
                                               std logic;
                  o sdram ras n
-- ras_n
                 o\_sdram\_we\_n
                                     : out
                                               std_logic;
                  o\_sdram\_clk
                                               std logic;
                                    : out
                            : out std logic vector(6 downto 0);
                  display
                  button : in std_logic
  );
end final exam;
architecture sch of final_exam is
  component final_cpu is
        port (
      clk clk
                          : in std logic := 'X'; — clk
```

```
reset_reset_n : in std_logic := 'X'; -- reset_n
                 : in std_logic;
      i2c\_sda\_in
                       : in std_logic;
      i2c\_scl\_in
      i2c\_sda\_oe
                       : out std logic;
                   : out std_logic;
      i2c scl oe
      green led export : out std logic;
      red led export : out std logic;
                 sdram addr
                                           std_logic_vector(12 downto 0);
                                  : out
                                           std_logic_vector(1 downto 0);
                 sdram\_ba
                                   : out
                 sdram\_cas\_n
                                  : out
                                           std_logic;
                 \operatorname{sdram} \_\operatorname{cke}
                                  : out
                                           std_logic;
                 sdram cs n
                                 : \mathbf{out}
                                           std_logic;
                 sdram dq
                                 : inout std logic vector (31 \text{ downto } 0) := (\text{ otherwise})
                                           std_logic_vector(3 downto 0);
                 sdram dqm
                                 : out
                                           std logic;
                 sdram ras n
                                 : out
                               : out
                                           std logic;
                 sdram we n
                                           std_logic;
                 sdram_clk_clk : out
                 button_export : in std_logic;
                 display_export : out std_logic_vector(6 downto 0)
-- export
         );
  end component final_cpu;
  \mathbf{signal} \  \, \mathbf{w}\_\mathbf{i} 2\mathbf{c}\_\mathbf{sda}\_\mathbf{in} \qquad \quad : \  \, \mathbf{std}\_\mathbf{logic} \, ;
  signal w_i2c_scl_in
                           : std_logic;
  signal w sdram clk : std logic;
begin
    b_i2c_scl \le '0' when w_i2c_scl_oe = '1' else 'Z';
    b_i2c_sda \le '0' when w_i2c_sda_oe = '1' else 'Z';
    w_i2c_scl_in \le b_i2c_scl;
    w i2c sda in \le b i2c sda;
         o_sdram_clk <= w sdram clk;
    u0 : component final cpu
        port map (
      clk_clk
                         \Rightarrow i_clk,
                                                           clk.clk
      reset\_reset\_n \implies i\_reset\_n,
                                                       reset.reset n
                 uart_rxd => i_uart_rxd,
                 uart_txd \implies o_uart_txd,
      green_led_export => green_led,
      red led export => red led,
      i2c\_sda\_in \implies w\_i2c\_sda\_in,
      i2c_scl_in \Rightarrow w_i2c_scl_in,
```

```
i2c\_sda\_oe \implies w\_i2c\_sda\_oe,
        i\,2\,c\,\_\,s\,c\,l\,\_\,o\,e\  \, =>\  \, w\,\_\,i\,2\,c\,\_\,s\,c\,l\,\_\,o\,e\  \, ,
                      sdram_addr
                                          \Rightarrow o sdram addr,
                      \operatorname{sdram}_{-}\operatorname{ba}
                                         => o_sdram_ba,
                      sdram_cas_n
                                         \Rightarrow o_sdram_cas_n,
                      \operatorname{sdram}_cke
                                           => o sdram cke,
                      sdram cs n
                                           \Rightarrow o sdram cs n,
                      sdram dq
                                           \Rightarrow b sdram dq,
                      sdram dqm
                                           \Rightarrow o sdram dqm,
                      sdram ras n
                                         \Rightarrow o sdram ras n,
                      sdram\_we\_n
                                           \Rightarrow o_sdram_we_n,
                      \operatorname{sdram} \operatorname{clk} \operatorname{clk} => \operatorname{w\_sdram} \operatorname{clk},
                      button_export => button,
                      display_export => display
end sch;
\mathbf{B}
      C Code
B.1
      Headers
 * Name: Zackary McClamma
 * Course: ECE 532
 * \quad Assignment: \quad Final \quad Exam
 * Date: 11 DEC 2019
  * File: hw5.h
  * */
#ifndef FINAL H
#define FINAL_H_
\#include < sys / alt irq.h>
\#include < sys / alt \_ timestamp . h>
#include "altera_avalon_pio_regs.h"
#include <time.h>
#include "alt_types.h"
#include "sys/alt irq.h"
#define I2C BASE 0x80000
#define UART BASE 0x60000
#define RED LED BASE 0x90000
#define GREEN LED BASE 0xA0000
#define SDRAM BASE 0x10000000
#define SDRAM SIZE WORDS 32000000
```

```
#define DISPLAY BASE 0x000D0000
#define BUTTON BASE 0x000E0000
\#define DMA BASE 0 \times 0000 \times 0000
typedef struct str timer regs{
         unsigned int stats;
         unsigned int control;
         unsigned int periodl;
         unsigned int periodh;
         unsigned int snapl;
         unsigned int snaph;
}timer regs;
typedef volatile struct {
         unsigned int uart rxdata;
         unsigned int uart txdata;
         unsigned int uart status;
         unsigned int uart_control;
         unsigned int uart_divisor;
         unsigned int uart eop;
}uart reg;
typedef volatile struct{
         unsigned int i2c_tfr_cmd;
         unsigned int i2c_rxdata;
         \mathbf{unsigned} \ \mathbf{int} \ \mathbf{i}\, \mathbf{2}\, \mathbf{c}\, \underline{\phantom{a}}\, \mathbf{c}\, \mathbf{trl} \; ;
         unsigned int i2c_iser;
         unsigned int i2c isr;
         unsigned int i2c status;
         unsigned int i2c tfr cmd fifo lvl;
         unsigned int i2c rx data fifo lvl;
         unsigned int i2c scl low;
         unsigned int i2c_scl_high;
         unsigned int i2c_sda_hold;
} i2c_reg;
typedef volatile struct {
         unsigned int data;
         unsigned int dir;
         unsigned int intmask;
         unsigned int edge;
         unsigned int outset;
         unsigned int outclear;
}gpio_regs;
typedef volatile struct {
         unsigned int dma status;
         unsigned int dma read addr;
         unsigned int dma write addr;
```

```
unsigned int dma_length;
                        {\bf unsigned\ int}\ {\rm dma\_res1}\,;
                        unsigned int dma_res2;
                        unsigned int dma_control;
                        unsigned int dma res3;
}dma_reg;
 int display values [] = \{0xC0, 0xF9, 0xA4, 0xB0, 0x99, 0x92, 0x82, 0xF8, 0x00, 0xF8, 0xF
 volatile int edge capture = 0;
 volatile int counter = 0;
 void i2c_init(void);
 void eep_write(unsigned short addr, unsigned char data);
 unsigned char eep read(unsigned short addr);
 void printMenu(void);
 void led on(int* base);
 void led off(int* base);
 void timer_isr(void);
 int sdram test ones(void);
 int sdram test zeros(void);
 int sdram_test_increment(void);
 void dma_start(unsigned int raddr, unsigned int waddr, unsigned int len);
 void dma wait();
 void dma_check(unsigned int start_addr);
 void dma init block();
 void increment_display();
 void init_button();
 void button_isr(void* context, alt_u32 id);
\#endif /* FINAL_H_* */
B.2
                 Source
   * Name: Zackary McClamma
   * Course: ECE 532
   * Assignment: Final Exam
   * Date: 11 DEC 2019
    * File: main.c
   * */
#include < stdio.h>
#include < system.h>
#include "final.h"
#include "includes.h"
```

```
OS EVENT *sem;
```

```
/{*}\ Definition\ of\ Task\ Stacks\ */
#define
          TASK STACKSIZE
                                 2048
OS STK
          task1 stk[TASK STACKSIZE];
OS STK
          task2 stk[TASK STACKSIZE];
OS STK
          task3 stk[TASK STACKSIZE];
/* Definition of Task Priorities */
\#define TASK1_PRIORITY
                              1
#define TASK2_PRIORITY
                              3
                                  2
#define TASK3 PRIORITY
/* Toggles the Green LED every 500ms */
void task1(void* pdata)
{
        while(1){
          INT8U err;
           //OSMutexPend(tex, 0, \&err);
           unsigned int* gled = GREEN LED BASE;
                   if(*gled == 0x01){
                            led _ off (GREEN_LED_BASE);
                         led on (GREEN LED BASE);
           //OSMutexPost(tex);
          OSTimeDlyHMSM (0, 0, 500);
}
/*Increment 7-Segment display*/
void task2(void* pdata)
{
        int* display = DISPLAY BASE;
        *display = display values [0];
        INT16U timeout = 0;
        INT8U err;
        \mathbf{while}(1)
        {
                 OSSemPend(sem, timeout, err);
                 if (edge capture !=0)
                 {
                         increment_display();
                         edge capture = 0;
                 }
        }
```

```
}
/*Display Menu and facilitate user selections */
void task3(void* pdata)
             INT8U err;
             i2c init();
             while (1)
                     int start , stop , opt , addr , data , addrSet , dataSet = 0;
                     unsigned int dma length = 1024*1024;
                     unsigned char read;
                     //display menu
                     printf("Options:\r\n");
                     printf("1) \ \ Write \ \ EEPROM \ \ \ \ ");
                     printf("2) \ \ Read\ EEPROM\ r\ n");
                     printf("3)_Turn_on_Red_LED(r n");
                     printf("4) \_Turn \_ off \_Red \_LED \ r \ n");
                     printf("5) DMA Test rn");
                     printf("6) \_SDRAM\_Test \setminus r \setminus n");
                     scanf("%d", &opt);
                     fflush (stdin);
                     printf("You_chose_option_%d\r\n",opt);
                     switch(opt){
                     // Write EEPROM
                     case 1:
                               addrSet = 0;
                               dataSet = 0;
                                \mathbf{while} (\mathbf{addrSet} = 0)
                                          printf ("Enter_Address:_");
                                          scanf("%d", &addr);
                                          fflush (stdin);
                                          printf(" \c \% d \ \ r \ \ n", \ addr);
                                          if((addr < 0) | (addr > 127))
                                          {
                                                     printf("Invalid_input_try_again\r\n");
                                          }
                                          else
                                          {
                                                     addrSet = 1;
                                \mathbf{while}(\mathbf{dataSet} == 0)
                                          printf("Enter_Data:_");
                                          scanf ("%d", &data);
                                          fflush (stdin);
                                          p \, r \, i \, n \, t \, f \, \left( \, " \, \lrcorner \% d \, \backslash \, r \, \backslash \, n \, " \, , \, \, \, d \, a \, t \, a \, \right);
```

```
if (data > 255)
                                                                                                                                        printf("Invalid_input_try_again\r\n");
                                                                                          }
                                                                                           else
                                                                                                                                        dataSet = 1;
                                            eep\_write(addr, data);
                                            OSTimeDlyHMSM(0, 0, 1, 0);
                                            break;
//Read EEPROM
case 2:
                                            addrSet = 0;
                                            \mathbf{while} (\mathbf{addrSet} = 0)
                                             {
                                                                                           printf ("Enter_Address:_");
                                                                                           {\rm scanf} \; (\, \tt " \% d \, \tt " \; , \; \& addr \, ) \, ;
                                                                                           fflush (stdin);
                                                                                           printf("\r\n");
                                                                                           if((addr < 0) | (addr > 127))
                                                                                                                                        printf("Invalid_input_try_again\r\n");
                                                                                          else
                                                                                          {
                                                                                                                                       addrSet = 1;
                                             }
                                            read = eep_read(addr);
                                             printf("Value\_at\_address\_\%d\_is\_\%d\backslash r\backslash n", addr, (int) readdress\_\%d\_is\_\%d\backslash r\backslash n", addr, (int) readdress\_\%d\_is\_\%d\_is\_\%d\backslash r\backslash n", addr, (int) readdress\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is\_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_\%d\_is_
                                            OSTimeDlyHMSM \left( \begin{smallmatrix} 0 \end{smallmatrix}, \begin{smallmatrix} 0 \end{smallmatrix}, \begin{smallmatrix} 1 \end{smallmatrix}, \begin{smallmatrix} 0 \end{smallmatrix});
                                            break;
//Turn Red LED on
case 3:
                                            led on (RED LED BASE);
                                            OSTimeDlyHMSM(0, 0, 1, 0);
                                            break;
// Turn Red LED off
case 4:
                                            led _ off (RED_LED_BASE);
                                            OSTimeDlyHMSM(0, 0, 1, 0);
                                            break;
//DMA Test
case 5:
                                              printf("Initializing\_1MB\_block\_to\_0x000A0000.\ \ r\ ");
```

```
dma_init_block();
                           printf ("Copying_1MB_block_to_0x10100000...");
                          start = OSTimeGet();
                          dma start (SDRAM BASE, 0x10100000, dma length);
                          stop = OSTimeGet();
                          printf("Process\_took\_\%f\_seconds \ r \ n", ((float)stop-(float))
                          dma check (0 \times 10100000);
                           printf("Copying_1MB_block_to_0x10200000...");
                          start = OSTimeGet();
                          {\tt dma\_start} \, (SDRAM\_BASE, \ 0x10200000 \, , \ dma\_length) \, ;
                          //dma_wait();
                          stop = OSTimeGet();
                          printf("Process\_took\_\%f\_seconds \ r \ n", ((float)stop - (float)stop)
                          dma check (0 \times 10200000);
                          break;
                 //SDRAM Test
                 case 6:
                          sdram_test_ones();
                          sdram_test_zeros();
                          sdram test increment();
                 default:
                           printf("Invalid\_option\_please\_try\_again.\r\n");
                          break;
            // OSTimeDlyHMSM(0, 0, 1, 0);
                 //OSMutexPost(tex);
                 //OSTimeDlyHMSM(0, 0, 0, 500);
           }
/st The main function creates two task and starts multi-tasking st/
int main(void)
 INT16U initSem = 1;
  sem = OSSemCreate(initSem);
  int tst;
  init button();
  tst = alt ic irq enable(0, 5);
  //Check if Interrupt was enabled successfully
  if (tst < 0) printf ("\nFailed_to_enable_interrupt,_enable_returned_%d\r\n", tst
  else printf("\n_{\n}Interrupt\n_{\n}Enabled.\r \n");
  //Initialize display to 0
  int* display = DISPLAY BASE;
   *display = display values[0];
```

```
OSTaskCreateExt(task1,
                    NULL,
                    (\mathbf{void} *) \& task1 \_ stk [TASK\_STACKSIZE-1],
                    TASK1_PRIORITY,
                    TASK1_PRIORITY,
                    task1 stk,
                    TASK STACKSIZE,
                    NULL,
                    0);
  OSTaskCreateExt(task2,
                    NULL,
                    (\mathbf{void} *) \& task2\_stk[TASK\_STACKSIZE-1],
                    TASK2 PRIORITY,
                    TASK2 PRIORITY,
                    task2 stk,
                    TASK STACKSIZE,
                    NULL,
                    0);
  OSTaskCreateExt(task3,
                    NULL,
                    (void *)&task3_stk[TASK_STACKSIZE-1],
                    TASK3 PRIORITY,
                    TASK3_PRIORITY,
                    {\tt task3\_stk} \; ,
                    TASK STACKSIZE,
                    NULL,
                    0);
  OSStart();
  return 0;
void led_on(int* base){
        INT8U err;
         //OSMutexPend(tex, 0, \& err);
        *base = 0x01;
        //OSMutexPost(tex);
        return;
void led off(int* base){
        INT8U err;
        //OSMutexPend(tex, 0, \&err);
        *base = 0x00;
        return;
```

}

}

```
void i2c_init(void){
          i2c\_reg *reg = I2C\_0 BASE;
          reg -> i2c \_scl \_low = 1000;
          reg \rightarrow i2c scl high = 1000;
          reg \rightarrow i2c sda hold = 500;
          reg \rightarrow i2c tfr cmd fifo lvl = 8;
          reg->i2c rx data fifo lvl = 8;
}
void eep_write(unsigned short addr, unsigned char data){
          i2c reg* reg = I2C 0 BASE;
          INT8U err;
          unsigned char addr low = addr >> 8;
          unsigned char addr high = addr & 0x00FF;
          //OSMutexPend(tex, 0, \&err);
          reg \rightarrow i2c ctrl = 0x1;
          reg \rightarrow i2c tfr cmd = 0x2A0;
          reg->i2c\_tfr\_cmd = addr\_high;
          reg->i2c\_tfr\_cmd = addr\_low;
          reg \rightarrow i2c tfr cmd = data \mid 0x100;
          while (reg \rightarrow i2c_status != 0);
          reg -> i2c \_ctrl = 0x0;
          //OSMutexPost(tex);
          OSTimeDlyHMSM (0, 0, 0, 5);
}
unsigned char eep read(unsigned short addr){
          i2c reg* reg = I2C 0 BASE;
          unsigned char addr low = addr >> 8;
          unsigned char addr high = addr & 0x00FF;
          unsigned char data;
          unsigned char tempData = 0;
          //OSMutexPend(tex, 0, \& err);
          reg \rightarrow i2c ctrl = 0x1;
          reg - i2c_tfr cmd = 0x2A0;
          reg \rightarrow i2c tfr cmd = addr high;
          reg \rightarrow i2c tfr cmd = addr low;
          reg \rightarrow i2c tfr cmd = 0x2A1;
          reg \rightarrow i2c tfr cmd = tempData \mid 0x100;
          while (reg\rightarrowi2c status != 0);
          \mathtt{data} \; = \; \mathtt{reg} \! - \! \! \! > \! \mathtt{i2c} \! \, \underline{\hspace{1pt}} \mathtt{rxdata} \; ;
          reg \rightarrow i2c ctrl = 0x0;
          //OSMutexPost(tex);
          return data;
```

```
}
int sdram test ones(void){
        unsigned int idx;
         unsigned int *sdram=SDRAM BASE;
         unsigned int start, stop;
         printf("\r\nWriting_ones_to_SDRAM...");
         start = OSTimeGet();
         for(idx = 0; idx < SDRAM SIZE WORDS; idx++)
                  sdram[idx] = 0xFFFFFFFF;
         }
         stop=OSTimeGet();
         printf("done. \ r \ n");
         printf("Process\_took\_%u\_seconds \ r \ n", (stop-start)/100);
         printf("Verifying_ones...");
         start=OSTimeGet();
         for (idx = 0; idx \le SDRAM SIZE WORDS; idx++)
                  if(sdram[idx] != 0xFFFFFFFF)
                           stop=OSTimeGet();
                           printf("MEMORY\_TEST\_FAILED! \ \ r \ n");
                           printf("Process\_took\_%u\_seconds\_\r\n",(stop-start)/100)
                           return 0;
                  }
         stop=OSTimeGet();
         printf("done. \ r \ n");
         printf("Process\_took\_\%u\_seconds \ \ r \ \ n"\ , \ \ (stop-start\ )\ /100);
         printf("Memory\_Test\_PASSED\r\n");
         return 0;
}
int sdram_test_zeros(void){
        unsigned int idx;
         unsigned int *sdram=SDRAM BASE;
         unsigned int start , stop;
         printf("\r\nWriting\_zeros\_to\_SDRAM...");
         start = OSTimeGet();
         \mathbf{for} (idx = 0; idx < SDRAM_SIZE_WORDS; idx++)
                  sdram[idx] = 0x000000000;
         }
         stop=OSTimeGet();
         printf("done.\r\n");
         printf("Process\_took\_\%u\_seconds \ \ r \ \ n", \ \ (stop-start)/100);
```

```
printf("Verifying_zeros...");
         start=OSTimeGet();
         for (idx = 0; idx \le SDRAM SIZE WORDS; idx++)
                   if(sdram[idx] != 0x00000000)
                            stop=OSTimeGet();
                             printf("MEMORY\_TEST\_FAILED! \ r \ n");
                             printf("Process\_took\_%u\_seconds\_\r\n",(stop-start)/100)
                            return 0;
                   }
         stop=OSTimeGet();
         printf("done.\r\n");
         printf("Process\_took\_%u\_seconds \ r \ n", (stop-start)/100);
         printf("Memory\_Test\_PASSED\r\n");
         return 0;
}
int sdram_test_increment(void)
         unsigned int idx;
         {\bf unsigned\ int\ *sdram=\!\!SDRAM\_BASE;}
         unsigned int start, stop;
         printf("\r\nWriting_incrementing_values_to_SDRAM...");
         start = OSTimeGet();
         \mbox{\bf for} \ (\ \mbox{id} \ x \ = \ 0 \ ; \mbox{id} \ x < \mbox{SDRAM\_SIZE\_WORDS} \ ; \mbox{id} \ x + +)
                   sdram[idx] = idx;
         stop=OSTimeGet();
         printf("done. \ r \ n");
         printf("Process\_took\_\%u\_seconds \ \ r \ \ ", \ \ (stop-start)/100);
         printf("Verifying_incremented_values...");
         start=OSTimeGet();
         for(idx=0;idx \le SDRAM SIZE WORDS;idx++)
                   if(sdram[idx] != idx)
                            stop=OSTimeGet();
                             printf("MEMORY\_TEST\_FAILED! \ r \ n");
                            printf("Process\_took\_%u\_seconds\_\rangle r. \ , (stop-start)/100)
                            return 0;
                   }
         stop=OSTimeGet();
         printf("done.\r\n");
```

```
printf("Process\_took\_%u\_seconds \ r \ n", (stop-start)/100);
        printf("Memory\_Test\_PASSED\r\n");
        return 0;
}
void button isr(void* context, alt u32 id){
        //Set context to edge capture ptr value (global value registered with I
        volatile int * edge capture ptr = (volatile int *) context;
        //Read edge capture register of Button
        *edge capture ptr = IORD ALTERA AVALON PIO EDGE CAP(BUTTON BASE);
        OSSemPost (sem);
        //Write 1 to edge capture register
        IOWR ALTERA AVALON PIO EDGE CAP(BUTTON BASE, 0x1);
        return;
}
void init button()
        //\mathit{Type} cast edge\_\mathit{capture} variable so it can be passed to register functions.
        void* edge_capture_ptr = (void*) &edge_capture;
        //Write 1 to IRQ Mask
        IOWR\_ALTERA\_AVALON\_PIO\_IRQ\_MASK(BUTTON\_BASE, 0x1);
        //Write 0 to edge capture of Button
        IOWR ALTERA AVALON PIO EDGE CAP(BUTTON BASE, 0x0);
        //Register\ Interrupt
        alt ic isr register (0,
                                                   (void*) button isr,
                                                   edge_capture_ptr,
                                                   0x0);
}
void increment_display()
        int* display = DISPLAY BASE;
        counter++;
        if (counter > 9)
                 counter = 0;
        *display = display_values[counter];
}
void dma_start(unsigned int raddr, unsigned int waddr, unsigned int len)
{
        dma reg *dmaPtr = DMA BASE;
        dmaPtr->dma read addr = raddr;
```

```
dmaPtr->dma_write_addr = waddr;
         dmaPtr->dma\_length = 2^20;
         dma wait();
}
void dma wait(void)
         dma reg *dmaPtr = DMA BASE;
         dmaPtr->dma control = 0x31;
         while ((dmaPtr->dma_status >> 0) & 1);
        dmaPtr->dma\_status \&= 0x0;
         //dmaPtr->dma\_control = 0x000000000;
}
void dma check(unsigned int start addr)
{
         unsigned int idx = 0;
         unsigned int *sdram=SDRAM_BASE;
         unsigned int stop, start;
         printf("Verifying_DMA_Copy...");
         start = OSTimeGet();
                  for (idx = 0; idx < ((1024*1024)/4); idx++)
                                    if(sdram[start\_addr + idx] != 0x000A0000)
                                             stop = OSTimeGet();
                                             printf("Process\_took\_\%g\_seconds \ r \ n", 
                                             printf("DMA\_Copy\_FAILED! \ r \ n");
                                            return;
                                   }
                  stop = OSTimeGet();
                  printf("done. \ r \ n");
                  printf("Process\_took\_\%g\_seconds \ \ r \ \ n", \ \ ((float)stop - (float)start) \\
                  printf("DMA\_Copy\_Successful.\r\n");
}
void dma_init_block()
         unsigned int idx;
         {\bf unsigned\ int\ *sdram=\!\!SDRAM\_BASE;}
         for(idx = 0; idx < ((1024*1024)/4); idx++)
                  sdram[idx] = 0x000A0000;
         }
}
```