CSE 351 Section – Virtual Memory

Exercises:

1) Name three specific benefits of using virtual memory:

2) What should happen to the TLB when a new entry is loaded into the page table base register?

3) Fill in the formulas below using *descriptions*, not variables:

   Page offset bits = $\log_2$(_____)

   Virtual address bits = _____ + page offset bits

   Physical address bits = physical page number bits + _____

   Virtual page number bits = $\log_2$(_____)

   Entries in a page table = _____

4) Fill in the following table:

VA width (n)	PA width (m)	Page size (P)	VPN width	PPN width	Bits in PTE (assume V, R, W, X)
32	32	16 KiB			
32	26			13	
	32		21		21
		32 KiB	25		25
64			48		28

5) **Processor:** 16-bit addresses, 256-byte pages

TLB: 8-entry fully associative with LRU replacement

- Track LRU using 3 bits to encode the order in which pages were accessed, with 0 being the most recent

At some time instant, the TLB for the current process is in the initial state given below.

Assume that all page table entries NOT in the initial TLB start as invalid.

- OS will assign new pages at the lowest available PPN starting at 0x17

Assume all pages can be read from and written to (ignore protection).

Fill in the final state of the TLB according to the access pattern below:

Access pattern:

1. Read `0x11F0`
2. Write `0x1301`
3. Write `0x20AE`
4. Write `0x2332`
5. Read `0x20FF`
6. Write `0x3415`

Initial TLB:

TLBT	PPN	Valid	LRU
0x01	0x11	1	0
0x00	0x00	0	7
0x10	0x13	1	1
0x20	0x12	1	5
0x00	0x00	0	7
0x11	0x14	1	4
0xAC	0x15	1	2
0xFF	0x16	1	3

Final TLB:

TLBT	PPN	Valid	LRU