

# Basic Computer Design Report

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# 1 Introduction

This report documents the simulation and testing of a basic computer design. The assembly program that was executed and the first part of simulation results can be found in the following parts. For the full simulation results, please refer to the "test\_res.txt".

## 2 Assembly Program

The assembly program used for the simulation is as follows:

Listing 1: Assembly Program

```
1 4009 // BUN 009
2 4020 // BUN
3 aaaa // Data into AC
4 0002 // 002
5 c230
6 c230
7 c230
8 c230
9 ffff // IZS check
10 F080 // ION
11 a003 // IND LDA 003
12 7200 // CMA
13 7100 // CME
14 1003 // ADD 003
15 6008 // ISZ 008
16 0004 // AND 004
17 F040 // IOF
18 7080 // CIR
19 7040 // CIL
20 7800 // CLA
21 7400 // CLE
22 7020 // INC
23 7010 // SPA
24 7008 // SNA
25 7004 // SZA
26 7002 // SZE
27 7001 // HLT
28 0000
29 0000
30 0000
31 0000
32 0000
33 C000 // IND BUN get back to the adress before interrupt
34 0000
35 0000
```

## 3 Simulation Results

The simulation results generated by running the assembly program on the basic computer design are presented below:

Listing 2: Simulation Results

```

1 0.00ns INFO          cocotb.BC_I
2 ***** DUT Signals *****
3 0.00ns INFO          cocotb.BC_I
4 PC: 000000000000    0x0
5 AR: 000000000000    0x0
6 IR: 0000000000000000 0x0
7 AC: 0000000000000000 0x0
8 DR: 0000000000000000 0x0
9 TR: 0000000000000000 0x0
10 Cycle count: 0
11
12 10000.00ns INFO      cocotb.BC_I
13 ***** DUT Signals *****
14 10000.00ns INFO      cocotb.BC_I
15 PC: 000000000000    0x0
16 AR: 000000000000    0x0
17 IR: 0000000000000000 0x0
18 AC: 0000000000000000 0x0
19 DR: 0000000000000000 0x0
20 TR: 0000000000000000 0x0
21 Cycle count: 1
22
23 20000.00ns INFO      cocotb.BC_I
24 ***** DUT Signals *****
25 20000.00ns INFO      cocotb.BC_I
26 PC: 000000000001    0x1
27 AR: 000000000000    0x0
28 IR: 0100000000001001 0x4009
29 AC: 0000000000000000 0x0
30 DR: 0000000000000000 0x0
31 TR: 0000000000000000 0x0
32 Cycle count: 2
33
34 30000.00ns INFO      cocotb.BC_I
35 ***** DUT Signals *****
36 30000.00ns INFO      cocotb.BC_I
37 PC: 000000000001    0x1
38 AR: 000000001001    0x9
39 IR: 0100000000001001 0x4009
40 AC: 0000000000000000 0x0
41 DR: 0000000000000000 0x0
42 TR: 0000000000000000 0x0
43 Cycle count: 3
44
45 40000.00ns INFO      cocotb.BC_I
46 ***** DUT Signals *****
47 40000.00ns INFO      cocotb.BC_I
48 PC: 000000000001    0x1
49 AR: 000000001001    0x9
50 IR: 0100000000001001 0x4009
51 AC: 0000000000000000 0x0
52 DR: 0000000000000000 0x0
53 TR: 0000000000000000 0x0
54 Cycle count: 4
55
56 50000.00ns INFO      cocotb.BC_I
57 ***** DUT Signals *****
58 50000.00ns INFO      cocotb.BC_I
59 PC: 000000001001    0x9
60 AR: 000000001001    0x9
61 IR: 0100000000001001 0x4009
62 AC: 0000000000000000 0x0
63 DR: 0000000000000000 0x0
64 TR: 0000000000000000 0x0
65 Cycle count: 5
66
67 60000.00ns INFO      cocotb.BC_I
68 ***** DUT Signals *****
69 60000.00ns INFO      cocotb.BC_I
70 PC: 000000001001    0x9
71 AR: 000000001001    0x9
72 IR: 0100000000001001 0x4009
73 AC: 0000000000000000 0x0
74 DR: 0000000000000000 0x0
75 TR: 0000000000000000 0x0
76 Cycle count: 6
77
78 70000.00ns INFO      cocotb.BC_I
79 ***** DUT Signals *****
80 70000.00ns INFO      cocotb.BC_I
81 PC: 000000001010    0xa
82 AR: 000000001001    0x9
83 IR: 1111000010000000 0xf080
84 AC: 0000000000000000 0x0
85 DR: 0000000000000000 0x0
86 TR: 0000000000000000 0x0
87 Cycle count: 7
88
89 80000.00ns INFO      cocotb.BC_I
90 ***** DUT Signals *****
91 80000.00ns INFO      cocotb.BC_I
92 PC: 000000001010    0xa
93 AR: 000010000000    0x80
94 IR: 1111000010000000 0xf080
95 AC: 0000000000000000 0x0
96 DR: 0000000000000000 0x0
97 TR: 0000000000000000 0x0
98 Cycle count: 8
99

```

```

100 90000.00ns INFO      cocotb.BC_I
101 ***** DUT Signals *****
102 90000.00ns INFO      cocotb.BC_I
103 PC: 000000001010      0xa
104 AR: 000010000000      0x80
105 IR: 1111000010000000 0xf080
106 AC: 0000000000000000 0x0
107 DR: 0000000000000000 0x0
108 TR: 0000000000000000 0x0
109 Cycle count: 9
110
111 00000.00ns INFO      cocotb.BC_I
112 ***** DUT Signals *****
113 00000.00ns INFO      cocotb.BC_I
114 PC: 000000001010      0xa
115 AR: 000000001010      0xa
116 IR: 1111000010000000 0xf080
117 AC: 0000000000000000 0x0
118 DR: 0000000000000000 0x0
119 TR: 0000000000000000 0x0
120 Cycle count: 10
121
122 10000.00ns INFO      cocotb.BC_I
123 ***** DUT Signals *****
124 10000.00ns INFO      cocotb.BC_I
125 PC: 000000001011      0xb
126 AR: 000000001010      0xa
127 IR: 1010000000000011 0xa003
128 AC: 0000000000000000 0x0
129 DR: 0000000000000000 0x0
130 TR: 0000000000000000 0x0
131 Cycle count: 11
132
133 20000.00ns INFO      cocotb.BC_I
134 ***** DUT Signals *****
135 20000.00ns INFO      cocotb.BC_I
136 PC: 000000001011      0xb
137 AR: 000000000011      0x3
138 IR: 1010000000000011 0xa003
139 AC: 0000000000000000 0x0
140 DR: 0000000000000000 0x0
141 TR: 0000000000000000 0x0
142 Cycle count: 12
143
144 30000.00ns INFO      cocotb.BC_I
145 ***** DUT Signals *****
146 30000.00ns INFO      cocotb.BC_I
147 PC: 000000001011      0xb
148 AR: 000000000010      0x2
149 IR: 1010000000000011 0xa003
150 AC: 0000000000000000 0x0
151 DR: 0000000000000000 0x0
152 TR: 0000000000000000 0x0
153 Cycle count: 13
154
155 40000.00ns INFO      cocotb.BC_I
156 ***** DUT Signals *****
157 40000.00ns INFO      cocotb.BC_I
158 PC: 000000001011      0xb
159 AR: 000000000010      0x2
160 IR: 1010000000000011 0xa003
161 AC: 0000000000000000 0x0
162 DR: 1010101010101010 0xaaaa
163 TR: 0000000000000000 0x0
164 Cycle count: 14
165
166 50000.00ns INFO      cocotb.BC_I
167 ***** DUT Signals *****
168 50000.00ns INFO      cocotb.BC_I
169 PC: 000000001011      0xb
170 AR: 000000000010      0x2
171 IR: 1010000000000011 0xa003
172 AC: 1010101010101010 0xaaaa
173 DR: 1010101010101010 0xaaaa
174 TR: 0000000000000000 0x0
175 Cycle count: 15
176
177 60000.00ns INFO      cocotb.BC_I
178 ***** DUT Signals *****
179 60000.00ns INFO      cocotb.BC_I
180 PC: 000000001011      0xb
181 AR: 000000000000      0x0
182 IR: 1010000000000011 0xa003
183 AC: 1010101010101010 0xaaaa
184 DR: 1010101010101010 0xaaaa
185 TR: 0000000000001011 0xb
186 Cycle count: 16
187
188 70000.00ns INFO      cocotb.BC_I
189 ***** DUT Signals *****
190 70000.00ns INFO      cocotb.BC_I
191 PC: 000000000000      0x0
192 AR: 000000000000      0x0
193 IR: 1010000000000011 0xa003
194 AC: 1010101010101010 0xaaaa
195 DR: 1010101010101010 0xaaaa
196 TR: 0000000000001011 0xb
197 Cycle count: 17
198

```

```

199 80000.00ns INFO      cocotb.BC_I
200 ***** DUT Signals *****
201 80000.00ns INFO      cocotb.BC_I
202 PC: 000000000001      0x1
203 AR: 000000000000      0x0
204 IR: 1010000000000011 0xa003
205 AC: 1010101010101010 0xaaaa
206 DR: 1010101010101010 0xaaaa
207 TR: 0000000000001011 0xb
208 Cycle count: 18
209
210 90000.00ns INFO      cocotb.BC_I
211 ***** DUT Signals *****
212 90000.00ns INFO      cocotb.BC_I
213 PC: 000000000001      0x1
214 AR: 000000000001      0x1
215 IR: 1010000000000011 0xa003
216 AC: 1010101010101010 0xaaaa
217 DR: 1010101010101010 0xaaaa
218 TR: 0000000000001011 0xb
219 Cycle count: 19
220
221 00000.00ns INFO      cocotb.BC_I
222 ***** DUT Signals *****
223 00000.00ns INFO      cocotb.BC_I
224 PC: 000000000010      0x2
225 AR: 000000000001      0x1
226 IR: 0100000000100000 0x4020
227 AC: 1010101010101010 0xaaaa
228 DR: 1010101010101010 0xaaaa
229 TR: 0000000000001011 0xb
230 Cycle count: 20
231
232
233
234
235
236
237
238
239 1090000.00ns INFO      cocotb.BC_I      BC I test ended successfully!
240 1090000.00ns INFO      cocotb.regression  basic_computer_test passed
241 *****
242 ** TEST                                STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
243 *****
244 ** cocotb_bcl_test.basic_computer_test  PASS      1090000.00      0.03  42585732.98 **
245 *****
246 ** TESTS=1 PASS=1 FAIL=0 SKIP=0          1090000.00      0.08  13741524.21 **
247 *****

```

## 4 Controller Design

The controller is designed with almost fully combinational parts except the needed Sequence Counter. Every output is calculated logically with assigned inputs. For debugging the last part of the commented code is used , it resides in Controller.v file. The design is fully taken from lecture notes. Every instruction is tested by me. Because of length of tests and their results only a part of it present in the report.