Basic Computer Design Report

Zafer Dogan Budak // 2515708

December 9, 2024

Contents

1 Introduction

This report documents the simulation and testing of a basic computer design. The assembly program that was executed and the first part of simulation results can be found in the following parts. For the full simulation results, please refer to the "test_res.txt".

2 Assembly Program

The assembly program used for the simulation is as follows:

Listing 1: Assembly Program

```
4009  // BUN 009
4020  // BUN
aaaa  // Data into AC
0002  // 002
c230
c230
c230
c230
ffff // IZS check
F080 // ION
a003 // IND LDA 003
7200 // CMA
7100 // CME
1003 // ADD 003
6008 // ISZ 008
0004 // AND 004
F040 // IOF
7080 // CIR
7040 // CIL
7800 // CLA
7400 // CLE
7020 // INC
7010 // SPA
7008 // SNA
7004 // SZA
7002 // SZE
7001 // HLT
0000
0000
0000
0000
0000
C000 // IND BUN get back to the adress before interrupt
0000
0000
```

3 Simulation Results

The simulation results generated by running the assembly program on the basic computer design are presented below:

Listing 2: Simulation Results

```
0.00ns INFO      cocotb.BC_I
********** DUT Signals ***************
0.00ns INFO      cocotb.BC_I
PC: 000000000000          0x0
AR: 000000000000          0x0
IR: 0000000000000000      0x0
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 0

10000.00ns INFO      cocotb.BC_I
********** DUT Signals ***************
10000.00ns INFO      cocotb.BC_I
PC: 000000000000          0x0
AR: 000000000000          0x0
IR: 0000000000000000      0x0
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 1

20000.00ns INFO      cocotb.BC_I
********** DUT Signals ***************
20000.00ns INFO      cocotb.BC_I
PC: 000000000001          0x1
AR: 000000000000          0x0
IR: 0100000000001001      0x4009
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 2

30000.00ns INFO      cocotb.BC_I
********** DUT Signals ***************
30000.00ns INFO      cocotb.BC_I
PC: 000000000001          0x1
AR: 000000001001          0x9
IR: 0100000000001001      0x4009
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 3

40000.00ns INFO      cocotb.BC_I
********** DUT Signals ***************
40000.00ns INFO      cocotb.BC_I
PC: 000000000001          0x1
AR: 000000001001          0x9
IR: 0100000000001001      0x4009
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 4

50000.00ns INFO      cocotb.BC_I
********** DUT Signals ***************
50000.00ns INFO      cocotb.BC_I
PC: 000000001001          0x9
AR: 000000001001          0x9
IR: 0100000000001001      0x4009
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 5

60000.00ns INFO      cocotb.BC_I
********** DUT Signals ***************
60000.00ns INFO      cocotb.BC_I
PC: 000000001001          0x9
AR: 000000001001          0x9
IR: 0100000000001001      0x4009
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 6

70000.00ns INFO      cocotb.BC_I
********** DUT Signals ***************
70000.00ns INFO      cocotb.BC_I
PC: 000000001010          0xa
AR: 000000001001          0x9
IR: 1111000010000000      0xf080
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 7

80000.00ns INFO      cocotb.BC_I
********** DUT Signals ***************
80000.00ns INFO      cocotb.BC_I
PC: 000000001010          0xa
AR: 000010000000          0x80
IR: 1111000010000000      0xf080
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 8

```

```
90000.00ns INFO     cocotb.BC_I
********** DUT Signals ***************
90000.00ns INFO     cocotb.BC_I
PC: 000000001010          0xa
AR: 000010000000          0x80
IR: 1111000010000000      0xf080
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 9

00000.00ns INFO     cocotb.BC_I
********** DUT Signals ***************
00000.00ns INFO     cocotb.BC_I
PC: 000000001010          0xa
AR: 000000001010          0xa
IR: 1111000010000000      0xf080
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 10

10000.00ns INFO     cocotb.BC_I
********** DUT Signals ***************
10000.00ns INFO     cocotb.BC_I
PC: 000000001011          0xb
AR: 000000001010          0xa
IR: 1010000000000011      0xa003
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 11

20000.00ns INFO     cocotb.BC_I
********** DUT Signals ***************
20000.00ns INFO     cocotb.BC_I
PC: 000000001011          0xb
AR: 000000000011          0x3
IR: 1010000000000011      0xa003
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 12

30000.00ns INFO     cocotb.BC_I
********** DUT Signals ***************
30000.00ns INFO     cocotb.BC_I
PC: 000000001011          0xb
AR: 000000000010          0x2
IR: 1010000000000011      0xa003
AC: 0000000000000000      0x0
DR: 0000000000000000      0x0
TR: 0000000000000000      0x0
Cycle count: 13

40000.00ns INFO     cocotb.BC_I
********** DUT Signals ***************
40000.00ns INFO     cocotb.BC_I
PC: 000000001011          0xb
AR: 000000000010          0x2
IR: 1010000000000011      0xa003
AC: 0000000000000000      0x0
DR: 1010101010101010      0xaaaa
TR: 0000000000000000      0x0
Cycle count: 14

50000.00ns INFO     cocotb.BC_I
********** DUT Signals ***************
50000.00ns INFO     cocotb.BC_I
PC: 000000001011          0xb
AR: 000000000010          0x2
IR: 1010000000000011      0xa003
AC: 1010101010101010      0xaaaa
DR: 1010101010101010      0xaaaa
TR: 0000000000000000      0x0
Cycle count: 15

60000.00ns INFO     cocotb.BC_I
********** DUT Signals ***************
60000.00ns INFO     cocotb.BC_I
PC: 000000001011          0xb
AR: 000000000000          0x0
IR: 1010000000000011      0xa003
AC: 1010101010101010      0xaaaa
DR: 1010101010101010      0xaaaa
TR: 0000000000001011      0xb
Cycle count: 16

70000.00ns INFO     cocotb.BC_I
********** DUT Signals ***************
70000.00ns INFO     cocotb.BC_I
PC: 000000000000          0x0
AR: 000000000000          0x0
IR: 1010000000000011      0xa003
AC: 1010101010101010      0xaaaa
DR: 1010101010101010      0xaaaa
TR: 0000000000001011      0xb
Cycle count: 17
```

```
80000.00ns INFO     cocotb.BC_I
*********** DUT Signals ***************
80000.00ns INFO     cocotb.BC_I
PC: 000000000001          0x1
AR: 000000000000          0x0
IR: 1010000000000011      0xa003
AC: 1010101010101010      0xaaaa
DR: 1010101010101010      0xaaaa
TR: 0000000000001011      0xb
Cycle count: 18

90000.00ns INFO     cocotb.BC_I
*********** DUT Signals ***************
90000.00ns INFO     cocotb.BC_I
PC: 000000000001          0x1
AR: 000000000001          0x1
IR: 1010000000000011      0xa003
AC: 1010101010101010      0xaaaa
DR: 1010101010101010      0xaaaa
TR: 0000000000001011      0xb
Cycle count: 19

00000.00ns INFO     cocotb.BC_I
*********** DUT Signals ***************
00000.00ns INFO     cocotb.BC_I
PC: 000000000010          0x2
AR: 000000000001          0x1
IR: 0100000000100000      0x4020
AC: 1010101010101010      0xaaaa
DR: 1010101010101010      0xaaaa
TR: 0000000000001011      0xb
Cycle count: 20


                                                    .
                                                    .
                                                    .
                                                    .


1090000.00ns INFO     cocotb.BC_I                    BC I test ended successfully!
1090000.00ns INFO     cocotb.regression              basic_computer_test passed
*******************************************************************************************
** TEST                                 STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
*******************************************************************************************
** cocotb_bc1_test.basic_computer_test   PASS     1090000.00           0.03    42585732.98  **
*******************************************************************************************
** TESTS=1 PASS=1 FAIL=0 SKIP=0                  1090000.00           0.08    13741524.21  **
*******************************************************************************************
```

4 Controller Design

The controller is designed with almost fully combinational parts except the needed Sequence Counter. Every output is calculated logically with assigned inputs. For debugging the last part of the commented code is used , it resides in Controller.v file. The design is fully taken from lecture notes. Every instruction is tested by me. Because of length of tests and their results only a part of it present in the report.