East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design
Expt No.: 2
Title: Design and Implementation of a Combinational Circuit

Objectives:
1. To design a combinational circuit from descriptive problem specification.
2. To implement a combinational circuit using AND-OR and OR-AND logic.

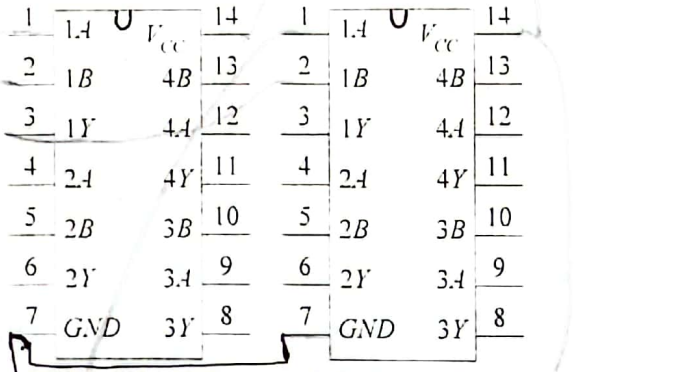
Theory:
The design procedure of a combinational circuit is discussed in Section 6.2 of Textbook 1. Students are advised to go through the above section of the Textbook 1 before preparing the pre-lab report.

Pre-Lab Report Questions:
Problem specification: In a combinational logic circuit, four input lines A, B, C, and D are being used to represent a 4-bit binary number with A as the MSB and D as the LSB. The circuit produces a high (logic 1) output only when the binary number is greater than 0101_2.

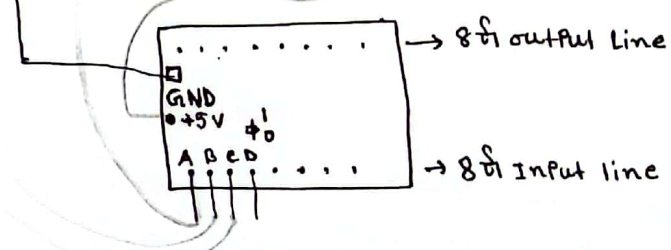
1. Prepare a truth table for the given combinational circuit. Represent the truth table in a 4-variable K-map.
2. Write simplified sum of products function from the K-map. Draw the AND-OR logic diagram for the simplified sum of products function.
3. Write simplified product of sums function from the K-map. Draw OR-AND logic diagram for the simplified product of sums function.

ICs Required:
7408 Quadruple 2-input AND gates
7432 Quadruple 2-input OR gates

Pin Diagram of the Required ICs:



7408 (4 2-In AND) 7432 (4 2-In OR)



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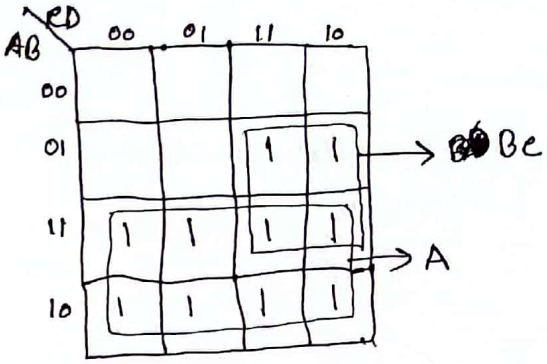
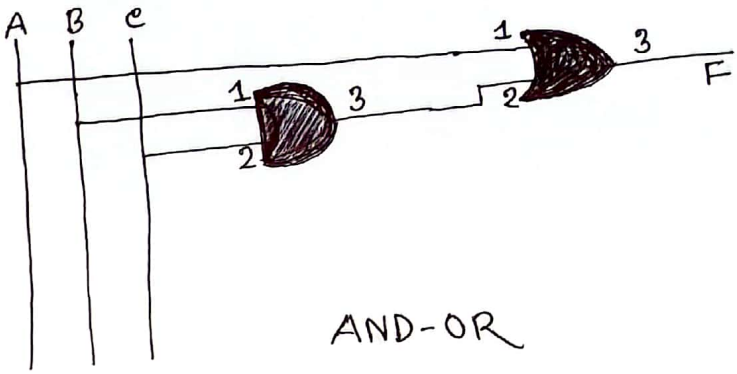
LAB-02

Truth table:

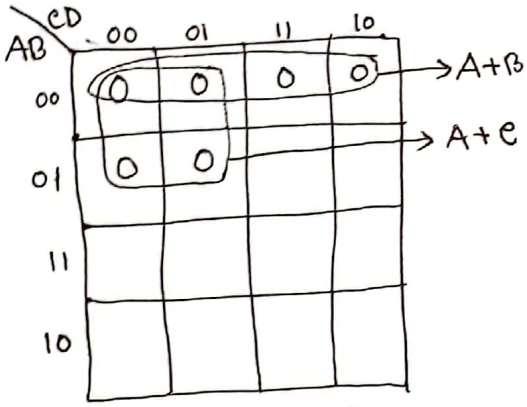
ABCD	F
0000	0
0001	0
0010	0
0011	0
0100	0
0101	0
0110	1
0111	1
1000	1
1001	1
1010	1
1011	1
1100	1
1101	1
1110	1
1111	1



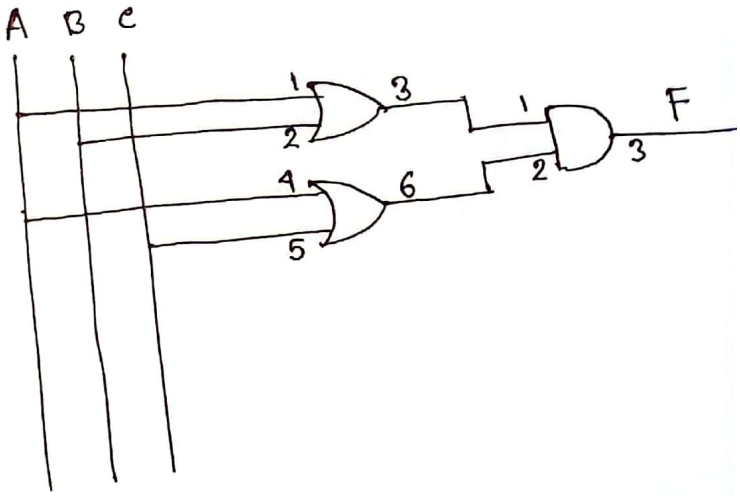
$F = A + Bc$



AND-OR



$F = (A+B)(A+C)$



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East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design
Expt No.: 4
Title: Binary Adder and Subtractor

Objectives:

1. To implement and test a full adder using discrete gates.
1. To implement and test a 4-bit 2's complement adder/subtractor using IC 7483 (4-bit binary parallel adder).

Theory:

Design of full-adder using discrete gates is discussed in Section 7.2 of textbook. The IC 7483 (4-bit binary parallel adder) is introduced in Section 7.8 of textbook. Design of a 4-bit 2's complement adder/subtractor using a 4-bit binary parallel adder is discussed in Section 7.6 of textbook.

Pre-Lab Report Questions:

Implementing and testing a full adder using discrete gates:

1. Draw the logic diagram of a full-adder using EXOR gates.
2. Write the truth table of a full-adder.

Implementing and testing a 4-bit 2's complement adder/subtractor using IC 7483 (4-bit binary parallel adder):

3. Draw the schematic diagram for implementing a 4-bit 2's complement adder/subtractor using IC 7483 (4-bit binary parallel adder). Write the operation of the circuit explaining how the mode selector input M determines the mode of operations as adder or subtractor.

2's complement addition and subtraction:

4. Perform the following 2's complement additions and subtractions using 4-bit data: লিখে আনতে হবে।

3 + 3	3 – 2
3 + 4	3 – 3
3 + 5 (overflow)	3 – 4

ICs Required:

7408 Quadruple 2-input AND gates
7432 Quadruple 2-input OR gates
7486 Quadruple 2-input EXOR gates
7483 4-bit binary parallel adder

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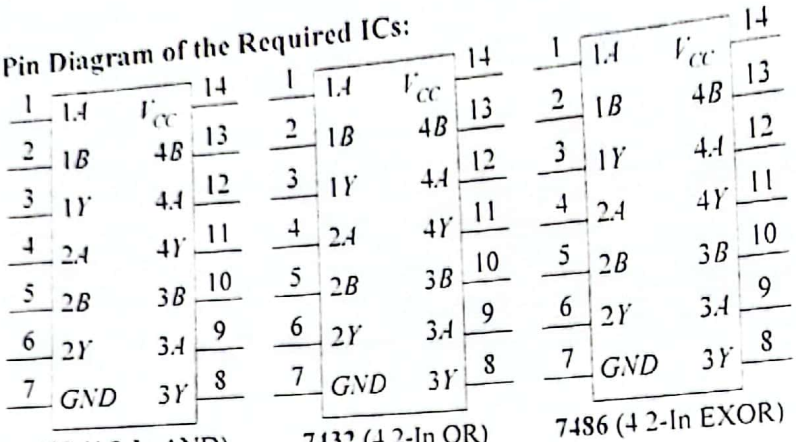
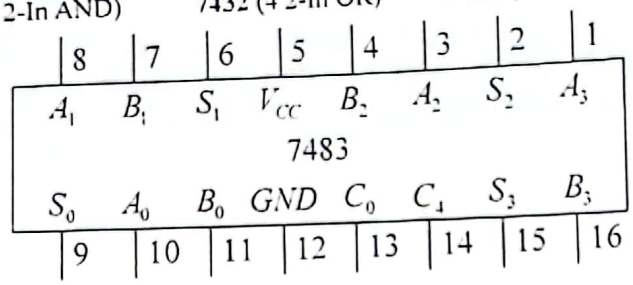
Pin Diagram of the Required ICs:



7408 (4 2-In AND) 7432 (4 2-In OR) 7486 (4 2-In EXOR)



Lab Procedure:

Implementing and testing a full adder using random gates:

1. Construct the logic diagram for a full-adder from your pre-lab report on the breadboard. Connect the three inputs of the circuit to three data switches and two outputs to two LED indicators.
2. Show the outputs of the circuit to your instructor.

Implementing and testing a 4-bit 2's complement adder/subtractor using IC 7483 (4-bit binary parallel adder):

3. Construct the schematic diagram for a 4-bit 2's complement adder/subtractor using IC 7483 from your pre-lab report. Connect the four A inputs to a fixed binary number 0011 (decimal 3) to two data switches and the four B inputs to four data switches. Connect the mode select input M to a data switch. Connect the four sum outputs S and carry output C_4 to five LED indicators.
4. Perform the following addition/subtraction operations.

3 + 3	3 – 2
3 + 4	3 – 3
3 + 5 (overflow)	3 – 4

5. Show the outputs of the circuit to your instructor.

Post-Lab Report Questions:

1. Write structural Verilog code for full-adder circuit form your pre-lab report and simulate it using Quartus II software.
2. Write behavioral Verilog code for a 4-bit parallel adder and simulate it using Quartus II software.

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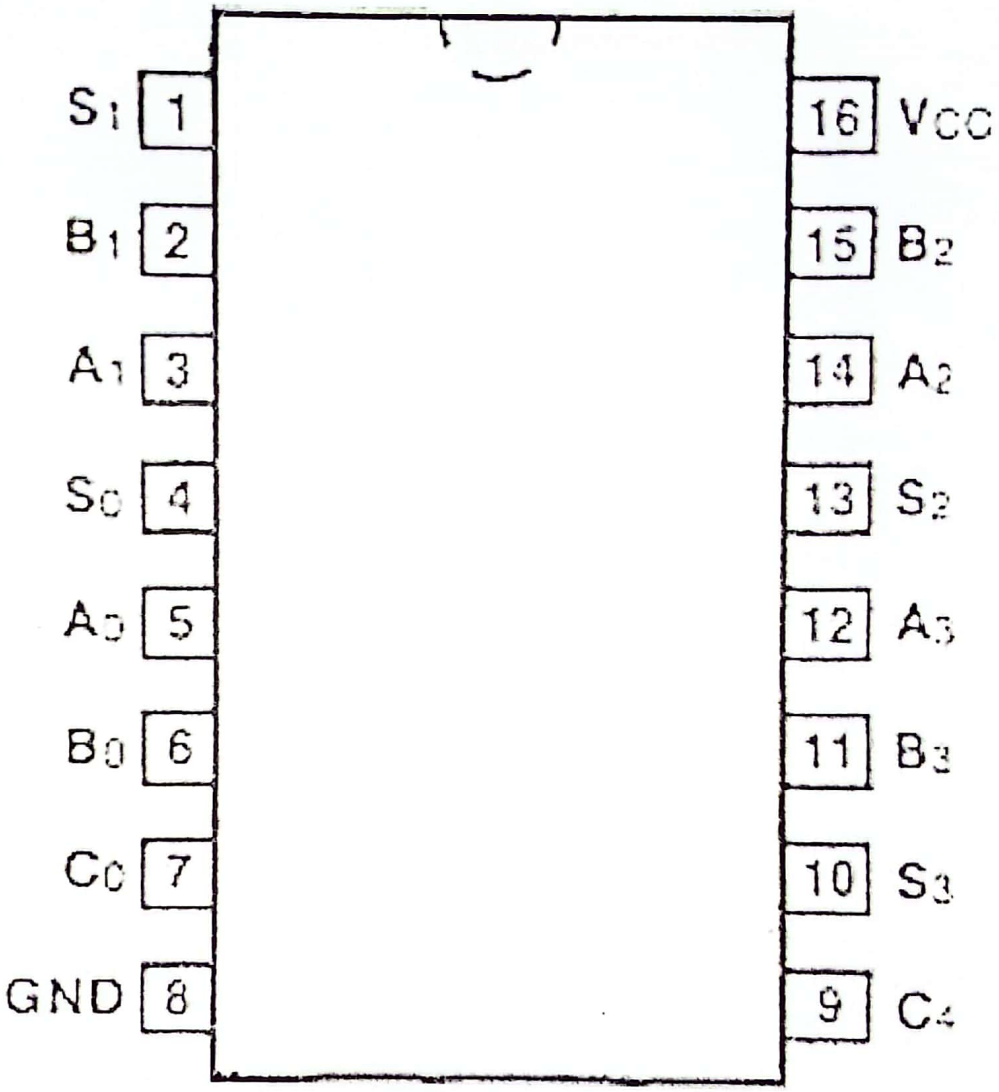
Pin Diagram of 74283



Adder

Expt-9

PreLab-4

Name: Saikat Sudipta Shuva
ID: 2020-2-60-167
CSE 345 section: 03

Date: 30-03-23

4. Perform the following 2's complement additions and subtractions using 4-bit data:

✓ i. 3+3

+3 → 0011
+3 → 0011

+6 → 0110

ii) +3+4

+3 → 0011
+4 → 0100

+7 → 0111

✓ iii) 3+5

+3 → 0011
+5 → 0101

+8 → 1000 [overflow]

$(-8)_{10} \rightarrow (1000)_2$

✓ iv) 3-2

= 3+(-2)

2 → 0010 $\xrightarrow{2's}$ 1110 = (-2)

2 2 8 4 0

+3 → 0011
-2 → 1110

+1 → 10001
Discard

v) 3-3

$= 3 + (-3)$

$3 \rightarrow 0011 \xrightarrow{2'S} 1101 = (-3)$

$+3 \rightarrow 0011$

$-3 \rightarrow 1101$

$0 \rightarrow 10000$

Discard

vi) 3-4

$= 3 + (-4)$

$4 \rightarrow 0100 \xrightarrow{2'S} 1100 = (-4)$

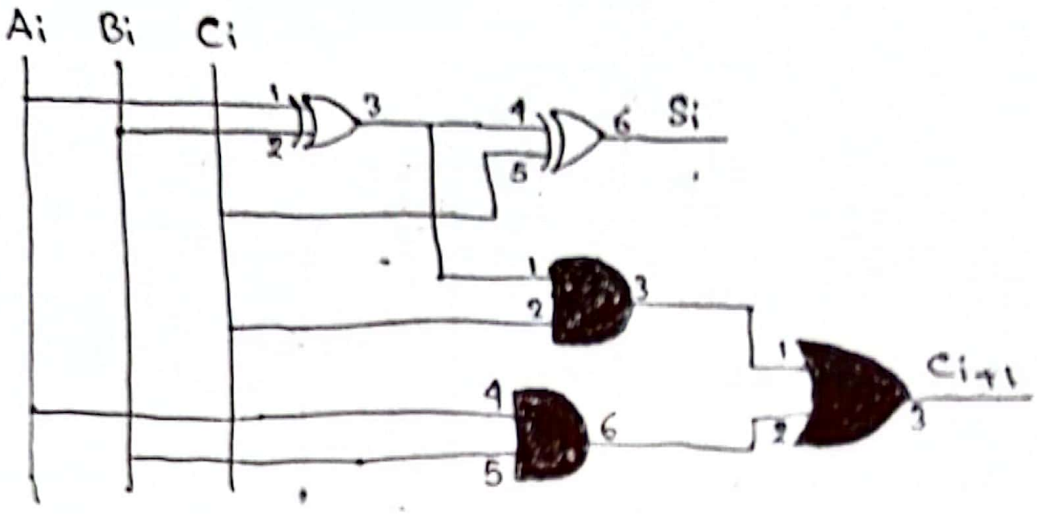
$+3 \rightarrow 0011$

$-4 \rightarrow 1100$

$-1 \rightarrow 1111$

$A_i \oplus B_i \oplus C_i$

$C_{i+1} = (A_i \oplus B_i) C_i + A_i B_i$



Truthtable:

Ai Bi Ci	C_{i+1}	S_i
000	0	0
001	0	1
010	0	1
011	1	0
100	0	1
101	1	0
110	1	0
111	1	1

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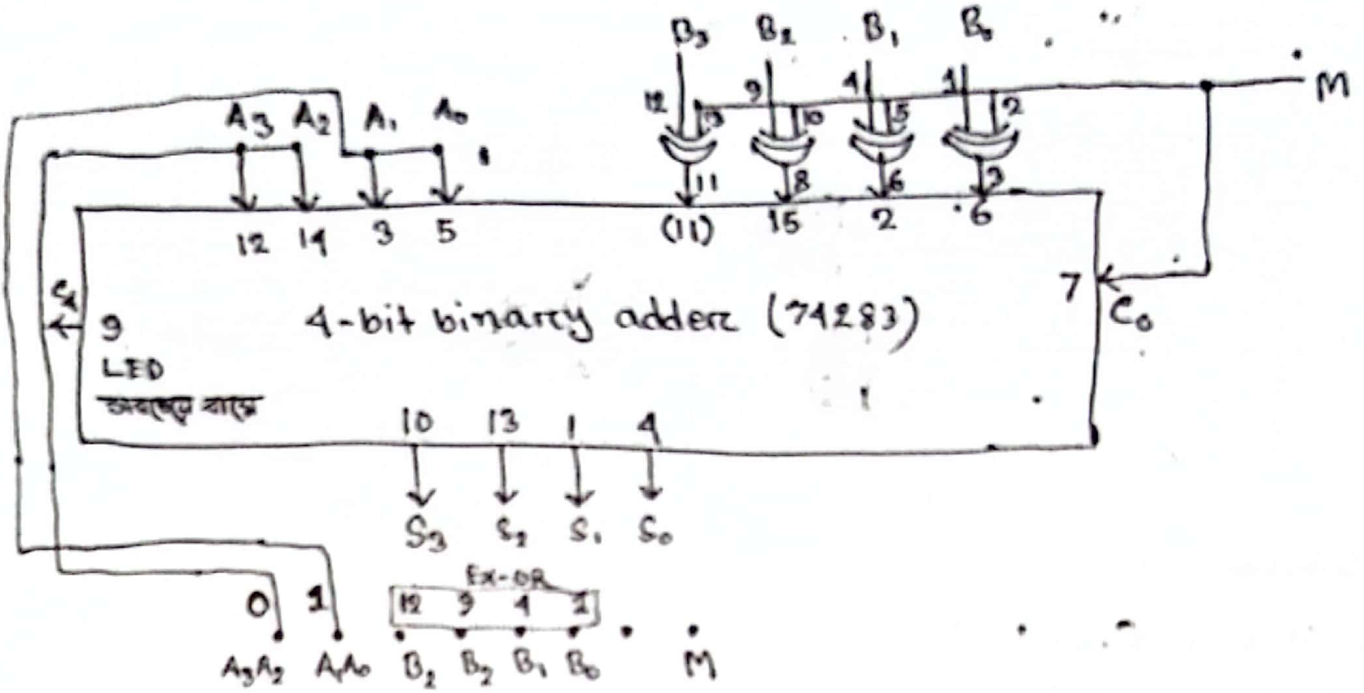
B3 B2 B1 B0
M
A3 A2 A1 A0
12 14 3 5
(11) 15 2 6
4-bit binary adder (74283)
9
LED
10 13 1 4
S3 S2 S1 C0
7
C0
Ex-OR
0 1
A3A2 A1A0 B2 B2 B1 B0 M

East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design
Expt No.: 5
Title: Decoder and Its Use in Combinational Logic Implementation

Objectives:

1. To implement and test a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input using random gates.
1. To implement and test combinational logic functions using IC 74138 (3-to-8-lines decoder with active-LOW outputs).

Theory:

Design of decoders using random gates is discussed in Section 8.3 of textbook 1. The IC 74138 (3-to-8-line decoder with active-LOW outputs) is introduced in Section 8.3 of textbook 1. Combinational logic implementation using decoders is also discussed in Section 8.3 of textbook 1.

Pre-Lab Report Questions:

Implementing and testing a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input using random gates:

1. Draw the logic diagram for a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input.
2. Write the truth table of the above decoder.

Implementing and testing combinational logic functions using the IC 74138 (3-to-8-lines decoder with active-LOW outputs):

3. Draw the schematic diagram for implementing the following two combinational logic functions using the IC 74138 (3-to-8-lines decoder with active-LOW outputs).

$$F_1(A,B,C) = \sum(1,2,4,7)$$
$$F_2(A,B,C) = \sum(0,5,6,7)$$

Binary Bit হিসেবে Input দিতে হবে।

ICs Required:

7404 Hex Inverters (NOT gates)
7410 Triple 3-input NAND gates
7420 Dual 4-input NAND gates
74138 3-to-8-line decoder with active-LOW outputs

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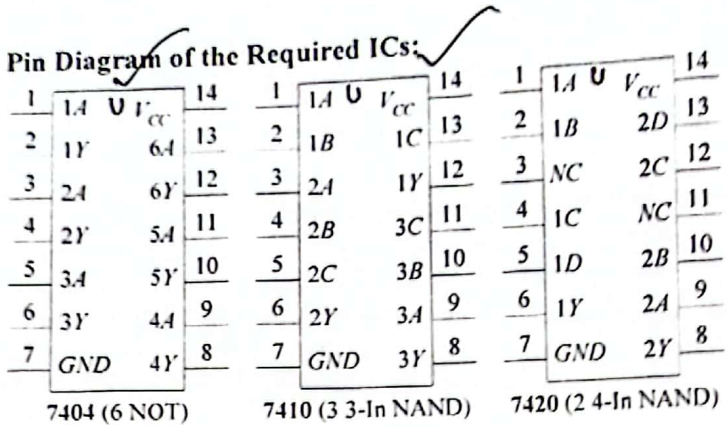
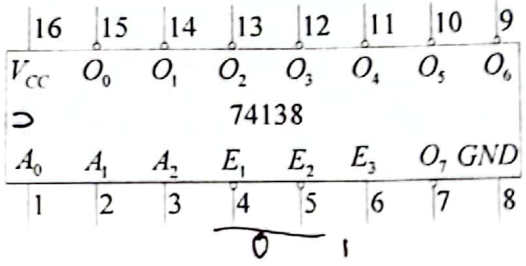
Pin Diagram of the Required ICs:



7404 (6 NOT) 7410 (3 3-In NAND) 7420 (2 4-In NAND)

→ No Connection.



Decoder

4, 5 number pin কে একি করে 0 input দিতে হবে।
6 " n কে 1 input এ "

Lab Procedure:

Implementing and testing a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input using random gates:

1. Construct the logic diagram for a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input from your pre-lab report using random gates. Connect the three inputs (A_1, A_0, and E) of the circuit to three data switches and four outputs to four LED indicators.
2. Apply binary 00 to 11 to A_1A_0 address inputs and observe the outputs by changing E enable input. Verify the operation.

Implementing and testing combinational logic functions using the IC 74138 (3-to-8-lines decoder with active-LOW outputs):

3. Construct the circuits for implementing the given combinational logic functions from your pre-lab report. Connect enable inputs E_1 and E_2 to fixed 0s and E_3 to a data switch. Use E_3 as active-HIGH enable input. Connect the input lines ABC ($A_2A_1A_0$) to three data switches. Connect the two function outputs to two LED indicators.
4. Prepare the truth tables of the circuit and verify that it implements the two given combinational logic functions.

Post-Lab Report Questions:

1. Verify that all experimental outputs agree with your pre-lab report.
2. Write structural Verilog code for the logic diagram for a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input from your pre-lab report and simulate it using Quartus II software.
3. Write behavioral Verilog code for 3-to-8-lines decoder with active-LOW outputs and simulate it using Quartus II software.

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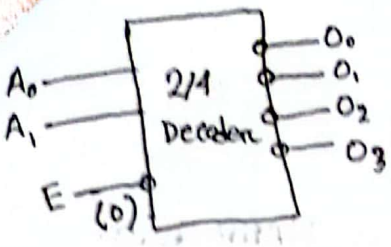
Expt-5

...ierc: 2 to 1

Adderc-Subtrcactorc – 1টি
Encoderc-decoderc – 2টি



Active-Low Enable Input and Active Low outputs.

Inputs			outputs			
E	A_1	A_0	O_3	O_2	O_1	O_0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

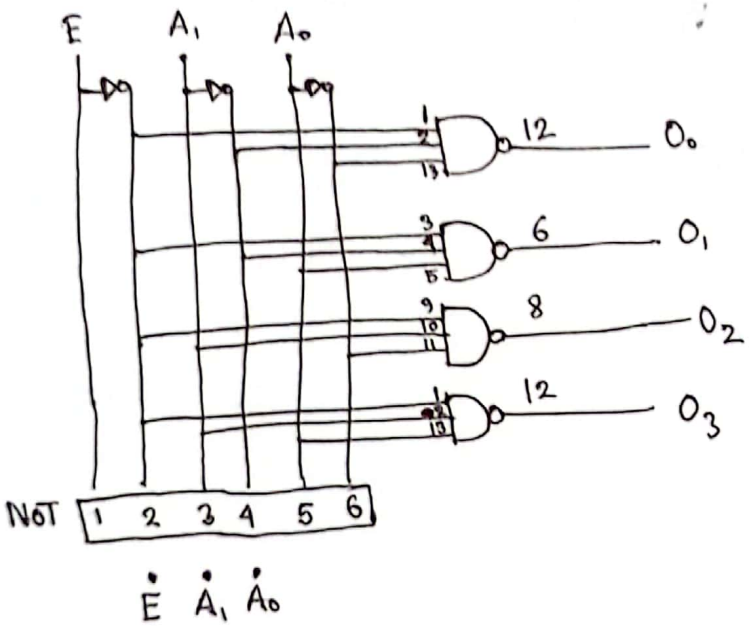
$O_0 = E + A_1 + A_0 = (E'A_1'A_0')'$

$O_1 = E + A_1 + A_0' = (E'A_1'A_0)'$

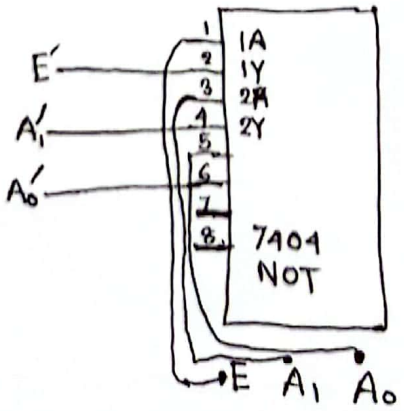
$O_2 = E + A_1' + A_0 = (E'A_1A_0')'$

$O_3 = E + A_1' + A_0' = (E'A_1A_0)'$

*3 input এর 2টি NAND Ic লাগবে।



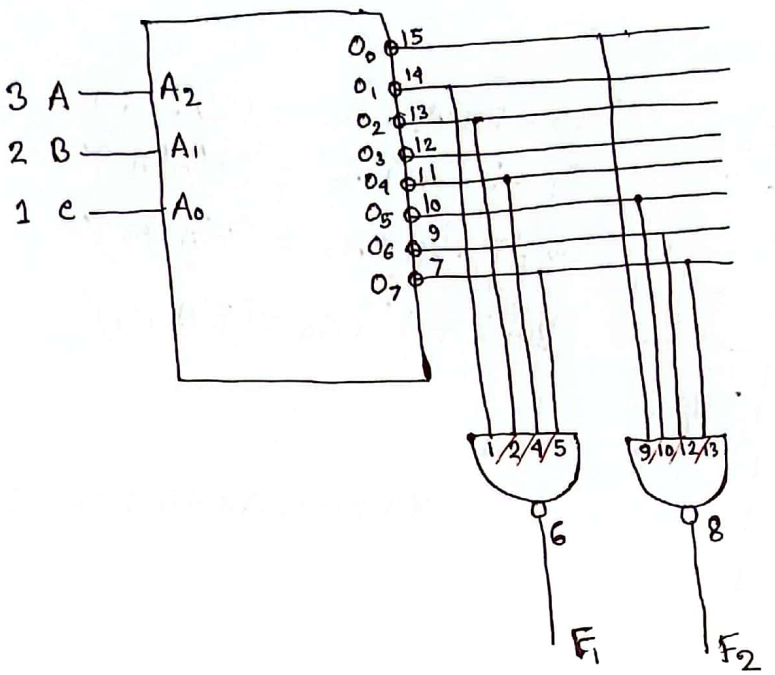
output
O_3 O_2 O_1 O_0



Decoder দিয়ে Function Implementation:

$F_1(A,B,C) = \Sigma(1,2,4,7)$

$F_2(A,B,C) = \Sigma(0,5,6,7)$



4 input NAND লাগবে।

Decoder এর 14 থেকে NAND এর 1
" " 13 " NAND " 2
" " 11 " " " 4
" " 7 " " " 5

E_3, E_4 শর্ট করে 0 তে connect করতে হবে।

3 2 1
A B C
A_2 A_1 A_0

Decoder এ যাবে।
Fixed হবে।

East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design
Expt No.: 6
Title: Multiplexer and Its Use in Combinational Logic Implementation

Objectives:

1. To implement and test a 4-to-1-line multiplexer with active-LOW enable input using random gates.
2. To implement and test combinational logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input).

Theory:

Design of multiplexers using random gates is discussed in Section 8.7 of textbook 1. The IC 74151 (8-to-1-line multiplexer with active-LOW enable input) is introduced in Section 8.7 of textbook 1. Combinational logic implementation using multiplexers is also discussed in Section 8.7 of textbook 1.

Pre-Lab Report Questions:

Implementing and testing a 4-to-1-line multiplexer with active-LOW enable input using random gates:

1. Write the truth table of a 4-to-1-line multiplexer with active-LOW enable input.
2. Draw the logic diagram of a 4-to-1-line multiplexer with active-LOW enable input using random gates.

Implementing and testing combinational logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input):

3. Prepare the implementation table for implementing the combinational logic function $F(A,B,C,D) = \sum(0,3,4,6,8,11,13,15)$ using an 8-to-1-line multiplexer.
4. Draw the logic diagram for implementing the above logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input).

ICs Required:

7404 Hex Inverters (NOT gates)
7421 Double 4-input AND gates
7432 Quadruple 2-input OR gates
74151 8-to-1-line multiplexer with active-LOW enable input

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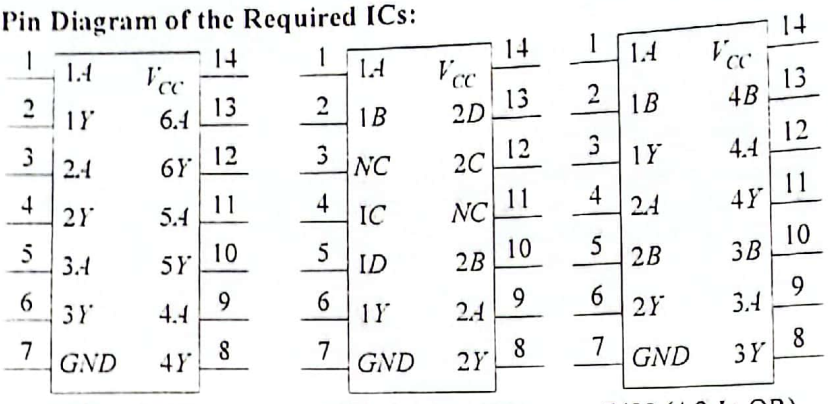
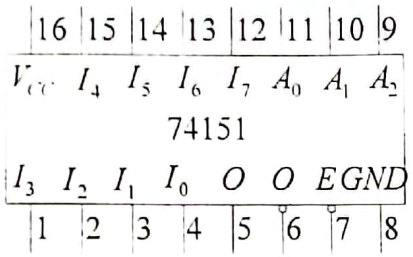
Pin Diagram of the Required ICs:



7404 (6 NOT) **7421** (2 4-In AND) **7432** (4 2-In OR)



Lab Procedure:

Implementing and testing a 4-to-1-line multiplexer with active-LOW enable input using random gates:

1. Construct the logic diagram for a 4-to-1-line multiplexer with active-LOW enable input from your pre-lab report using random gates. Connect the four data inputs I_0 through I_3 to an arbitrary 4-bit binary number. Connect A_1, A_0, and E to three switches and the output O to an LED indicator.
2. Apply binary 00 to 11 to address lines A_1A_0 and observe the outputs by changing E input. Check that, when the circuit is enabled, the output is equal to the selected data input. Prepare the observed truth table indicating the inputs applied.

Implementing and testing combinational logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input):

3. Construct the logic diagram for implementing the logic function $F(A,B,C,D) = \sum(0,3,4,6,8,11,13,15)$ from your pre-lab report using IC 74151 (8-to-1-line multiplexer with active-LOW enable input).
4. Prepare the truth table of the circuit and verify that it implements the given combinational logic function.

Post-Lab Report Questions:

1. Verify that all experimental outputs agree with your pre-lab report.
2. Write structural Verilog code for the logic diagram for a 4-to-1-line multiplexer with active-LOW enable input from your pre-lab report and simulate it using Quartus II software.
3. Write behavioral Verilog code for a 4-to-1-line multiplexer with active-LOW enable input and simulate it using Quartus II software.

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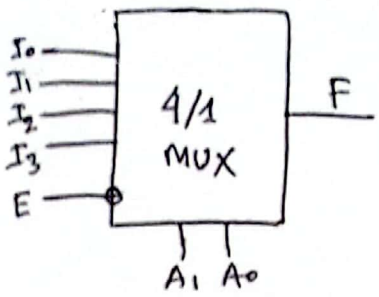
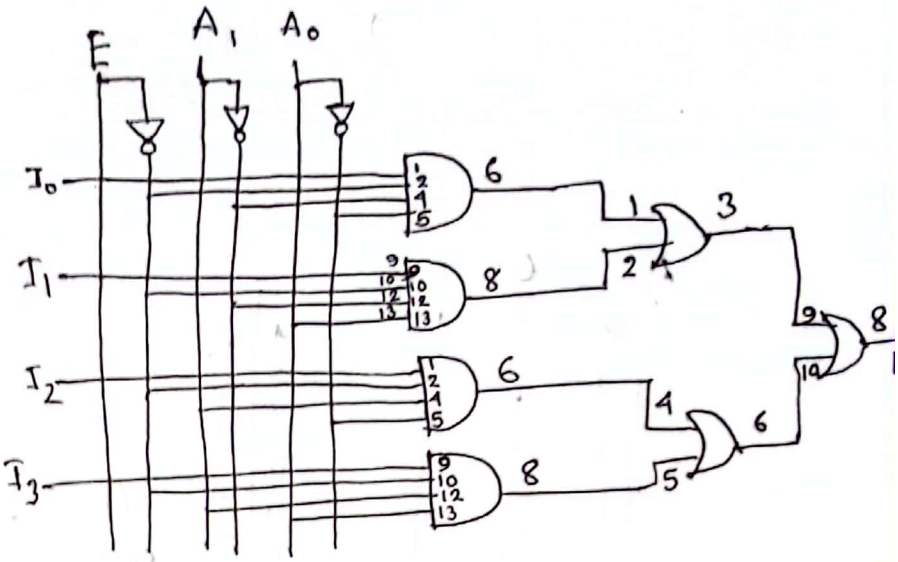
Lab-6

7421 IC দুইটি লাগবে (4 input AND)



E	A_1	A_0	O
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



$F = I_0 E' A_1' A_0' + I_1 E' A_1' A_0 + I_2 E' A_1 A_0' + I_3 E' A_1 A_0$

E A_1 A_0 I_0 I_1 I_2 I_3

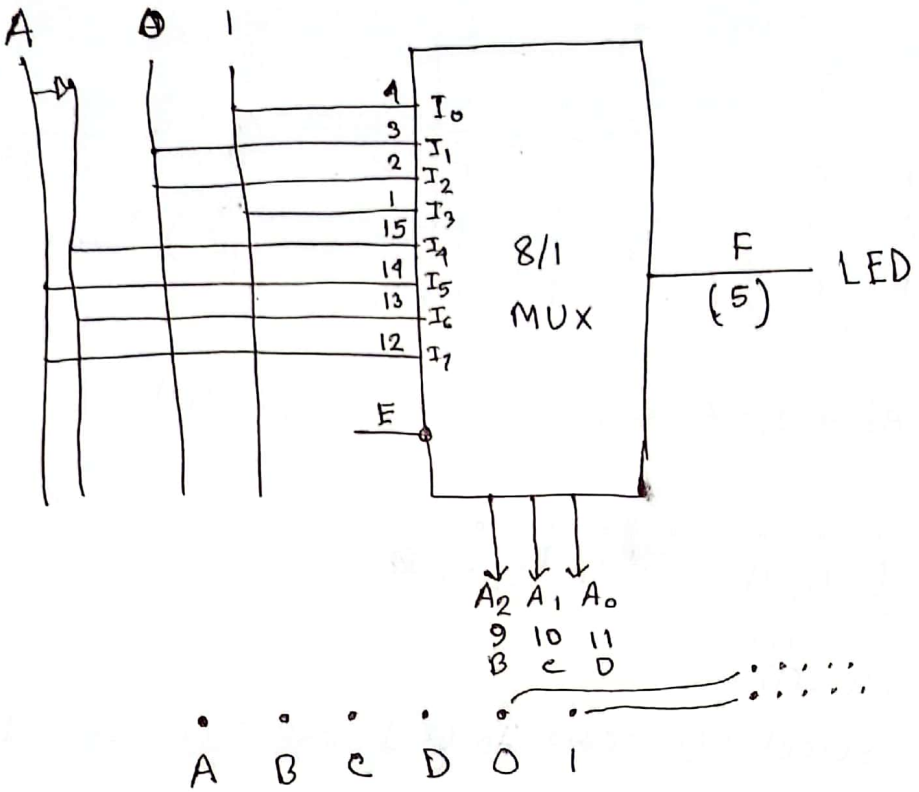
(3টিকে Not করতে হবে)

* 000 নিলে I_0 select হবে এজন্য I_0 কে 1 করতে হবে। $I_0 = 1$ দিলে LED জ্বলবে।

* $F(A,B,C,D) = \Sigma(0,3,4,6,8,11,13,15)$ এগুলোর জন্য LED জ্বলবে।

Implementation table:

A'	(0)	1	2	(3)	(4)	5	(6)	7
A	(8)	9	10	(11)	12	(13)	14	(15)
	1	0	0	1	A'	A	A'	A



0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111