KAUNAS UNIVERSITY OF TECHNOLOGY

THE FIRST PRINCIPLES OF DIGITAL LOGIC

Laboratory work 4: Counters

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KAUNAS, 2022

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1- Assignment:

Assignment	Initial Value	Increment	M1	Final value
8	2	2	8	16

2- Objective:

To draw a truth table, design the schematic and run the simulation of a counter that has an initial value of 2, increment by 2, a final value of 16 and M1 is equals to 8,
To draw a truth table of the next state of the M1.
To design a schematic for a counter M1 combined with M1.
To design a modified schematic for M1 with the implementation of FPGA.

3-Procedure:

2;2;16	Q4	Q3	Q2	Q1	Q0
2	0	0	0	1	0
4	0	0	1	0	0
6	0	0	1	1	0
8	0	1	0	0	0
10	0	1	0	1	0
12	0	1	1	0	0
14	0	1	1	1	0
16	1	0	0	0	0

Figure 1. Truth table for final value 16 with initial value and increment by 2.

Truth Table for the next state:

	Q4	Q3	Q2	Q1	Q0
4	0	0	1	0	0
6	0	0	1	1	0
8	0	1	0	0	0
10	0	1	0	1	0
12	0	1	1	0	0
14	0	1	1	1	0
16	1	0	0	0	0
2	0	0	0	1	0

Figure 2. Truth table for the next state for final value 16 with initial value and increment by 2.

We did the truth table for a 5-bit universal register, and afterwards we did Karnaugh maps for each bit. designed its schematic that perform the following operations.

d0=0

d1	00	01	11	10
00				1
01	1			1
11				
10	1			

d1= !q2 !q1 + !q4 q2 !q1

Figure 3. Karnaugh map of the bit d1.

d2	00	01	11	10
00		1		1
01		1		1
11				
10				

d2= !q4 (q2 XOR q1)

Figure 4. Karnaugh map of the bit d2.

d3	00	01	11	10
00			1	
01	1	1		1
11				
10				

d3= !q4 q3 (!q2 + !q1) + !q4 !q3 q2 q1

Figure 5. Karnaugh map of the bit d3.

d4	00	01	11	10
00				
01			1	
11				
10				

d4= !q4 q3 q2 q1

Figure 6. Karnaugh map of the bit d4.

After drawing the truth table and the K-maps, we designed its schematic that perform the following operations.

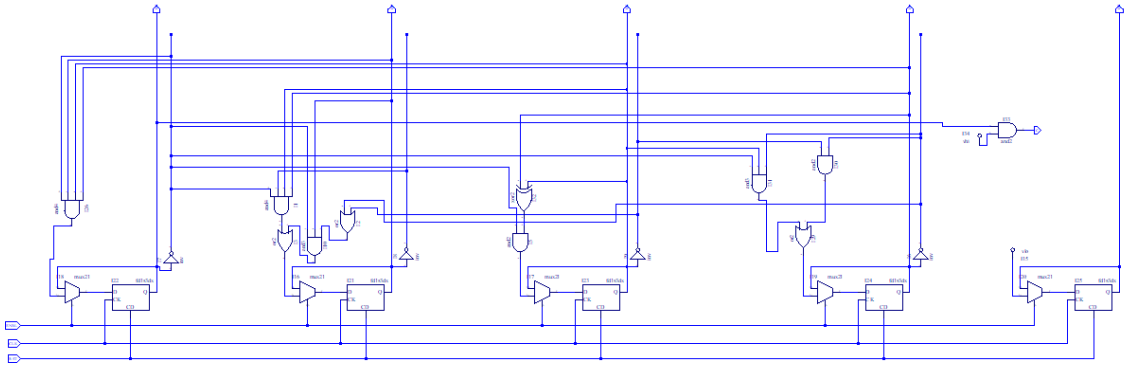

Figure 7. Schematic of a counter, final value 16 with initial value and increment by 2.

Afterwards, we change the properties of the project to VHDL, then we design a schematic for a counter M1 combined with M1.

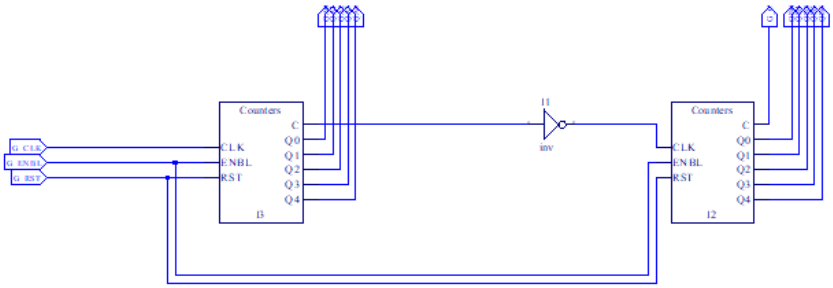

Figure 8. Schematic of a counter M1 combined with M1.

And then we run the simulation. We remove unwanted signals and set our clock, reset to 1 and enable to 0, we run the simulation, then we force the reset 0 and enable to 1, and then we run the simulation multiple times until the carry signal do a rising edge on the final value 16.

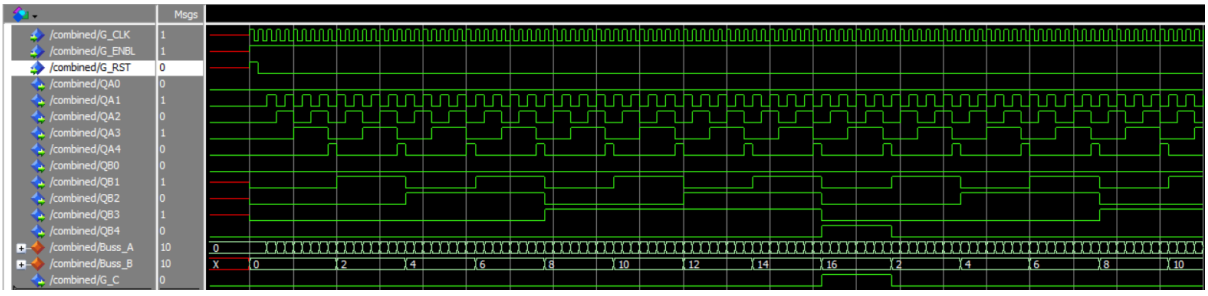

Figure 9. Timing Diagram of the counter M1 combined with M1.

FPGA Implementation:

We must do some minor modification for our circuits to function on FPGA board. The list of modifications is provided below. All the outputs must be inverted, Asynchronous reset signal must be inverted since we are working with asynchronous.

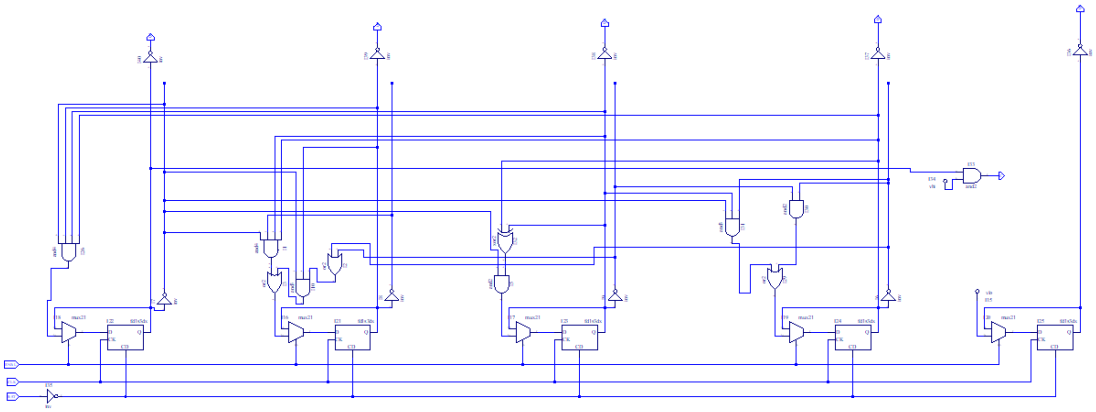

Figure 10. Modified schematic of the counter M1 combined with M1.

Now we need to generate a JEDEC file. It is done in Process tab, by double-clicking the JEDEC label. Once we have a design adapted to FPGA, we need to assign IO in your circuit to physical IO ports on the FPGA boards.

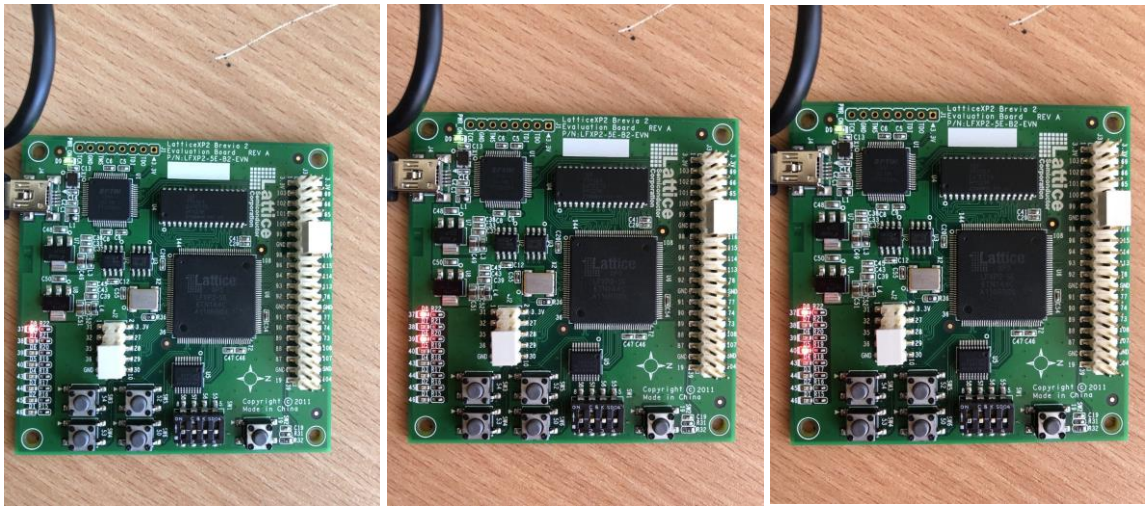

Figure 11. Results of FPGA.

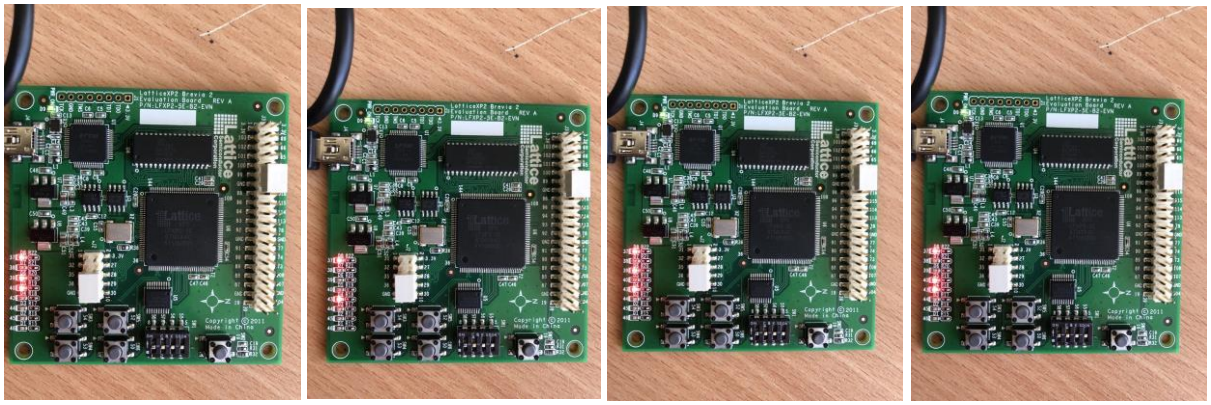

Figure 12. Results of FPGA.

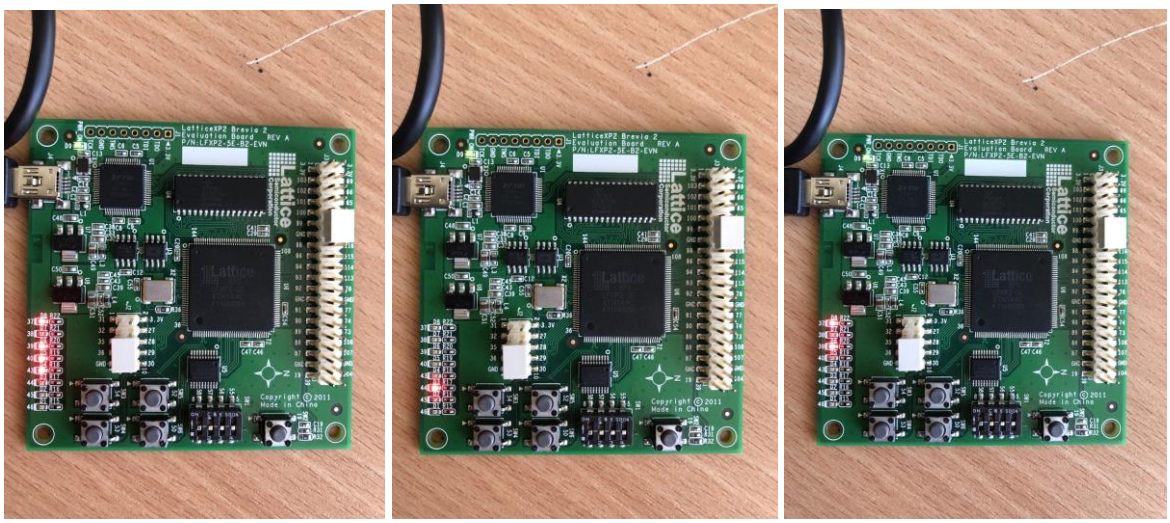

Figure 13. Results of FPGA.

4-Conclusion:

In this Laboratory work, we have drawn a truth table, a next state truth table and designed the schematic of a 5-bit Counter that has an initial value of 2 while incrementing by 2 with a final value of 16 and M1 has a value of 8. So, we can conclude that the counter is used in digital electronics for **counting purpose**, they can count specific event happening in the circuit. In addition, we were able to manually edit the functions of each and every button of a Lattice XP2, which is designed with LatticeXP2 FPGAs, therefore, to be able to count a specific event.