KAUNAS UNIVERSITY OF TECHNOLOGY

THE FIRST PRPICNICPLES OF DIGITAL LOGIC

Laboratory work 1: Digital feedbackless circuits

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1. Assignment:

#353:
0,2,5,11,21,27,28,31,40,46,47,51,52,53,57,60,61,62

2. Objective:

Familiarise with combinational and sequential digital logic circuits, and the analogue-digital interface. Know the representation of basic gates and digital electronic components. Understand Boolean algebra and be able to convert verbal descriptions of requirements into Boolean notation. Understand the need to simplify logic functions and reduce them to use specific gate types; be able to use Boolean algebra and Karnaugh maps to achieve these tasks.

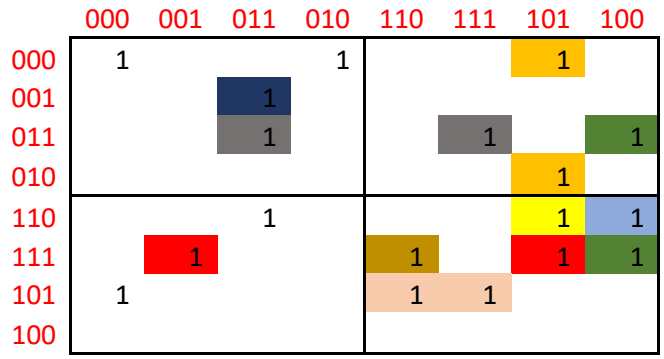
3. Procedure:
3.1 Truth Table:

Truth table is a table where the combination of values taken by their logical variables. A logic function is created, which the designed circuit must produce. This function can be presented as a truth table for the given the sequence of number, which is going to be represented in the minimized equation and tested in the schemes, is 0,2,5,11,21,27,28,31,40,46,47,51,52,53,57,60,61,62. Firstly, each number will be presented in binary by the truth table.

X5	X4	X3	X2	X1	X0	
32	16	8	4	2	1	
0	0	0	0	0	0	0
0	0	0	0	1	0	2
0	0	0	1	0	1	5
0	0	1	0	1	1	11
0	1	0	1	0	1	21
0	1	1	0	1	1	27
0	1	1	1	0	0	28
0	1	1	1	1	1	31
1	0	1	0	0	0	40
1	0	1	1	1	0	46
1	0	1	1	1	1	47
1	1	0	0	1	1	51
1	1	0	1	0	0	52
1	1	0	1	0	1	53
1	1	1	0	0	1	57
1	1	1	1	0	0	60
1	1	1	1	0	1	61
1	1	1	1	1	0	62

3.2 K-Maps

When every number is converted into the binary system, they can be implemented into the Karnaugh map. The Karnaugh map method is where the function is minimized, to achieve a minimal form. This form can be further rearranged, as to simplify logic gate design.



3.3 Calculation
For 1st Part Diagram:

X5	X4	X3	X2	X1	X0	
0	-	1	0	1	1	!X5X3!X2X1X0
0	1	1	-	1	1	!X5X4X3X1X0
0	0	0	0	-	0	!X5!X4!X3!X2!X0
1	1	-	1	0	-	X5X4X2!X1
0	-	0	1	0	1	!X5!X3X2!X1X0
-	1	1	1	0	0	X4X3X2!X1!X0
1	-	1	1	1	0	X5X3X2X1!X0
1	0	1	1	1	-	X5!X4X3X2X1
1	1	1	-	0	1	X5X4X3!X1X0
1	1	0	0	1	1	X5X4!X3!X2X1X0
1	0	1	0	0	0	X5!X4X3!X2!X1!X0

By the help of Karnaugh map, there can be applied minimization of the initial expression, so sum of the binary can be merged and then converted into the combination of the variables and by using the axiom of Boolean algebra, the combinations can be represented as the expression:

!X5 (X3!X2X1X0 + X4X3X1X0 + !X4!X3!X2!X0) +
X2!X1 (X5X4 + !X5!X3X0 + X4X3!X0) +
X5X3 (X2X1!X0 + !X4X2X1 + X4!X1X0) +
X5!X2 (X4!X3X1X0 + !X4X3!X1!X0

Now, this obtained expression can be used to create the 1st Part Diagram scheme.

For 2nd Part Diagram: Application of DeMorgan's law:

After running the schematic and obtaining the correct results of the assignment given, DeMorgan's law can be applied by simply applying the same schematic but replacing AND and OR gates by NAND Gates.

For 3rd Part Diagram: Mux41:

D0, D2, D1, D3 are equals to the sum of the presented combinations. Before applying them into the scheme, they can be minimized by Karnaugh maps:

	00	01	11	10
00	1			1
01		1		
11				
10			1	

(F=00)

!X3!X2!X0 + !X3X2!X1X0 + X3!X2X1X0

	00	01	11	10
00				
01		1		
11	1		1	
10			1	

(F=01)

X3X2!X1!X0 + !X3X2!X1X0 + X3X1X0

	00	01	11	10
00				
01				
11			1	1
10	1			

(F=10)

X3!X2!X1!X0 + X3X2X1

	00	01	11	10
00			1	
01	1	1		
11	1	1		1
10		1		

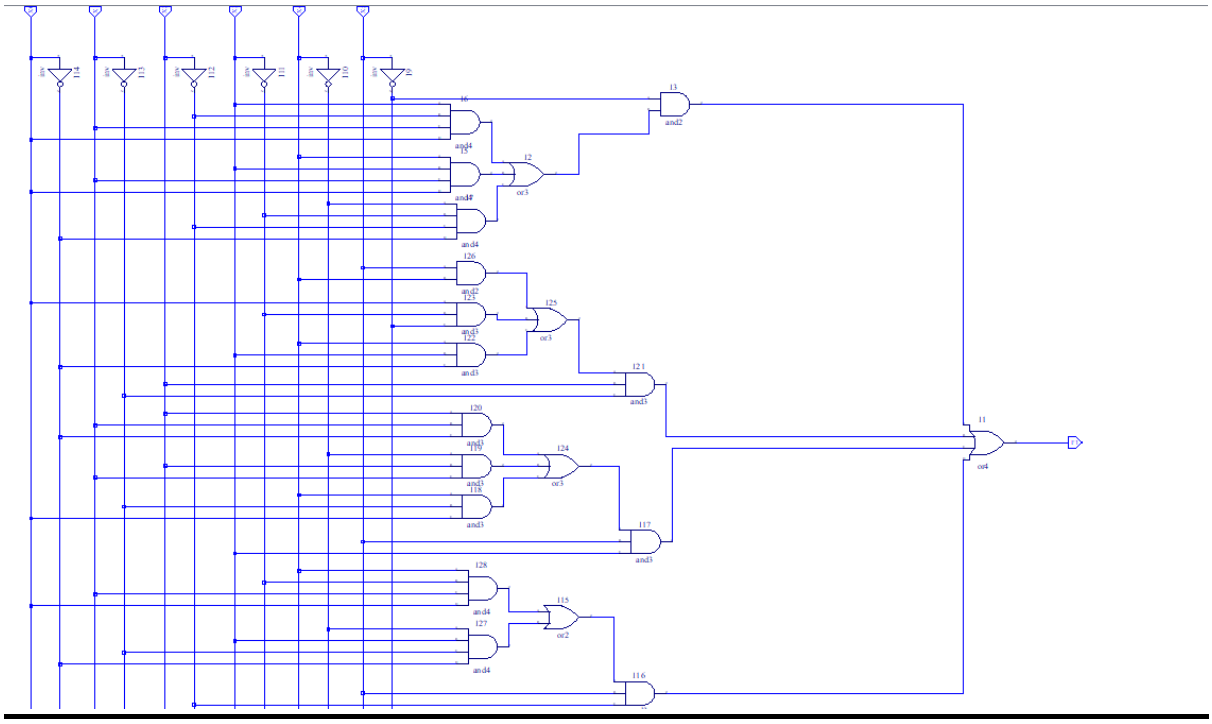
(F=11)

X2!X1 + !X3!X2X1X0 + X3X2!X0 + X3!X1X0

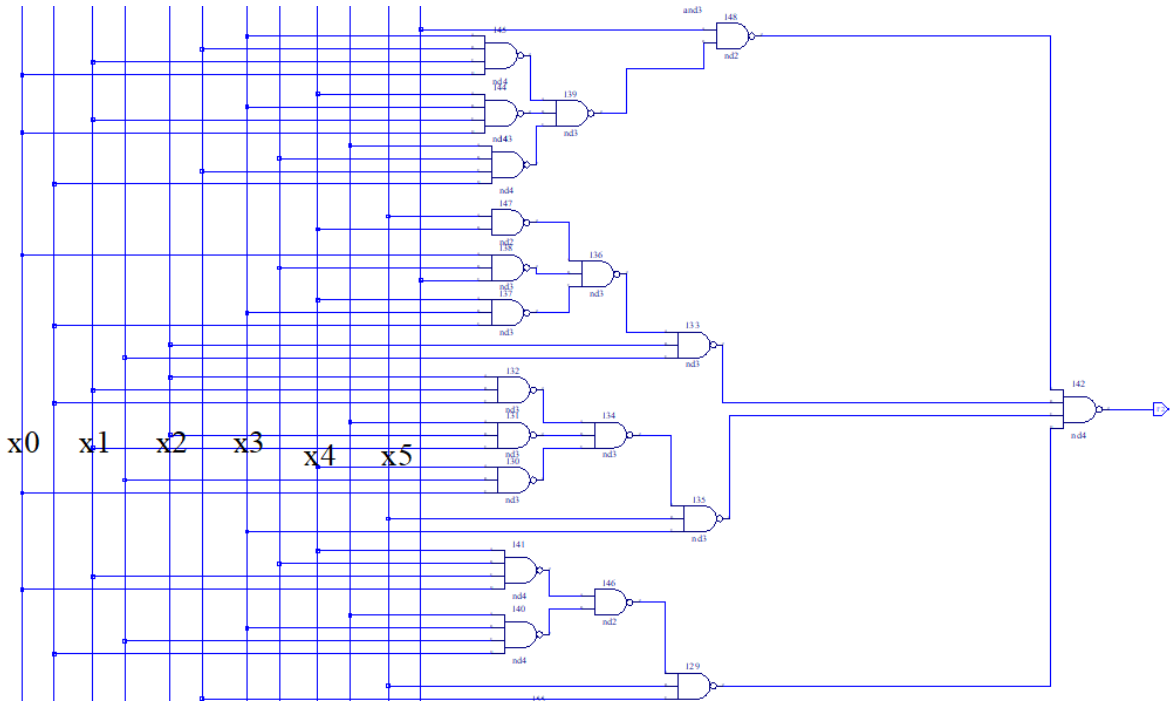
By use of uniting law, four expressions can be written from the Karnaugh maps. Now, the scheme of each expression can be made and connect to the multiplexer.

4. Schematic Diagrams:

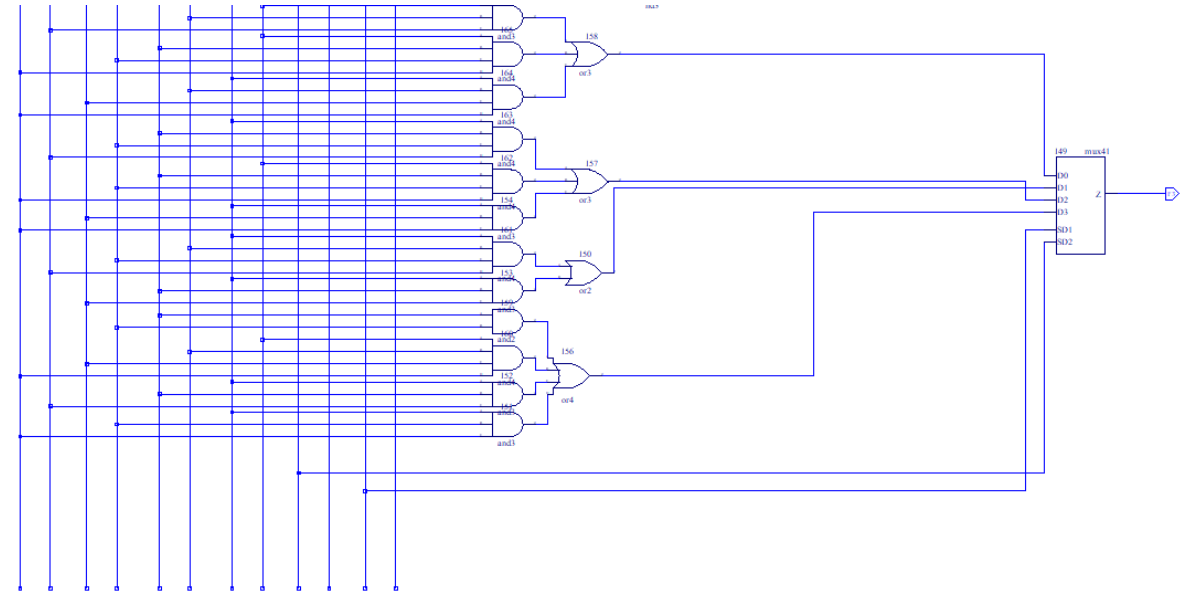
4.1 1st Part Diagram:



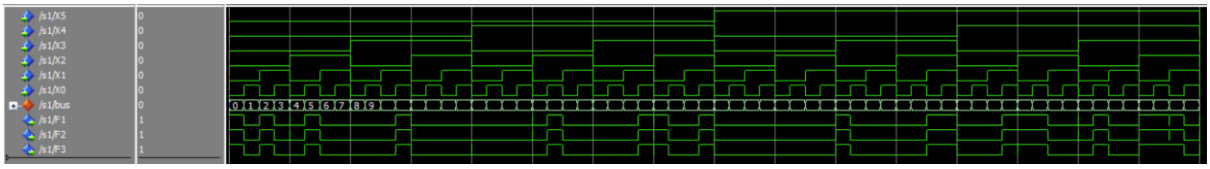
2nd Part Diagram: Application of DeMorgan's law:



For 3rd Part Diagram: Mux41:



5. Results:



6. Conclusion:

In this Laboratory work we were able to familiarise with combinational and sequential digital logic circuits, and the analogue-digital interface. We were able to represent schematics and the corresponding gates and digital electronic components. In addition, we were able to understand the Boolean algebra and we to convert verbal descriptions of requirements into Boolean notation. We were able understand the need to simplify logic functions and reduce them to use specific gate types; In addition, we were able to use Boolean algebra and Karnaugh maps to achieve these tasks. And since the result we obtained was the same as the data in the truth table, our truth table and Karnaugh map were created without errors. Using the test, we conclude that all three schematics are operational.