KAUNAS UNIVERSITY OF TECHNOLOGY

THE FIRST PRINCIPLES OF DIGITAL LOGIC

Laboratory work 2: LATCHES AND FLIP-FLOPS

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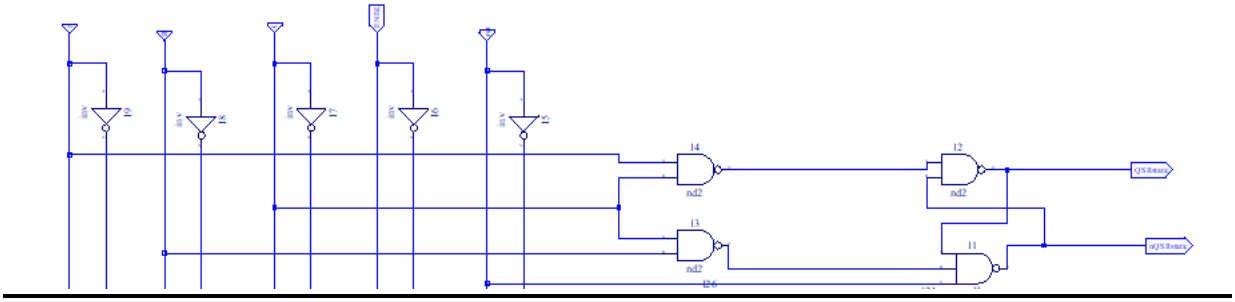
1. Assignment: SR Flip-Flop Figure 3.14 a C1 C2

2. Objective:

Constructing the schematics of the circuit of an SR gated latch, SR master-slave gated latch, a SR Flip-Flop and a circuit using D flip-flop from elements library (use fd1sdx from Lattice Diamond). And determining the functionality of the circuit.

3. Procedure:

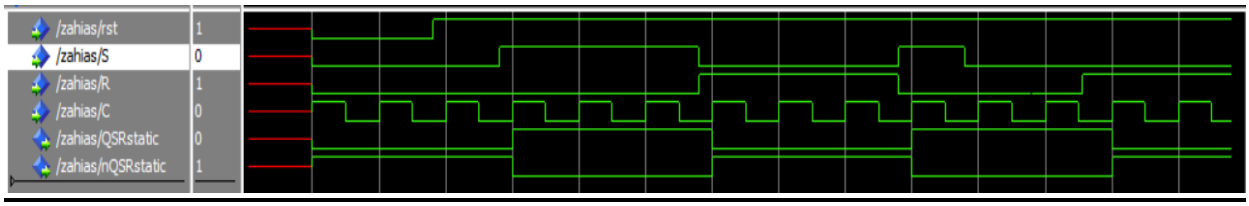
We start by designing a SR gated latch with a reset input, which resets the latch to a known state ('0'). From the outset, there should be a clock signal for the fact that the circuit works when the clock is high. At that point Q_SR_Static begins when the S signal beginnings and finishes when the R signal beginnings. when there is no R signal, Q_SR_Static will end in the Reset(rst) signal.



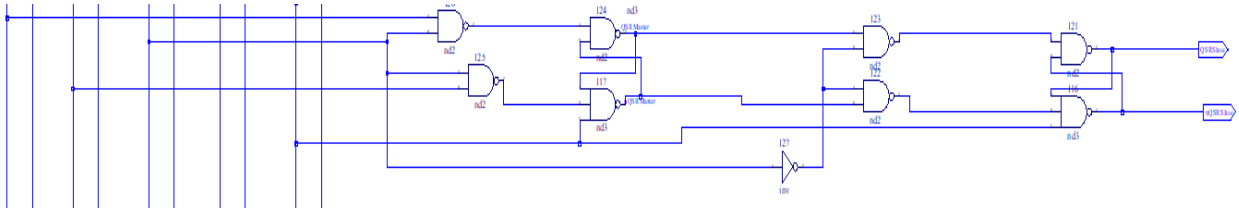
The functionality of the latch is described by the SR latch truth table:

R	S	Q_{t+1}	Action
0	0	Q_t	Hold state
1	0	0	Set logic 0
1	1	x	Restricted
0	1	1	Set logic 1

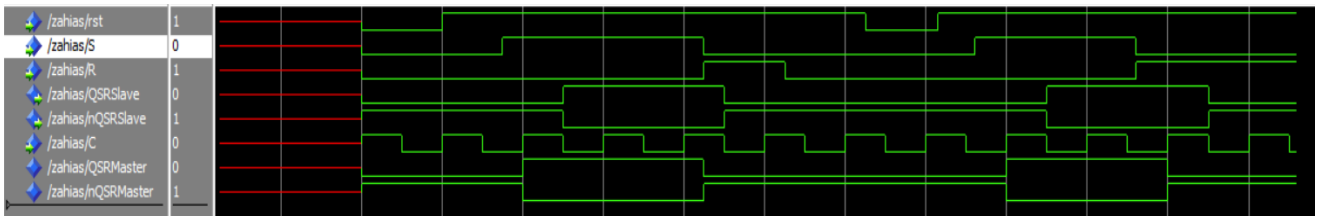
After a simulation time of 200 ns, we get the timing diagrams:



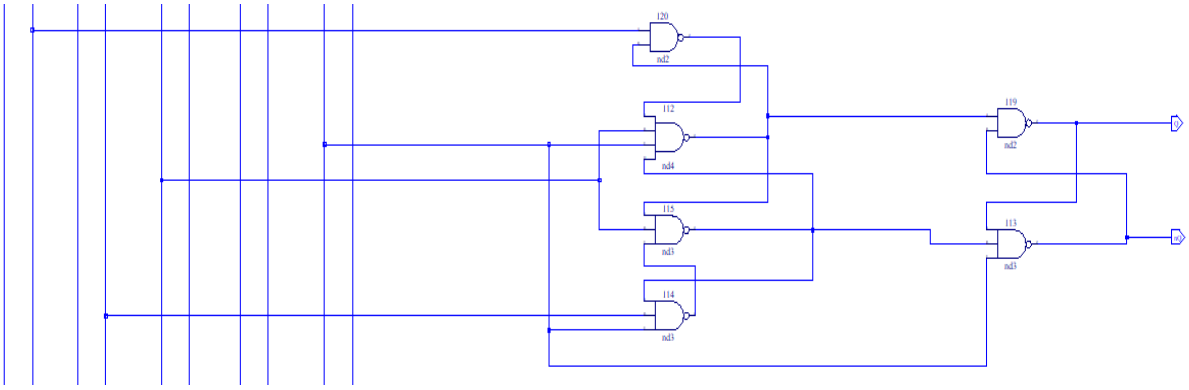
Now we must design a Master-Slave type SR latch.



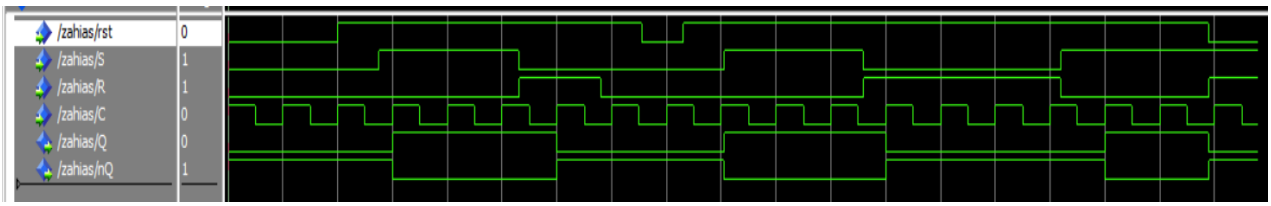
Master slave comprises of two interconnected circuits: Master and slave. Q_SR_Slave and nQ_SR_Slave are signs of the Master-Slave latch. At the point when C is 1, the Master circuit works yet the slave does not work. The slave begins working when C is 0 and works till when C will be again 0. Q_SR_Slave signal starts from the falling edge that matches with S and finishes in likewise again falling edge that matches with R.
Once a test is designed, we get the following simulation results:



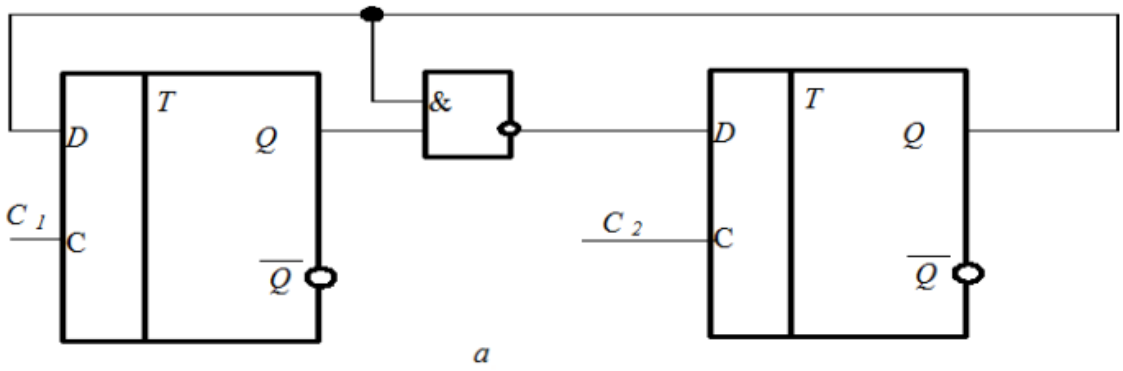
After that, we should design the SR Flip-Flop.



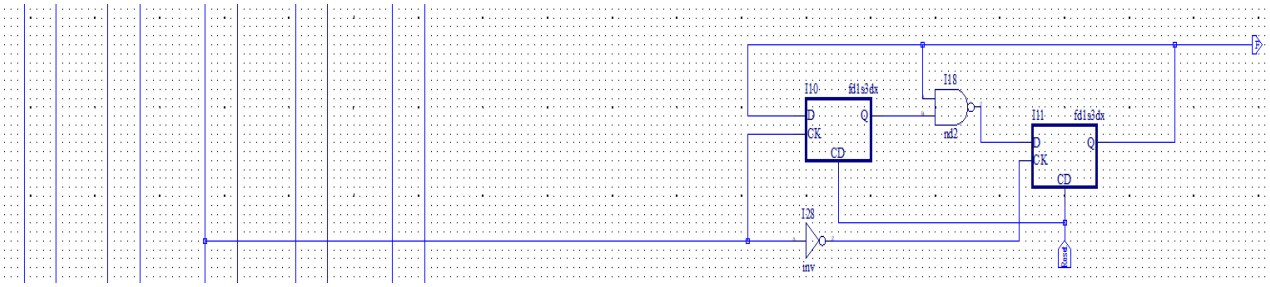
Q and nQ are the output signals of flip flop. Schematic is connected to our initial inputs. Q starts when clock signal C and Set signal S is high, and it finishes when reset signal is low.



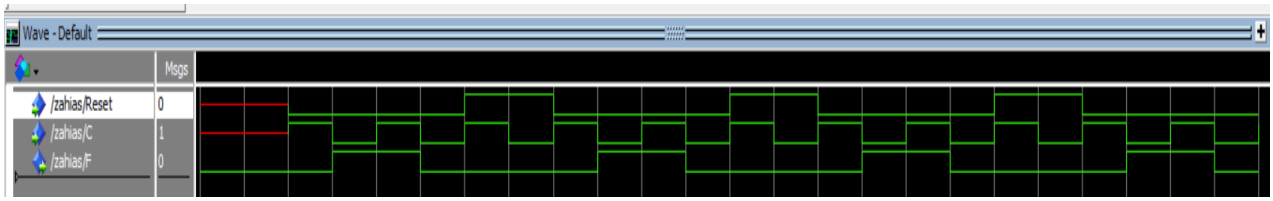
For designing the schematic shown in fig 3.14a, we shall use D type flip-flop from elements library. The C input of the circuit is connected to a single source, according to the work assignment.



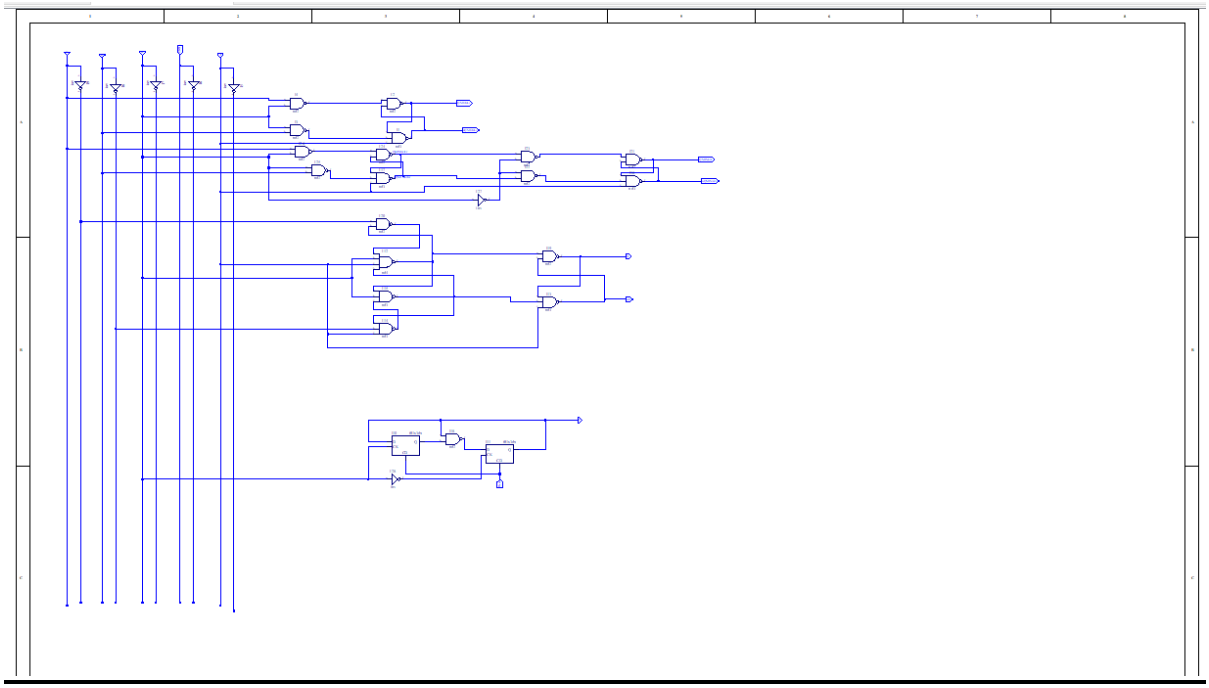
F is the output signal of flip flop. F signal starts when C starts to run, and it ends when reset starts. We need to note that, starting of reset is also necessary.



We also note that the frequency of the clock signal C is thrice the frequency of the output signal F.



4. Schematic Diagrams:



5. Conclusion:

In this Laboratory work we designed the schematics of the circuit of an SR gated latch, SR master-slave gated latch, a SR Flip-Flop and a circuit using D flip-flop from elements library (using fd1sdx from Lattice Diamond). Also, by running and analyzing the simulation, we understood the applications of latches and Flip-Flops and how they are being used as a frequency divider and as a Storage device.