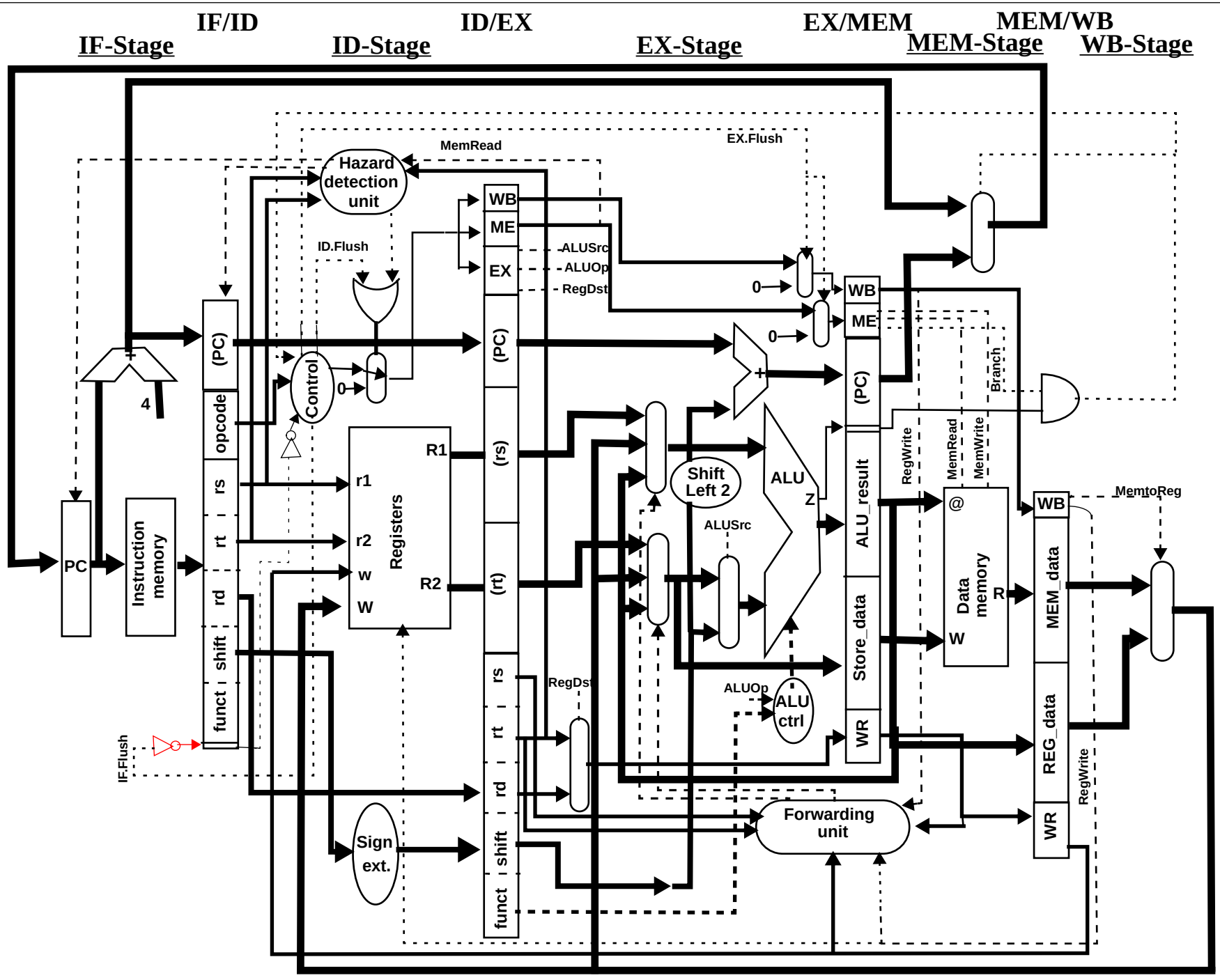
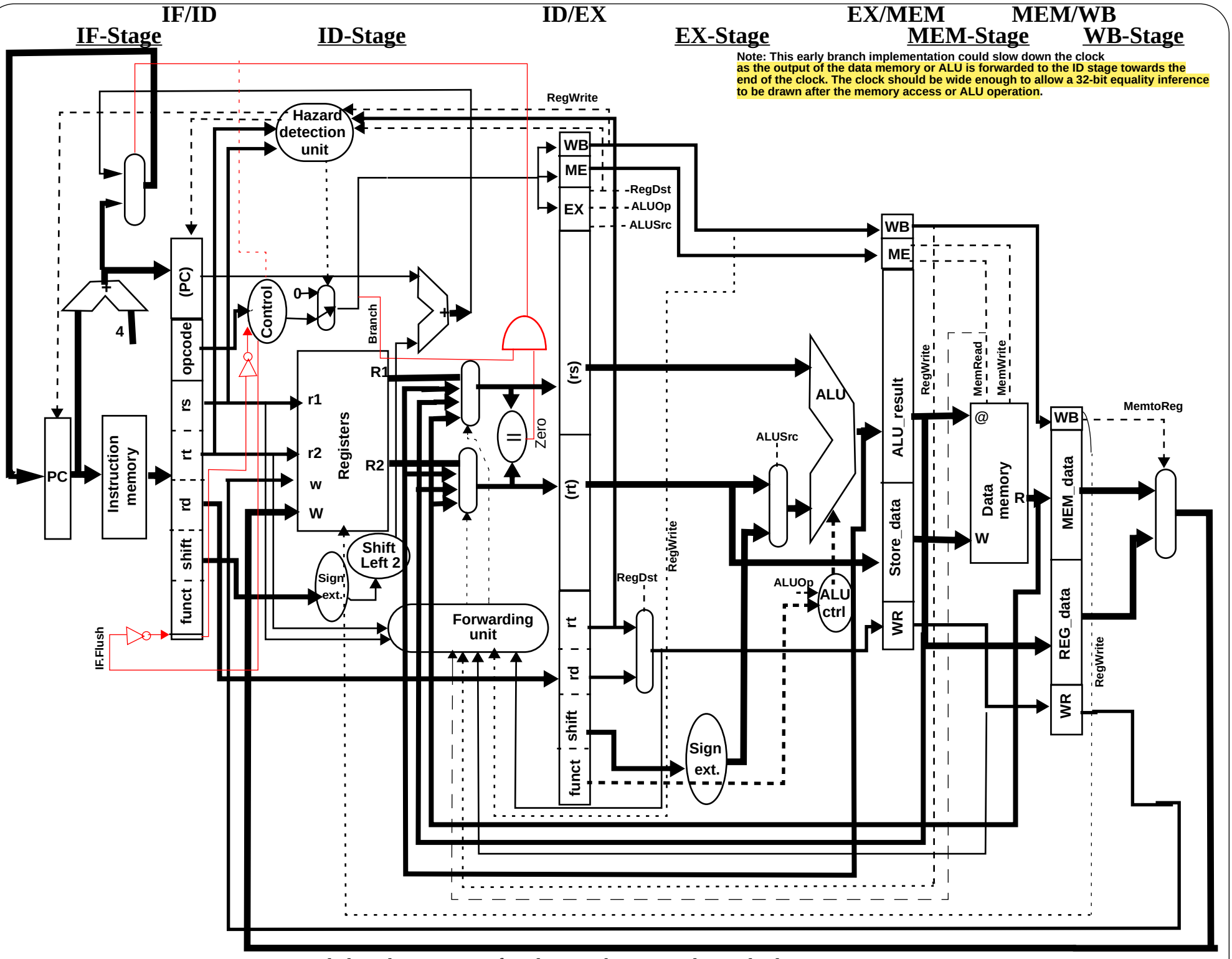



Pipelined CPU (Late Branch from 1st Ed.) for the EE457 class Lab #6

3/26/2000

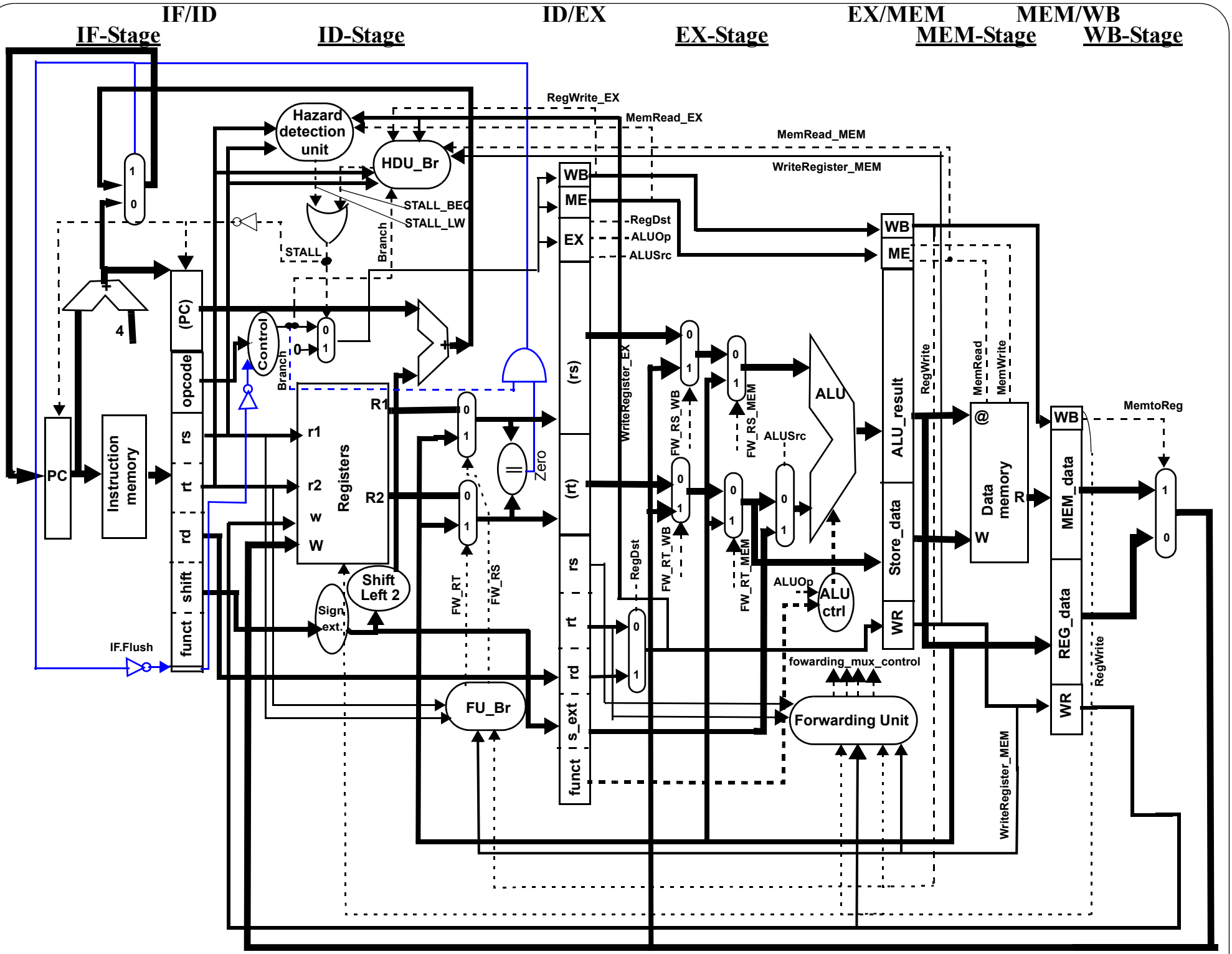
Original drawing provided by Prof. Dubois




Detailed implementation of Early Branch suggested in 2nd Ed.

5/24/99

Original drawing provided by Prof. Dubois. Early branch implementation by Gandhi Puvvada




Detailed implementation of Early Branch suggested in 3rd Ed.

## The pseudo code for the Early Branch design:

==========

**FU (the original Forwarding Unit in EX stage):**

**1. EX Hazard:**

```
if [
    | EX/MEM.RegWrite
    | and (EX/MEM.WriteRegister =/= 0)
    | and (EX/MEM.WriteRegister == ID/EX.ReadRegister_RS)
   ]
then make FW_RS_MEM = 1 (i.e. make ALUSelA = 10; make EX1 = true)

if [
    | EX/MEM.RegWrite
    | and (EX/MEM.WriteRegister =/= 0)
    | and (EX/MEM.WriteRegister == ID/EX.ReadRegister_RT)
   ]
then make FW_RT_MEM = 1 (i.e. make ALUSelB = 10; make EX2 = true)
```

**2. MEM Hazard:**

```
if [
    | MEM/WB.RegWrite
    | and (MEM/WB.WriteRegister =/= 0)
    | and (MEM/WB.WriteRegister == ID/EX.ReadRegister_RS)
    | and (EX1 =/= true)
   ]
then make FW_RS_WB = 1 (i.e. make ALUSelA = 01)

if [
    | MEM/WB.RegWrite
    | and (MEM/WB.WriteRegister =/= 0)
    | and (MEM/WB.WriteRegister == ID/EX.ReadRegister_RT)
    | and (EX2 =/= true)
   ]
then make FW_RT_WB = 1 (i.e. make ALUSelB = 01)
```

==========

==========

**FU_Br (New Forwarding Unit in ID stage to serve the early branch):**

```
If [
    | EX/MEM.RegWrite
    | and (EX/MEM.WriteRegister =/= 0)
    | and (EX/MEM.WriteRegister == IF/ID.ReadRegister_RS)
   ]
then make FW_RS = 1

If [
    | EX/MEM.RegWrite
    | and (EX/MEM.WriteRegister =/= 0)
    | and (EX/MEM.WriteRegister == IF/ID.ReadRegister_RT)
   ]
then make FW_RT = 1
```

==========

**HDU (Original Hazard Detection Unit in ID stage):**

Note: Here **`ID/EX.WriteRegister`** refers to the WriteRegister after the mux governed by RegDst.
We could replace it with **`ID/EX.WriteRegisterRt`** .

```
If [
    | ID/EX.MemRead
    | and (ID/EX.WriteRegister =/= 0)
    | and {(ID/EX.WriteRegister == IF/ID.ReadRegister_RS)
    |       or
    |       (ID/EX.WriteRegister == IF/ID.ReadRegister_RT)}
   ]
then make STALL_LW = 1
```

==========

**HDU_Br (New Hazard Detection Unit in ID stage to serve the early branch):**

Note: Here **`ID/EX.WriteRegister`** refers to the WriteRegister after the mux governed by RegDst.

```
If [
    | Branch
    | and [
    |       | [ ID/EX.RegWrite
    |       |   | and (ID/EX.WriteRegister =/= 0)
    |       |   | and |{ (ID/EX.WriteRegister == IF/ID.ReadRegister_RS)
    |       |   |     |    or
    |       |   |     |    (ID/EX.WriteRegister == IF/ID.ReadRegister_RT)}
    |       |   ]
    |       |   or
    |       |   [ EX/MEM.MemRead
    |       |   | and (EX/MEM.WriteRegister =/= 0)
    |       |   | and |{ (EX/MEM.WriteRegister == IF/ID.ReadRegister_RS)
    |       |   |     |    or
    |       |   |     |    (EX/MEM.WriteRegister == IF/ID.ReadRegister_RT)}
    |       |   ]
    |       ]
   ]
then make STALL_BEQ = 1
```

==========