In the Name of God, the Compassionate, the Merciful

Shiraz University

COMPUTER SCIENCE AND ENGINEERING DEPARTMENT

Project title : MIPs pipelined processor in java

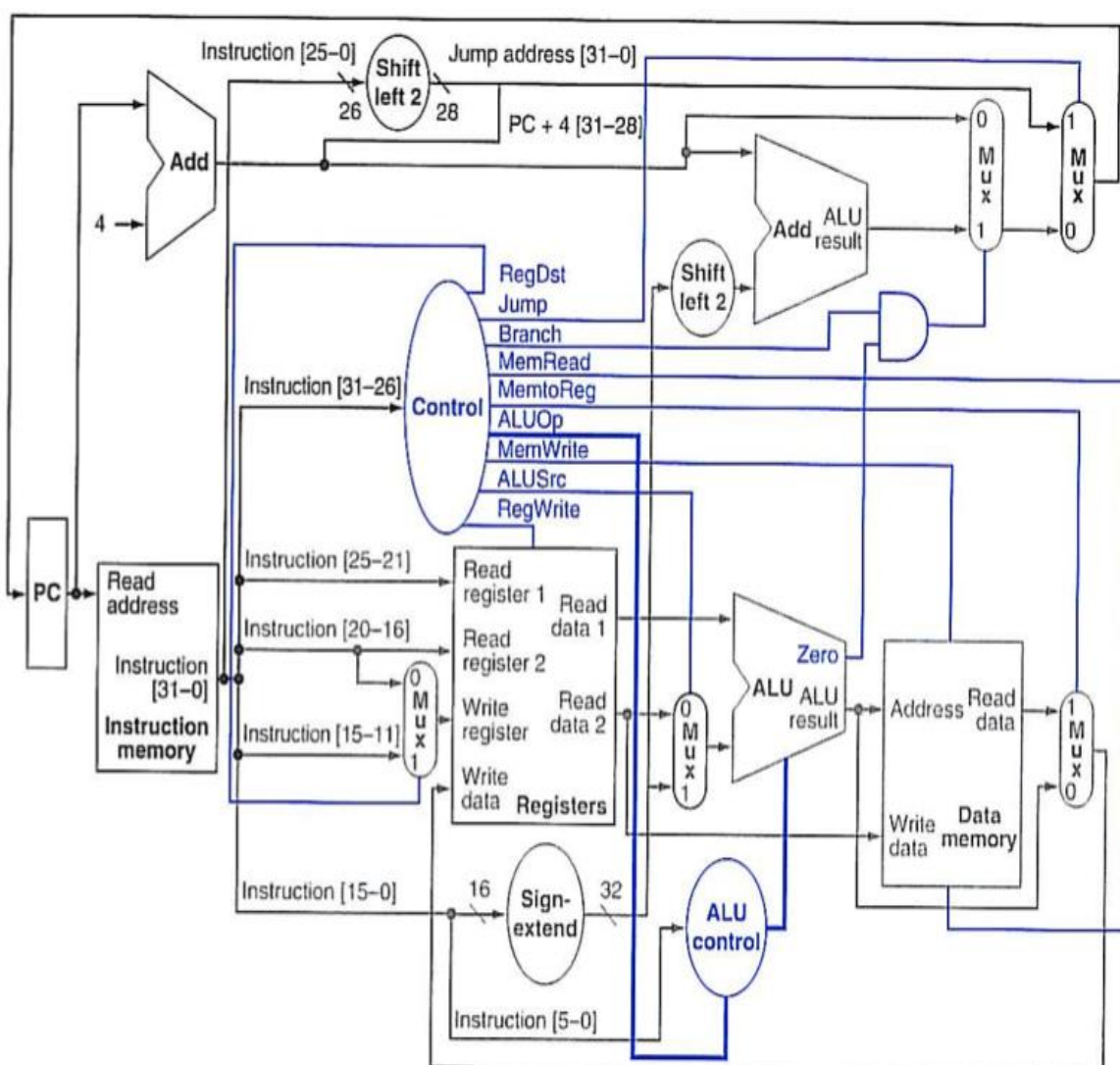Professor : Dr. mousavi

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Introduction :

This documentation consists of the summery of the project . here we explain some courses of the whole project.

The purpose of this project is to implement simplified pipelined cpu MIPS with java .
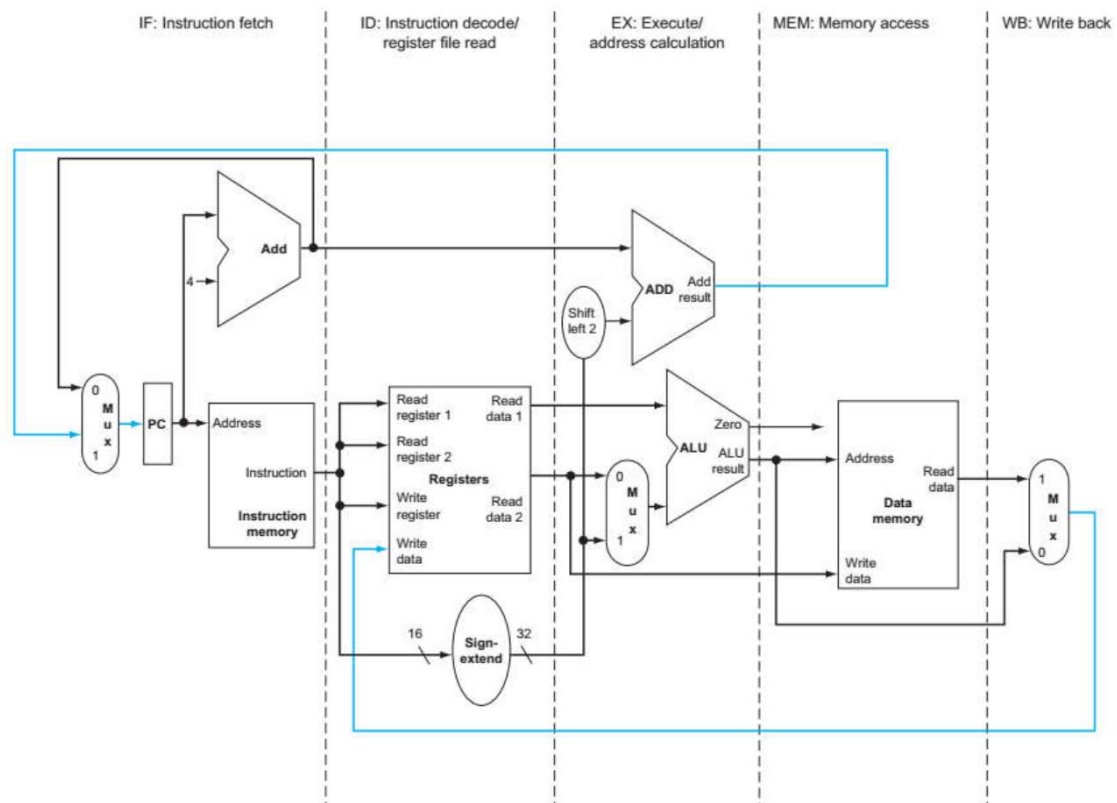
The total scheme of the project is based on picture below (figure 1):

This is what we are planning to design

But before that we need to think more basic so we don't consider hazard detection and control unit and just focus on pipelined design

The start of the project is with this scheme (figure 2):

This project supports :

1. R-type instructions: add, subtract, and, or, and set less than, nor and xor .

2. I-Type instructions: load word, store word, and branch

3. The jump instruction is also supported

4. hazard detection and forwarding

So first of all we create a class named PipelinedRegs which consists of all pipeline registers and then we use it in the Main class . There is 4 of them .

After that we start to write functions to do the duties of stages :

- IF , ID , EX , MEM , WB

We get the list of instructions from a specified file and at the end we write the outputs in 3 separated files including progress path , memory path and register path. We can see the process in these files .

Then we can make a function for control unit that sets its 9 signals to send to the other parts of cpu . so it can tell each file what to do .

After writing a function for control unit we can write some functions for ALU cause it consists of different operations .

At the end we design a hazard detection for our Cpu MIPS .