California State University

Final Project

EGCP 446

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Students

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The Cypher Vault

Introduction:

Digital Safe design is the process of designing and developing digital products or services with a focus on safety, security, and privacy. It involves incorporating best practices and principles to minimize risks and vulnerabilities that may arise during the use of digital products or services.

Effective Digital Safe design involves our collaboration between users and security experts, and other stakeholders to identify potential risks and vulnerabilities and determine the best ways to mitigate them.

For demonstration purposes our program consists of a 3 binary digit number that will activate the Digital Safe this can be connected to as much digits as the user desires.

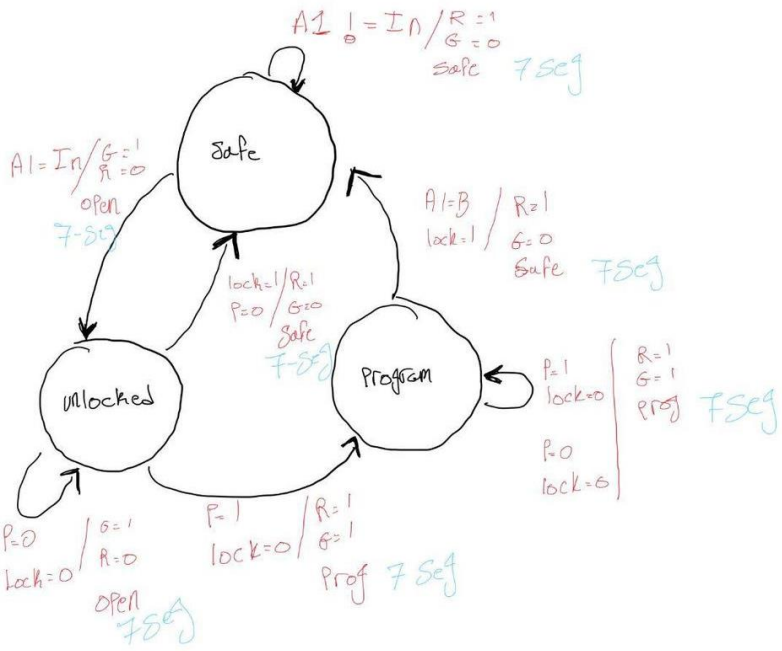
Procedure:

We have started this program with building a Diagram that would help us with the code later on

Our code consists of:

- Mealy finite state machine
- Clock Divider
- seven segment display Decoder
- Top Module

Our Mealy machine has 3 states which are presented in the state diagram below:



This part of the program almost deals with everything it takes in 3 input pins. Initial state is safe our predefined code for the safe is 111. The user enters this PIN to go into the next stage which is the UNLOCKED Stage from There the user can use the same PIN or use a new one the user can press Program button to set a new pin or Lock to use the existing PIN and lock the Safe. If the user presses the Program button he will enter the program state where he can set the new pin from the switches after he sets the new pin the user presses the lock button to set the new pin and lock the safe.

The mealy machine consists of 10 inputs:

- 3 inputs to enter the pin to unlock the safe
- 3 inputs to enter a different pin if the user wants to change the pin
- 1 input for a lock button
- 1 input for a program button
- Clock
- Reset

It also consists of 8 outputs:

- 4 outputs that feed the 7 segment display module
- 4 LED outputs that show us the status of each state

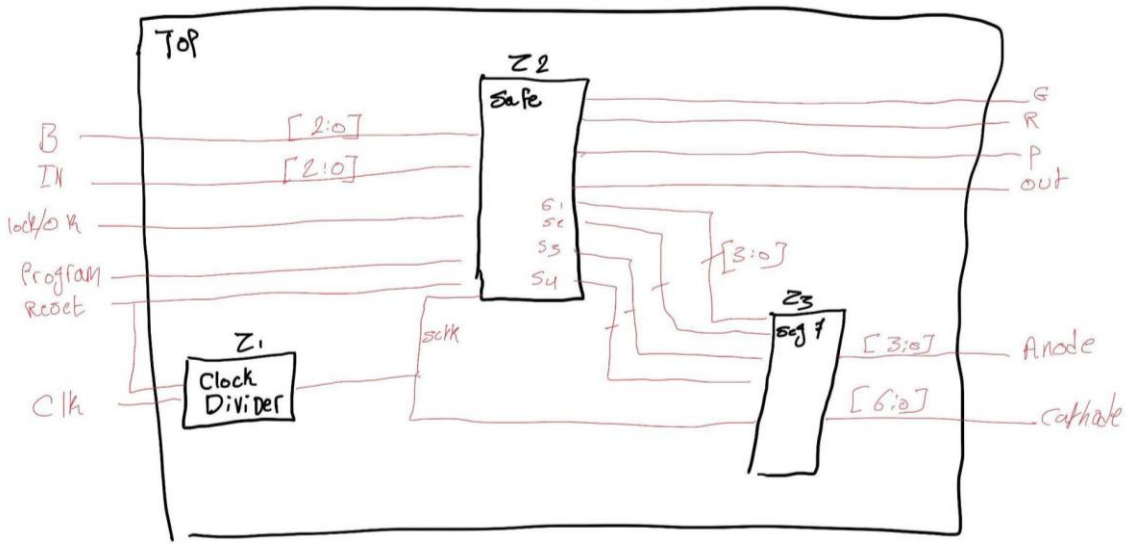
The clock divider module sets the specific clock that we want for our design it is set to 100Hz

- The clock divider module has 2 inputs
    - reset
    - Clock from the original board
- output that provides the entire hardware our specific Clock

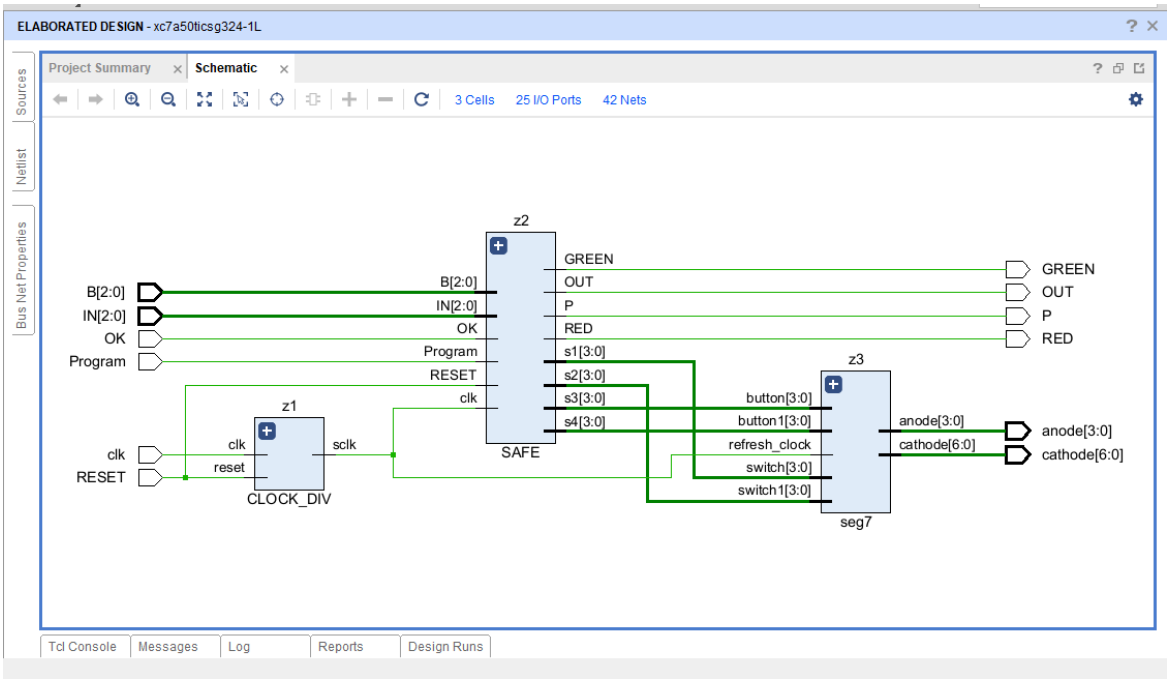
The seven segment display module consist of different modules:

- Refresh counter : This modules refreshes a counter to feed the module for the anode control module.
- Anode Control : depending on the counter from the refresh counter it chooses a specific digit in the segment to display a character in a specific Digit.
- BCD control: gets the feedback/output from the Finite state machine to interpret them as a BCD so it can pass it to the BCD to cathode module.
- BCDtoCathode : gets a BCD that has predefined values in the module to turn on specific LEDs in the segment to display a character it takes in 4 digits and outputs 7 digits it acts as a decoder.

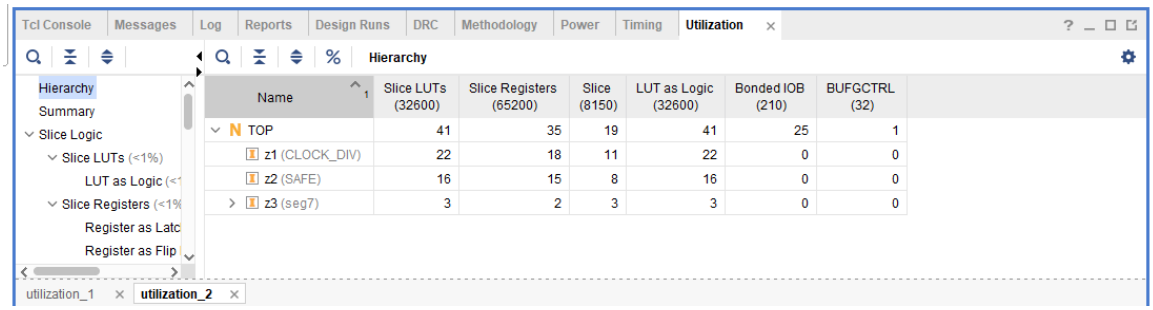
Top Module connects all of the modules together and here is a system Diagram to show how thev are connected:



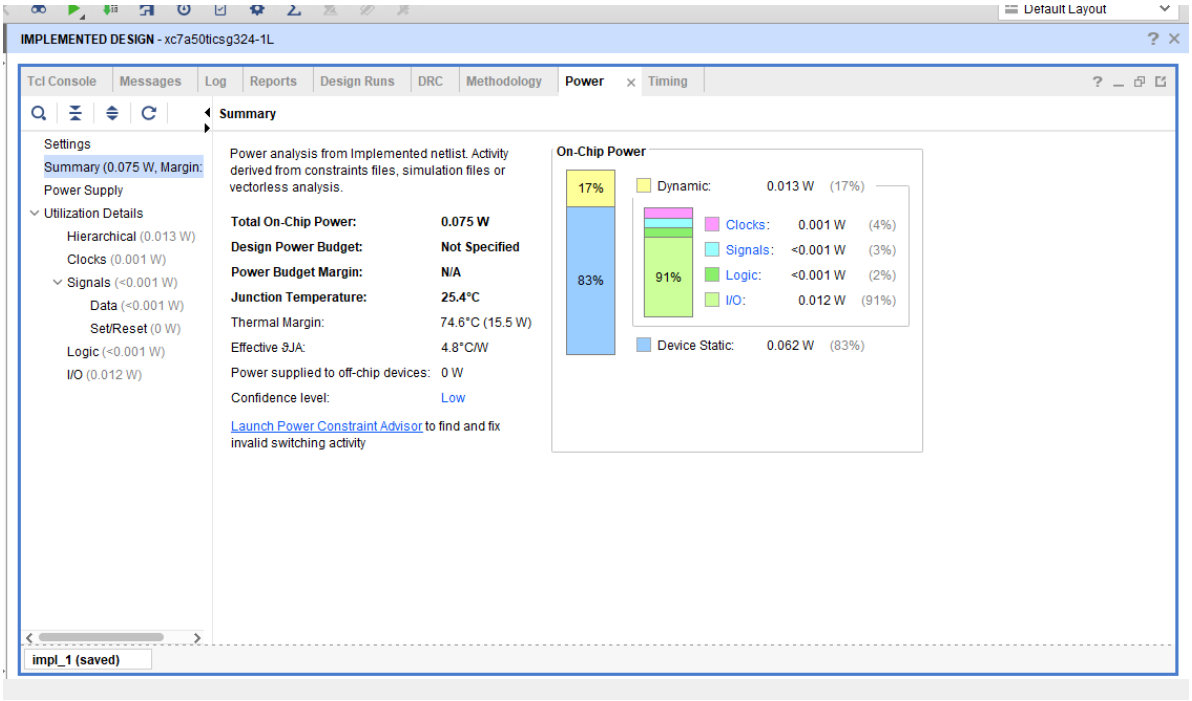
RTL Schematic:



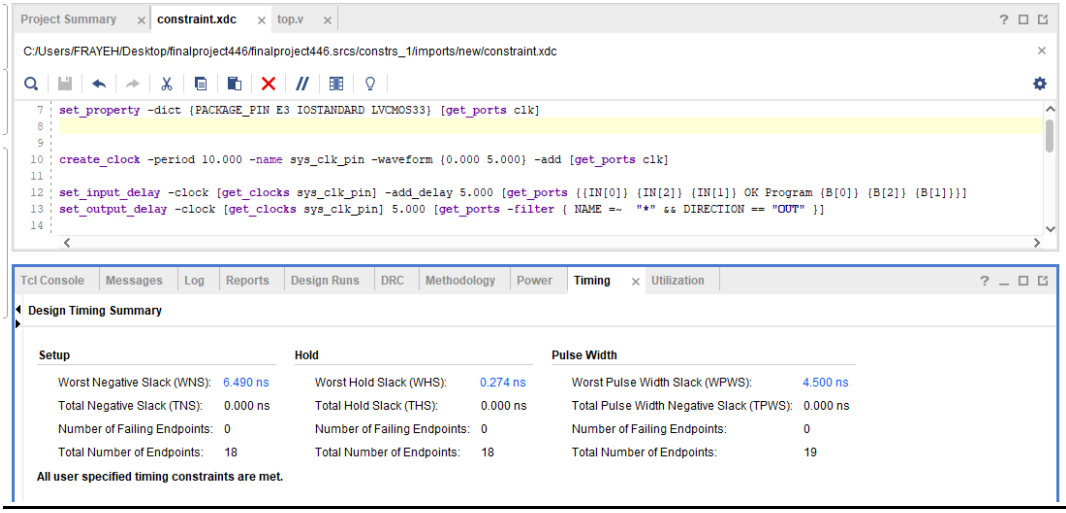
Area report:



Power report:



Static timing analsys:



Summary/Challenges:

This project has been definetly interesting we have combined many techniques and many topics that we have learned throughout the semester, we have combined finite state machines with a seven segment display. A clock divider that syncs everything together. We have used structural modeling to make it easier for a programmer to read. Our project is working fully functional and the way we want it to be.

We have faced many challenges while designing this Digital Safe we changed our code and its structure many times to get what we have achieved.

If we were to redo this project and make it more challenging we would definitely have combined a memory to take in inputs and save the sequence of the inputs and have them input in a specific sequence.

References:

Only references used are the lecture notes.