Notes:

1) Active Low Signals Names end in B or _B

2) PCI Edge Connector P1 is keyed as 3.3V ONLY

3) +IOV for PCI edge connector is wired to 3.3V

4) Ref. Sheet 6:

   PCIe CEM Spec, Pg. 56 footnotes:

   - By default the PETpx and PETnx pins shall be connected to the PCI Express transmitter differential pair on the system board, and the PCI Express receiver pair on the add-in card

   - By default the PERpx and PERnx pins shall be connected to the PCI Express receiver differential pair on the system board, and the PCI Express transmitter pair on the add-in card

5) Schematics updated to Rev 02 on 2-27-08

6) Rev 02 change (sheet 8):

   -R394, R402 changed from 4.7K 0402 to 1.0K 0402 (stiffer pulldown)

ML555 PCB:
Latest Schematics Revision:
-Rev 02 on 2-27-08

Xilinx PCB Schematic Number: 0381219

Xilinx

TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280444		
SIZE: C	DWG NO: 0381219	REV: 02	
DRAWN BY: DAVID NAYLOR	SCALE:	SHEET: 1 of 37	2-27-2008_10:46

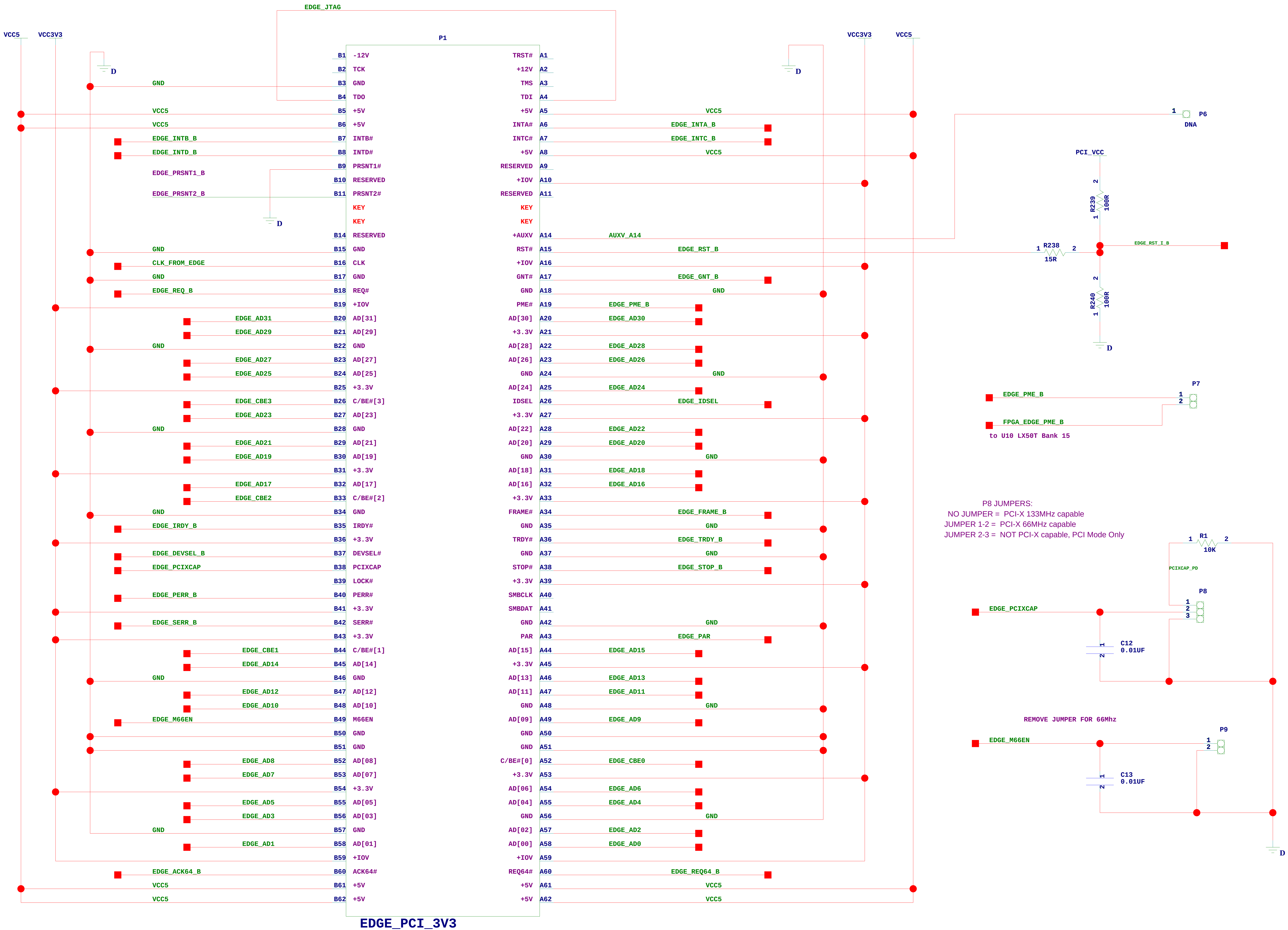
ML555 Schematic Sheet List

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		2 of 37	2-27-2008_10:44



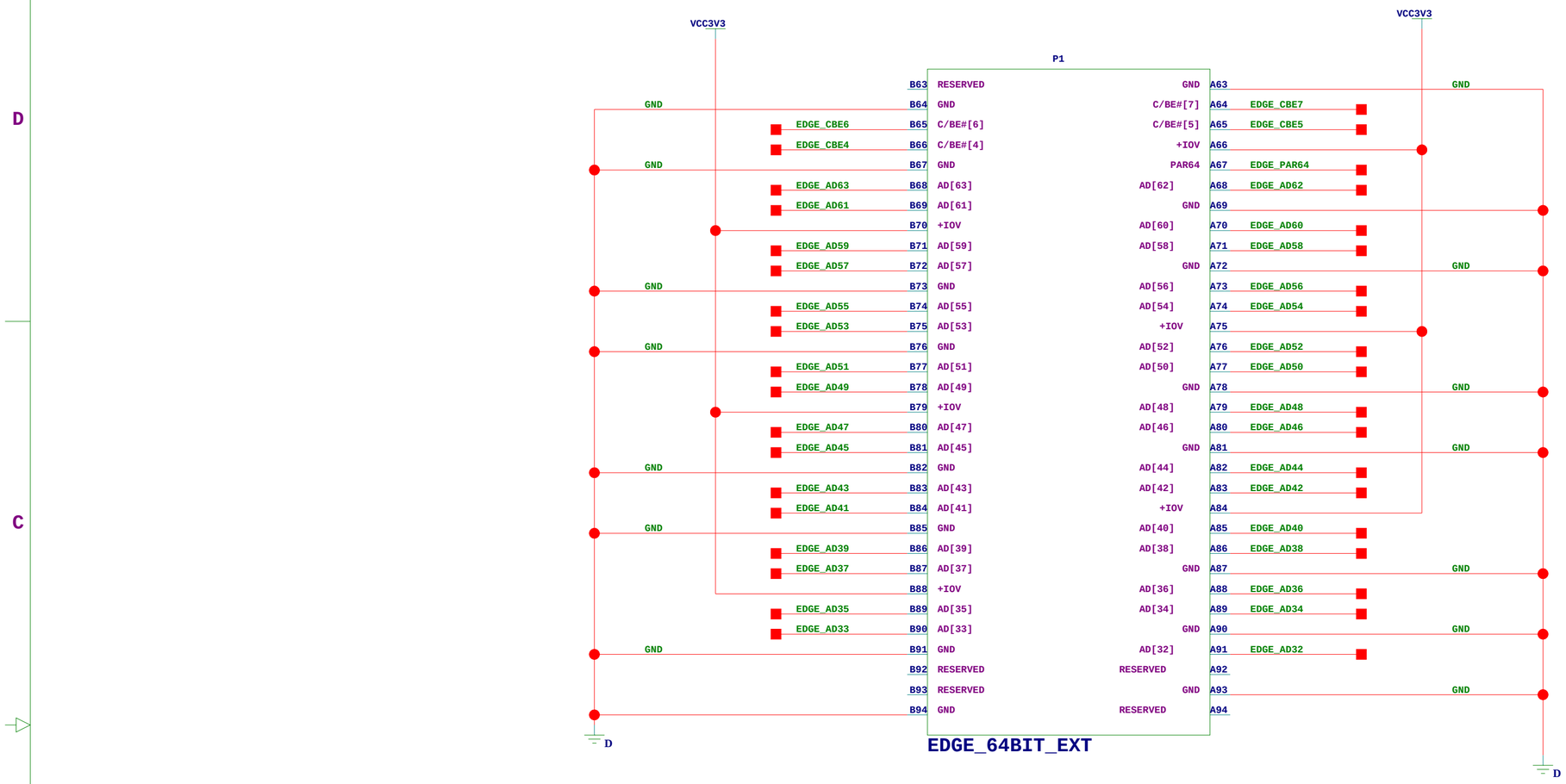
PCI EDGE CONNECTOR 3.3V 32-bit SECTION

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE C | DWG NO 0381219 | REV 02

DRAWN BY DAVID NAYLOR | SCALE | SHEET 3 of 37 | 2-27-2008_10:44



PCI EDGE CONNECTOR 3.3V 64-bit EXTENSION

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	of	
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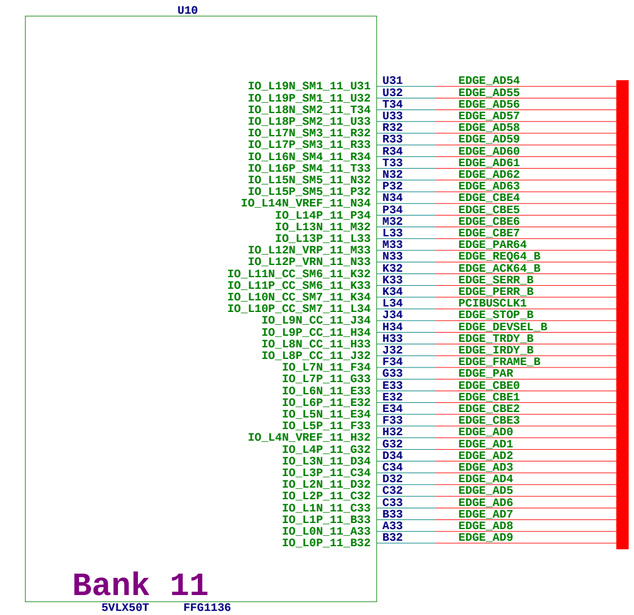
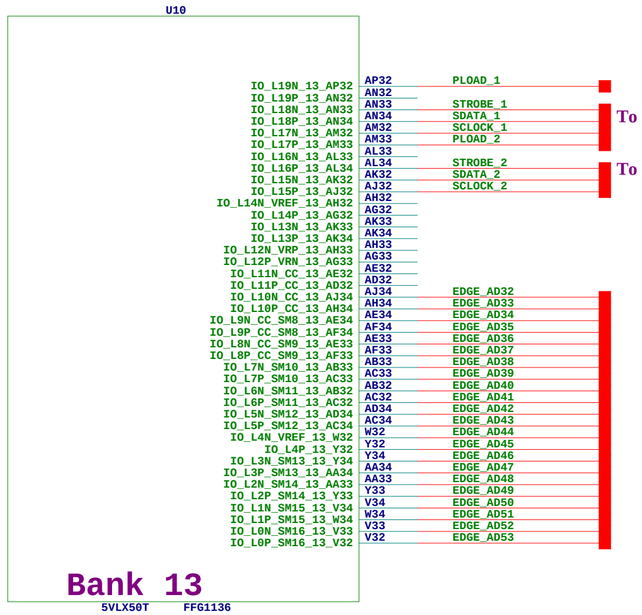
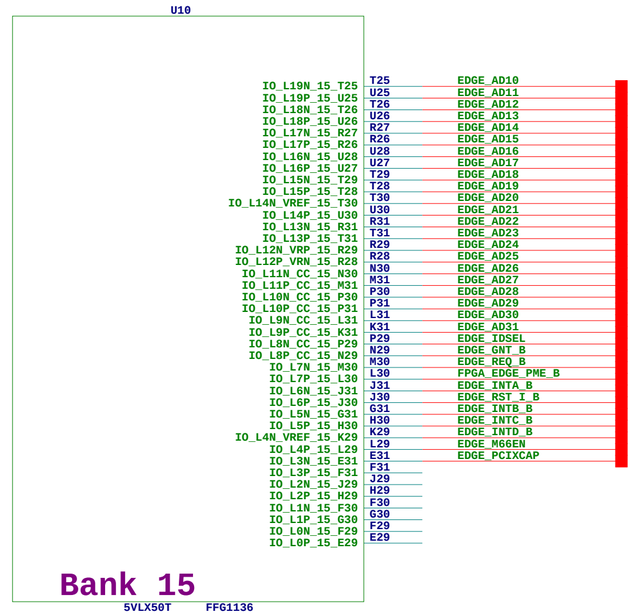


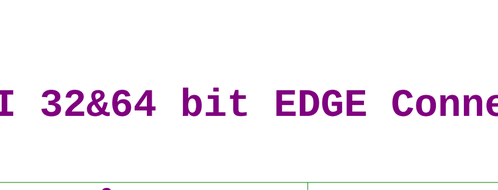


To Sheet24 U8

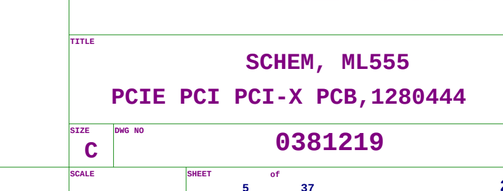
To Sheet25 U7

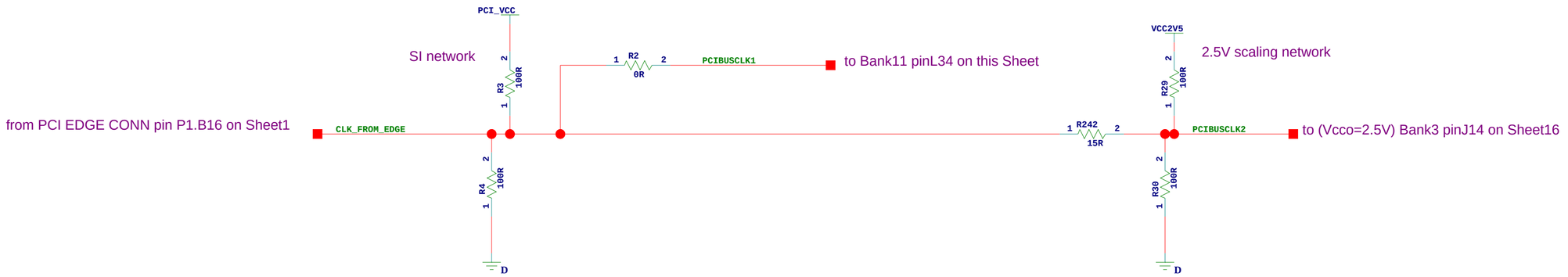


PCI 32-bit I/F



PCI 64-bit EXTENSION I/F





Banks 11,13,15

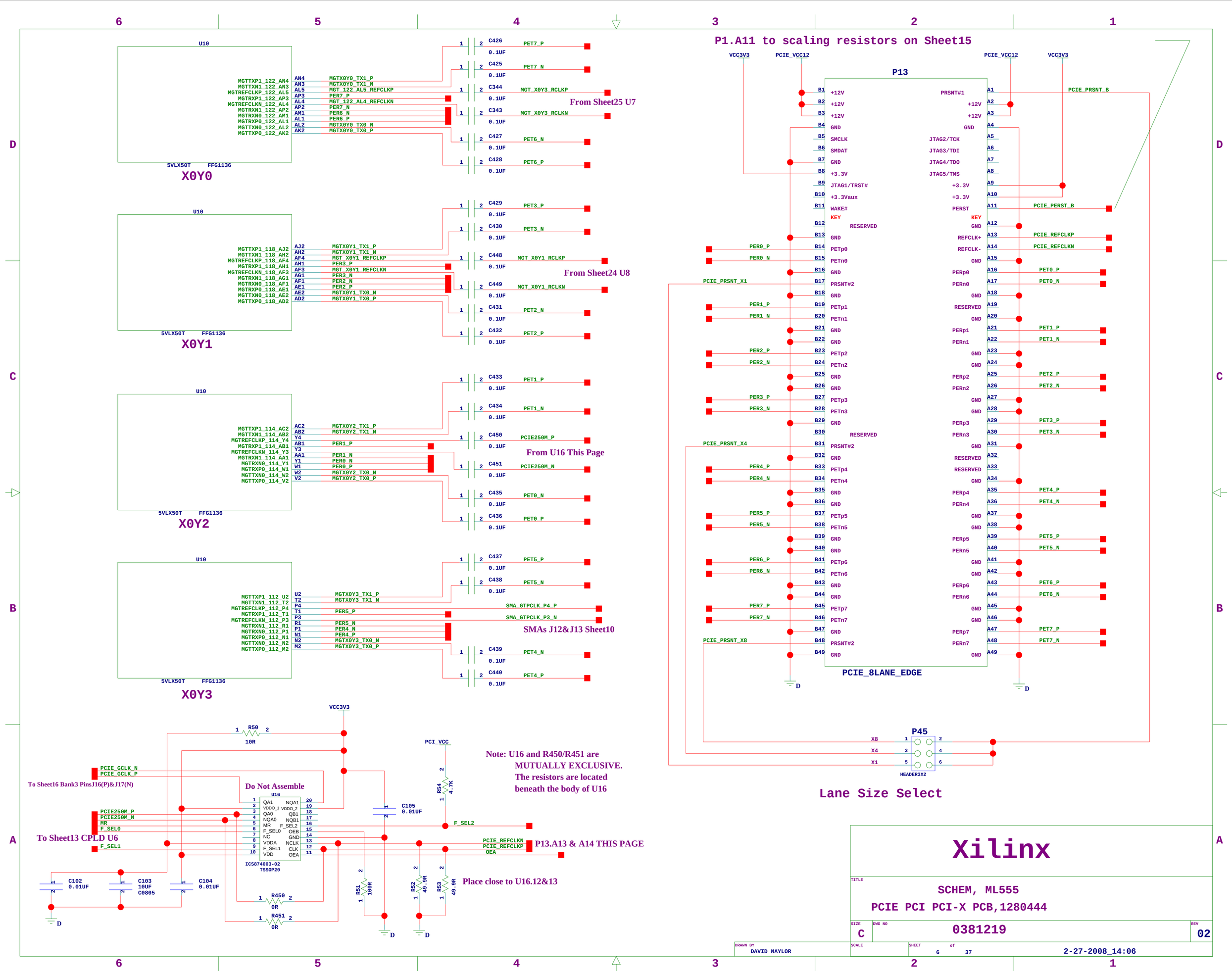
PCI 32&64 bit EDGE Connector Bank I/F

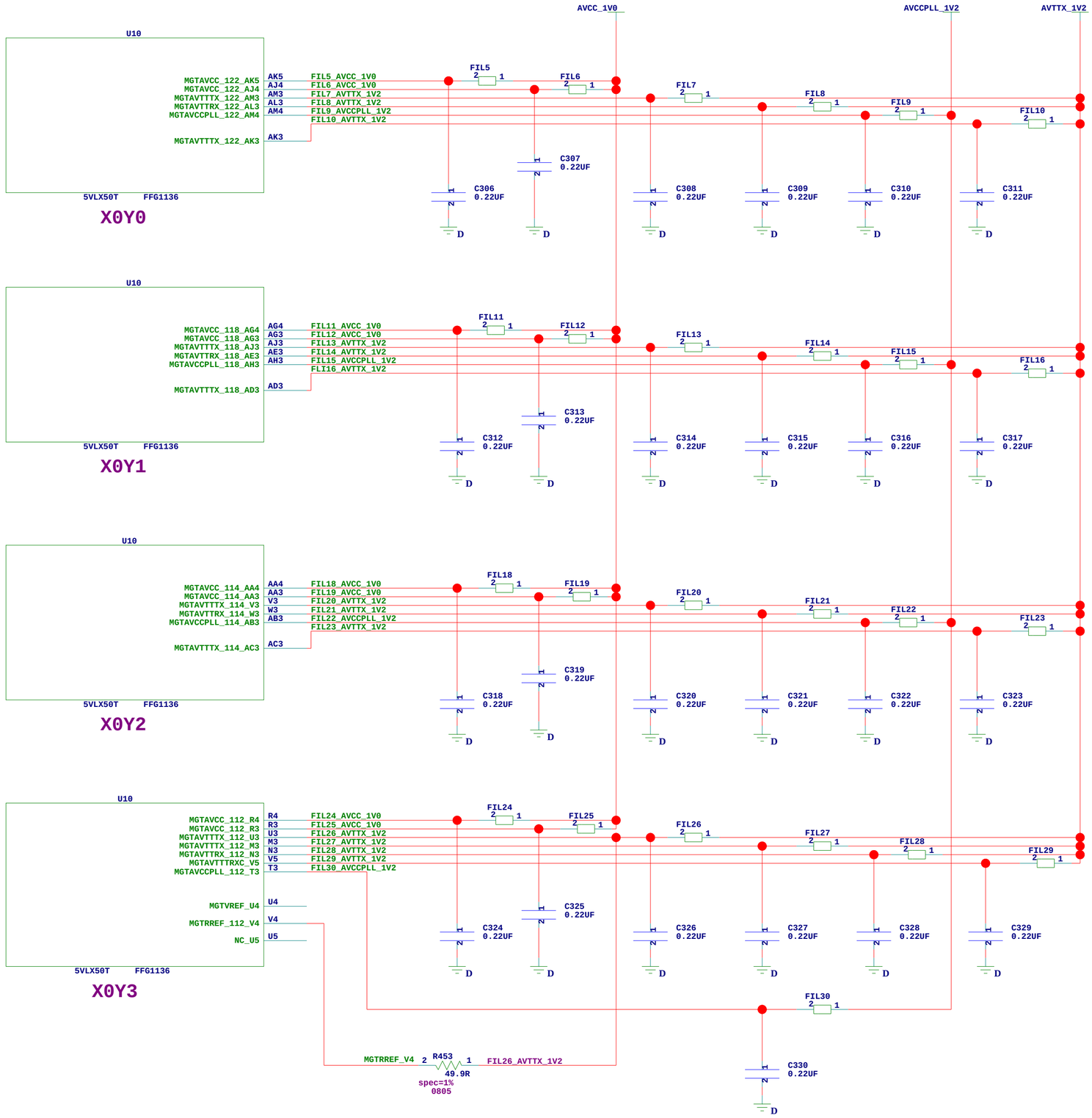
Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		5 of 37	2-27-2008_14:05


P1.A11 to scaling resistors on Sheet15
U10
5VLX50T FFG1136
X0Y0
X0Y1
X0Y2
X0Y3
From Sheet25 U7
From Sheet24 U8
From U16 This Page
SMAs J12&J13 Sheet10
P13
PCIE_8LANE_EDGE
P45
HEADER3X2
Lane Size Select
Do Not Assemble
To Sheet16 Bank3 PinsJ16(P)&J17(N)
To Sheet13 CPLD U6
P13.A13 & A14 THIS PAGE
Place close to U16.12&13
Note: U16 and R450/R451 are MUTUALLY EXCLUSIVE. The resistors are located beneath the body of U16
ICS874003-02 TSSOP20
Xilinx
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444
0381219
DAVID NAYLOR
2-27-2008_14:06



Note: For more detailed information concerning MGT power and filtering requirements, see the Xilinx UG196 Virtex-5 FPGA RocketIO GTP Transceiver User Guide

MGT X0Y0,X0Y1,X0Y2,X0Y3 Power Blocks

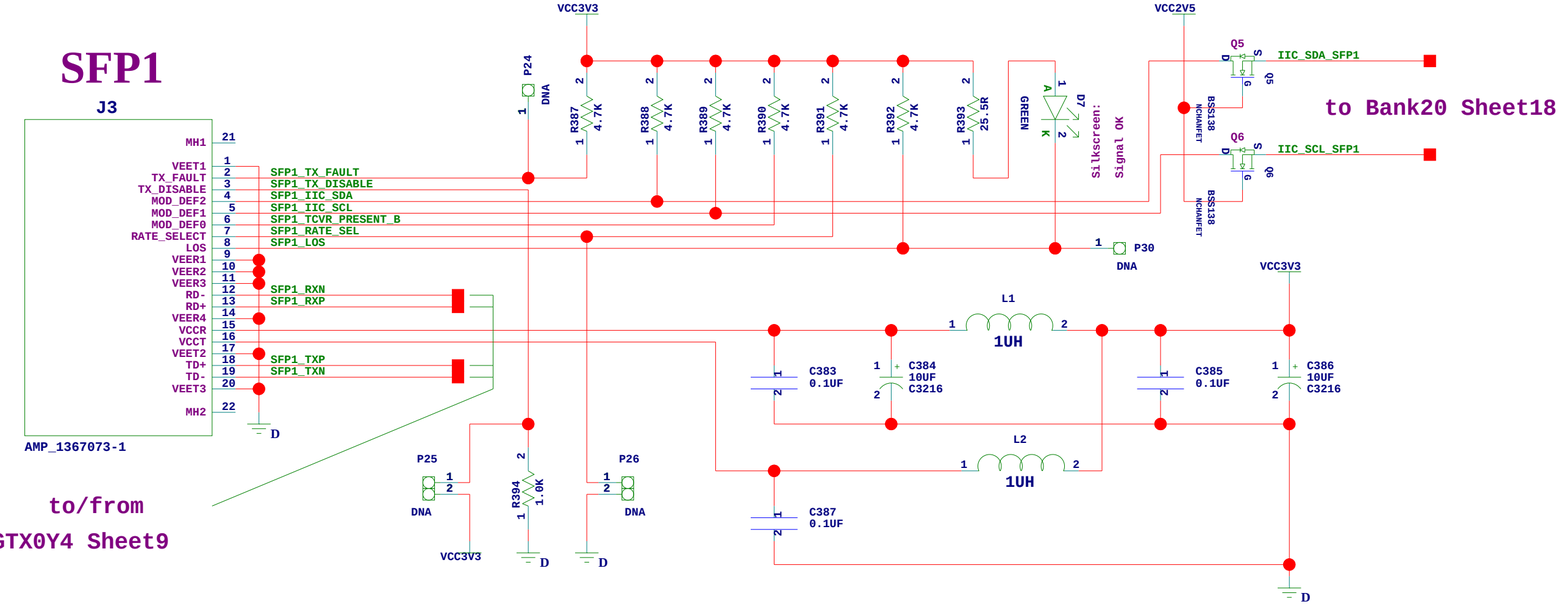
Xilinx

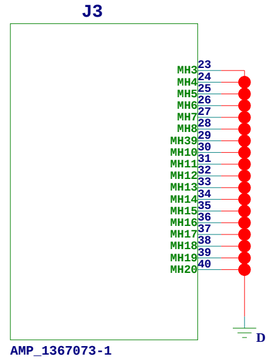
TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

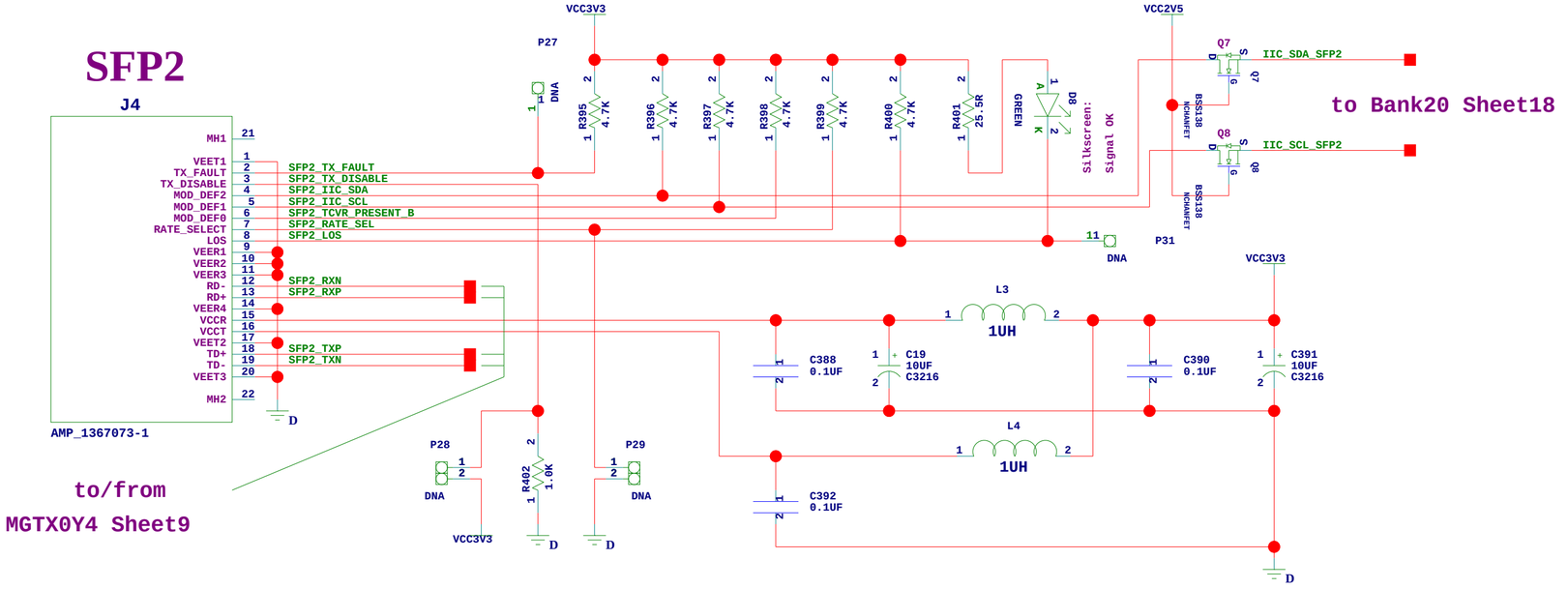
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		7 of 37	2-27-2008_14:07

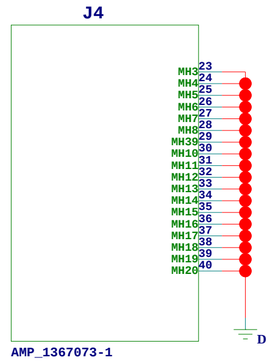
SFP1





SFP2





2xSFP

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	of	
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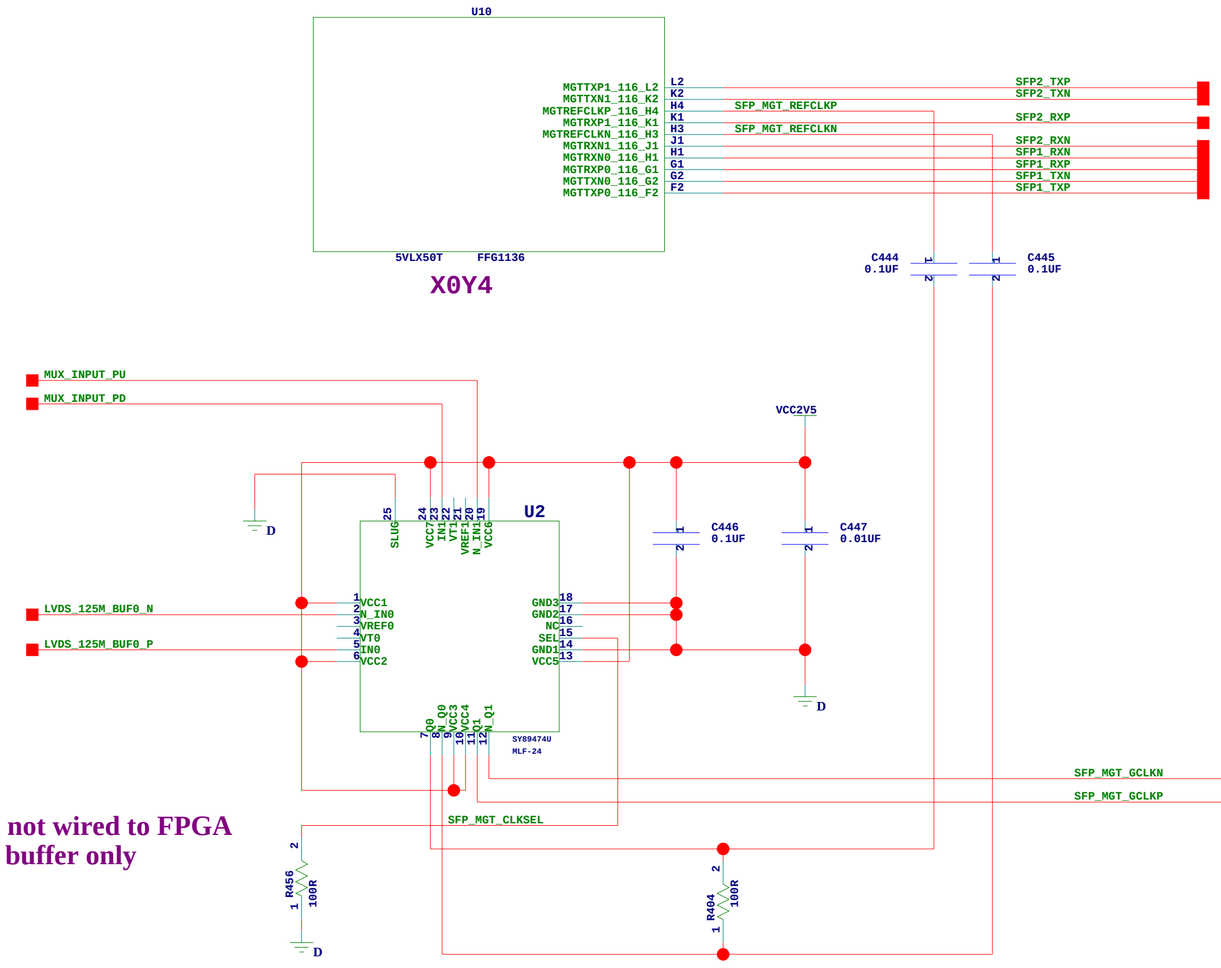


to SFP1&2 Sheet8

IN1 biased
From Sheet11 R42/43

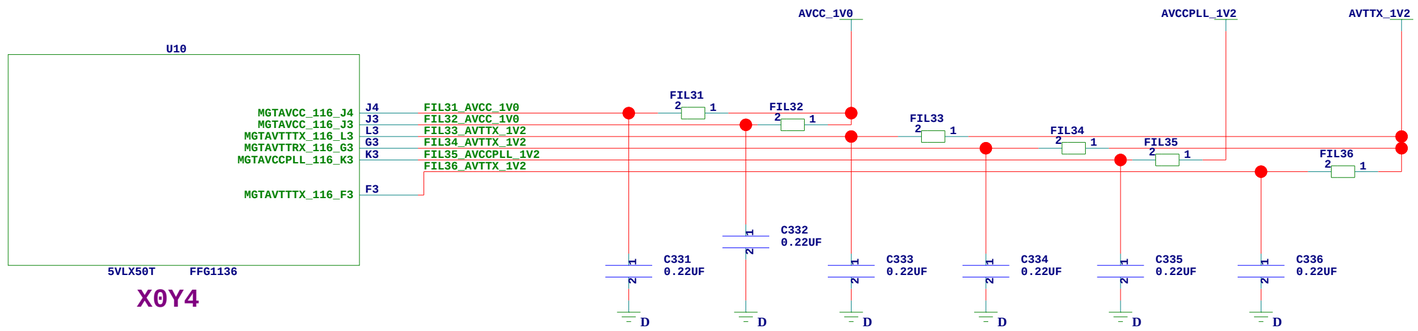
From Sheet11 U11

To Bank3 GCLK Sheet16

SFP_MGT_CLKSEL not wired to FPGA
U2 used as clock buffer only

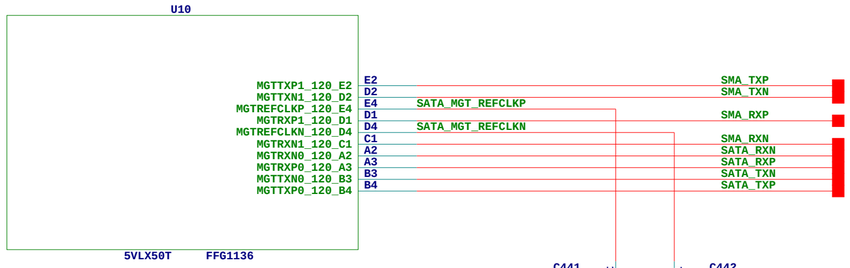
Clock Mux:

Sel:	Q0 Out:
0	LVDS_125M (default)
1	IN1 tied to static levels via p/u & p/d resistors

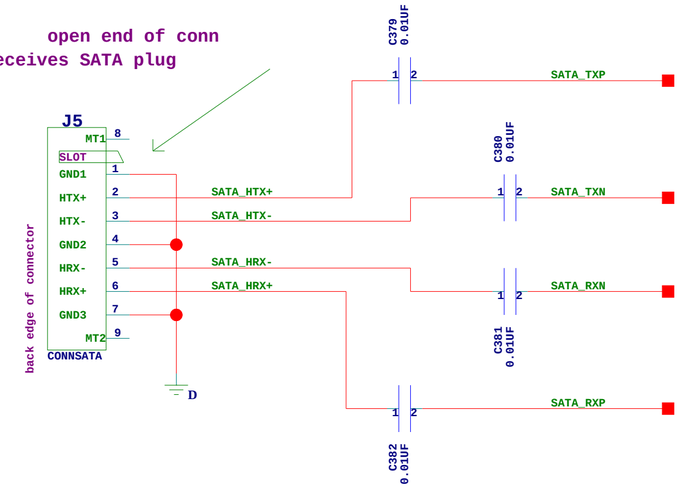


MGT X0Y4 SFP I/F & Power Block

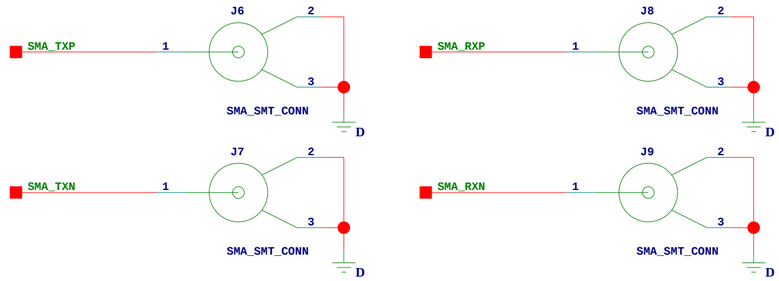
Xilinx	
TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280444
SIZE	C
DWG NO	0381219
REV	02
DRAWN BY	DAVID NAYLOR
SCALE	
SHEET	9 of 37
	2-27-2008_14:07



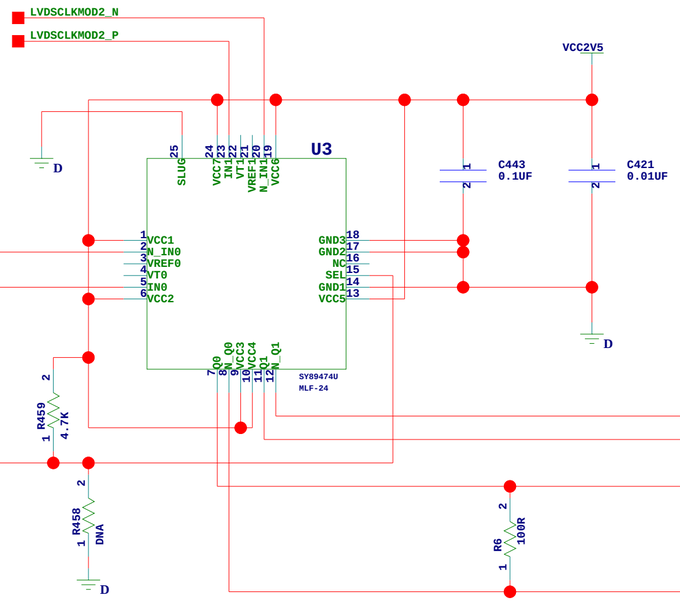
open end of conn
which receives SATA plug



SMA TX and RX



From Sheet25 U7



From Sheet11 U11

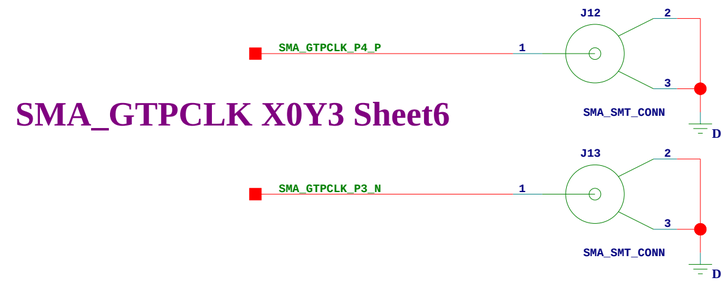
SATA_MGT_CLKSEL wired to FPGA

Bank3 pin H15 Sheet 16

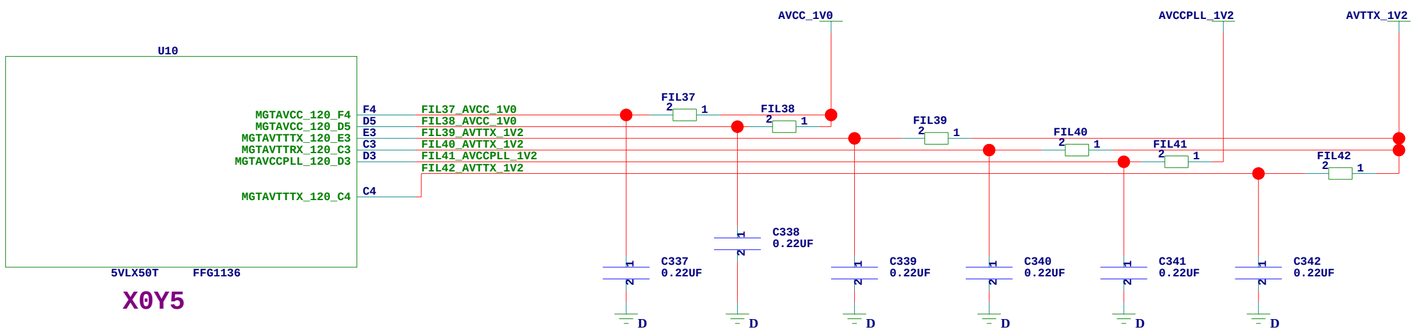
To Bank3 GCLK Sheet16

Clock Mux:

Sel:	Q0 Out:
0	LVDS_125M
1	LVDSCLKMOD2 (default)



SMA_GTPCLK X0Y3 Sheet6



SATA Conn,4xSMA,MGT X0Y5 & Power Block

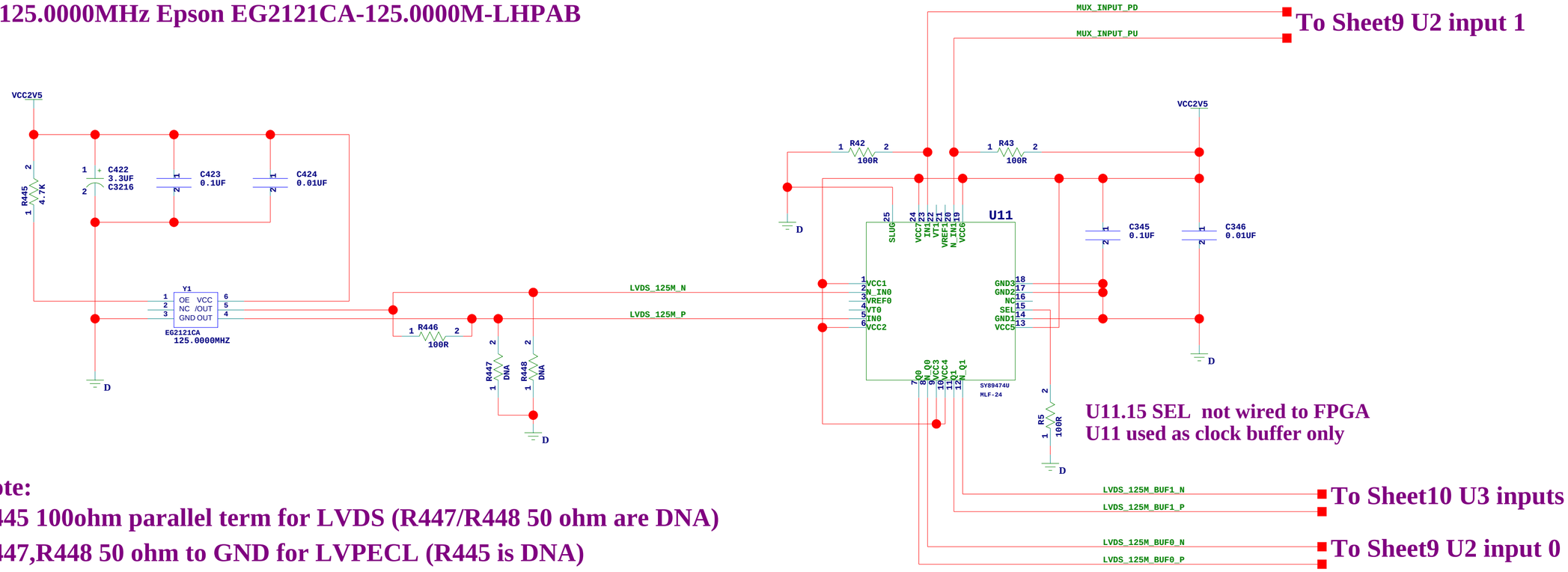
Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		10	37	2-27-2008_14:08

125.0000MHz Epson EG2121CA-125.0000M-LHPAB



To Sheet9 U2 input 1

U11.15 SEL not wired to FPGA
U11 used as clock buffer only

To Sheet10 U3 inputs

To Sheet9 U2 input 0

Note:
R445 100ohm parallel term for LVDS (R447/R448 50 ohm are DNA)
R447,R448 50 ohm to GND for LVPECL (R445 is DNA)

Clock Mux:

Sel:	Q0 Out:
0	LVDS_125M (default)
1	IN1 tied to static levels via p/u & p/d resistors

125MHz Osc Y1 & LVDS Clock Mux U11

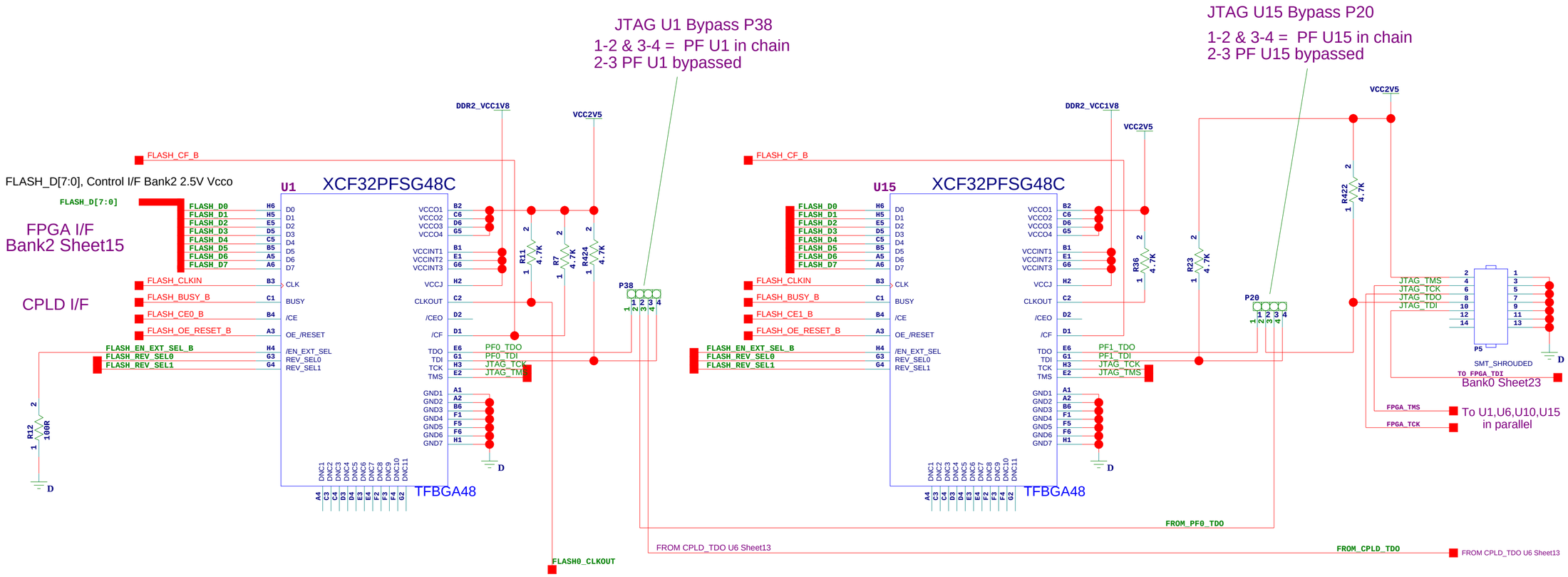
Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		11 of 37	2-27-2008_11:17

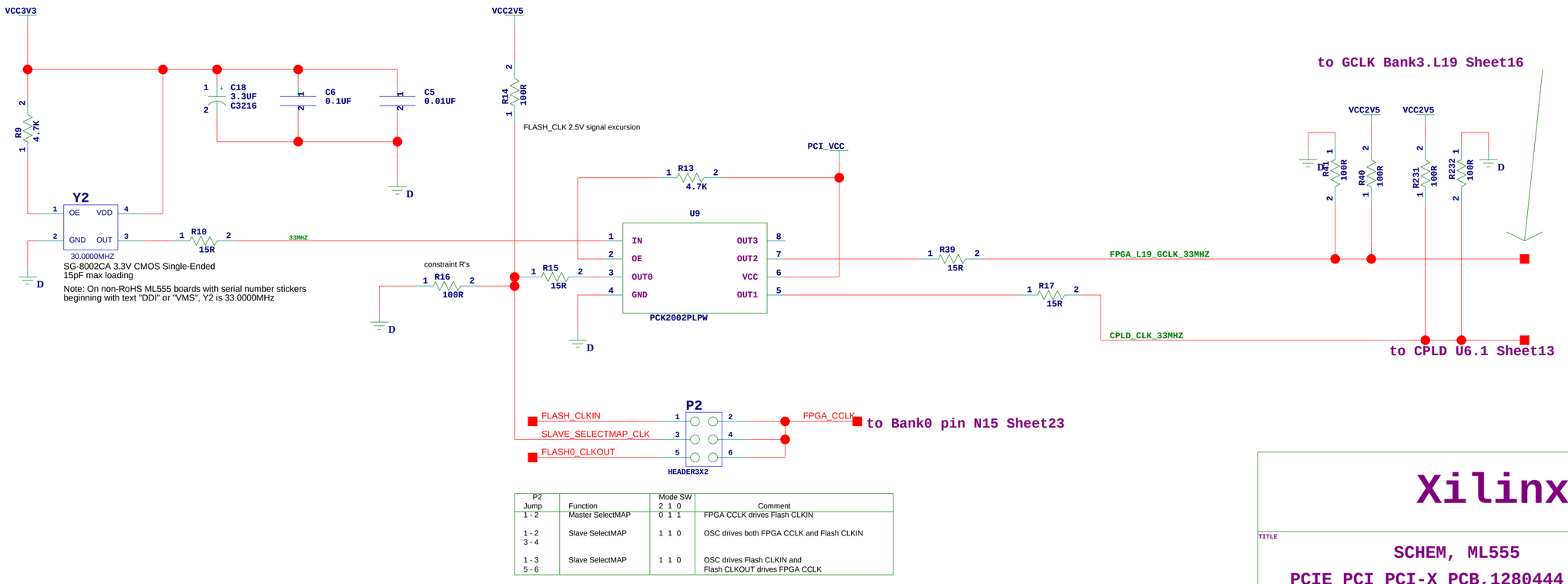
Platform Flash, JTAG I/F



(Bypassable) (Bypassable) (Bypassable)

Loop=JTAG P5=>LX50T U10=>CPLD U6=>PF0 U1=>PF1 U15=>JTAG P5

P5 2mm JTAG conn. is Xilinx Parallel Cable IV or Platform USB Cable compatible



P2 Jump	Function	Mode SW 2 1 0	Comment
1 - 2	Master SelectMAP	0 1 1	FPGA CCLK drives Flash CLKIN
1 - 2 3 - 4	Slave SelectMAP	1 1 0	OSC drives both FPGA CCLK and Flash CLKIN
1 - 3 5 - 6	Slave SelectMAP	1 1 0	OSC drives Flash CLKIN and Flash CLKOUT drives FPGA CCLK

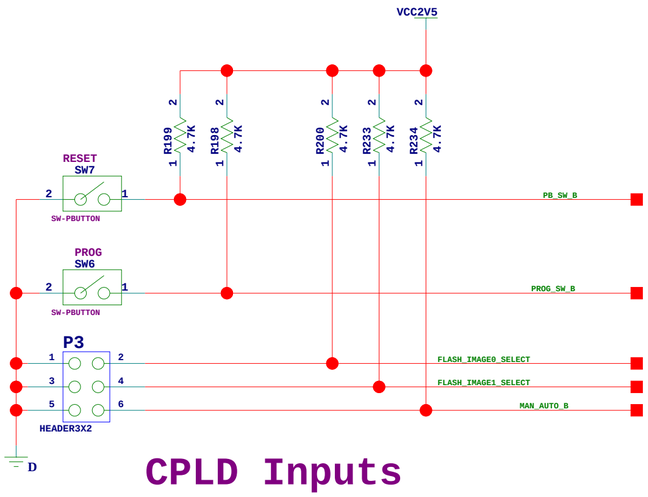
Platform Flash Clock Select

Xilinx

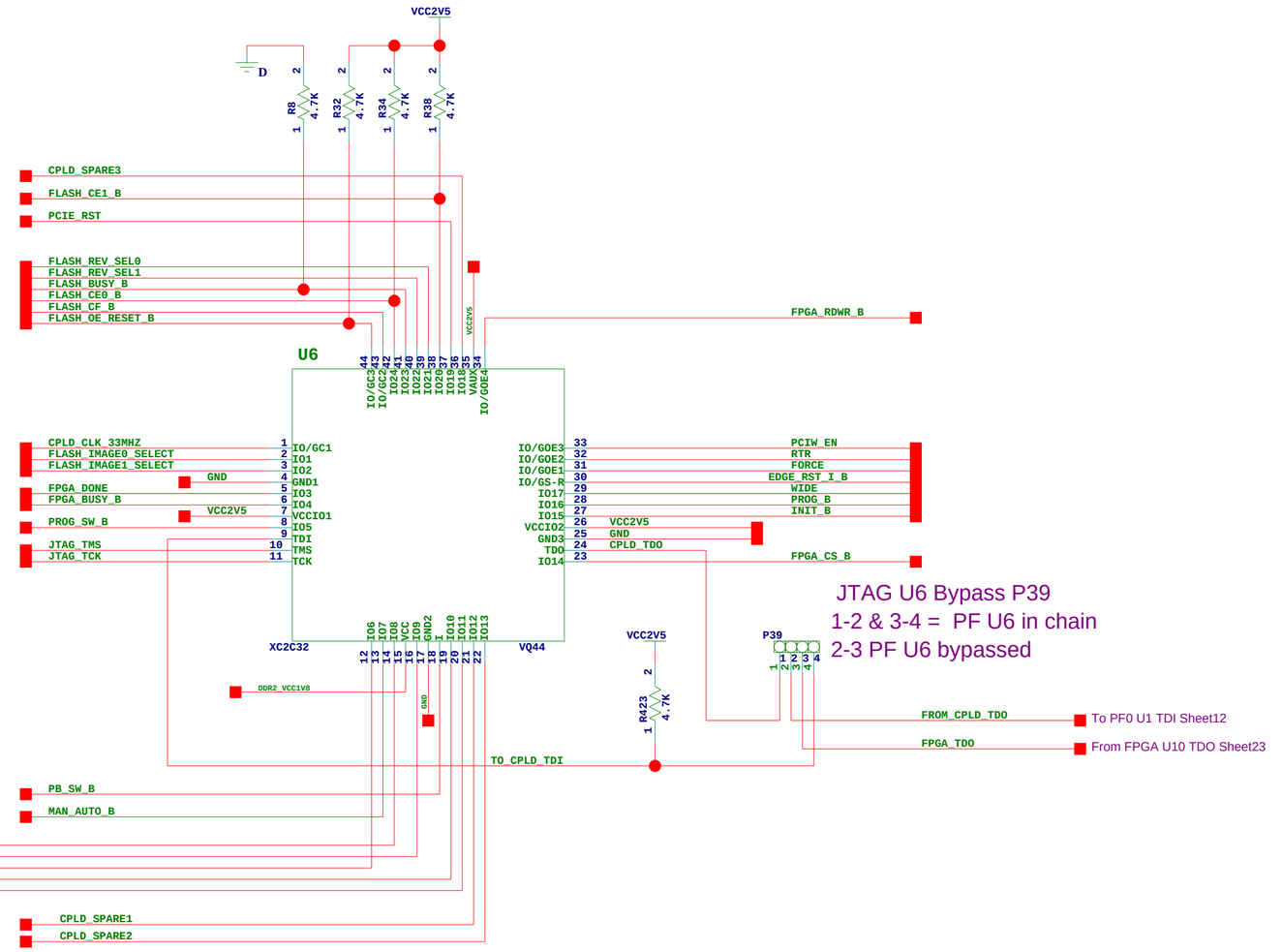
TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

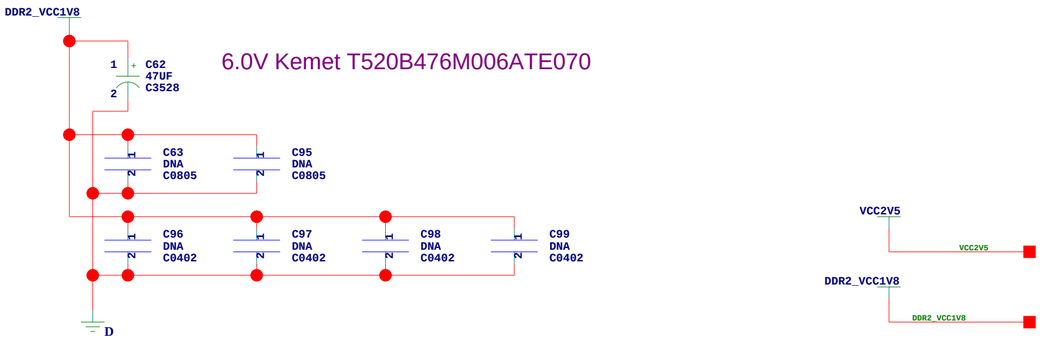
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		12 of 37	2-27-2008_10:44



CPLD Inputs



1.8V CPLD



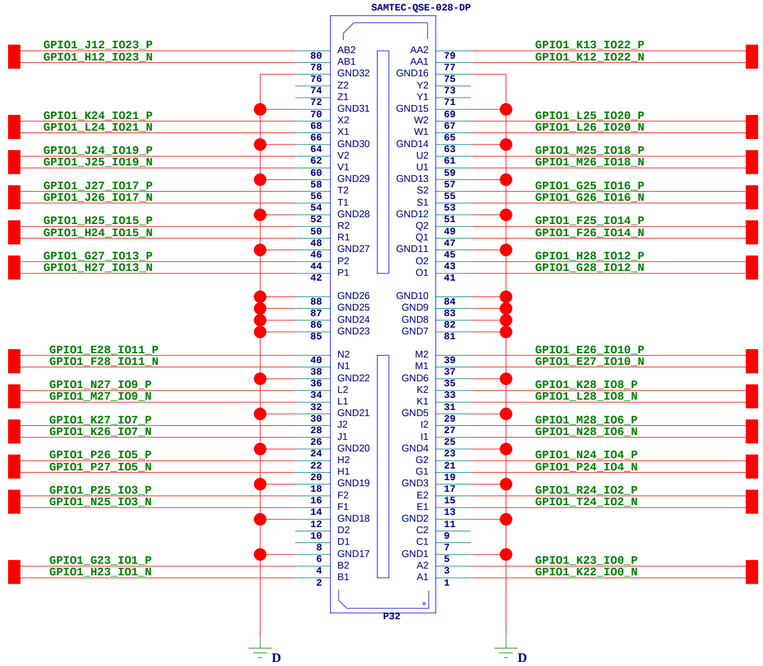
Dynamic Reconfig. CPLD

Xilinx

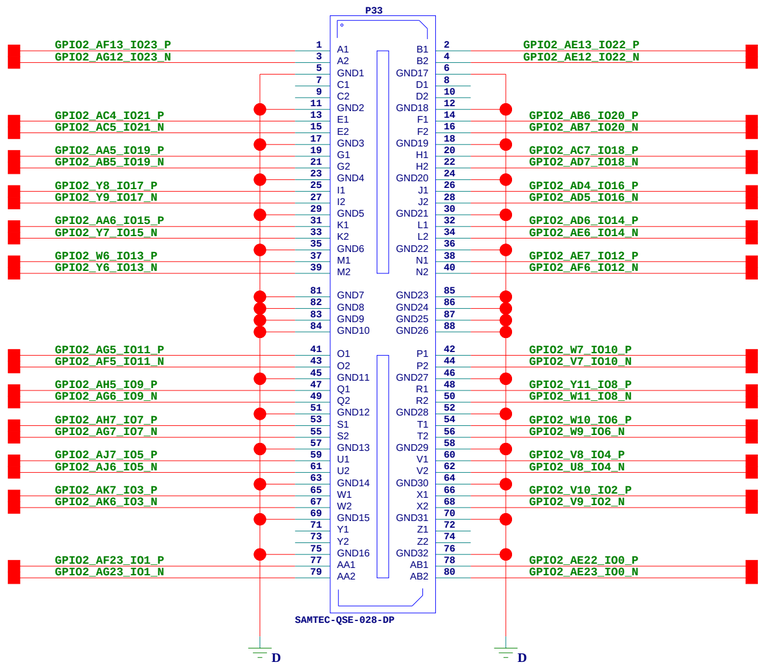
TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		13 of 37	2-27-2008_11:17



GPIO1



GPIO2

GPIO1_[21:02] P32 <=> Bank19
GPIO1_[23,22,01,00] P32 <=> Bank1

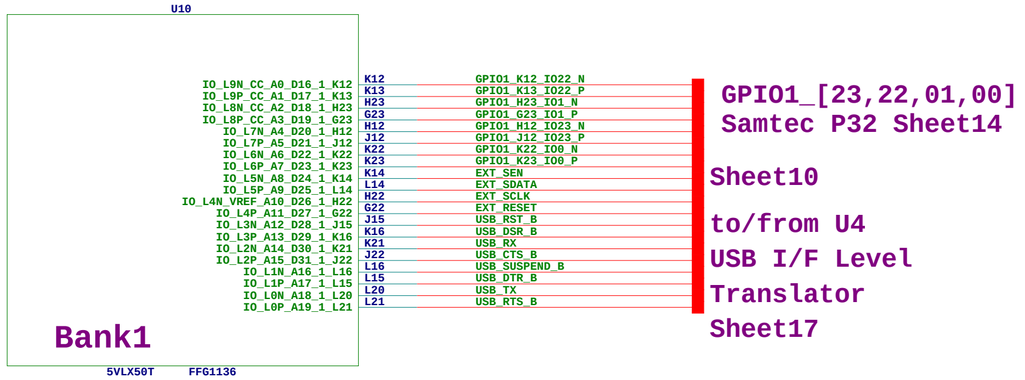
GPIO2_[21:02] P33 <=> Bank18
GPIO2_[23,22,01,00] P33 <=> Bank2

Sheet15

GPIO - 2xQSE SamtecDP Connector

Xilinx

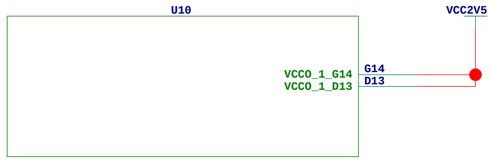
TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280444
SIZE	C
DWG NO	0381219
REV	02
DRAWN BY	DAVID NAYLOR
SCALE	
SHEET	14 of 37
	2-27-2008_14:10

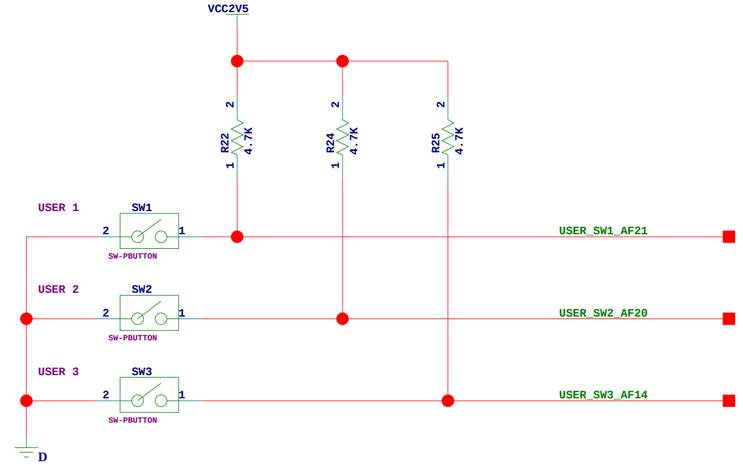


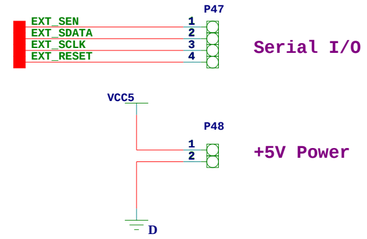
GPIO1_[23,22,01,00]
Samtec P32 Sheet14

Sheet10

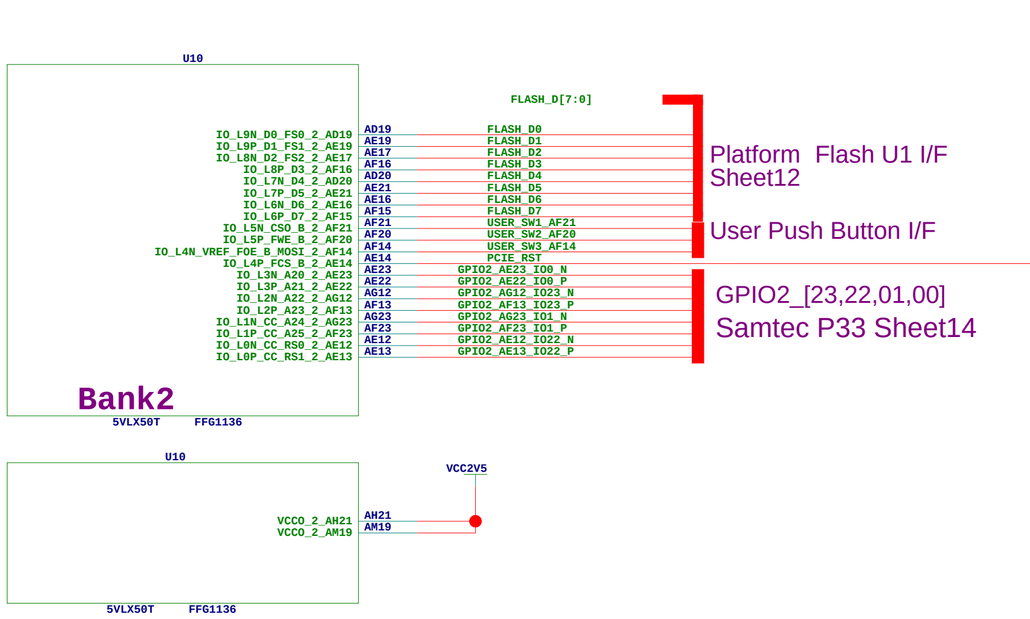
to/from U4
USB I/F Level
Translator
Sheet17







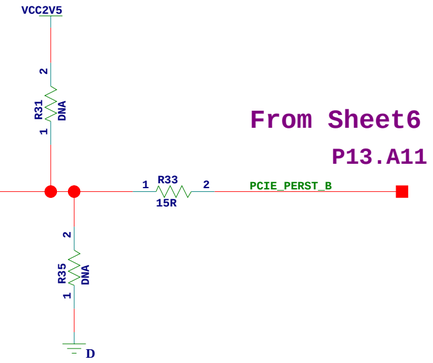
Samtec Mezzanine Board Support



Platform Flash U1 I/F
Sheet12

User Push Button I/F

GPIO2_[23,22,01,00]
Samtec P33 Sheet14



Also to Sheet13 CPLD U6.37

Bank1 USB-UART I/F,GPIO1

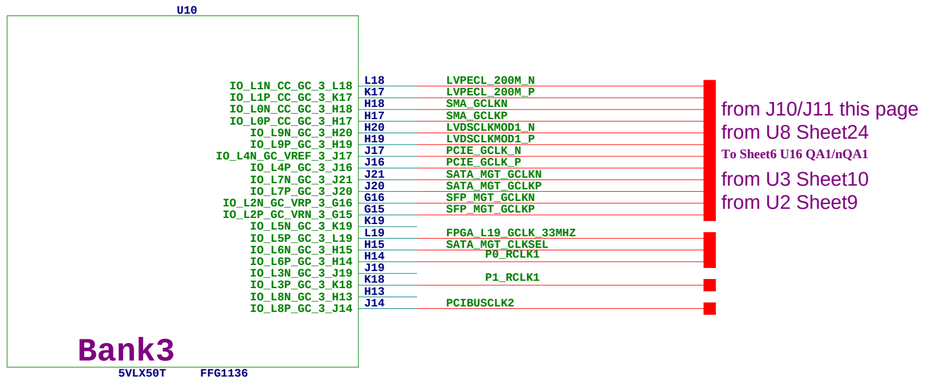
Bank2 PF U1 I/F,GPIO2,UserPB

Xilinx

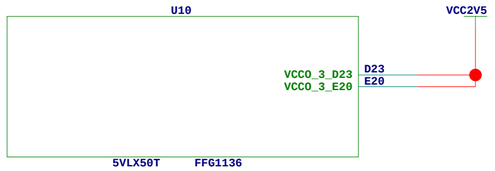
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

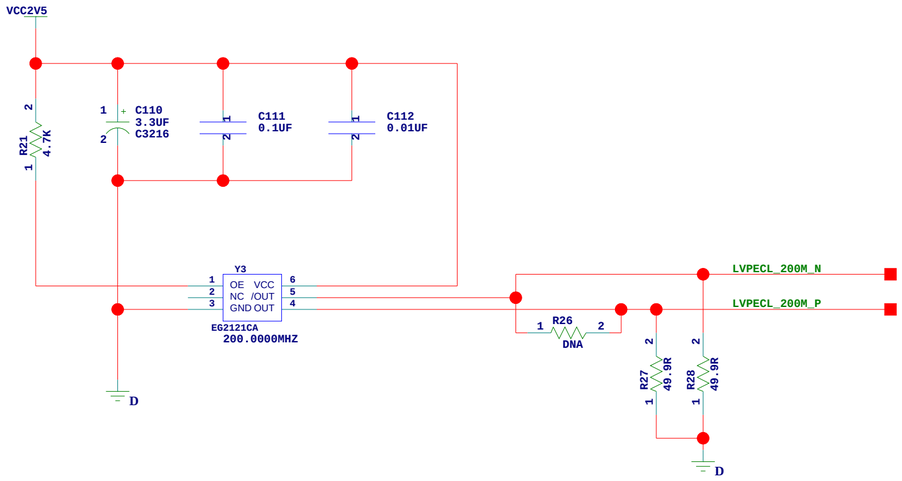
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		15 of 37	2-27-2008_14:12

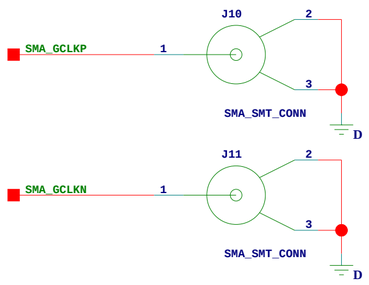


from J10/J11 this page
from U8 Sheet24
To Sheet6 U16 QA1/nQA1
from U3 Sheet10
from U2 Sheet9



200.0000MHz Epson EG2121CA-200.0000M-PHPAB





Bank3 Global Clock

200MHz Osc Y3 LVPECL

Bank3 Clocks

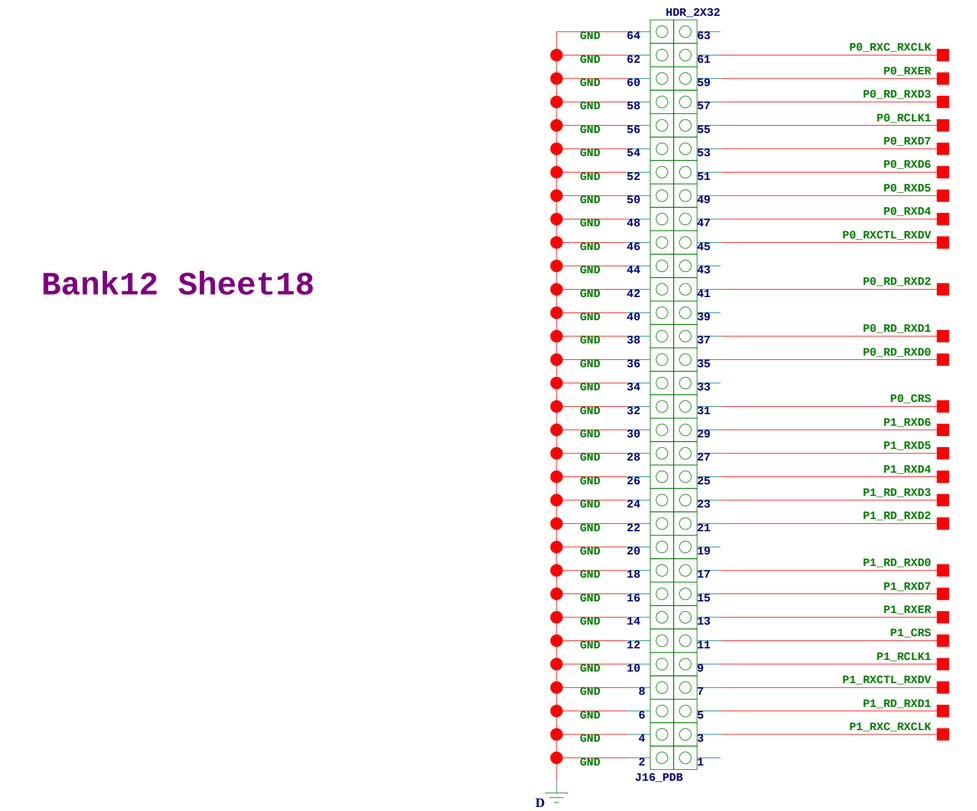
Xilinx

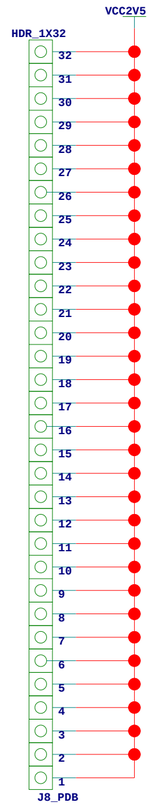
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

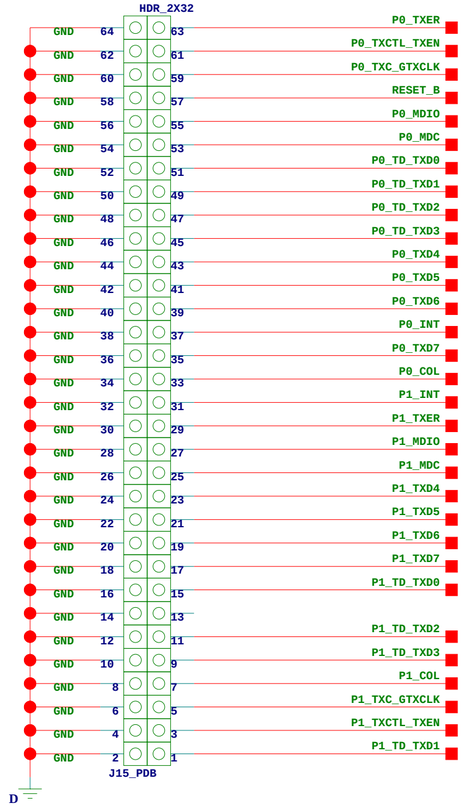
SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		16	37	2-27-2008_14:13

HW-AFX-BERG-EPHY Interface

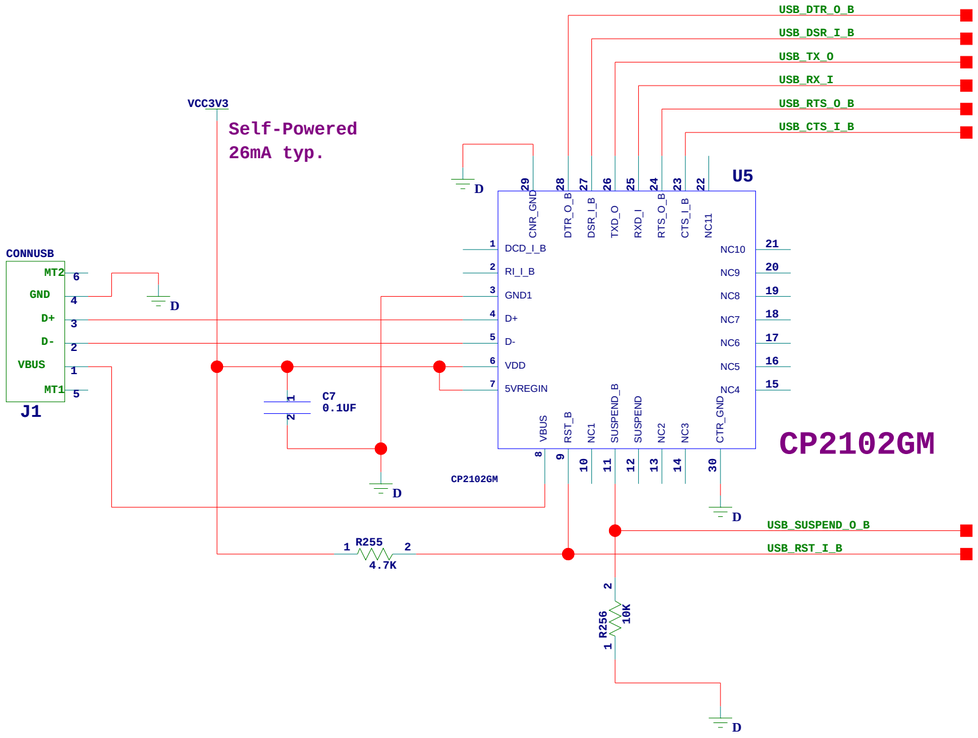


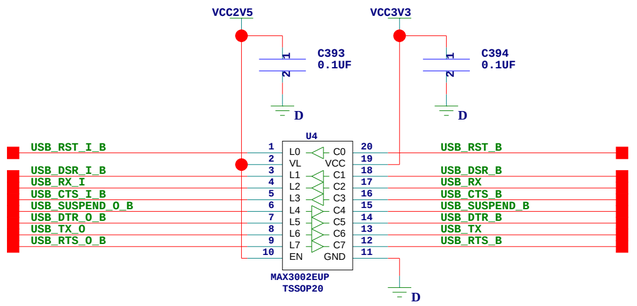




Bank12 Sheet18

Bank20 Sheet18





To/From FPGA
Bank1 Sheet15

USB to RS232 Converter
(full UART interface implementation)

BERG EPHY Header

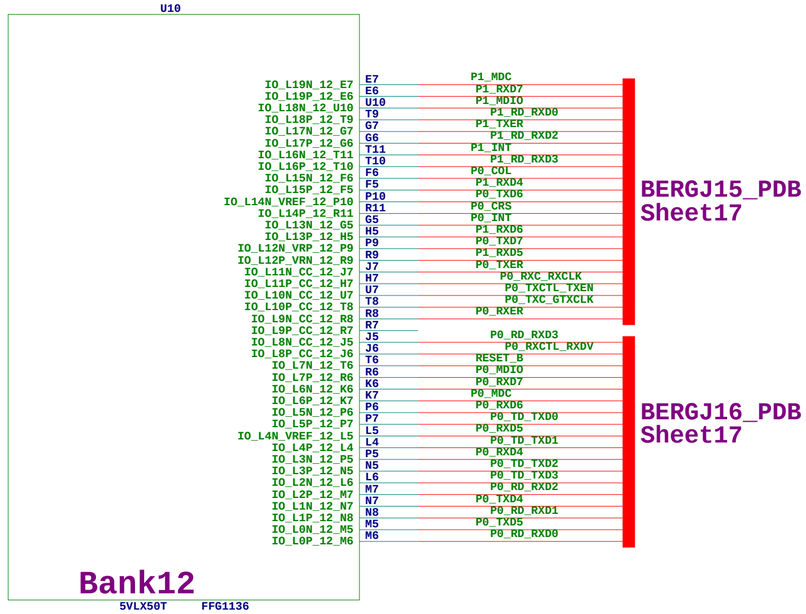
USB to RS232 Converter

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

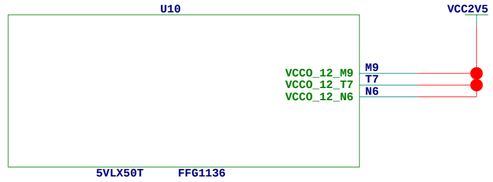
SIZE	DWG NO	REV
C	0381219	02

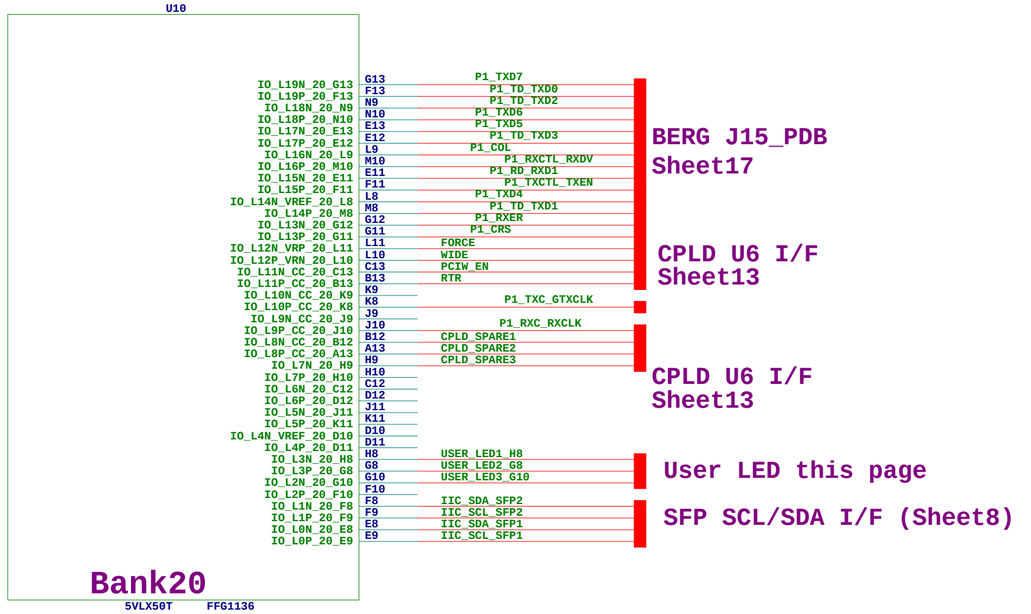
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		17 of 37	2-27-2008_11:24



BERGJ15_PDB
Sheet17

BERGJ16_PDB
Sheet17





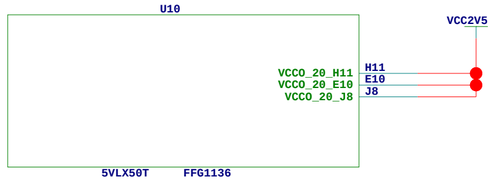
BERG J15_PDB
Sheet17

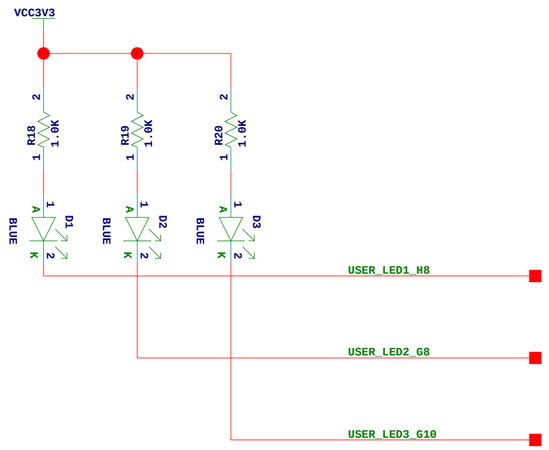
CPLD U6 I/F
Sheet13

CPLD U6 I/F
Sheet13

User LED this page

SFP SCL/SDA I/F (Sheet8)





Bank12 BERG I/F

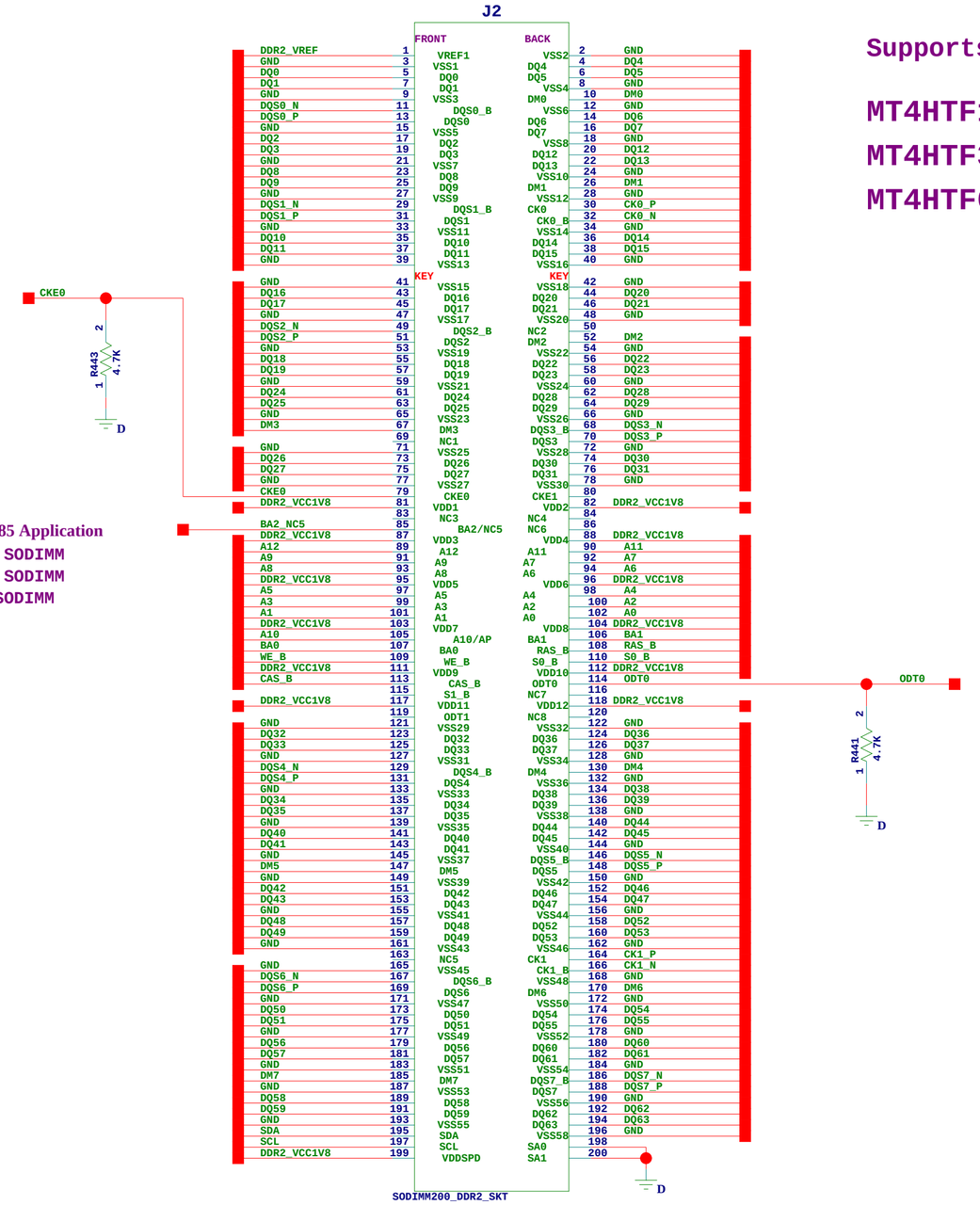
Bank20 BERG HDR, CPLD I/F

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		18 of 37	2-27-2008_14:15



Pin85 Application

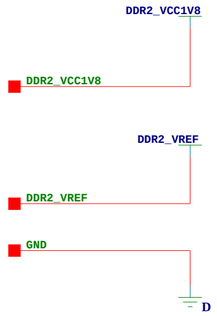
- NC for 256MB SODIMM
- NC for 512MB SODIMM
- BA2 for 1GB SODIMM

Supports Micron single rank SODIMMs:

MT4HTF1664HY-667 128MB

MT4HTF3264HY-667 256MB

MT4HTF6464HY-53E 512MB



SODIMM DDR-2 200-pin 1.8V memory socket

121 pin interface

Xilinx

TITLE

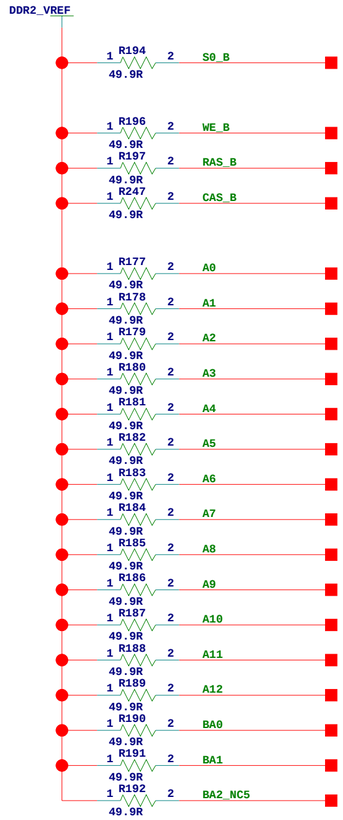
SCHEM, ML555

PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

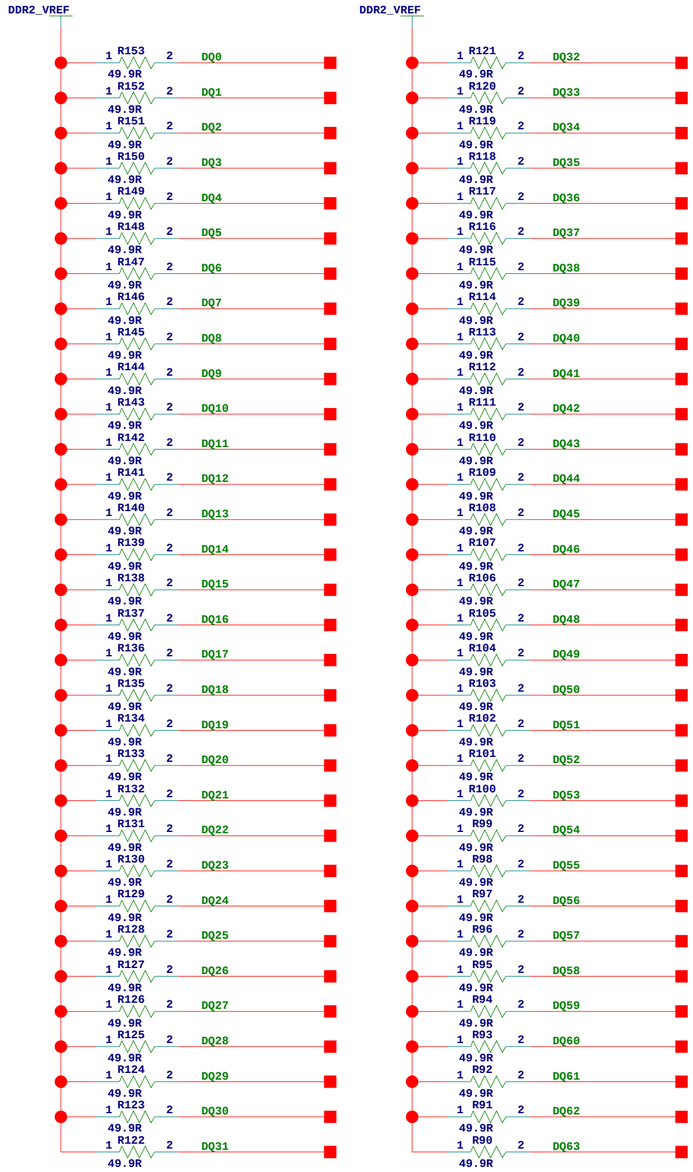
DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		19	37	2-27-2008_11:24

SODIMM End of bus



For DQS, ODT active on the memory module

FPGA End of bus



For DQS, FPGA will implement DIFF_SSTL18_II

DDR-2 SODIMM Terminations

Xilinx

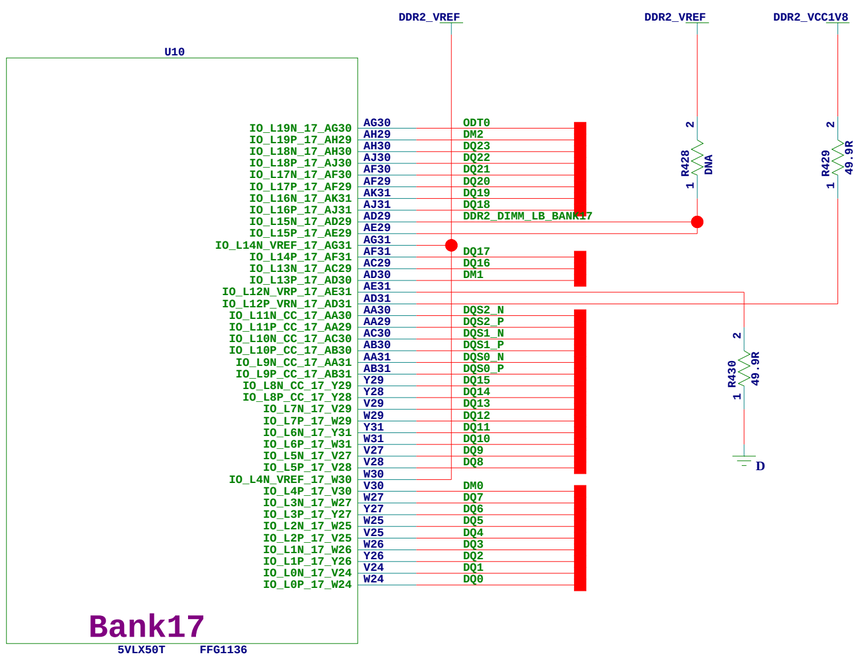
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		20 of 37	2-27-2008_11:24

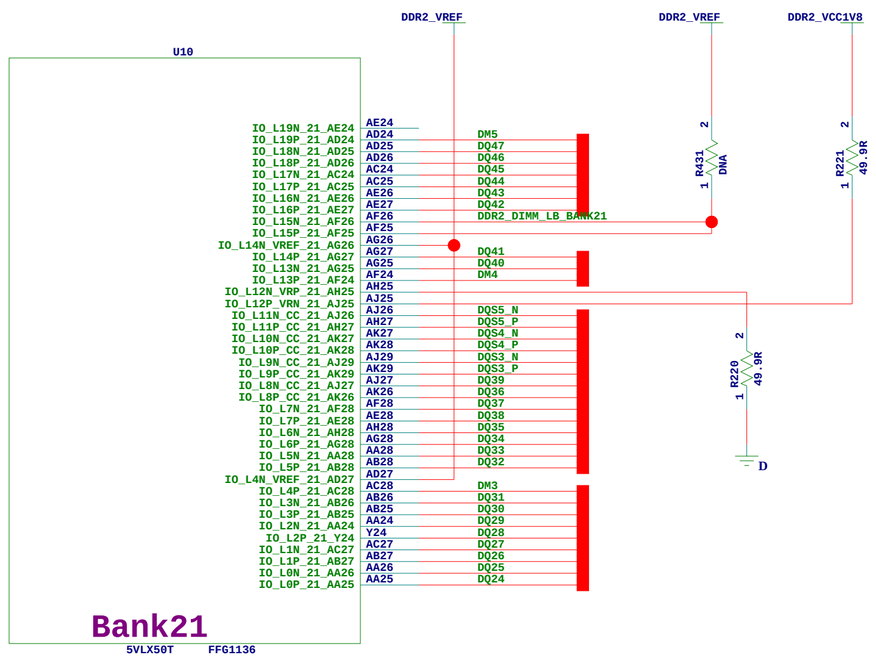
CK0: DQ[31:0]

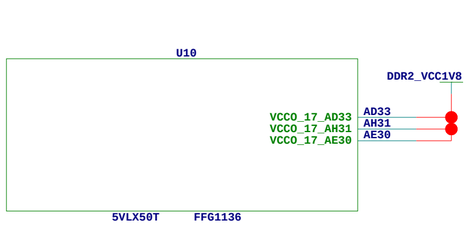
LOOP LENGTH = SUM (CK0 + DQS0)

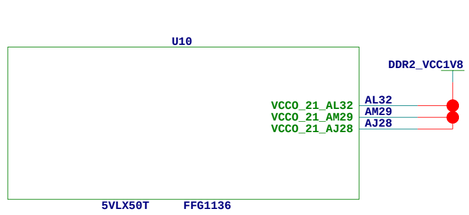


CK0: DQ[31:0] CK1: DQ[63:32]

LOOP LENGTH = SUM (CK1 + DQS4)







Banks 17,21 DDR2 SODIMM I/F to Sheet19

Xilinx

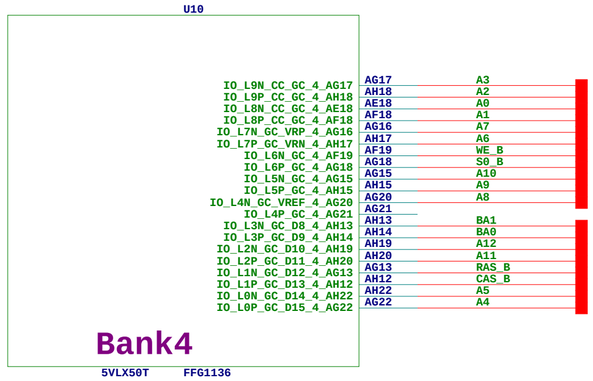
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

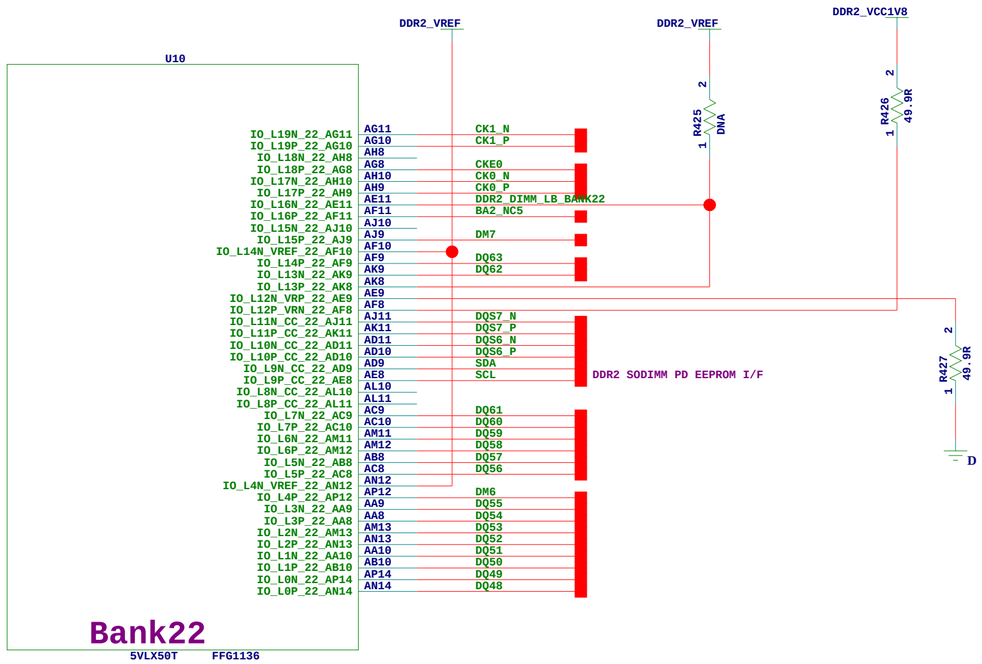
SIZE	DWG NO	REV
C	0381219	02

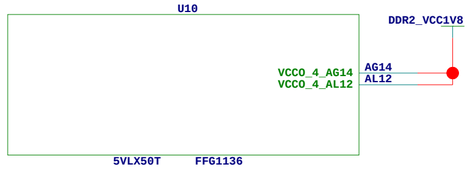
DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		21	37	2-27-2008_14:15

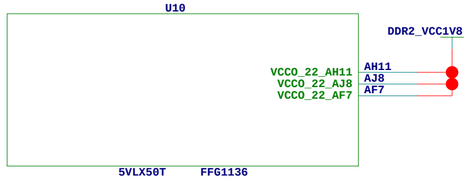
CK1: DQ[63:32]

LOOP LENGTH = SUM (CK1 + DQS6)









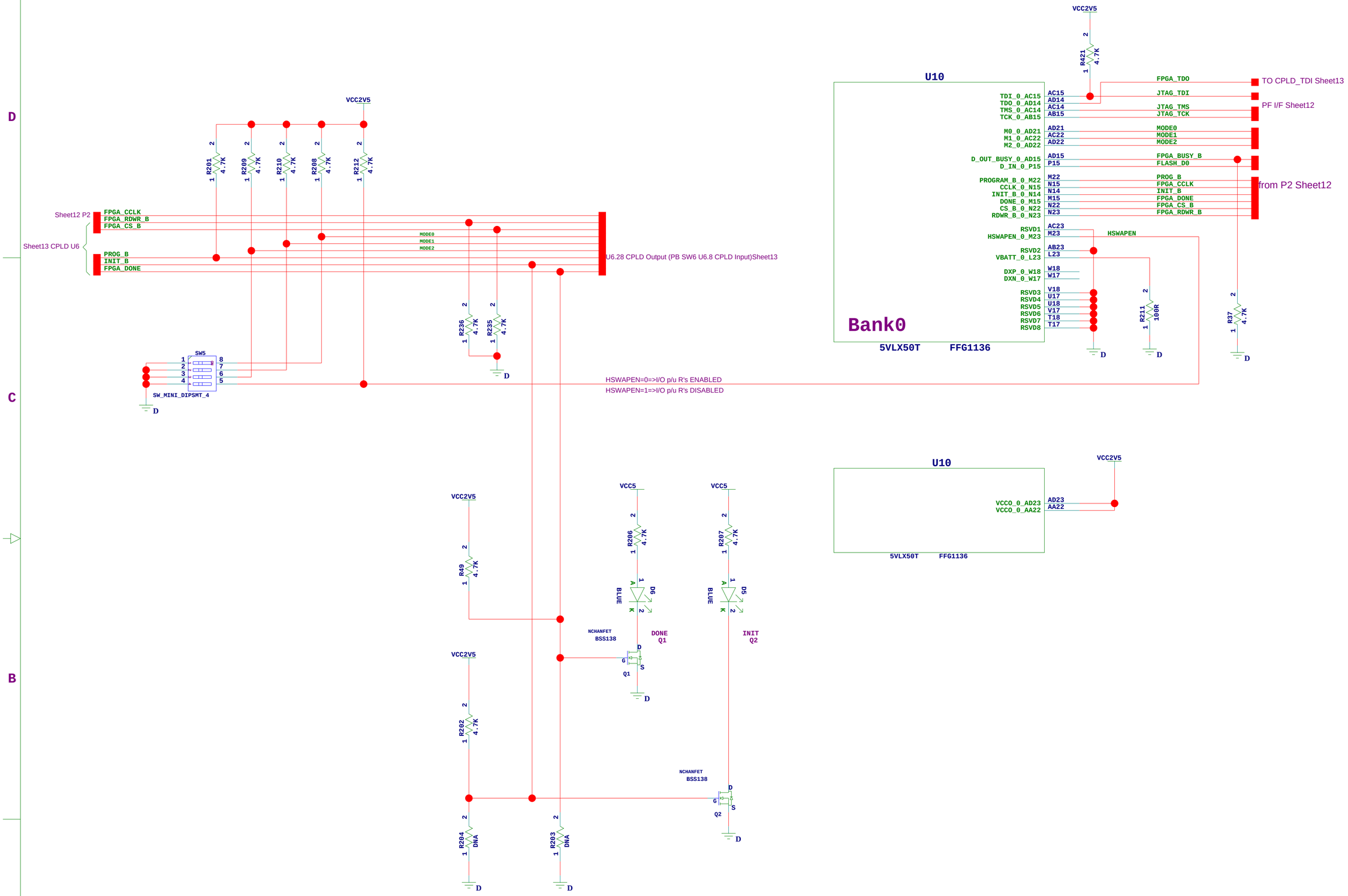
Banks 4,22 DDR2 SODIMM I/F to Sheet19

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		22	37	2-27-2008_14:15



Bank0 CONFIGURATION I/F

Xilinx

TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280444
SIZE	C
DWG NO	0381219
REV	02
DRAWN BY	DAVID NAYLOR
SCALE	
SHEET	23 of 37
	2-27-2008_14:17

Freq. Load Button

Xtal Sel

VCO Sel

Parallel Freq. Set

10MHz

to Sheet16
Bank3 GCLK SODIMM I/F

to Sheet25 SW17.9

to Sheet6
MGT X0Y1 MGTREFCLK

Programmable ICS "Clock_1" 31.25MHz - 700MHz

ICS8442AY

SW-PBUTTON

SW_MINI_DIPSMT_8

MA-505
10MHZ

NCHANFET
BSS138

TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280444
SIZE	C
DWG NO	0381219
REV	02
DRAWN BY	DAVID NAYLOR
SCALE	
SHEET	24 of 37
	2-27-2008_11:24

Xilinx

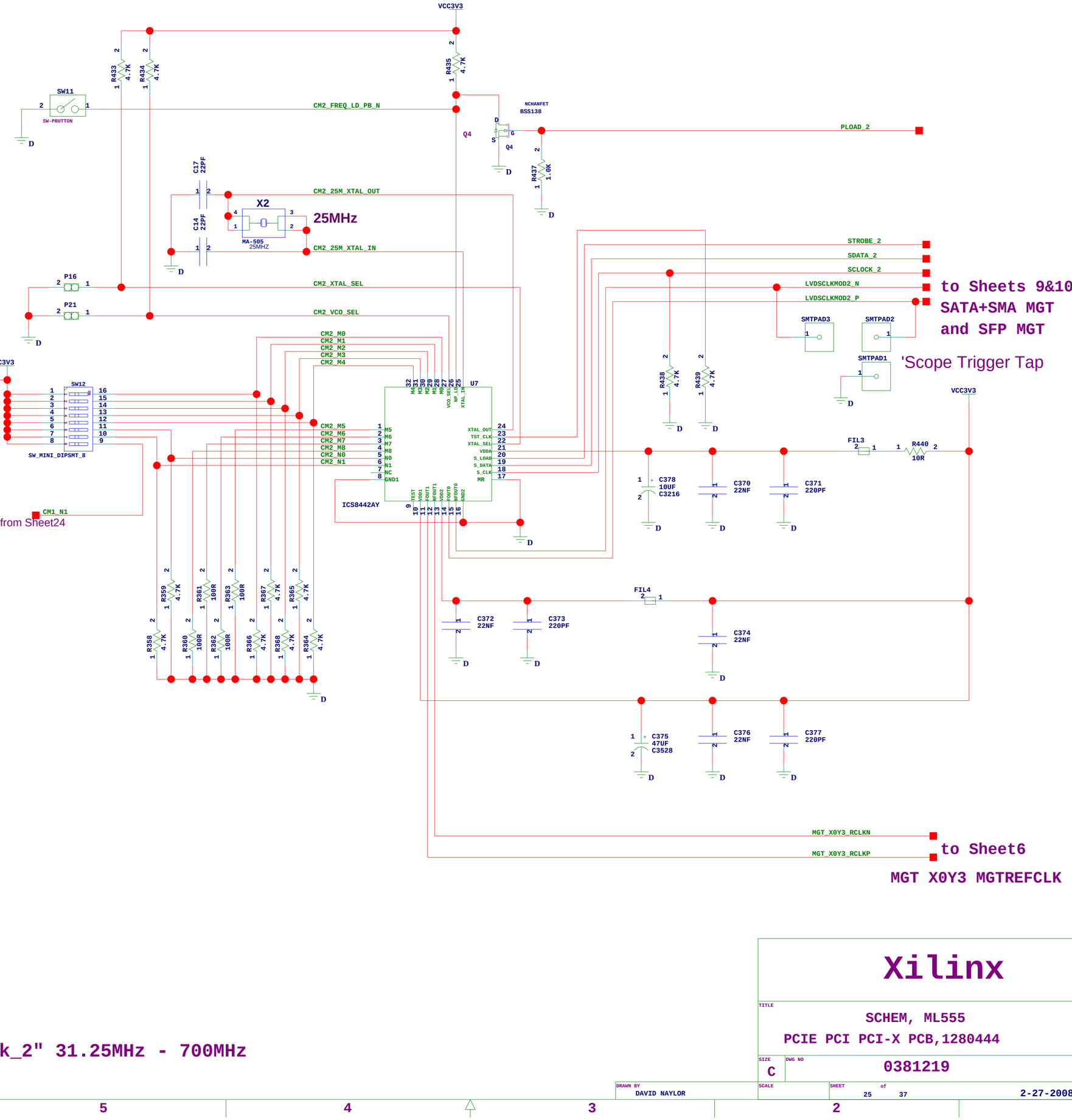
Freq. Load Button

Xtal Sel

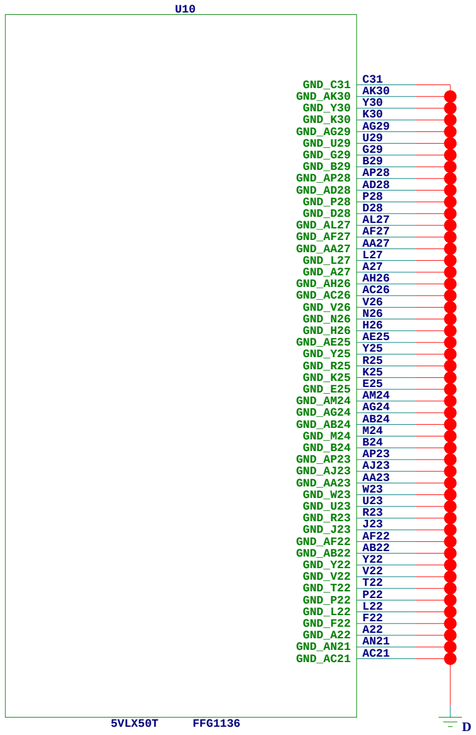
VCO Sel

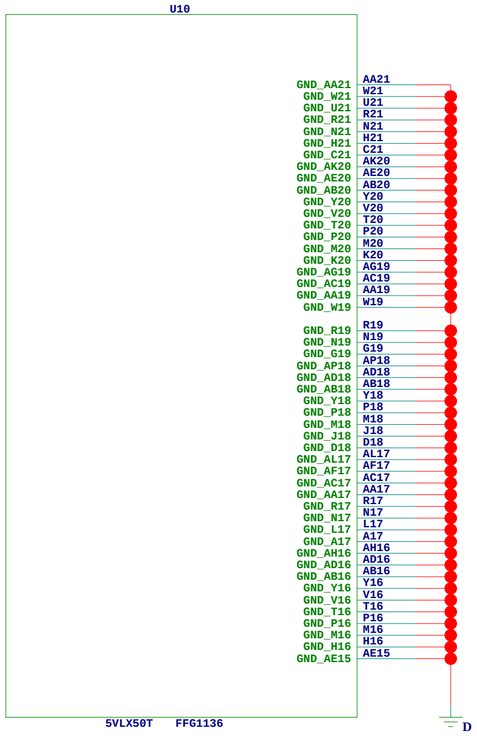
Parallel Freq. Set

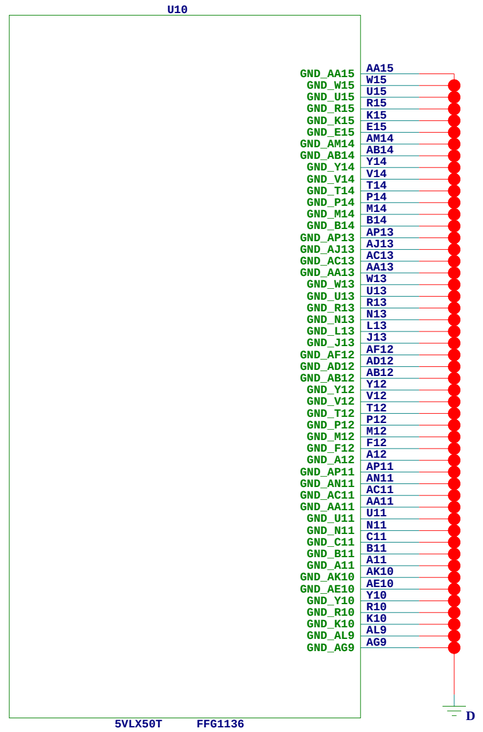
Programmable ICS "Clock_2" 31.25MHz - 700MHz

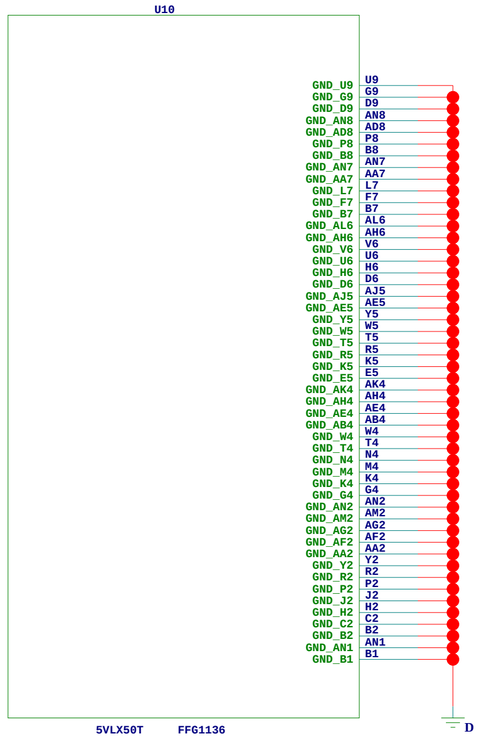


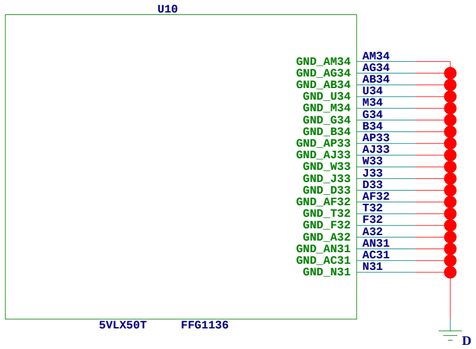
Xilinx	
TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280444
SIZE	C
DWG NO	0381219
REV	02
DRAWN BY	DAVID NAYLOR
SCALE	
SHEET	25 of 37
	2-27-2008_11:24

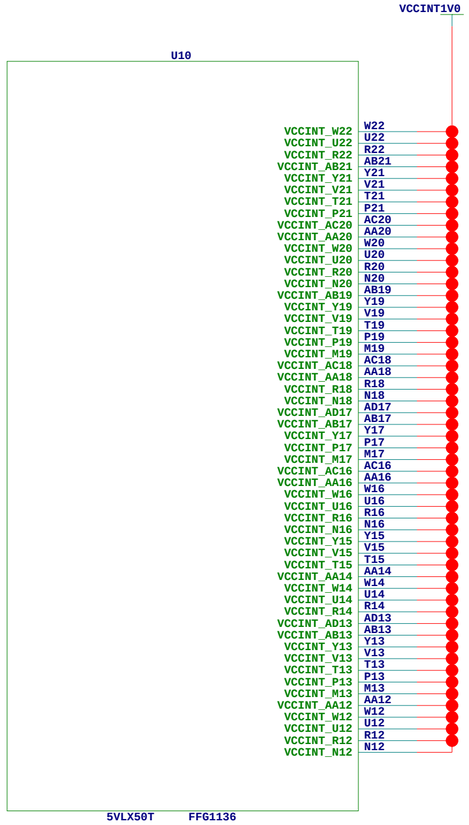


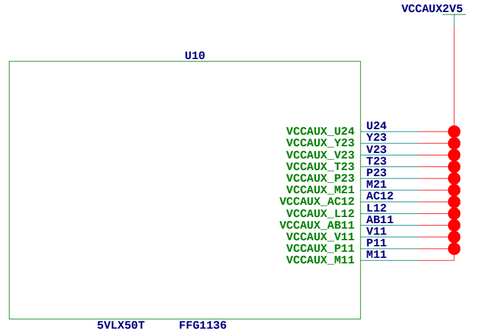


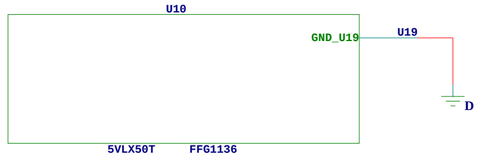












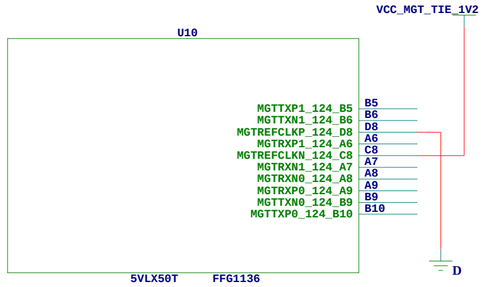
FPGA Core Power, and GND

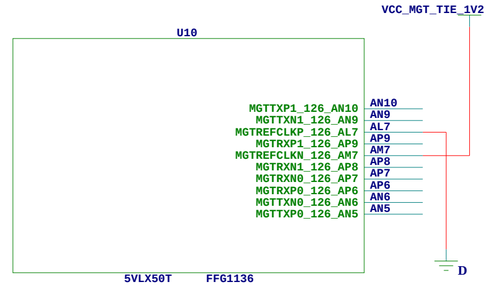
Xilinx

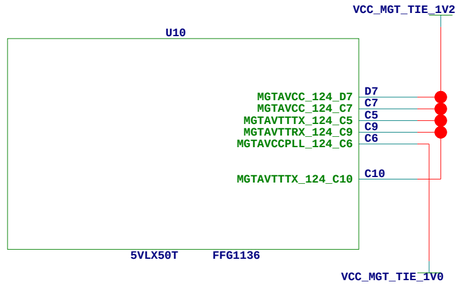
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

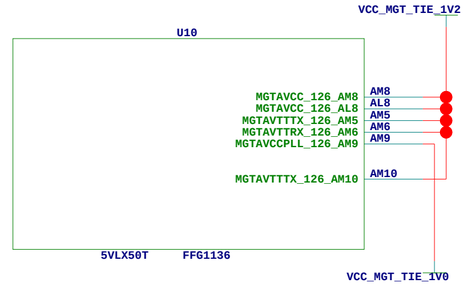
SIZE	DWG NO	REV
C	0381219	02

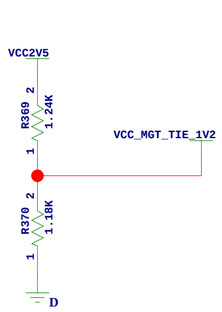
DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		26	37	2-27-2008_14:22

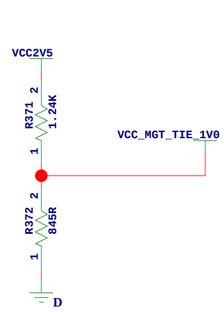












GTP TIE OFF TAPS

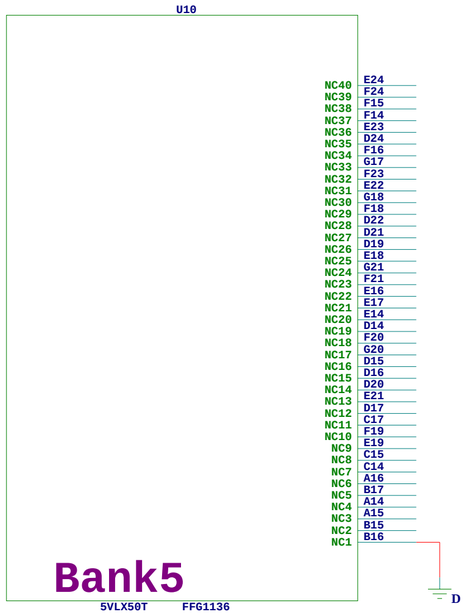
Unused MGTs

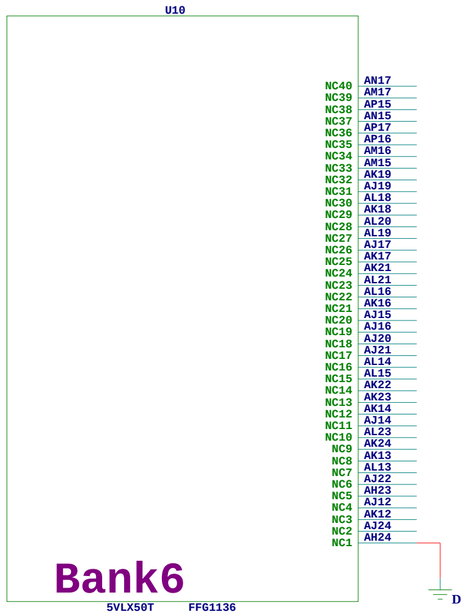
Xilinx

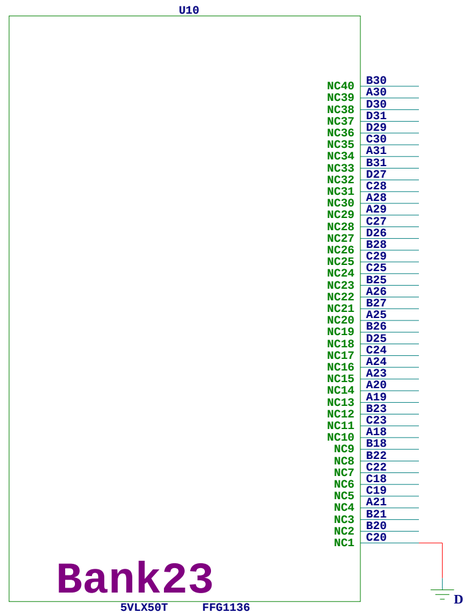
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

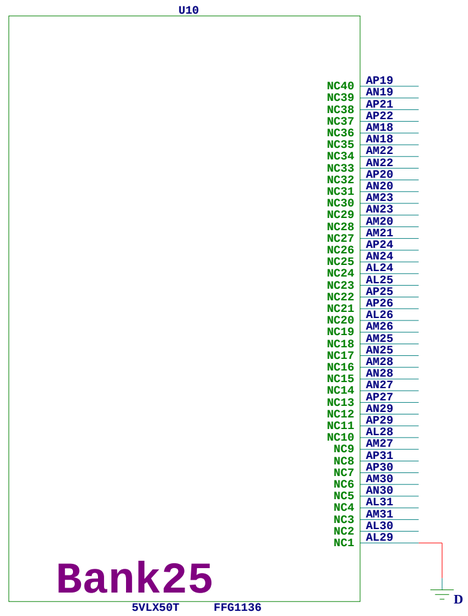
SIZE	DWG NO	REV
C	0381219	02

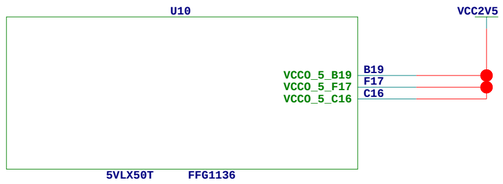
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		27 of 37	2-27-2008_14:22

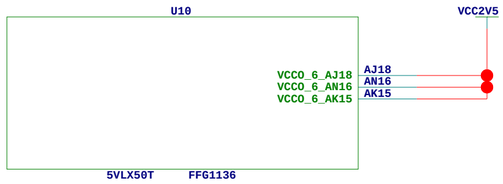


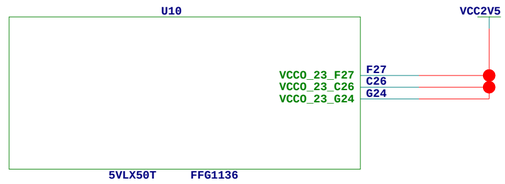


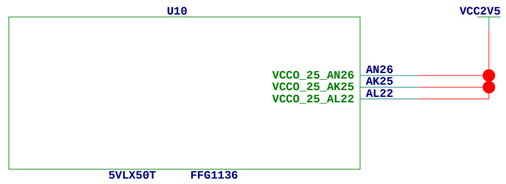




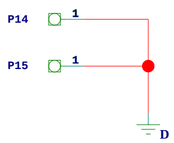








GND TP

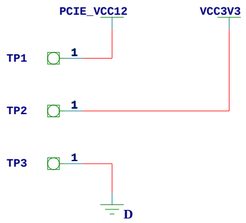


Fiducials

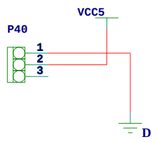
Comp Side

Solder Side

Stand-Alone Power Taps



PTH Holes to solder wire into



Radian INF35001-16
Fan Heat Sink Power

Metal Bracket Mounting Holes
(0.116" 4-40 clearance)

EPHY Daughter Card Standoff Mounting Holes
(0.144" 6-32 clearance)

Banks 5,6,23,25 are N/C

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

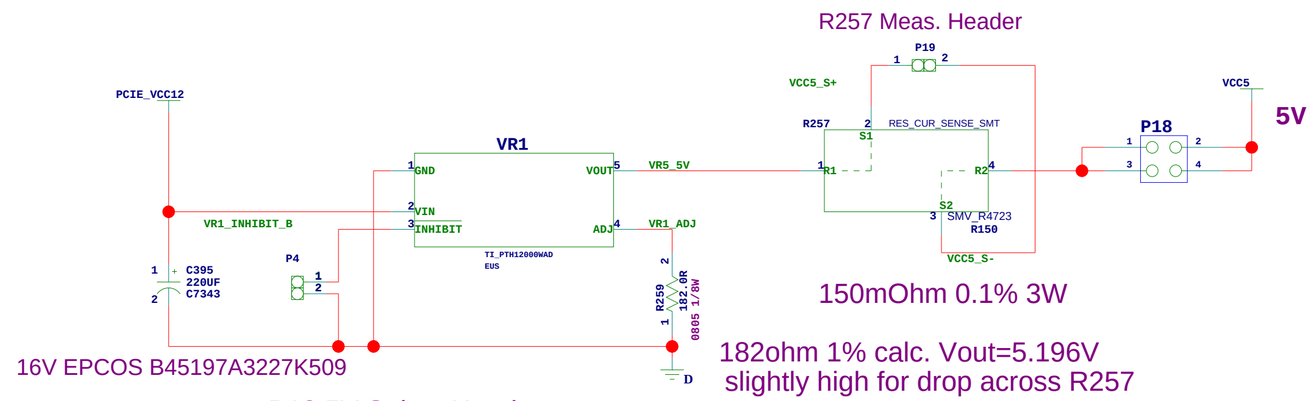
SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		28 of 37	2-27-2008_14:22

PCIe 12V input conversion to VCC5

PCIe 12.0V @ 5.5A (75W Slot)
PCIe 3.3V @ 3.0A (75W Slot)

PCI   5.0V @ 5.0A (25W Slot)
PCI   3.3V @ 7.6A (25W Slot)



16V EPCOS B45197A3227K509

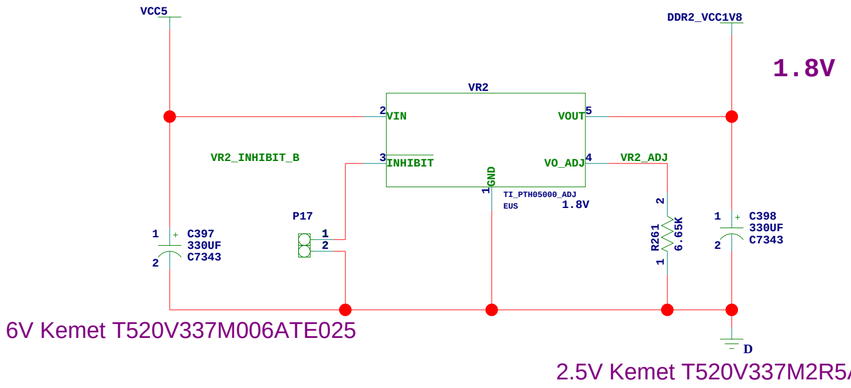
150mOhm 0.1% 3W

182ohm 1% calc. Vout=5.196V
slightly high for drop across R257
(typ. VCC5 = 5.08V)

P18 5V Select Header

1-2 & 3-4 ON = PCIe Mode
1-2 & 3-4 OFF = PCI/PCI-X Mode

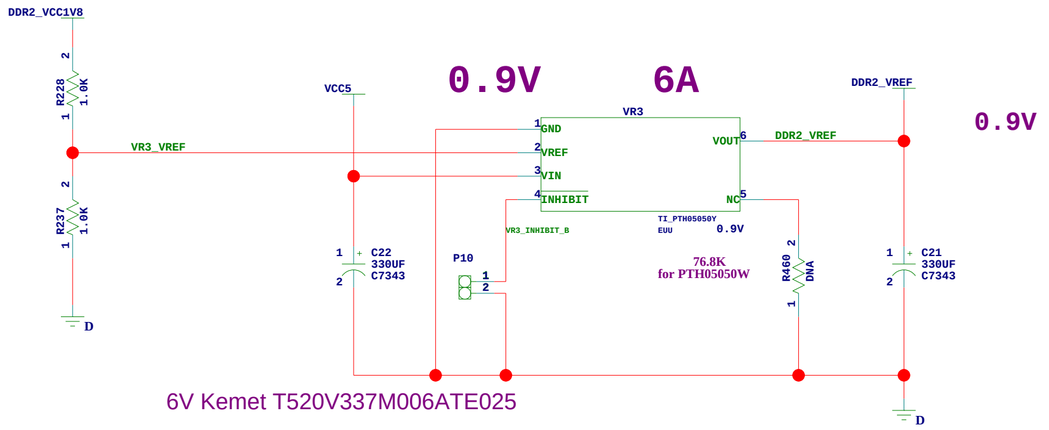
5V input to DDR2 1.8V output



6V Kemet T520V337M006ATE025

2.5V Kemet T520V337M2R5ATE025

1.8V DDR2 reference input to 0.9V DDR-2 Vtt



6V Kemet T520V337M006ATE025

2.5V Kemet T520V337M2R5ATE025

VR1 PTH12000 12Vin-to-5Vout
VR2 PTH05000 5Vin-to-1.8Vout
VR3 PTH05050 1.8V/2 in-to-0.90V out

Power Regulators - Sheet 1

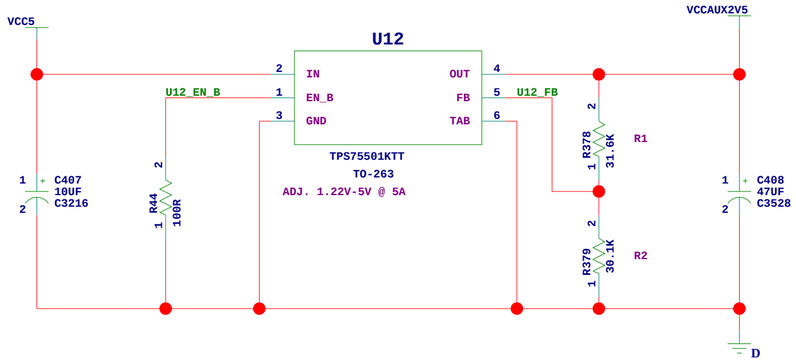
Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

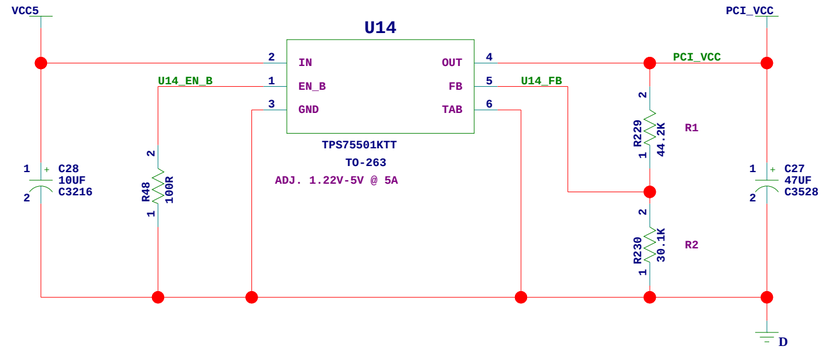
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		29 of 37	2-27-2008_11:24

2.5089V @5A
U12 2.5V Vccaux



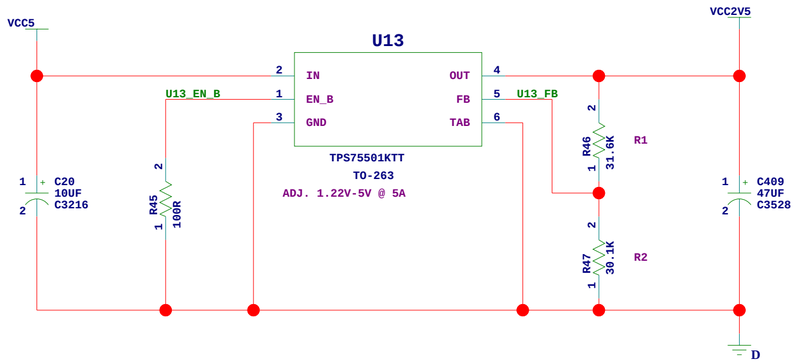
6.0V Kemet T520B476M006ATE070

3.0214V @5A
U14 3.0V PCI_VCC



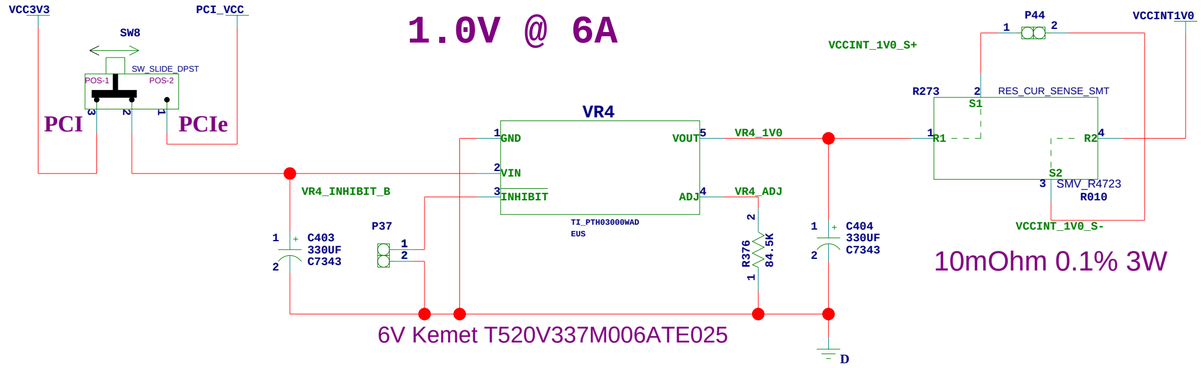
6.0V Kemet T520B476M006ATE070

2.5089V @5A
U13 2.5V Vcco



6.0V Kemet T520B476M006ATE070

3.0V input to FPGA Vccint 1.0V @ 6A



6V Kemet T520V337M006ATE025

10mOhm 0.1% 3W

Bus Mode	SW8 Position	VCCNIT_1V0 via VR4 from
PCIe	2	U14 PCI_VCC 3.0V Regulator
PCI/PCI-X	1	PCI Bus 3.3V

VR4 PTH03000 3.3Vin-to-1.0Vout (Vccint)

U12 TPS75501 5Vin-to-2.5Vout (Vccaux)

U13 TPS75501 5Vin-to-2.5Vout (Vcco)

U14 TPS75501 5Vin-to-3.0Vout (PCI_VCC)

1Vx4A=4W

4W/3V=1.33A

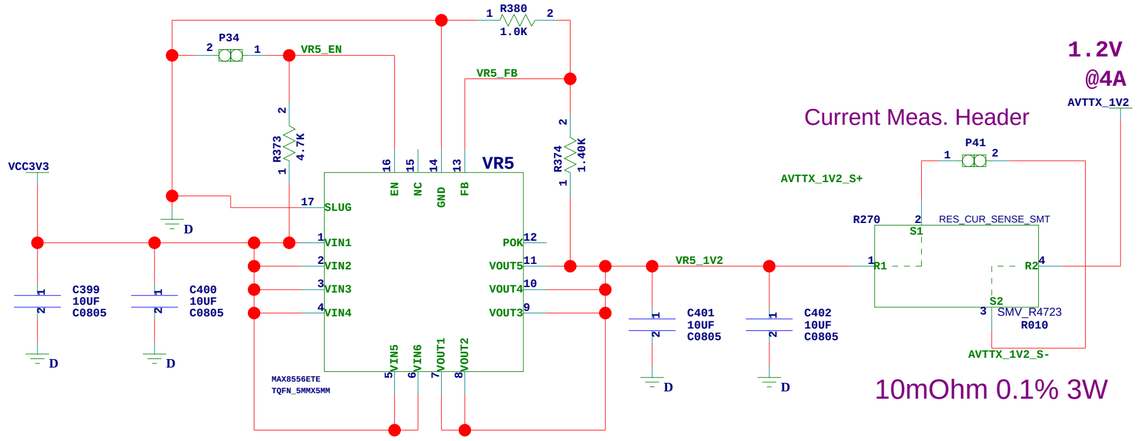
Power Regulators - Sheet 2

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		30 of 37	2-27-2008_11:24

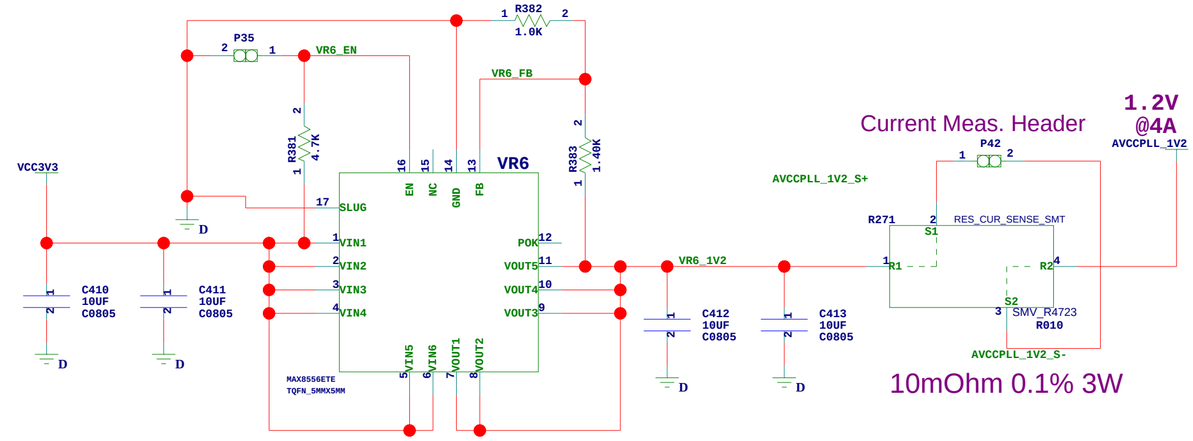


1.2V
@4A

AVTTX_1V2

Current Meas. Header

10mOhm 0.1% 3W

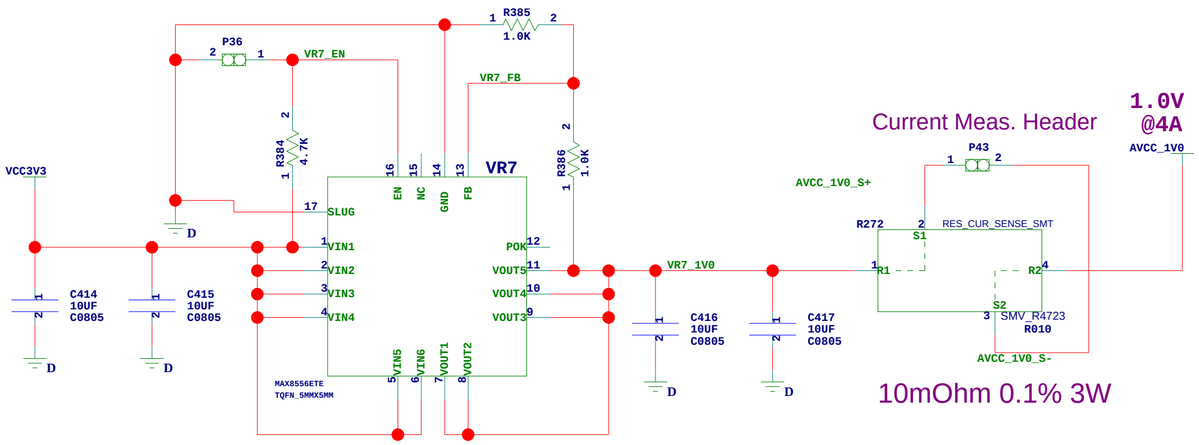


Current Meas. Header

1.2V
@4A

AVCCPLL_1V2

10mOhm 0.1% 3W



Current Meas. Header

1.0V
@4A

AVCC_1V0

10mOhm 0.1% 3W

Note: For more detailed information concerning MGT power and filtering requirements, see the Xilinx UG196 Virtex-5 FPGA RocketIO GTP Transceiver User Guide

Power Regulators - Sheet 3

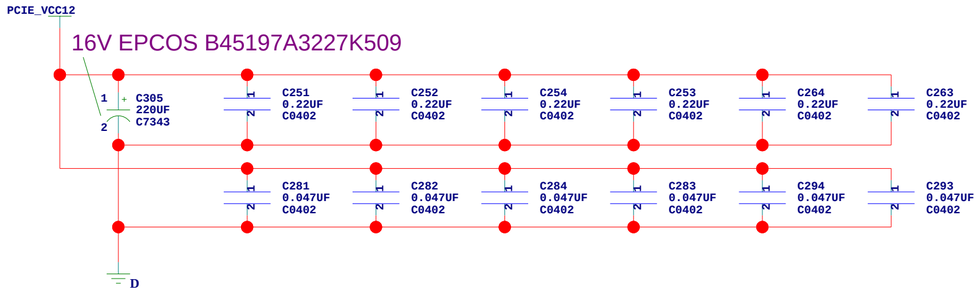
Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

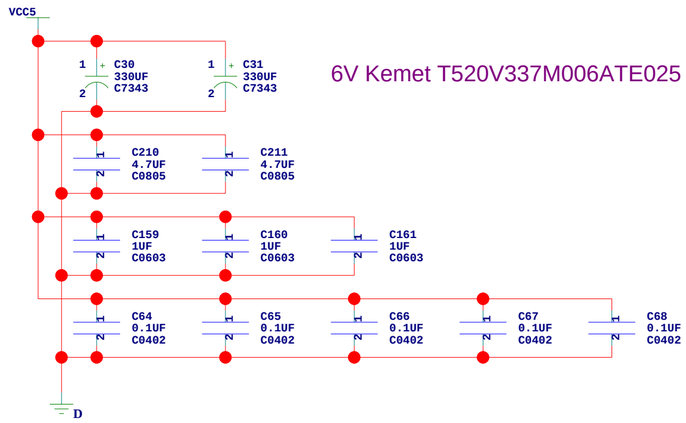
SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		31	37	2-27-2008_11:24

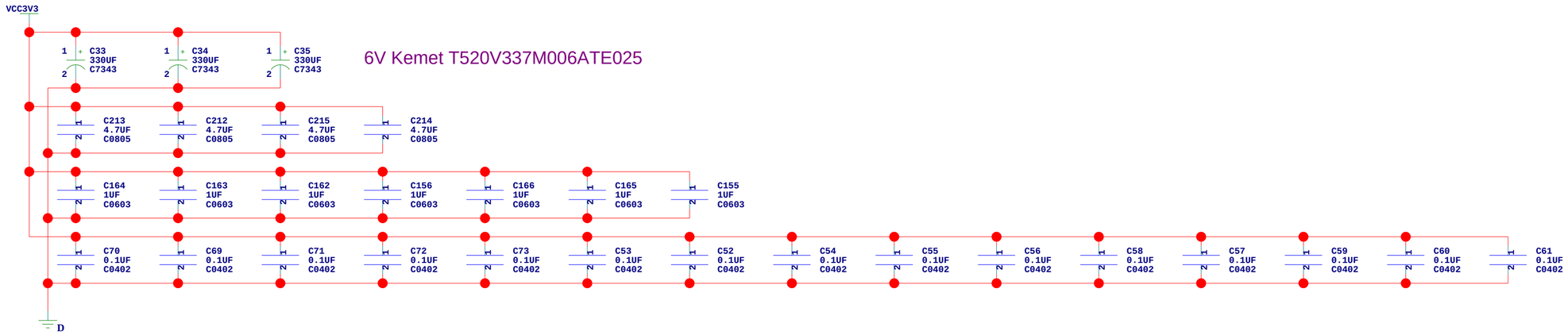
+12V from PCIe Edge Conn P13



5V VR1 Output + PCI Edge Conn P1



PCIe/PCI Edge +3.3V



Decoupling CAPS Page 1:

Decoupling CAPS for PCI Edge Conn.:
+12V(PCIe),+5V(PCI),+3.3V(both)

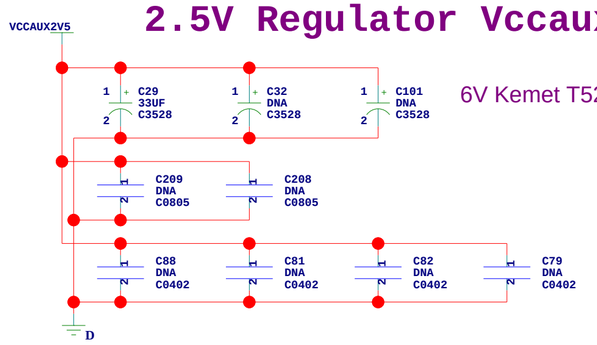
Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

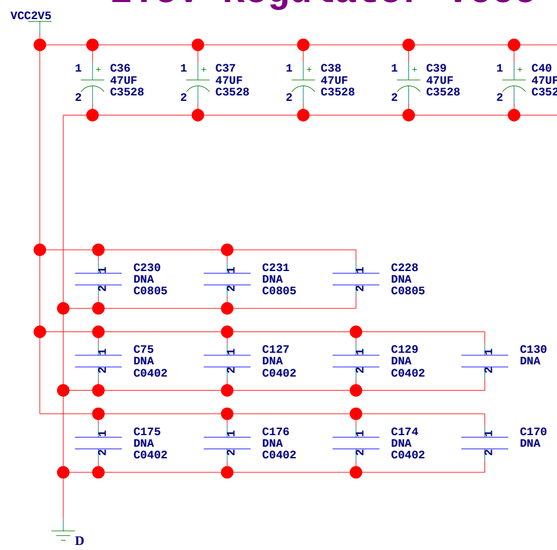
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		32 of 37	2-27-2008_11:24

2.5V Regulator Vccaux



6V Kemet T520V336M006ATE040

2.5V Regulator Vcco



6.0V Kemet T520B476M006ATE070

Reference Sheet 1, Note 4:

PCIe CEM Spec, Pg. 56 footnotes:

MGTs X0Y0,X0Y1,X0Y2,X0Y3 PCIe 8-Lane Edge Connector I/F

Decoupling CAPS Page 2:

Decoupling Caps for:

2.5V Regulator Vcco

2.5V Regulator Vccaux

Xilinx

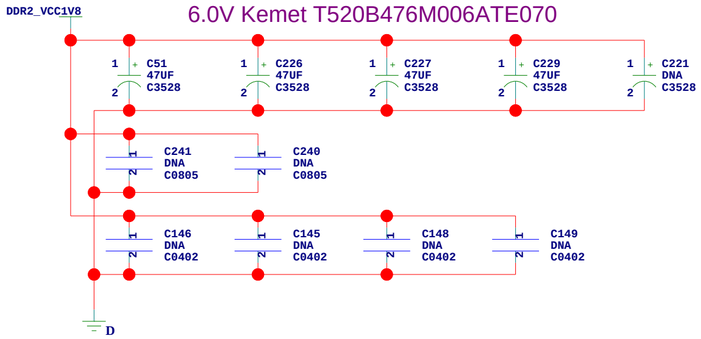
TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		33 of 37	2-27-2008_11:24

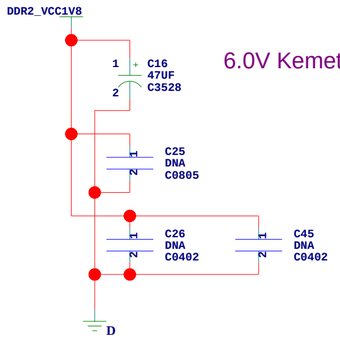
1.8V FPGA Vcco (Mem I/F)

6.0V Kemet T520B476M006ATE070



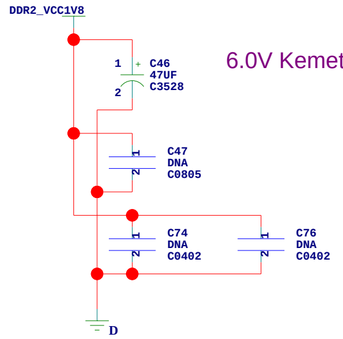
1.8V PF U1 Vccint

6.0V Kemet T520B476M006ATE070



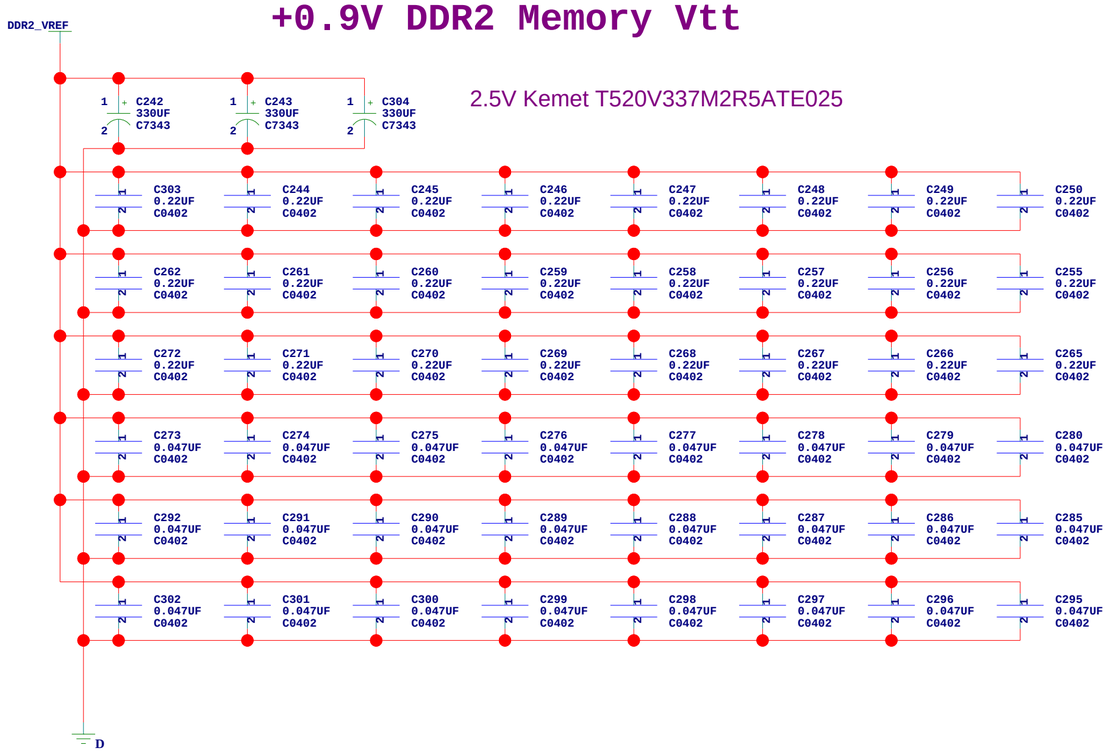
1.8V PF U15 Vccint

6.0V Kemet T520B476M006ATE070



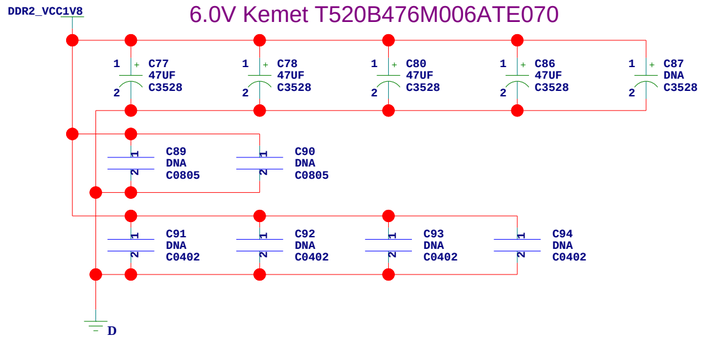
+0.9V DDR2 Memory Vtt

2.5V Kemet T520V337M2R5ATE025



1.8V Mem SODIMM

6.0V Kemet T520B476M006ATE070



Decoupling CAPS Page 3:

Decoupling Caps for:

1.8V Reg.Mem.SODIMM+FPGA Bank Vcco

1.8V Reg.PF Vccint

0.9VRegulator Vtt (84 PullUp R's on Sht20)

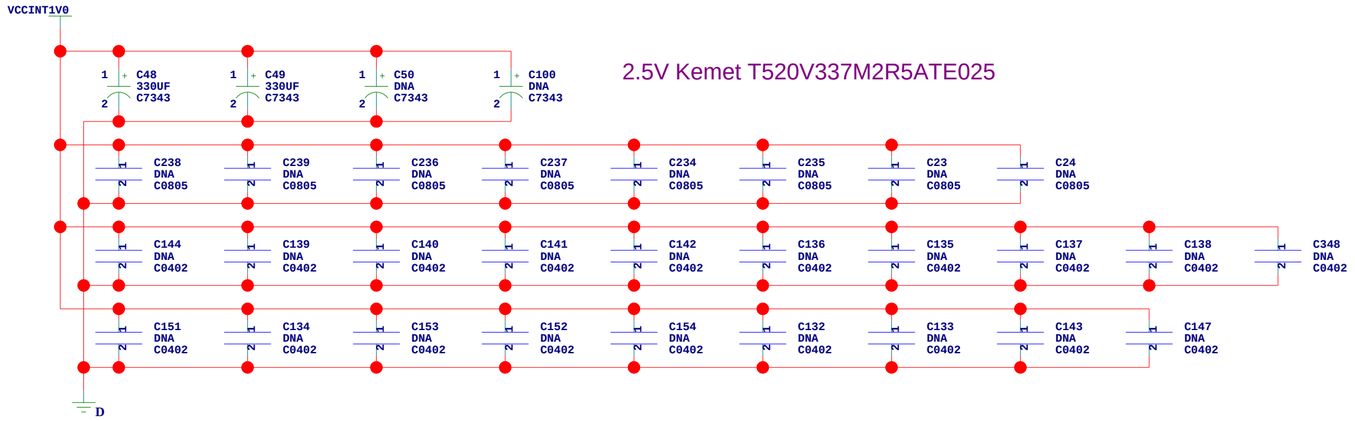
Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

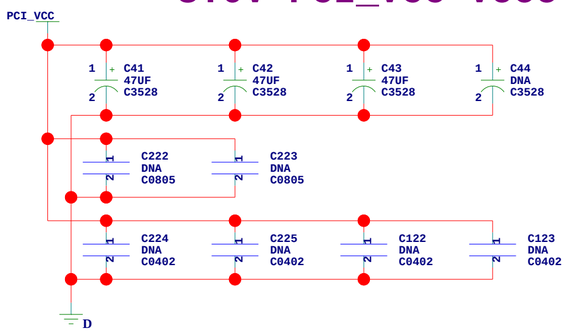
SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		34 of 37	2-27-2008_11:24

1.0V FPGA Vccint



3.0V PCI_VCC Vcco



Decoupling CAPS Page 4:

Decoupling Caps for:

- 1.0V Regulator FPGA Vccint
- 3.0V Regulator PCI_VCC Vcco

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	02

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		35	37	2-27-2008_11:24

VR5 MAX8556/7
AVTTTX/RX 1.2V
4A
MGT Supply

P34 Inhibit

VR6 MAX8556/7
AVCCPLL 1.2V
4A
MGT Supply

P35 Inhibit

VR7 MAX8556/7
AVCC 1.0V
4A
MGT Supply

P36 Inhibit

P4 Inhibit

VR1 PTH12000
PCIe12V=>VCC5
6A

P18

1 2 3 4

Jumper = on for PCIe
Jumper = off for PCI/PCI-X

VR2 PTH05000
DDR2_1V8
6A

P17 Inhibit

1.8V DDR2 SODIMM

0.9V DDR2 Vref

VR3 PTH05050
DDR2_VREF
6A

P10 Inhibit

0.9V DDR2 Vref

U14 TPS75501
PCI_VCC (3.0V)
5A

FPGA Vcco
3.0V PCI I/F

U13 TPS75501
VCCO_2V5
5A

FPGA Vcco

U12 TPS75501
VCCAUX_2V5
5A

FPGA Vccaux

PCIe POS-2
SW8
PCI POS-1

1 2 3

VR4 PTH03000
VCCINT_1V0
6A

FPGA Vccint

Motherboard PCIe Slot/Conn. Sources 3.3V and 12V

PCIe 3.3V@3.0A

PCIe 12V@5.5A

PCI 3.3V@7.6A

Motherboard PCI Slot/Connector Sources 3.3V and 5V

PCI 5V@5.0A

Voltage Regulator Topology

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	E8

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		36	37	2-27-2008_11:24

PCI/PCI-X 64-bit Edge Connector

SFP#1

SFP#2

Platform Flash
&
CPLD

5vlx50t-ff1136

PTH03000
Vout=1.0V/6A

PTH05000
Vout=1.8V/6A

PTH05050
Vout=0.9V/6A

HW-AFX-BERG-EPHY I/F

DDR2 SODIMM

HW-AFX-BERG-EPHY Outline

SATA

CLKIN SMA I/F

JTAG Conn.

MGT SMA I/F

GTPCLK SMA I/F

USB "B"

USB/UART
+Level Shifter

Samtec#1

Samtec#2

PTH12000
Vout=5V/6A

PCIe 8-Lane Edge Connector

GTP Power Regs

3 X MAX8557
on back of board

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280444

SIZE	DWG NO	REV
C	0381219	E8

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		37	37	2-27-2008_11:24

ML555 Block Diagram, PCB Component Side