PILLAR ROCK

Montevina Mobile Platform
CUSTOMER REFERENCE BOARD

Fab 3

Rev. 1.0

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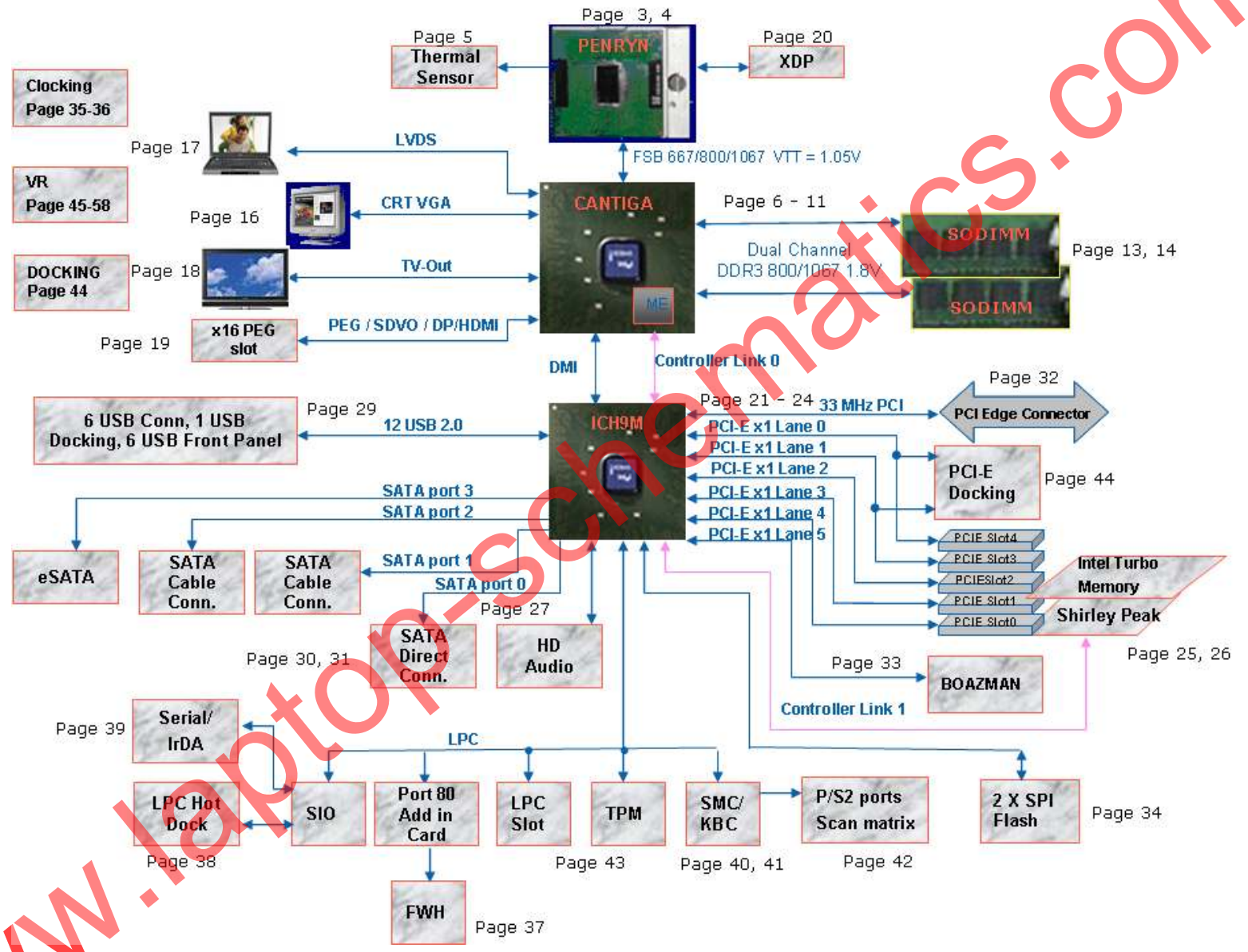

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MONTEVINA CUSTOMER REFERENCE PLATFORM

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
+VBATA	6V-14.1V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	Battery Rail in Mobile Power Mode
+VBAT	6V-14.1V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	Battery Rail in Mobile Power Mode
+VBATS	6V-14.1V	S0/M0	Battery Rail in Mobile Power Mode
+V12S	12V	S0/M0	Only on in DT Power Mode
-V12A	-12V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	Only on in DT Power Mode
-V12S	-12V	S0/M0	Only on in DT Power Mode
+V5A	5V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	
+V5	5V	S0/M0, S3/M1, S3/M-off	
+V5S	5V	S0/M0	
+V3.3A	3.3V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	
+V3.3M	3.3V	S0/M0, (S3-S5)/M1, S3/(M-off w/WOL_EN)	LAN
+V3.3M_CK505	3.3V	S0/M0, (S3-S5)/M1	Clock, MCH
+V3.3	3.3V	S0/M0, S3/M1, S3/M-off	
+V3.3S	3.3V	S0/M0	
+V1.8	1.8V	S0/M0, (S3-S5)/M1, S3/M-off	DDR core
+V1.5S	1.5V	S0/M0	
+V1.05M	1.05V	S0/M0, (S3-S5)/M1	
+V1.05S	1.05V	S0/M0	GMCH, ICH core, and FSB rail
+V0.9	0.9V	S0/M0, (S3-S5)/M1, S3/M-off	DDR command & control pull up.
+VCC_CORE	0.35V-1.5V	S0/M0	CPU core rail
+VCC_GFXCORE	0.7V-1.25V	S0/M0	GMCH Graphics core rail

I2C / SMB Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH_M3
DB800 Clock Buffer	1101 110x	DC	SMB_ICH_M3
SO-DIMM0	1010 000x	A0	SMB_ICH_M2
SO-DIMM1	1010 010x	A4	SMB_ICH_M2
SO-DIMM0 Thermal Sensor	0011 000x	30	SMB_ICH_M2
SO-DIMM1 Thermal Sensor	0011 010x	34	SMB_ICH_M2
DDR Thermal Sensor	0100 110x	4C	SMB_ICH_M2
I2C Bus Expander	0011 xxxx	3x	SMB_ICH
Ambient Lighr Sensor	0111 001x	72	ALS
EMA Display	0011 110x	3C	EMA
CPU Thermal Sensor	1001 100x	98	SMB_THRM
IMVP6 Amb. Temp. Sensor	1001 101x	9A	SMB_THRM
Battery A	0001 110x	1C	SMB_BS
Battery B	0001 111x	1E	SMB_BS
Board ID Port Expander	0011 000x	30	SMB_BS
Docking Port Expander	0011 001x	32	SMB_BS
Skin Temperature Sensor	1001 100x	98	SMB_BS
H8	TBD	TBD	SMB_ME
PCI-Slot3	TBD	TBD	SMB_ICH_A1
PCI-Gold Finger	TBD	TBD	SMB_ICH_A1
PCI-Express Slot1-5	TBD	TBD	SMB_ICH_A1
Docking	TBD	TBD	SMB_ICH_A1
PCIe x16 Slot (PEG)	TBD	TBD	SMB_ICH_S4
TPM Header	TBD	TBD	SMB_ICH_S4
ITP-XDP	TBD	TBD	SMB_ICH_S4

Buses labeled SMB_ICH_xx come out of ICH, via an I2C expander.
The rest come out of EC.

Jumper / Switch Settings

Jumper	Default	Description	Page
J1G1	1-2	BSEL2	35
J1G3	1-2	BSEL1	35
J1G5	1-2	BSEL0	35
J2B2	All OPEN	CPU CORE VID	52
J2G1	1-X	Force Shutdown	56
J2H2	All OPEN	GFX CORE VID	49
J3C1	1-2, 3-4	CPU thermal sensor	5
J3J2	1-X	Power ON Latch	5
J4H1	1-X	No ME G3 to M1 support	36
J4J2	1-2	SATA Power Enable	31
J5G1	1-X	SRTC RST	21
J5H2	1-X	CMOS Clear	21
J7A1	1-2	In-circuit SMC Programming	39
J7E1	1-2	SIO Reset	38
J7H1	1-2	SATA interlock switch for port0	30
J7H2	1-X	TPM PHYSICAL PRESENCE	22
J8B1	1-2	PM_Lan_enable	40
J8B2	1-2	In-circuit SMC Programming	39
J8C1	1-X	SELCETING SPI0 or SPI1 TO BE REPROGRAMMED	34
J8F2	1-X	BIOS recovery	23
J8G1	1-X	SV Setup	63
J8G3	1-X	SMC_MD2	40
J8G4	1-X	CRB/SV detect	64
J8G5	1-2	SMC_MD1	40
J8G6	1-X	ESC disable	40
J8H1	1-2	Boot Block Strap	31
J9C1	1-X	PROGRAMMING SPI1	34
J9D1	1-X	PROGRAMMING SPI0	34
J9F1	1-2	ME Enable	40
J9G2	1-2	Boot Block Programming	42
J9H1	1-X	NM	42
J9H2	1-2	SATA interlock switch for port1	31
J9H3	1-X	LID Position	41
J9H4	1-X	Virtual Battery	41

Changes for Pillar Rock with PM GMCH SKU

SL No	DO STUFF	STUFF
1	U6E2, U6E3, U6E4	
2	L5F1	
3	R5E5, R5F9, R5T16, R5U3, R5U11, R5U14, R5U21, R6V1	R5E4, R5T5, R5T8, R5T9, R5T10, R5T12, R5T17
4	C5E8, C5E9, C5E11, C5E12, C5E13, C5E14, C5E15, C5T12, C5T13, C5U1, C5U2, C5U3	C5E8,C5E9,C5T13,C5U3 with 0 Ohm 0402 size res IPN A93549-001
5	FB5F1, FB5F2, FB5T1	
6	J2G1(3 4), J2G1(5 6), J2G1(7 8)	J2G1(1 2), J2G1(13 14)

PCI Devices

Device	IDSEL #	REQ/GNT #	Interrupts
Slot 3	AD18	2 2	D, C, A, B
LAN	(AD24 internal)		

Net Naming Conventions

Suffix
= Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

LEDs and Switches

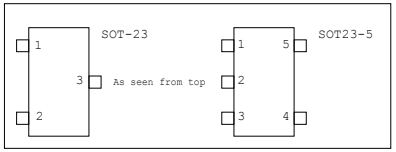
LED	Page	Reference
xTA Activity	21	CR7H1
VID0	39	CR1B1
VID1	39	CR1B2
VID2	39	CR1B3
VID3	39	CR1B4
VID4	39	CR1B5
VID5	39	CR1B6
VID6	39	CR1B7
Num Lock	40	CR9G1
Scroll Lock	40	CR9G3
Caps Lock	40	CR9G2
S3	57	CR5H6
M0/M1	57	CR5H3
S4	57	CR5H7
S5	57	CR5H5
S0	57	CR5H4
System Power Good	57	CR7H3
LT Status	64	CR8G1

Switch	Default	Description	Page
SW9H1	1 - 2	Virtual Docking	41
SW9H3	1 - 2	Virtual Battery	41
SW9H2	1 - 2	LID Switch	41
SW7J1	1 - 2	Hybrid GFX switch	41
SW1C1		Power Button	56
SW1C2		Reset Button	56
SW8E1		Net Detect	56

Power States

	SLP_S3#	S4_STATE#	SLP_S4#	SLP_S5#	SLP_M#	+V*A	+V3.3M_WOL	+V1.05M	+V3.3M	+V1.8/+V0.9	+V5/+V3.3	+V*S	Clocks
S0 (Full on)/M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON
S3 (Suspend to RAM)/M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	OFF	only MCH BCLK
S3 (Suspend to RAM)/Moff	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
S3 (Suspend to RAM)/Moff w/WOL_EN	LOW	HIGH	HIGH	HIGH	LOW	ON	ON	OFF	OFF	ON	ON	OFF	OFF
S4 (Suspend to Disk)/M1	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	OFF	OFF	only MCH BCLK
S5 (Soft Off)/M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	ON	ON	ON	OFF	OFF	only MCH BCLK
S4 (Suspend to Disk)/Moff	LOW	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5 (Soft Off)/Moff	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF

PCB Footprints



Wake Events

Wake Events	State Supported
RI# from serial port	S3
PME# from PCI, mini PCI slot/device, LPC slot/device	S3
PCI Express, mini PCI Express, Express-card wake event	S3/M1
Wake on LAN	S3/M1
LID switch attached to SMC	S3
USB	S3
HDA wake on ring	S3
SmLink for AOLII	S3
Hot Key from Scan matrix keyboard	S3
PS/2 Keyboard/mouse	S3
PWRBTN#	S3
Netdetect	S3, S4, S5 / M1

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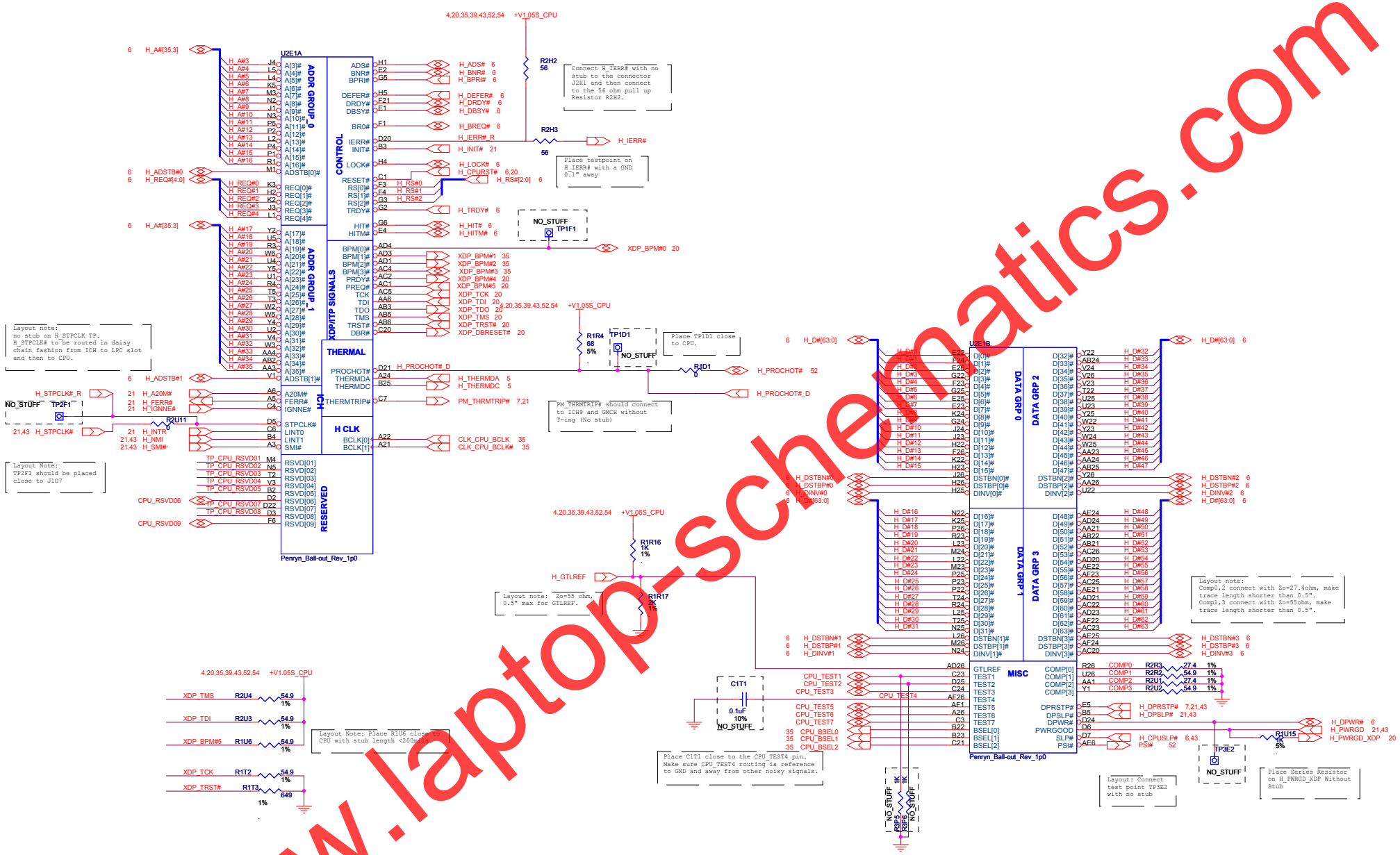

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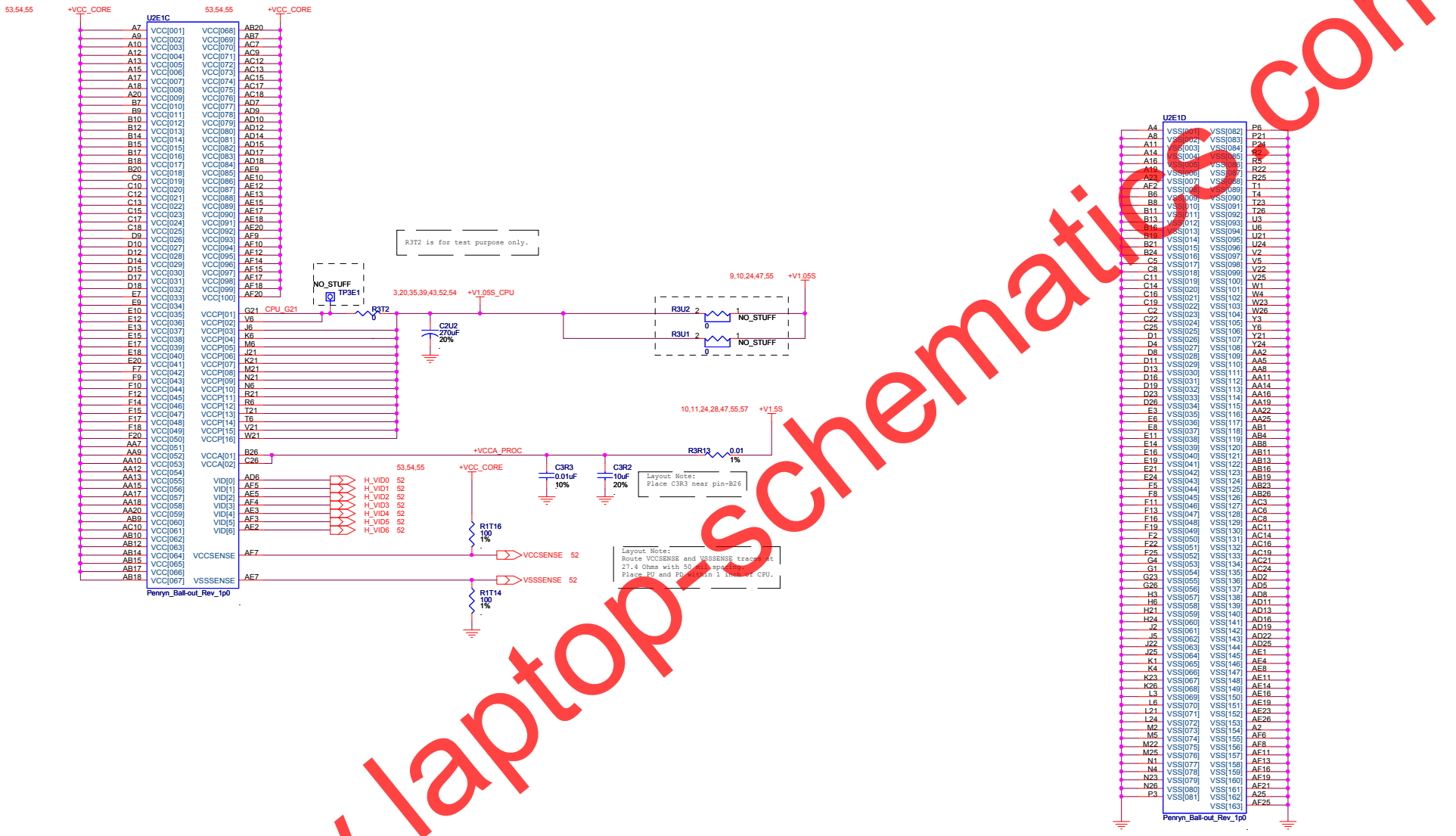

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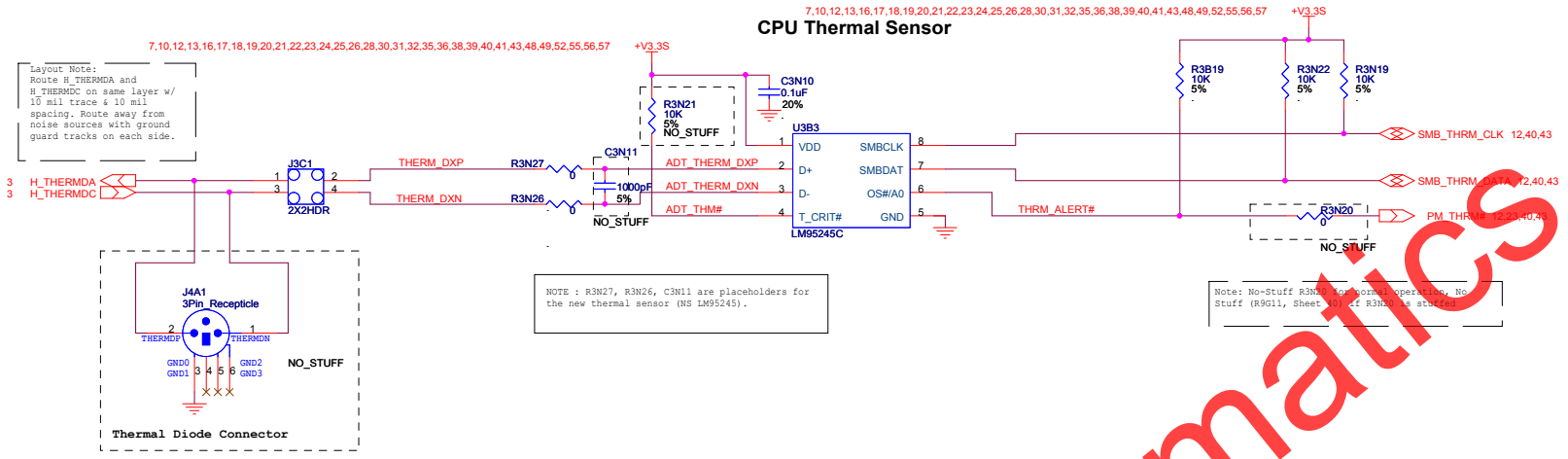

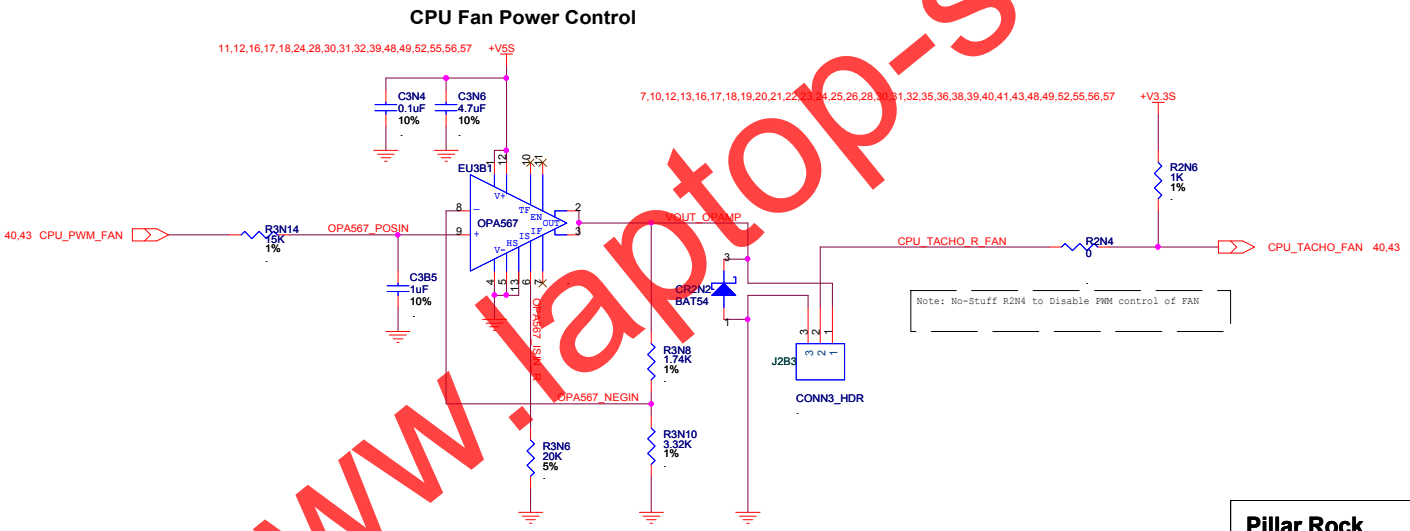

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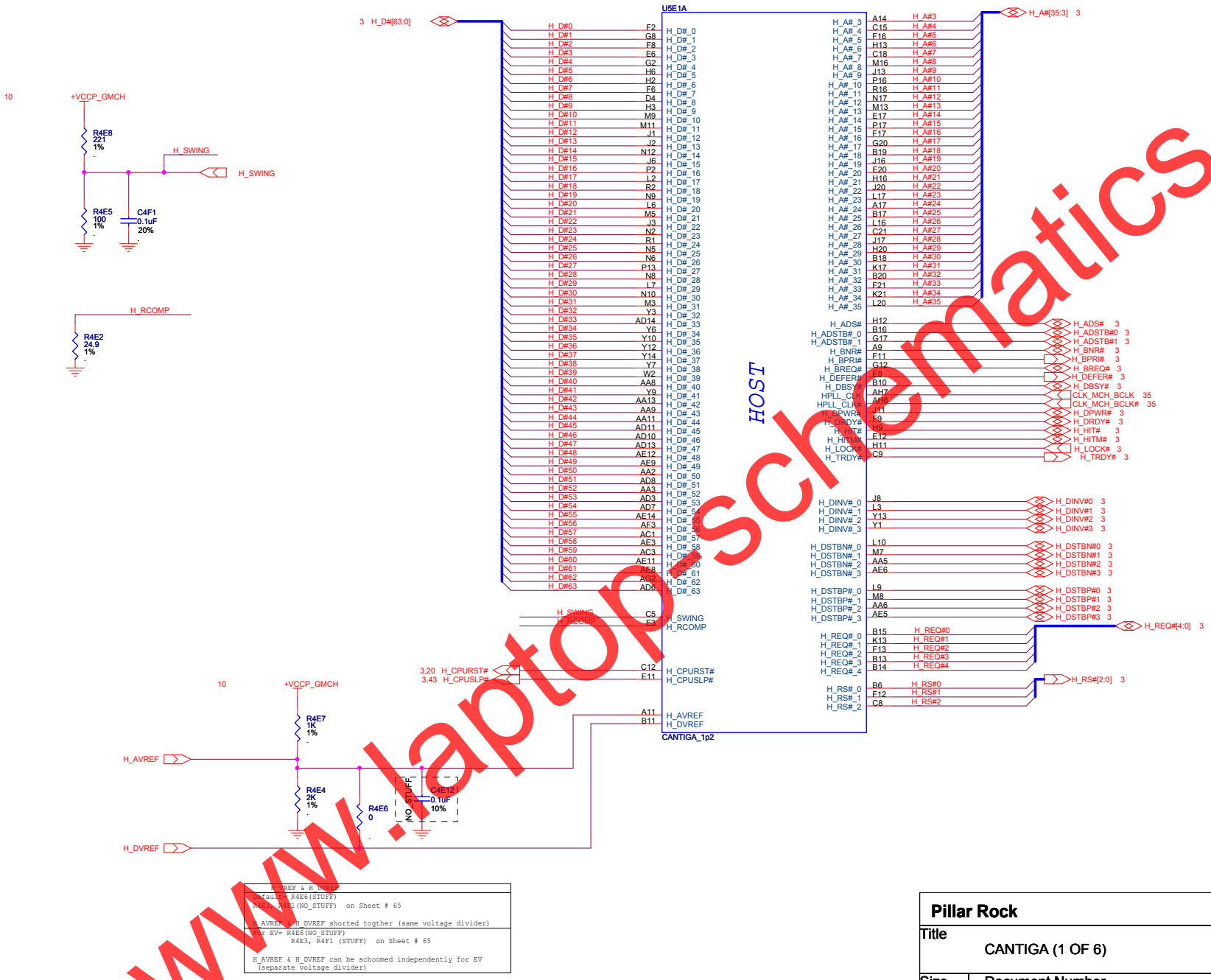

H_AVREF & H_DVREF
default: R4E6(STUFF)
R4E3, R4F1(NO_STUFF) on Sheet # 65

If AVREF & H_DVREF shorted togther (same voltage divider)
For EV= R4E6(NO_STUFF)
R4E3, R4F1 (STUFF) on Sheet # 65

H_AVREF & H_DVREF can be schoomed independently for EV
(separate voltage divider)

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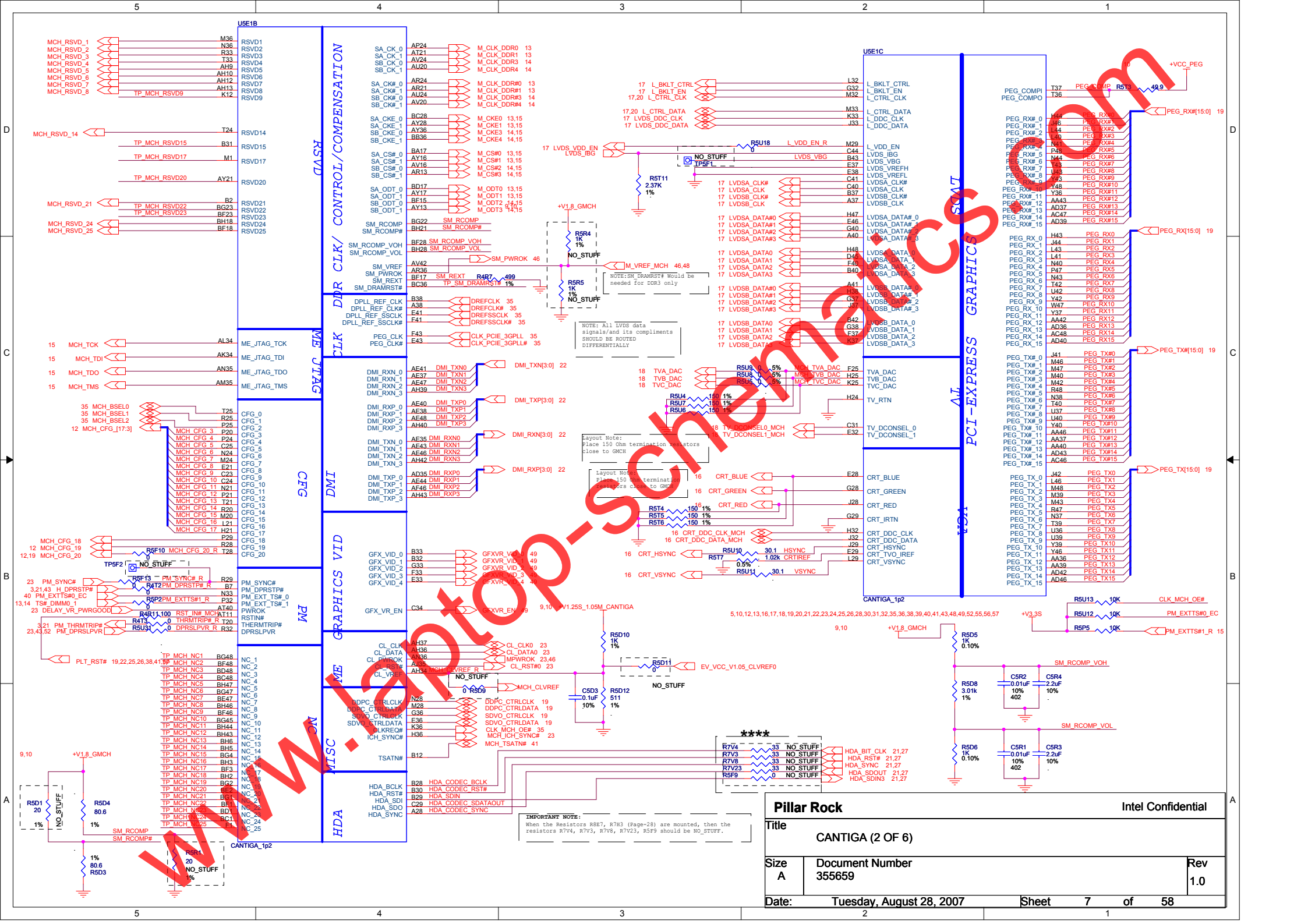

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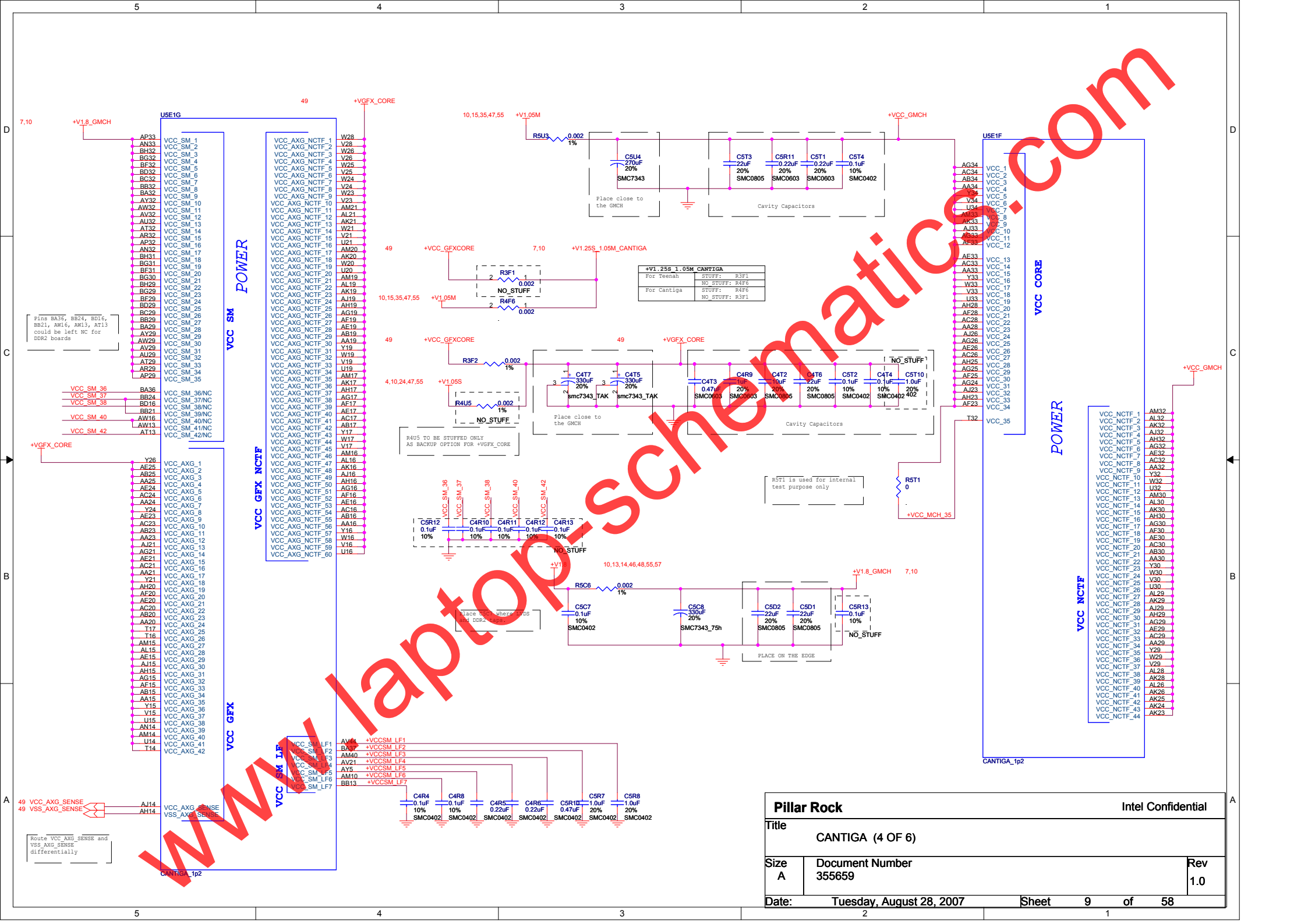

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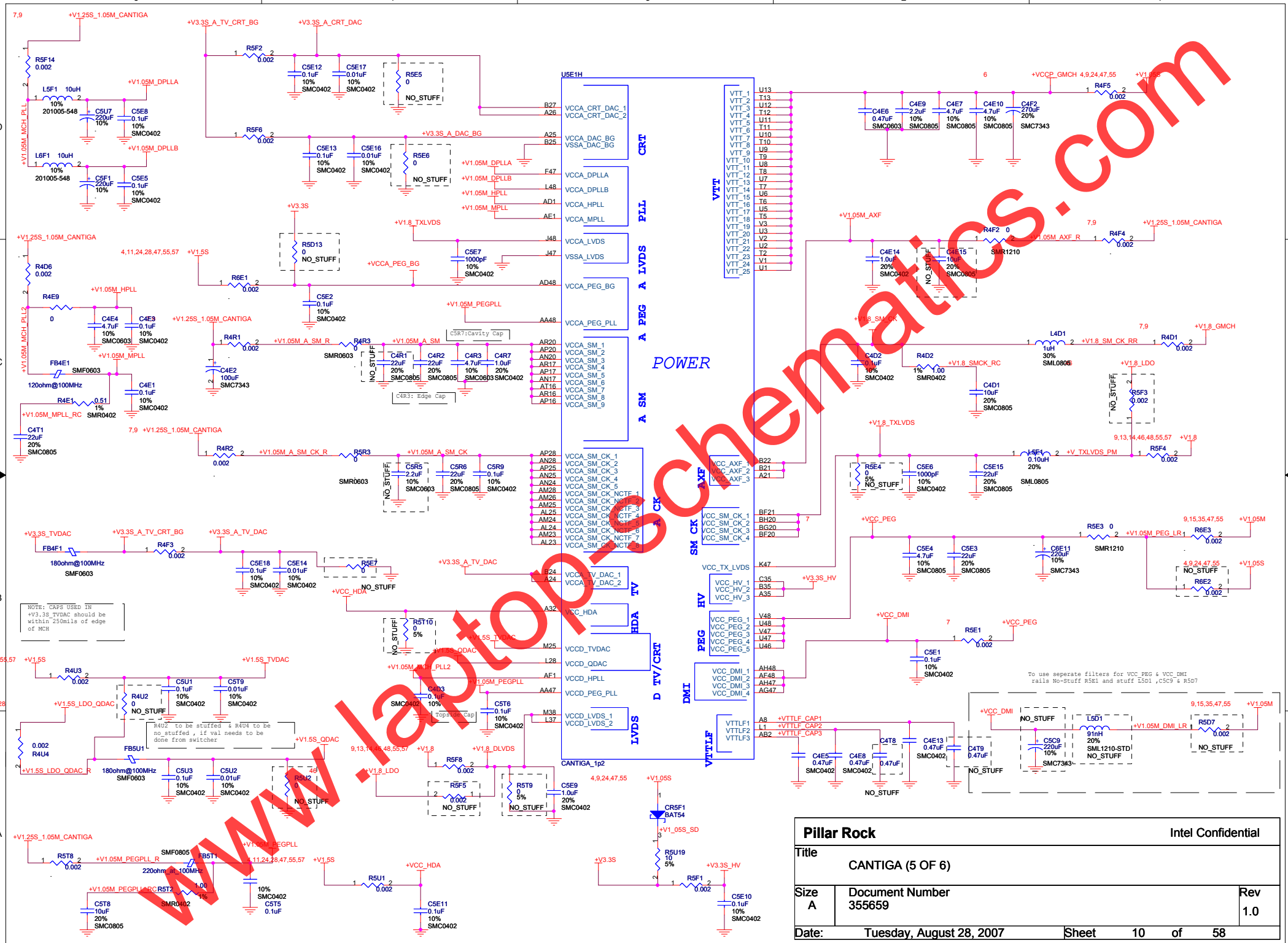

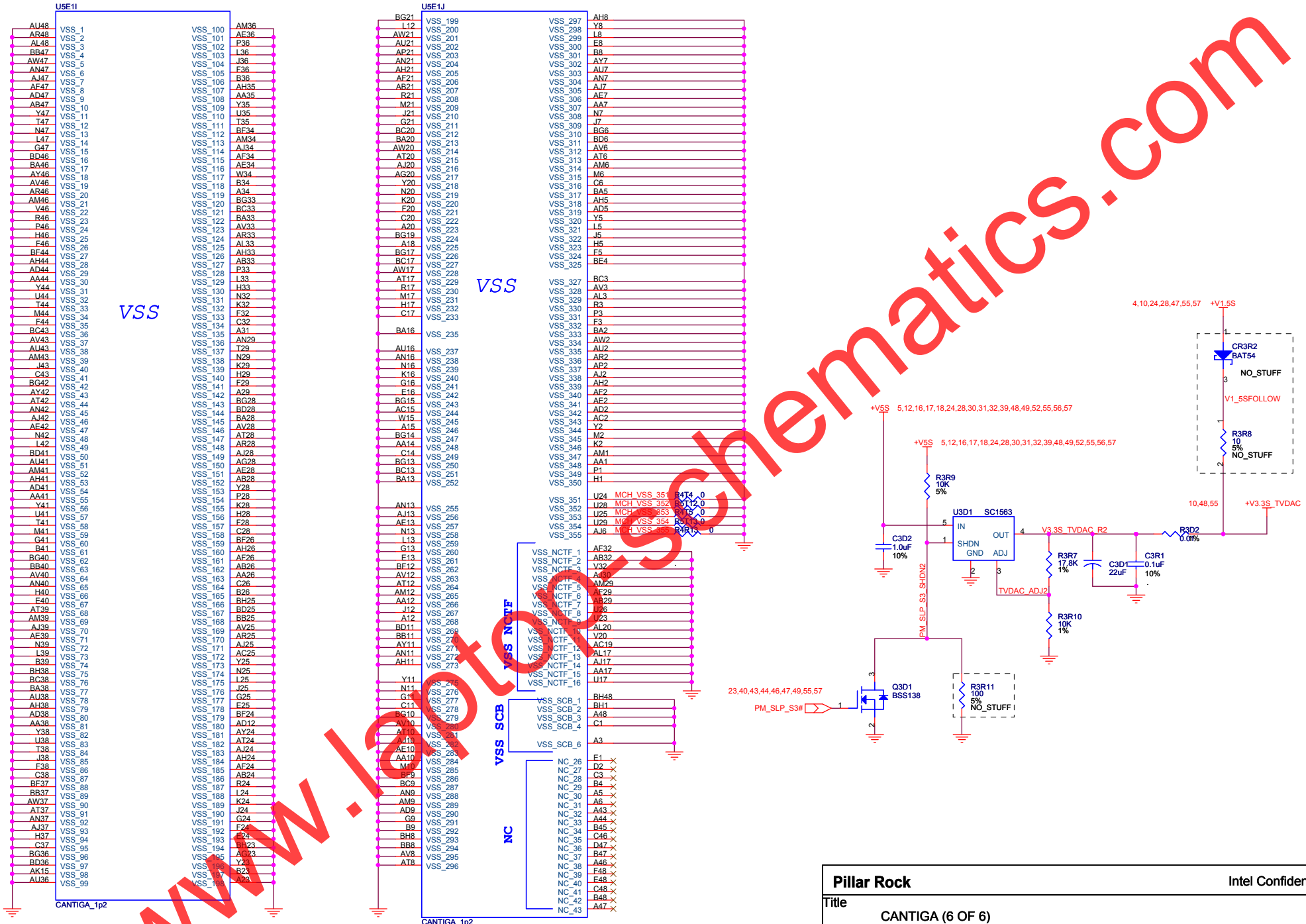

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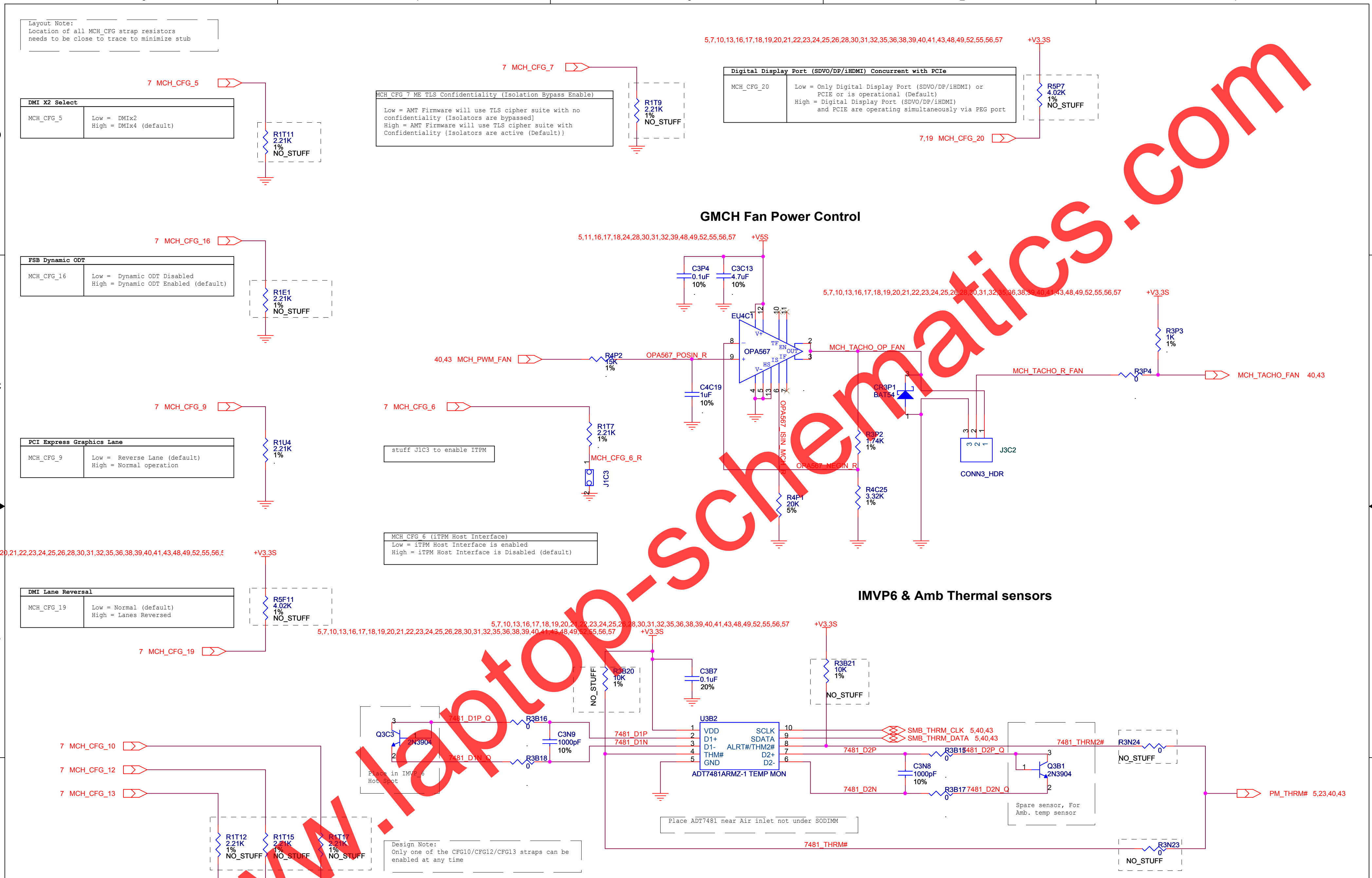

Layout Note: Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub
DMI X2 Select
MCH_CFG_5 Low = DMIx2 High = DMIx4 (default)
7 MCH_CFG_5
R1T11 2.21K 1% NO_STUFF
MCH_CFG_7 ME TLS Confidentiality (Isolation Bypass Enable)
Low = AMT Firmware will use TLS cipher suite with no confidentiality (Isolators are bypassed)
High = AMT Firmware will use TLS cipher suite with Confidentiality (Isolators are active (Default))
7 MCH_CFG_7
R1T9 2.21K 1% NO_STUFF
Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe
MCH_CFG_20 Low = Only Digital Display Port (SDVO/DP/iHDMI) or PCIe or is operational (Default)
High = Digital Display Port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
5,7,10,13,16,17,18,19,20,21,22,23,24,25,26,28,30,31,32,35,36,38,39,40,41,43,48,49,52,55,56,57 +V3.3S
R5P7 4.02K 1% NO_STUFF
7,19 MCH_CFG_20
GMCH Fan Power Control
5,11,16,17,18,24,28,30,31,32,39,48,49,52,55,56,57 +V5S
C3P4 0.1uF 10%
C3C13 4.7uF 10%
EU4C1 OPA567
FSB Dynamic ODT
MCH_CFG_16 Low = Dynamic ODT Disabled High = Dynamic ODT Enabled (default)
7 MCH_CFG_16
R1E1 2.21K 1% NO_STUFF
40,43 MCH_PWM_FAN
R4P2 15K 1%
OPA567_POSIN_R
C4C19 1uF 10%
MCH_TACHO_OP_FAN
5,7,10,13,16,17,18,19,20,21,22,23,24,25,26,28,30,31,32,35,36,38,39,40,41,43,48,49,52,55,56,57 +V3.3S
R3P3 1K 1%
MCH_TACHO_R_FAN
R3P4 0
MCH_TACHO_FAN 40,43
CR3P1 BAT54
J3C2 CONN3_HDR
R3P2 1.74K 1%
OPA567_NEGIN_R
OPA567_ISIN_MCH
R4C25 3.32K 1%
R4P1 20K 5%
PCI Express Graphics Lane
MCH_CFG_9 Low = Reverse Lane (default) High = Normal operation
7 MCH_CFG_9
R1U4 2.21K 1%
7 MCH_CFG_6
stuff J1C3 to enable ITPM
R1T7 2.21K 1%
MCH_CFG_6_R
J1C3
MCH_CFG_6 (iTPM Host Interface)
Low = iTPM Host Interface is enabled
High = iTPM Host Interface is Disabled (default)
DMI Lane Reversal
MCH_CFG_19 Low = Normal (default) High = Lanes Reversed
+V3.3S
R5F11 4.02K 1% NO_STUFF
7 MCH_CFG_19
IMVP6 & Amb Thermal sensors
+V3.3S
R3B20 10K 1% NO_STUFF
C3B7 0.1uF 20%
R3B21 10K 1% NO_STUFF
Q3C3 2N3904
Place in IMVP6 Hot Spot
7481_D1P_Q
R3B16 0
C3N9 1000pF 10%
7481_D1N_Q
R3B18 0
U3B2 ADT7481ARMZ-1 TEMP MON
VDD D1+ D1- THM# GND SCLK SDATA ALRT#/THM2# D2+ D2-
7481_D1P 7481_D1N
SMB_THRM_CLK 5,40,43
SMB_THRM_DATA 5,40,43
7481_THRM2#
R3N24 0 NO_STUFF
7481_D2P
R3B15 0 7481_D2P_Q
C3N8 1000pF 10%
7481_D2N
R3B17 0 7481_D2N_Q
Q3B1 2N3904
Spare sensor, For Amb. temp sensor
PM_THRM# 5,23,40,43
Place ADT7481 near Air inlet not under SODIMM
7481_THRM#
R3N23 0 NO_STUFF
7 MCH_CFG_10
7 MCH_CFG_12
7 MCH_CFG_13
R1T12 2.21K 1% NO_STUFF
R1T15 2.21K 1% NO_STUFF
R1T17 2.21K 1% NO_STUFF
Design Note: Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time

XOR / ALLZ / Clock Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode Enabled
0	1	All-Z Mode Enabled
1	1	Normal Operation (Default)

MCH_CFG_10 (PCIE Loopback enable)
Low = Enabled
High = Disabled (Default)

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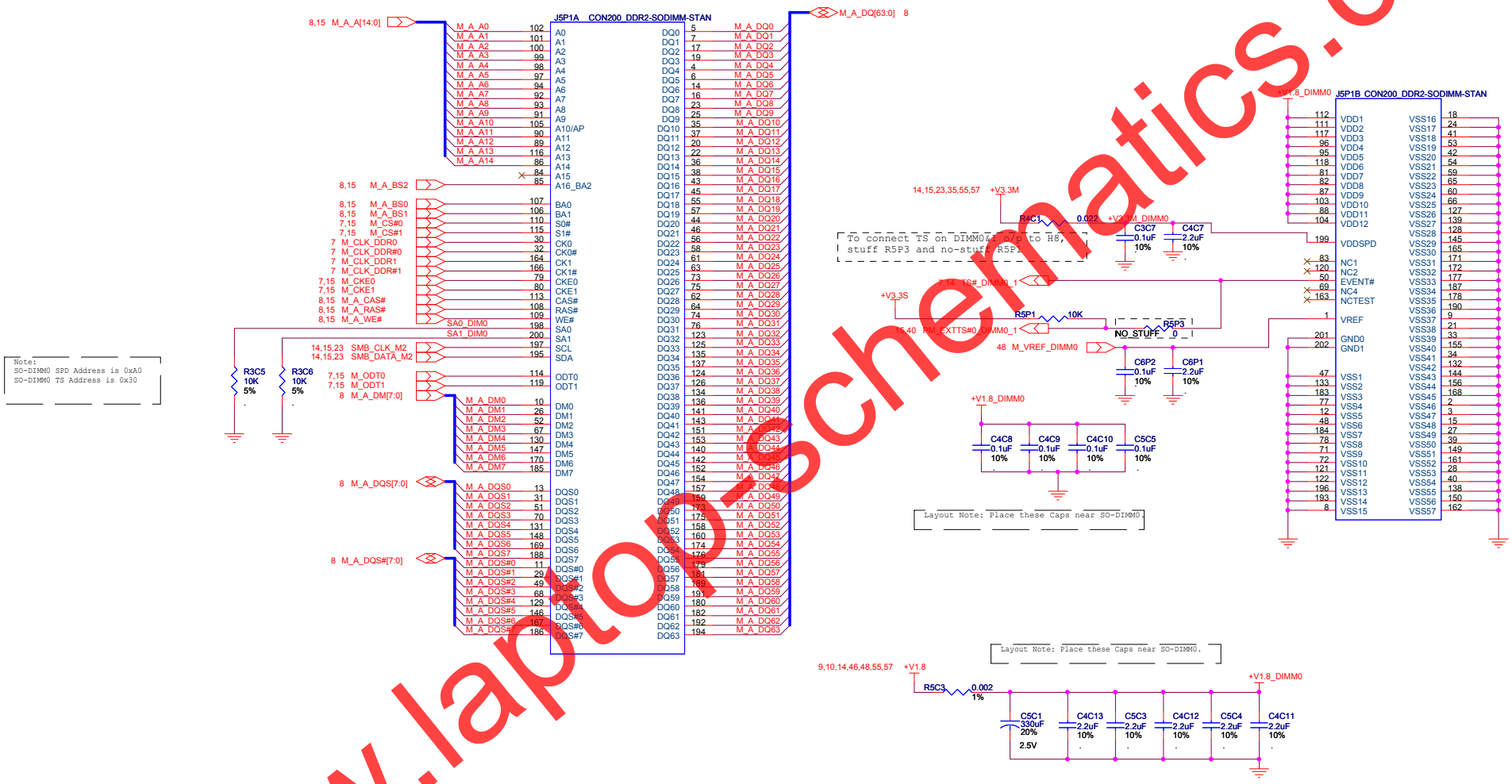

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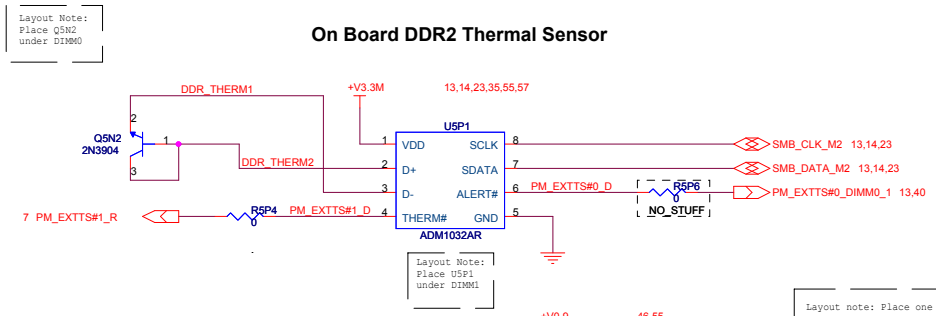
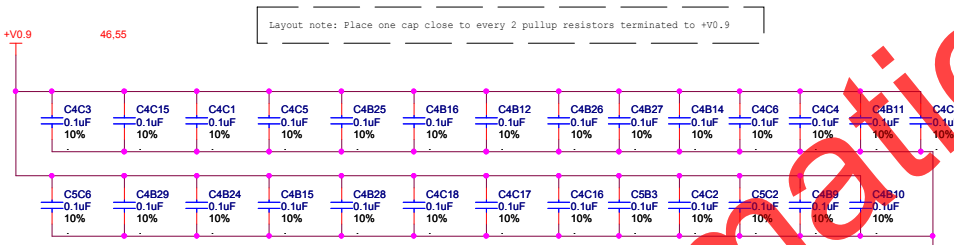
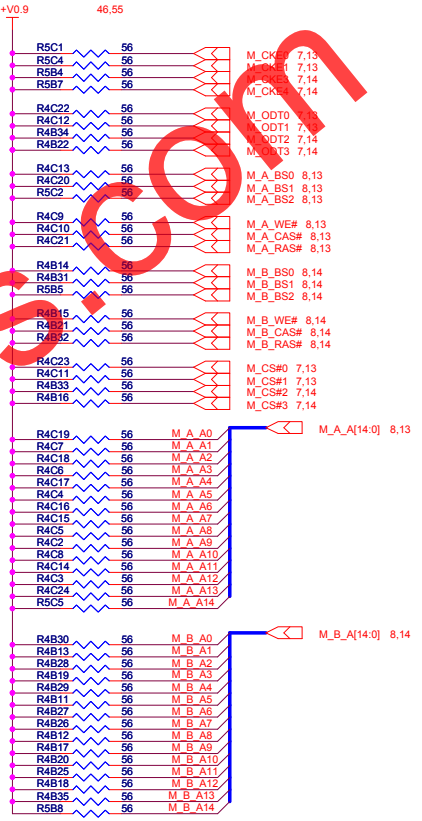
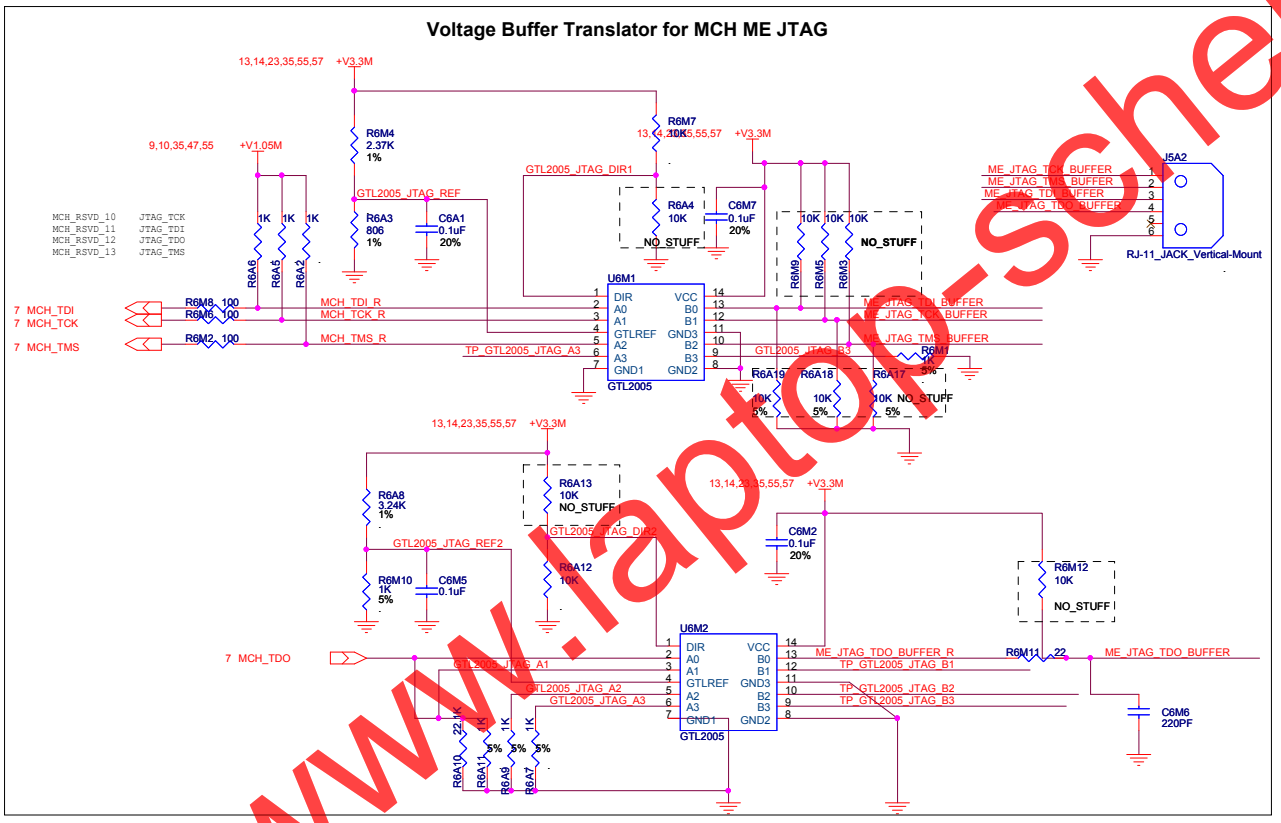
On Board DDR2 Thermal Sensor







Voltage Buffer Translator for MCH ME JTAG



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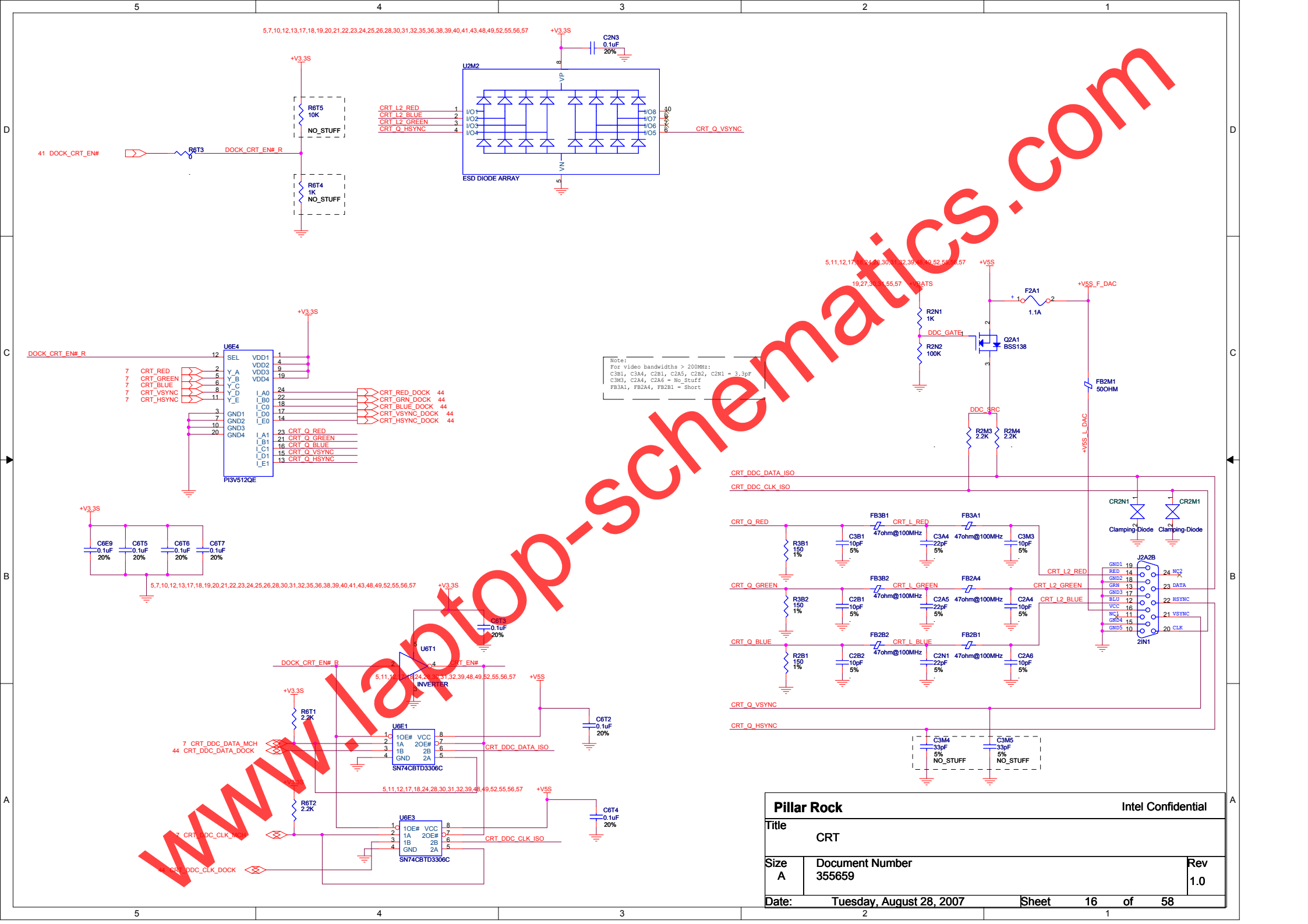

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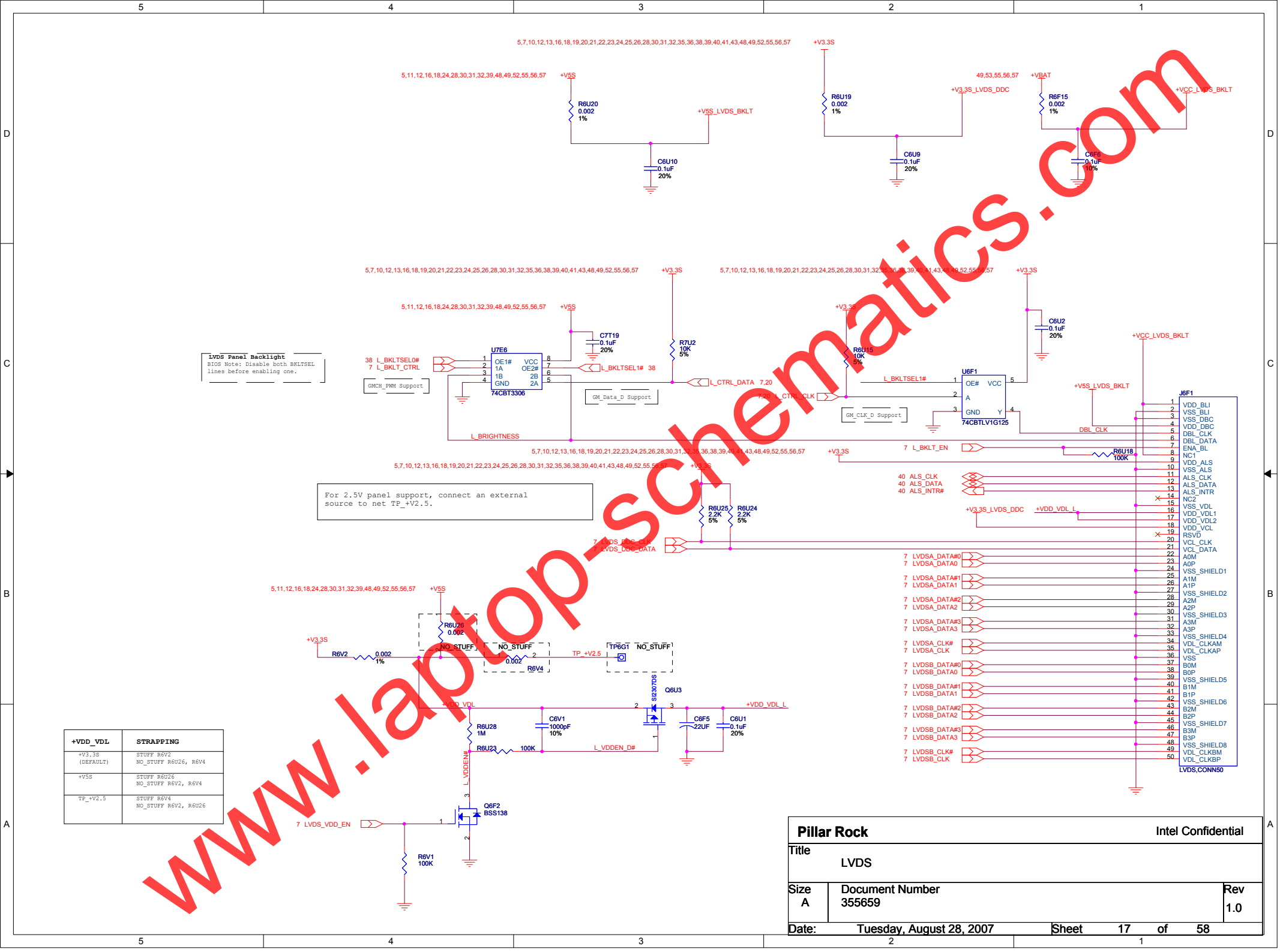
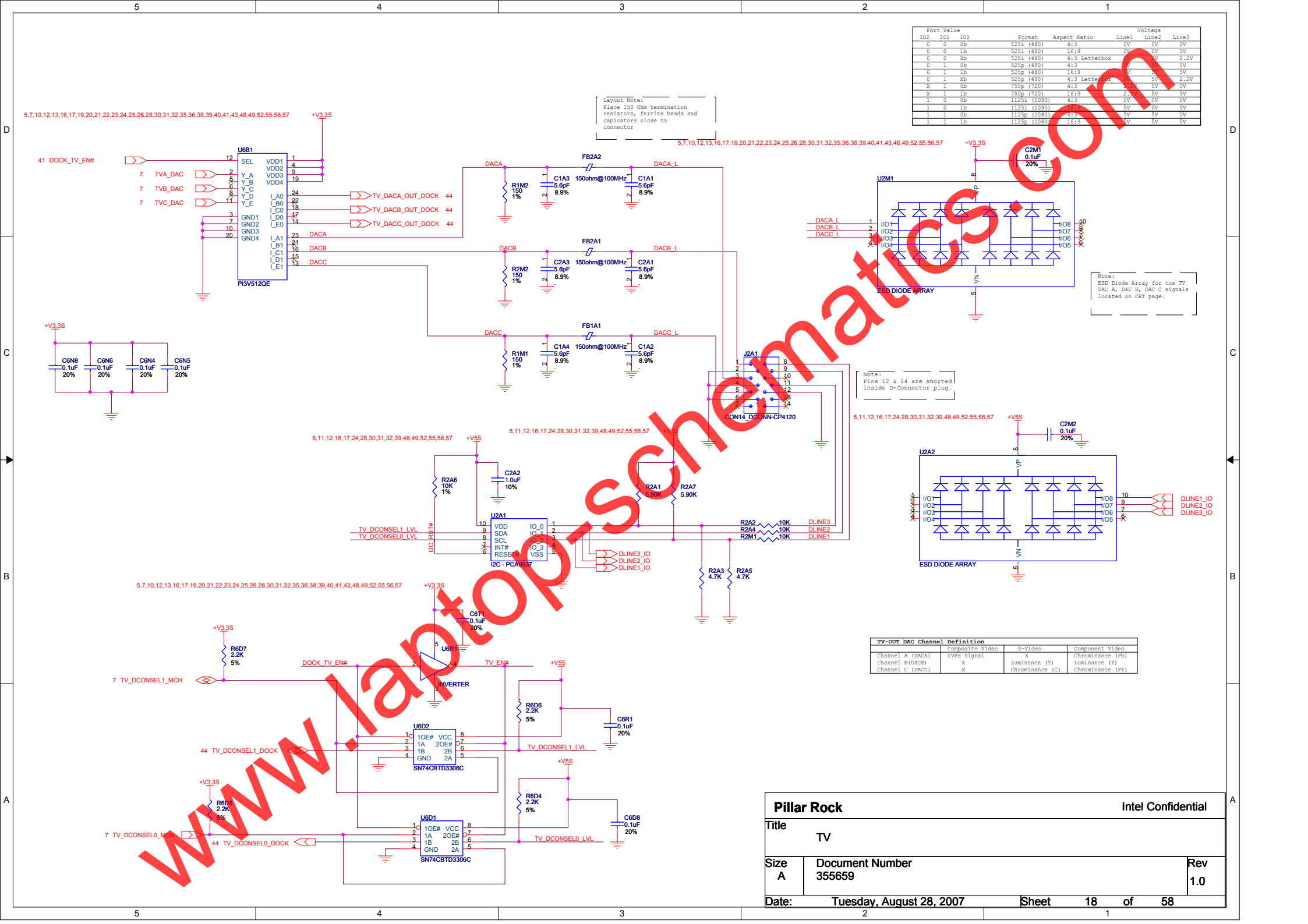
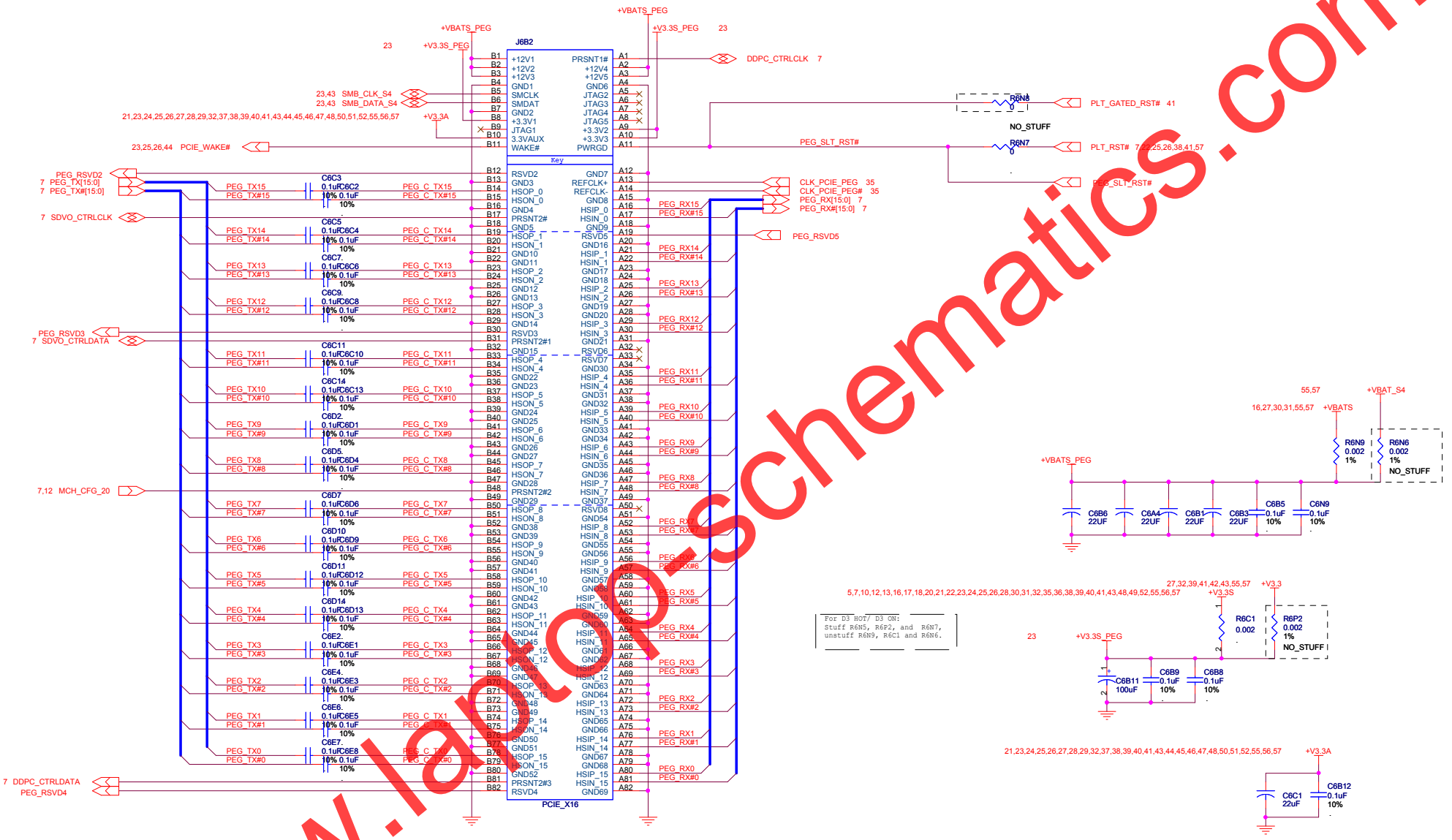
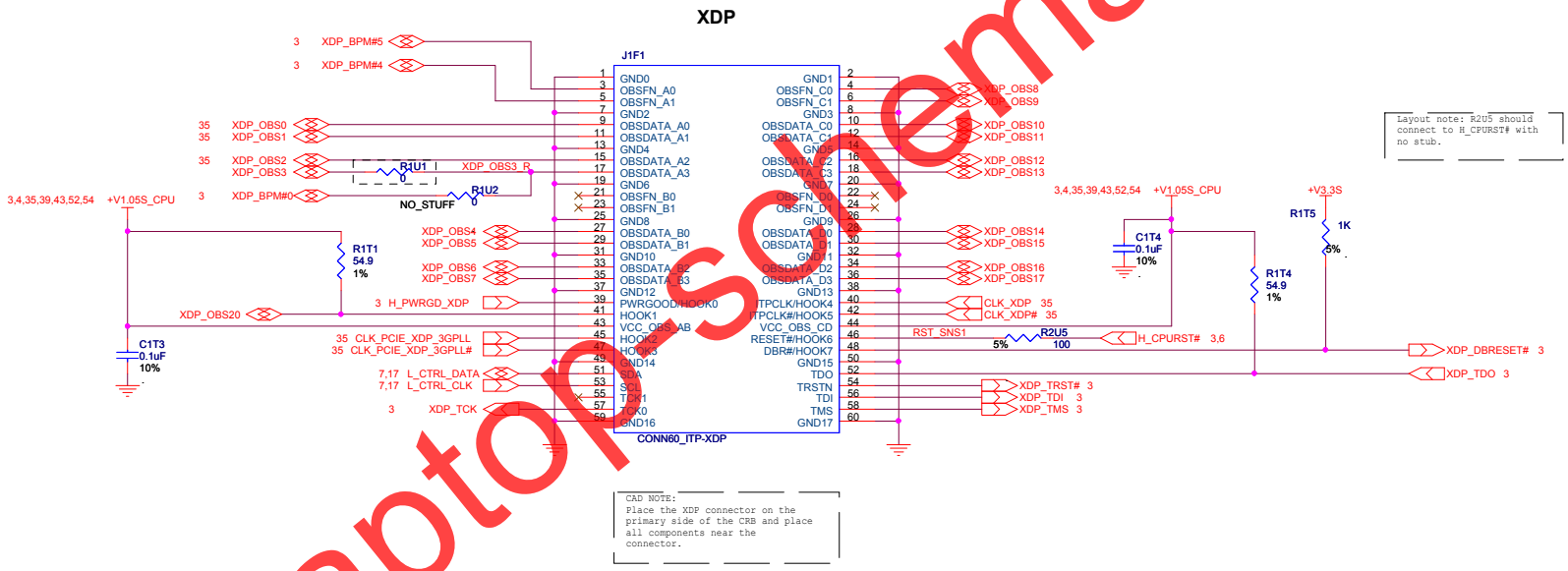


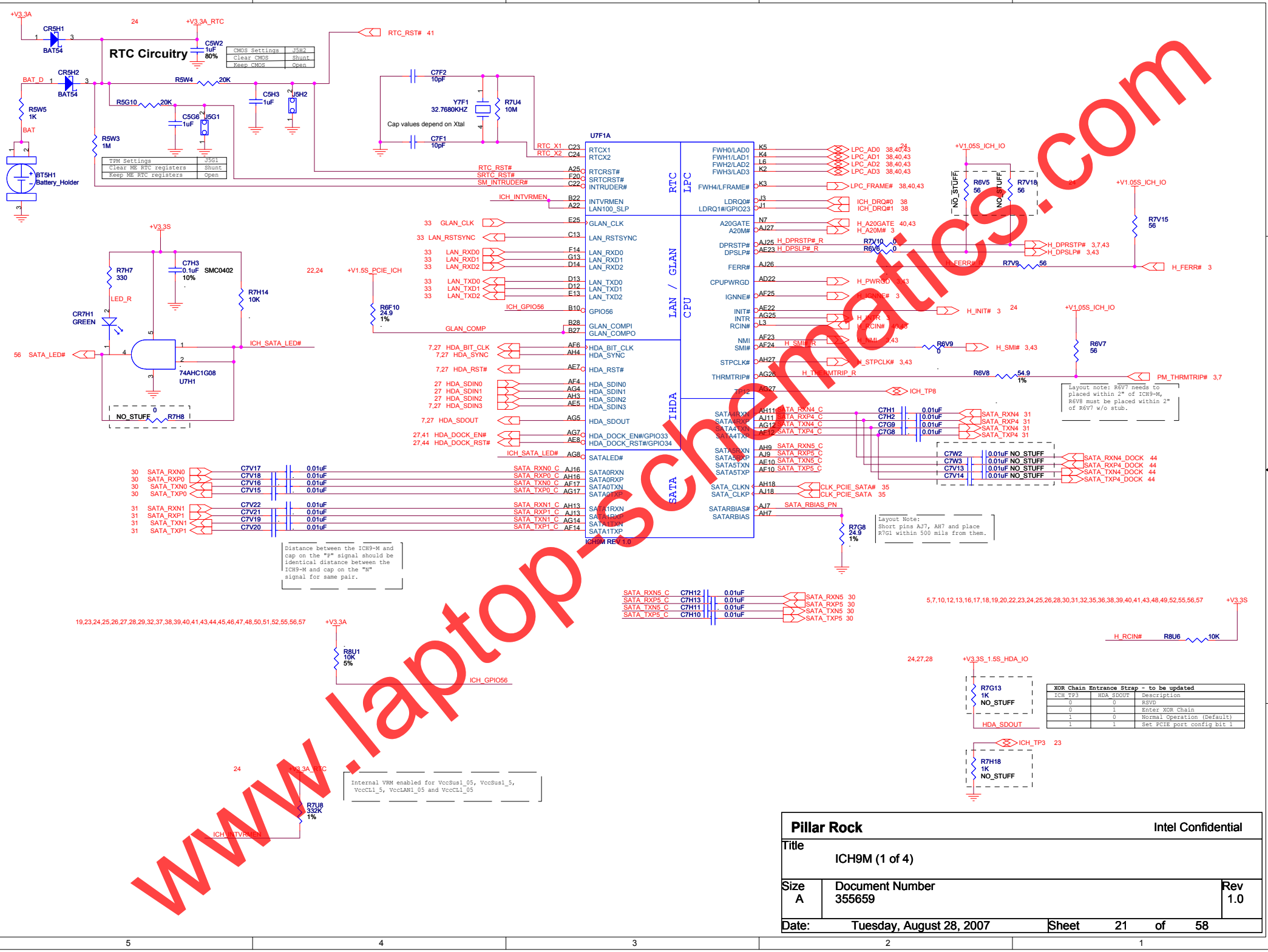


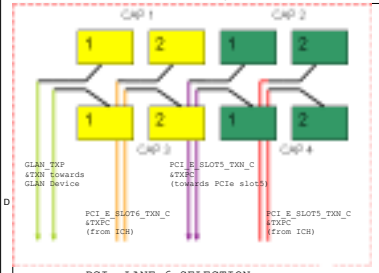


Pillar Rock		Intel Confidential
Title	PCIE GRAPHICS	
Size A	Document Number 355659	Rev 1.0
Date: Tuesday, August 28, 2007	Sheet 19 of 58	



Pillar Rock		Intel Confidential
Title: XDP		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 20 of 58	





PCIe LANE 6 SELECTION

Lane 6 can be connected to LAN or Slot 5 depending on the stuffing option described below. Placed the components such that CAP1 (0603)Pad2 & CAP2 Pad1 are next to each other as shown above. The Placement is such that a 0603 Capacitor can be placed there . Similar placement followed for CAP3 and CAP4. This approach is same for RX Path also.

NO_STUFF

44 PCIE_RXN1_DOCK — R6U29 0 — PCIE_RXN1_R
44 PCIE_RXP1_DOCK — R6U27 0 — PCIE_RXP1_R
44 PCIE_TXN1_DOCK — C6F11 0.1uF — PCIE_TXN1_C
44 PCIE_TXP1_DOCK — C6F10 0.1uF — PCIE_TXP1_C

44 PCIE_RXN2_DOCK — R6U22 0 — PCIE_RXN2_R
44 PCIE_RXP2_DOCK — R6U21 0 — PCIE_RXP2_R
44 PCIE_TXN2_DOCK — C6U8 0.1uF — PCIE_TXN2_C
44 PCIE_TXP2_DOCK — C6U7 0.1uF — PCIE_TXP2_C

25 PCIE_RXN1_SLOT1 — R6F19 0 — PCIE_RXN1_R
25 PCIE_RXP1_SLOT1 — R6F18 0 — PCIE_RXP1_R
25 PCIE_TXN1_SLOT1 — C6U12 0.1uF — PCIE_TXN1_C
25 PCIE_TXP1_SLOT1 — C6U11 0.1uF — PCIE_TXP1_C

25 PCIE_RXN2_SLOT2 — R6F17 0 — PCIE_RXN2_R
25 PCIE_RXP2_SLOT2 — R6F16 0 — PCIE_RXP2_R
25 PCIE_TXN2_SLOT2 — C6F9 0.1uF — PCIE_TXN2_C
25 PCIE_TXP2_SLOT2 — C6F8 0.1uF — PCIE_TXP2_C

26 PCIE_RXN3_SLOT3 — C6U6 0.1uF — PCIE_TXN3_C
26 PCIE_RXP3_SLOT3 — C6U4 0.1uF — PCIE_TXP3_C
26 PCIE_TXN3_SLOT3
26 PCIE_TXP3_SLOT3

26 PCIE_RXN4_SLOT4 — C6U5 0.1uF — PCIE_TXN4_C
26 PCIE_RXP4_SLOT4 — C6U3 0.1uF — PCIE_TXP4_C
26 PCIE_TXN4_SLOT4
26 PCIE_TXP4_SLOT4

26 PCIE_RXN5_SLOT5 — R6F14 0 — PCIE_RXN5_SLOT5_R
26 PCIE_RXP5_SLOT5 — R6F11 0 — PCIE_RXP5_SLOT5_R
26 PCIE_TXN5_SLOT5 — C6F4 0.1uF — PCIE_TXN5_C
26 PCIE_TXP5_SLOT5 — C6F2 0.1uF — PCIE_TXP5_C

33 GLAN_RXN — R6F12 0 — GLAN_RXN_R
33 GLAN_RXP — R6F13 0 — GLAN_RXP_R
33 GLAN_TXN — C6F3 0.1uF — PCIE_TXN6_C
33 GLAN_TXP — C6F1 0.1uF — PCIE_TXP6_C

34 SPI_CLK — R7F8 15 — SPI_CLK_R
34 SPI_CS#0 — R7F9 15 — SPI_CS#0_R
34 SPI_CS#1 — R7F7 15 — SPI_CS#1_R

U7F1D

PCI-Express

PERN1 N29 — PCIE_RXN1_R
PERP1 N28 — PCIE_RXP1_R
PETN1 P27 — PCIE_TXN1_C
PETP1 P26 — PCIE_TXP1_C
PERN2 L29 — PCIE_RXN2_R
PERP2 L28 — PCIE_RXP2_R
PETN2 M27 — PCIE_TXN2_C
PETP2 M26 — PCIE_TXP2_C
PERN3 J29
PERP3 J28
PETN3 K27
PETP3 K26
PERN4 G29
PERP4 G28
PETN4 H27
PETP4 H26
PERN5 E29 — PCIE_RXN5_SLOT5_R
PERP5 E28 — PCIE_RXP5_SLOT5_R
PETN5 F27 — PCIE_TXN5_C
PETP5 F26 — PCIE_TXP5_C
PERN6/GLAN_RXN C29 — GLAN_RXN_R
PERP6/GLAN_RXP C28 — GLAN_RXP_R
PETN6/GLAN_TXN D27 — PCIE_TXN6_C
PETP6/GLAN_TXP D26 — PCIE_TXP6_C

SPI

SPI_CLK D23 — SPI_CLK_R
SPI_CS0# D24 — SPI_CS#0_R
SPI_CS1#/GPIO58/CLGPIO6 F23 — SPI_CS#1_R
SPI_MOSI D25
SPI_MISO E23

USB

OC0#/GPIO59 N4 — USB_OC#0
OC1#/GPIO40 N5 — USB_OC#1
OC2#/GPIO41 N6 — USB_OC#2
OC3#/GPIO42 P6 — USB_OC#3
OC4#/GPIO43 M1 — USB_OC#4
OC5#/GPIO29 N2 — USB_OC#5
OC6#/GPIO30 M4 — USB_OC#6
OC7#/GPIO31 M3 — USB_OC#7
OC8#/GPIO44 N3 — USB_OC#8
OC9#/GPIO45 N1 — USB_OC#9
OC10#/GPIO46 P5 — USB_OC#10
OC11#/GPIO47 P3 — USB_OC#11

USBRBIAS AG2 — USBRBIAS_PN — R7G5 22.6 1%
USBRBIAS# AG1

ICH9M REV 1.0

Direct Media Interface

DMI0RXN V27 — DMI_RXN0_R — R6F5 0 — DMI_RXN0 7
DMI0RXP V26 — DMI_RXP0_R — R6F6 0 — DMI_RXP0 7
DMI0TXN U29 — DMI_TXN0_R — R6U2 0 — DMI_TXN0 7
DMI0TXP U28 — DMI_TXP0_R — R6U1 0 — DMI_TXP0 7
DMI1RXN Y27 — DMI_RXN1_R — R6F3 0 — DMI_RXN1 7
DMI1RXP Y26 — DMI_RXP1_R — R6F4 0 — DMI_RXP1 7
DMI1TXN W29 — DMI_TXN1_R — R6U4 0 — DMI_TXN1 7
DMI1TXP W28 — DMI_TXP1_R — R6U3 0 — DMI_TXP1 7
DMI2RXN AB27 — DMI_RXN2_R — R6F7 0 — DMI_RXN2 7
DMI2RXP AB26 — DMI_RXP2_R — R6F8 0 — DMI_RXP2 7
DMI2TXN AA29 — DMI_TXN2_R — R6U6 0 — DMI_TXN2 7
DMI2TXP AA28 — DMI_TXP2_R — R6U5 0 — DMI_TXP2 7
DMI3RXN AD27 — DMI_RXN3_R — R6F1 0 — DMI_RXN3 7
DMI3RXP AD26 — DMI_RXP3_R — R6F2 0 — DMI_RXP3 7
DMI3TXN AC29 — DMI_TXN3_R — R6U8 0 — DMI_TXN3 7
DMI3TXP AC28 — DMI_TXP3_R — R6U7 0 — DMI_TXP3 7

DMI_CLKN T26 — CLK_PCIE_ICH# 35
DMI_CLKP T25 — CLK_PCIE_ICH 35
DMI_ZCOMP AF29
DMI_IRCOMP AF28 — DMI_IRCOMP_R — R6G5 24.9 1% — +V1.5S_PCIE_ICH 21,24

USBP0N AC5 — USB_PN0 29
USBP0P AC4 — USB_PP0 29
USBP1N AD3 — USB_PN1 29
USBP1P AD2 — USB_PP1 29
USBP2N AC1 — USB_PN2 29
USBP2P AC2 — USB_PP2 29
USBP3N AA5 — USB_PN3 29
USBP3P AA4 — USB_PP3 29
USBP4N AB2 — USB_PN4 29
USBP4P AB1 — USB_PP4 29
USBP5N AA1 — USB_PN5 29
USBP5P AA2 — USB_PP5 29
USBP6N W5 — USB_PN6 29
USBP6P W4 — USB_PP6 29
USBP7N Y1 — USB_PN7 29
USBP7P Y2 — USB_PP7 29
USBP8N W1 — USB_PN8 29
USBP8P W2 — USB_PP8 29
USBP9N V2 — USB_PN9 — R8G4 — USB_PN9_R 44
USBP9P V3 — USB_PP9 — R8G6 0 — USB_PP9_R 44
USBP10N U5 — USB_PN10 29 — R8V4 0 — USB_PP9_R_FPIO 29
USBP10P U4 — USB_PP10 29
USBP11N U1 — USB_PN11 29 — R8V3 NO_STUFF — USB_PP9_R_FPIO 29
USBP11P U2 — USB_PP11 29 — NO_STUFF

24,33,34,44,48,55,57 +V3.3M_WOL
R9D9 1K SPI_MOSI_R_3.2V
J9D2
R7U11 15 SPI_MOSI_R
34 SPI_SI
34 SPI_SO

Layout Note:
R7U11,R7F7,R7F8,R7F9 to be placed within 600mils of U7F1

Buffer to reduce loading on PLT_RST#.
+V3.3S
C7T4 0.1uF 20%
U8E2 74AHC1G08
40,43 BUF_PLT_RST#
PLT_RST#
R8T6 100K

U7F1B

PCI

32 PCI_AD[31:0]
PCI_AD0 D11 — AD0
PCI_AD1 C8 — AD1
PCI_AD2 D9 — AD2
PCI_AD3 E12 — AD3
PCI_AD4 E9 — AD4
PCI_AD5 C9 — AD5
PCI_AD6 E10 — AD6
PCI_AD7 B7 — AD7
PCI_AD8 C7 — AD8
PCI_AD9 C5 — AD9
PCI_AD10 G11 — AD10
PCI_AD11 F8 — AD11
PCI_AD12 F11 — AD12
PCI_AD13 E7 — AD13
PCI_AD14 A3 — AD14
PCI_AD15 D2 — AD15
PCI_AD16 F10 — AD16
PCI_AD17 D5 — AD17
PCI_AD18 D10 — AD18
PCI_AD19 B3 — AD19
PCI_AD20 F7 — AD20
PCI_AD21 C3 — AD21
PCI_AD22 F3 — AD22
PCI_AD23 F4 — AD23
PCI_AD24 C1 — AD24
PCI_AD25 G7 — AD25
PCI_AD26 H7 — AD26
PCI_AD27 D1 — AD27
PCI_AD28 G5 — AD28
PCI_AD29 H6 — AD29
PCI_AD30 G1 — AD30
PCI_AD31 H3 — AD31

REQ0# F1 — PCI_REQ#0 32
GNT0# G4 — PCI_GNT#0 32
REQ1#/GPIO50 B6 — PCI_REQ#1 32
GNT1#/GPIO51 A7 — PCI_GNT#1 32
REQ2#/GPIO52 F13 — ICH_GPIO52
GNT2#/GPIO53 F12 — ICH_GPIO53
REQ3#/GPIO54 E6 — PCI_REQ#3 32
GNT3#/GPIO55 F6 — PCI_GNT#3 32

C/BE0# D8 — PCI_CBE#0 32
C/BE1# B4 — PCI_CBE#1 32
C/BE2# D6 — PCI_CBE#2 32
C/BE3# A5 — PCI_CBE#3 32

IRDY# D3 — PCI_IRDY# 32
PAR E3 — PCI_PAR 32
PCIRST# R1 — PCI_RST# 32,41
DEVSEL# C6 — PCI_DEVSEL# 32
PERR# F4 — PCI_PERR# 32
PLOCK# C2 — PCI_LOCK# 32
SERR# J4 — PCI_SERR# 32
STOP# A4 — PCI_STOP# 32
TRDY# F5 — PCI_TRDY# 32
FRAME# D7 — PCI_FRAME# 32

PLTRST# G14 — PLT_RST# 7,19,25,26,38,41,57
PCICLK D4 — CLK_PCIF_ICH 36
PME# R2 — PCI_PME# 32,43

Interrupt I/F

INT_PIRQA# J5
INT_PIRQB# E1
INT_PIRQC# J6 — 32 INT_PIRQC#
INT_PIRQD# E4
PIRQE#/GPIO2 H4 — INT_PIRQE# 32
PIRQF#/GPIO3 K6 — INT_PIRQF# 32
PIRQG#/GPIO4 F2 — INT_PIRQG# 32
PIRQH#/GPIO5 G2 — INT_PIRQH# 32

ICH9M REV 1.0

ICH9M Pullups

+V3.3S

PCI_FRAME# RP8C1A 1 — 8 8.2K
PCI_IRDY# RP8C1B 2 — 7 8.2K
PCI_TRDY# RP8C1C 3 — 6 8.2K
PCI_STOP# RP9D1A 1 — 8 8.2K
PCI_SERR# RP9D1D 4 — 5 8.2K
PCI_DEVSEL# RP8C1D 4 — 5 8.2K
PCI_PERR# RP9D1C 3 — 6 8.2K
PCI_LOCK# RP9D1B 2 — 7 8.2K
PCI_REQ#0 RP9B1A 1 — 8 8.2K
PCI_REQ#1 RP9C1B 2 — 7 8.2K
ICH_GPIO52 RP9C1D 4 — 5 8.2K
PCI_REQ#3 RP9C1C 3 — 6 8.2K

INT_PIRQA# RP9C1A 1 — 8 8.2K
INT_PIRQB# RP9B1D 4 — 5 8.2K
INT_PIRQC# RP9B2A 1 — 8 8.2K
INT_PIRQD# RP9B1C 3 — 6 8.2K
INT_PIRQE# RP9B2B 2 — 7 8.2K
INT_PIRQF# RP9B2C 3 — 6 8.2K
INT_PIRQG# RP9B2D 4 — 5 8.2K
INT_PIRQH# RP9B1B 2 — 7 8.2K

PCI_GNT#3

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default (Jumper 1-X)

J8G7

PCI_GNT#0 R8F10 1K 5% PCI_GNT#0_R
SPI_CS#1

GNT#0 and SPI_CS#1 have a weak internal pull up

Boot BIOS Strap

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

R7F3 1K NO_STUFF
J8H1
Default : 1-2

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Title: ICH9M (2 of 4)			
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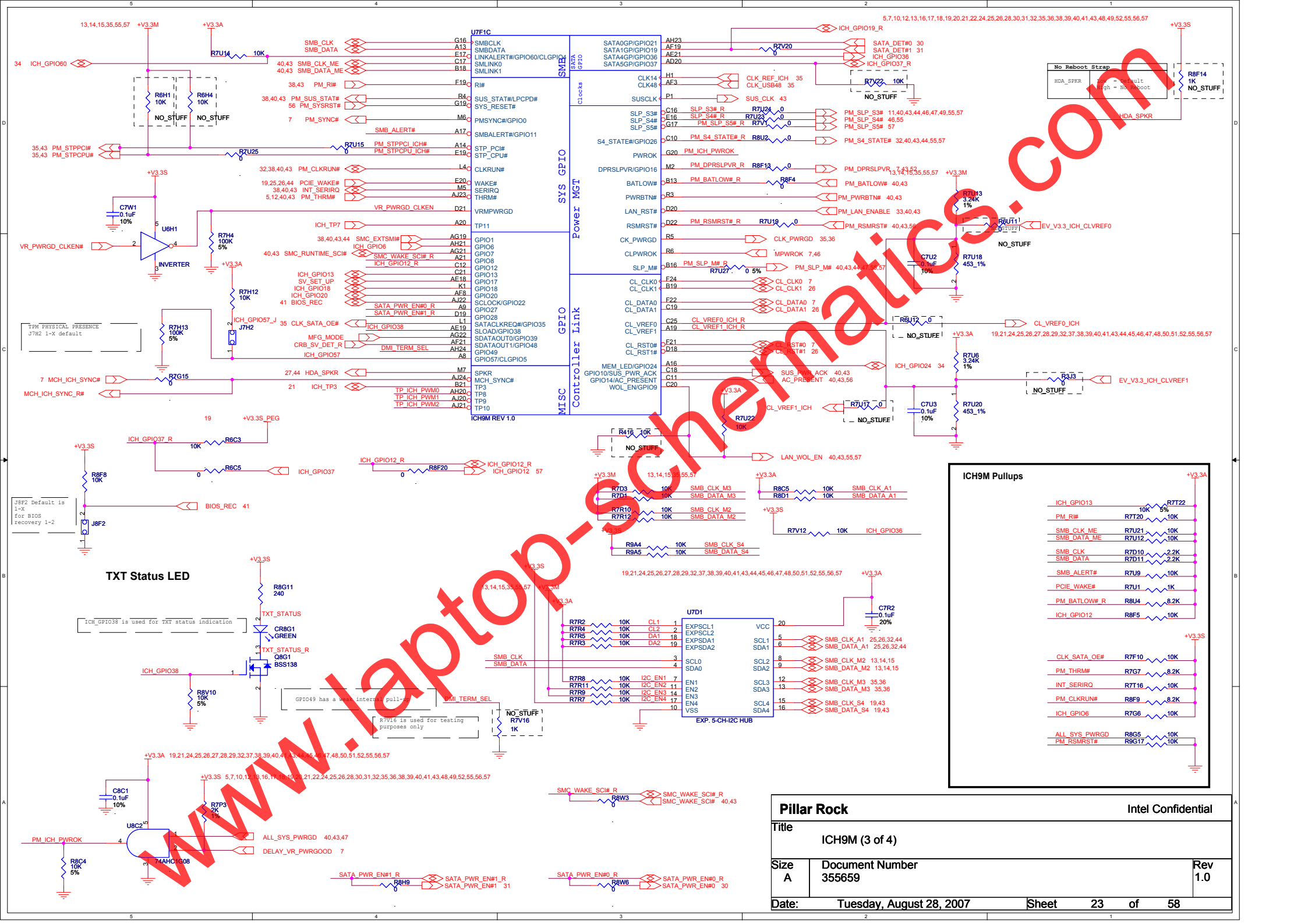

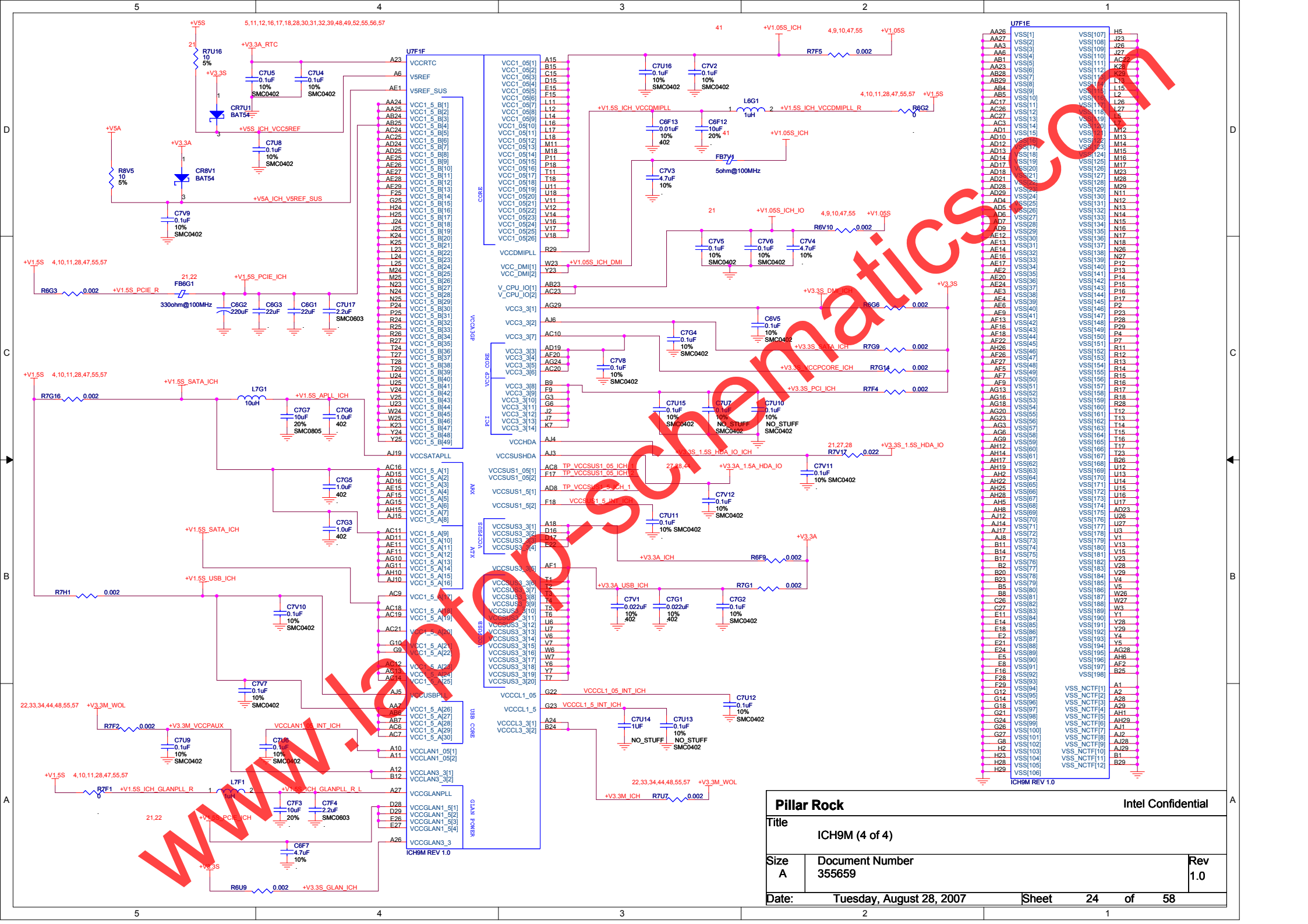
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ICH9M REV 1.0
U7F1E
ICH9M REV 1.0
Pillar Rock
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ICH9M (4 of 4)
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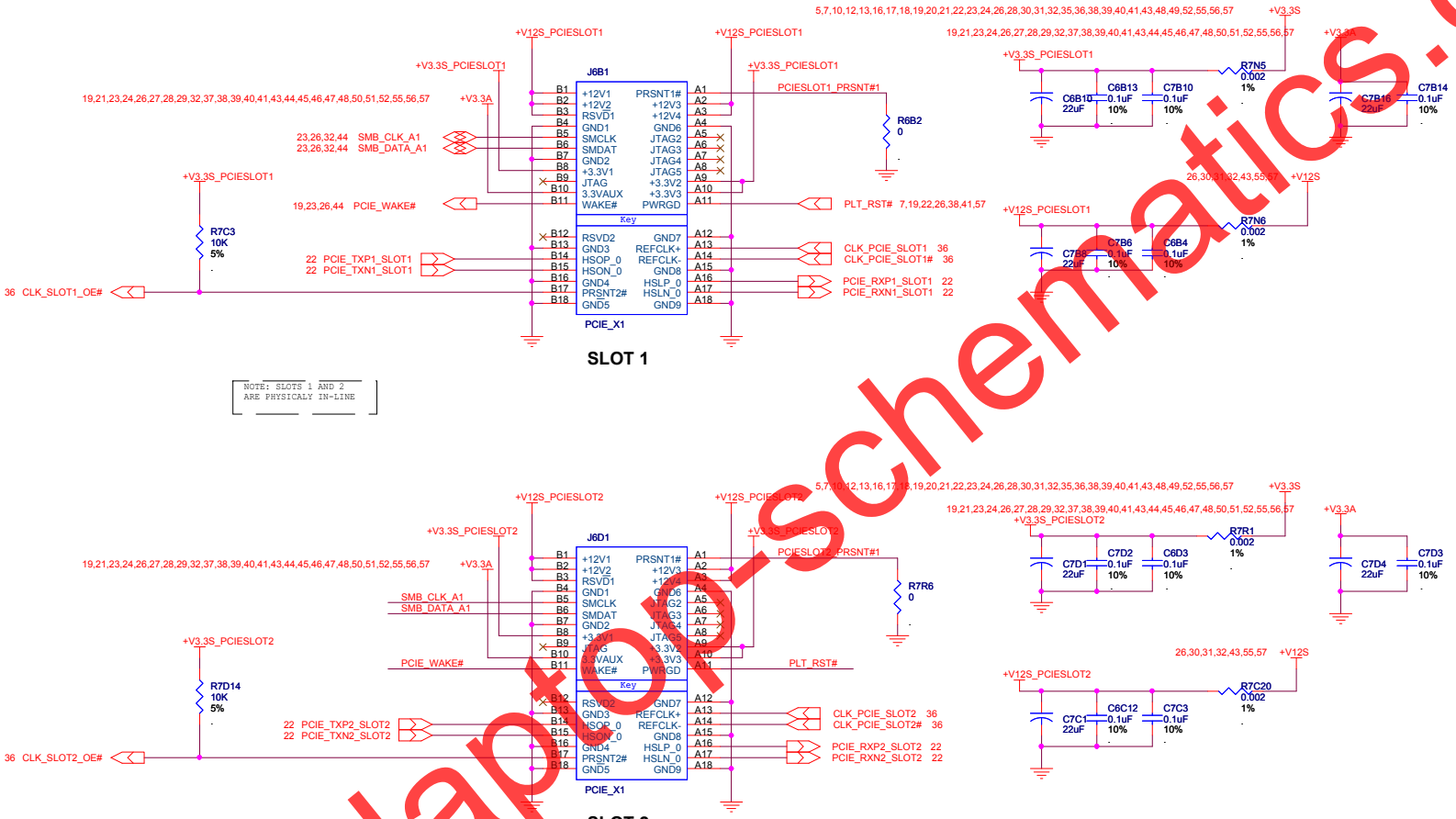

Pillar Rock		Intel Confidential
Title	PCI-E Slots (1 & 2)	
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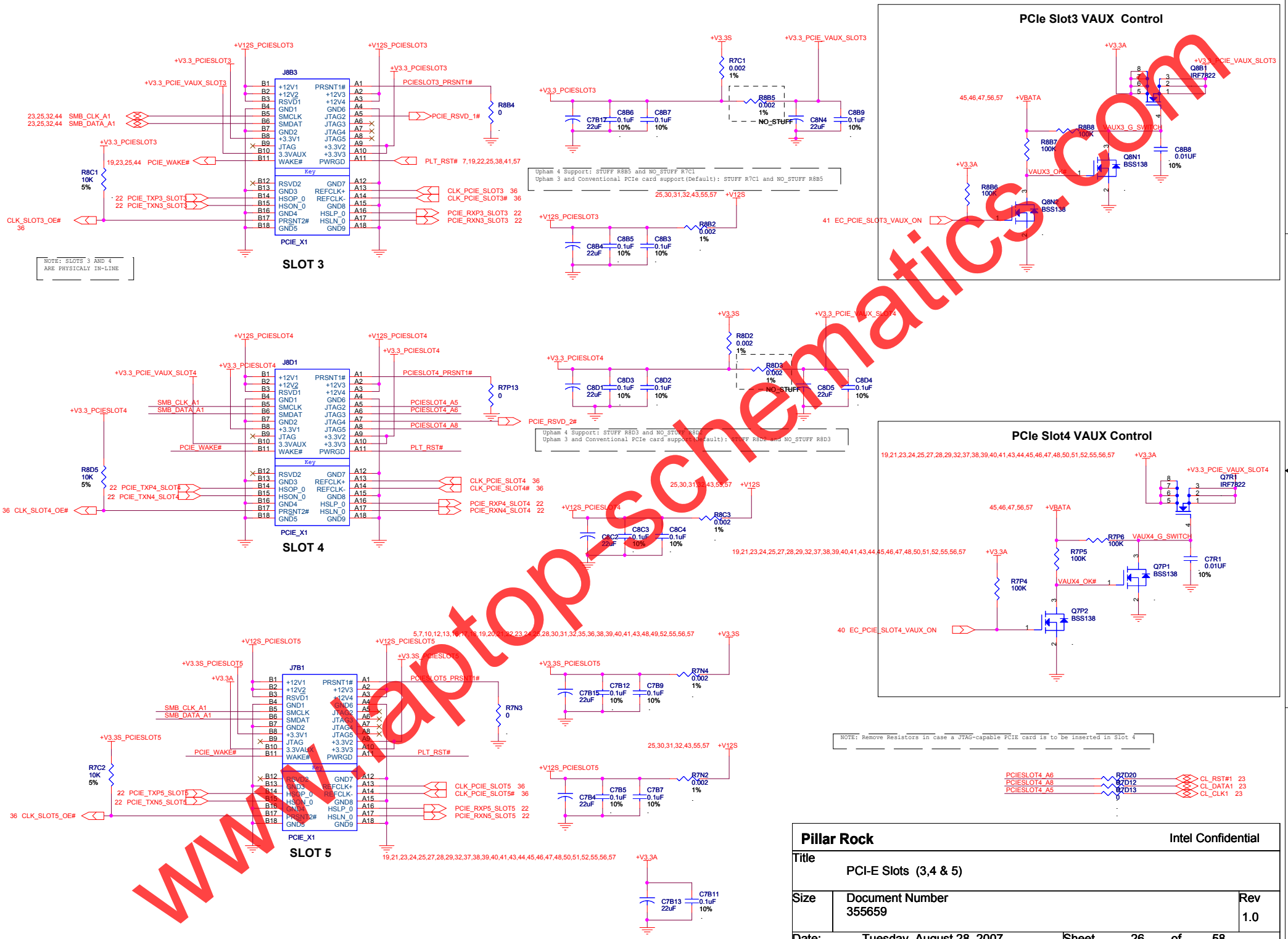

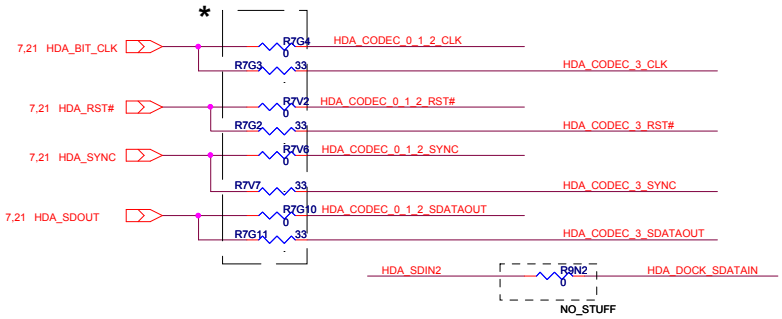

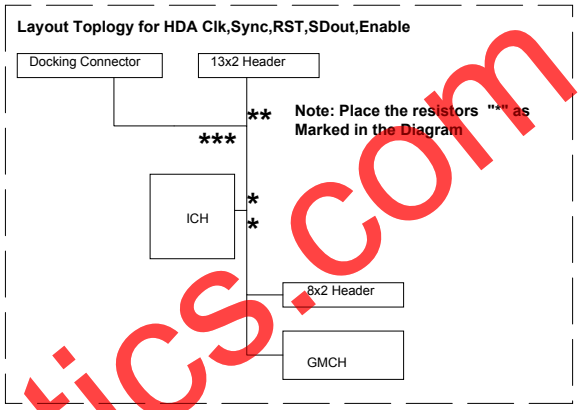

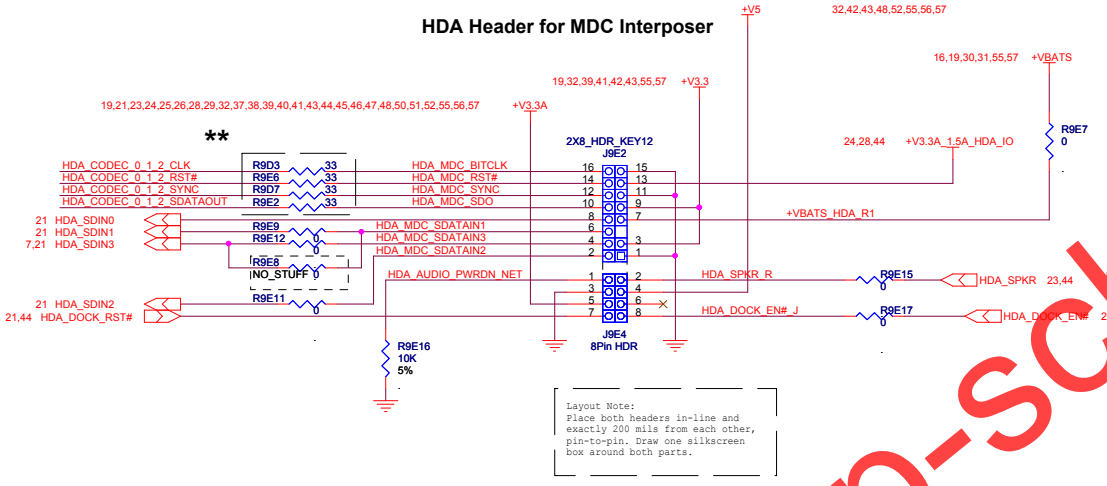

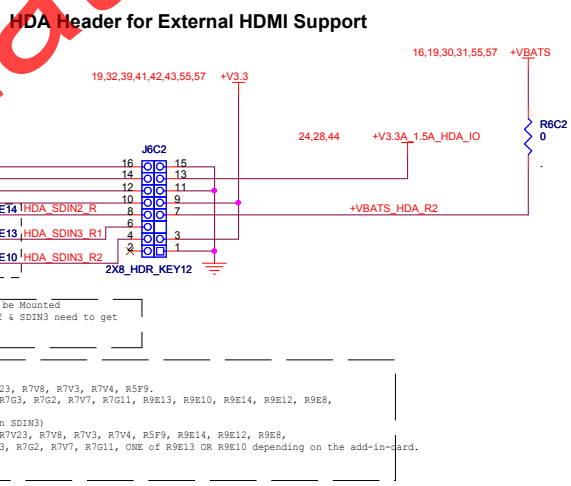

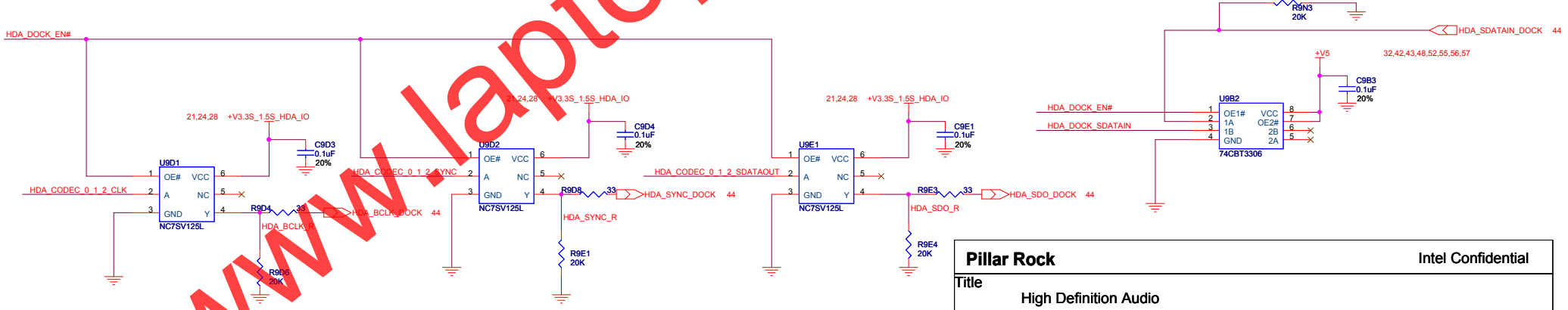

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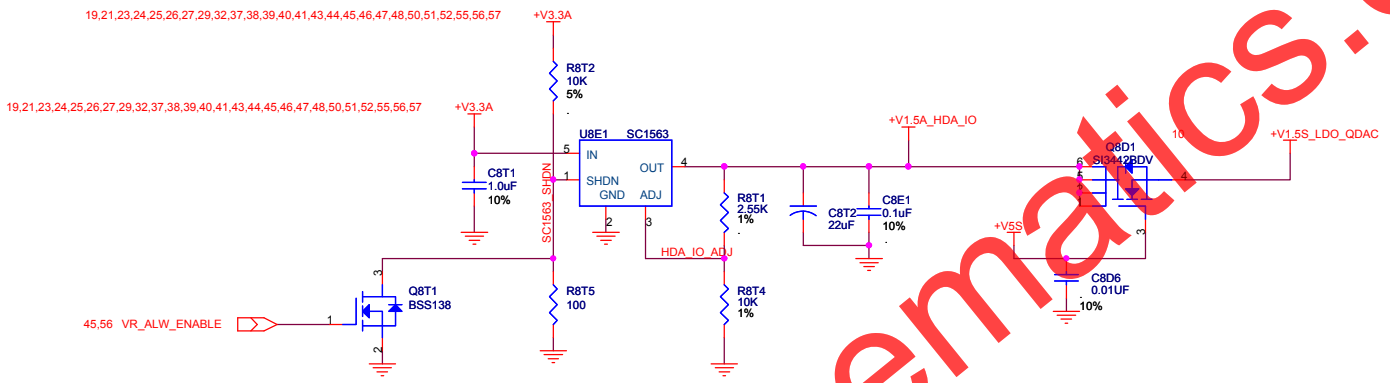
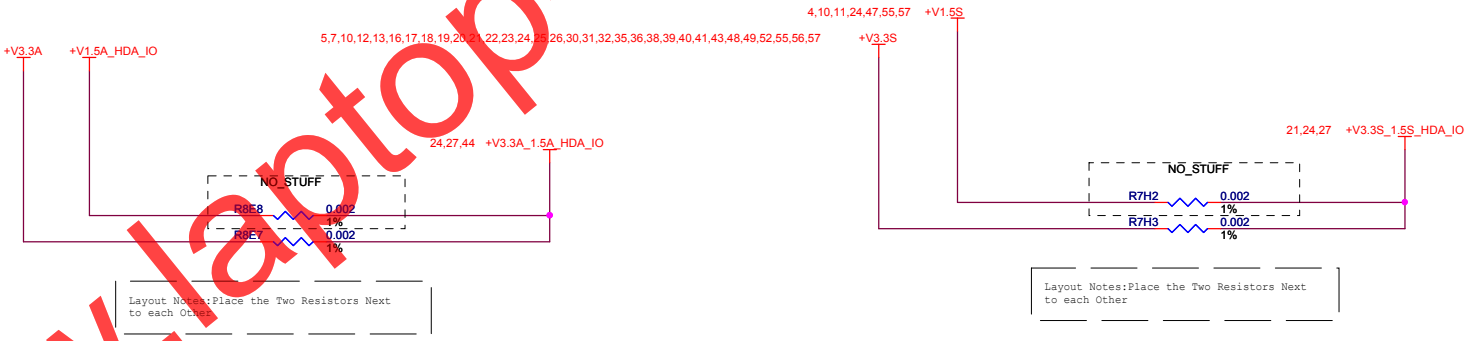
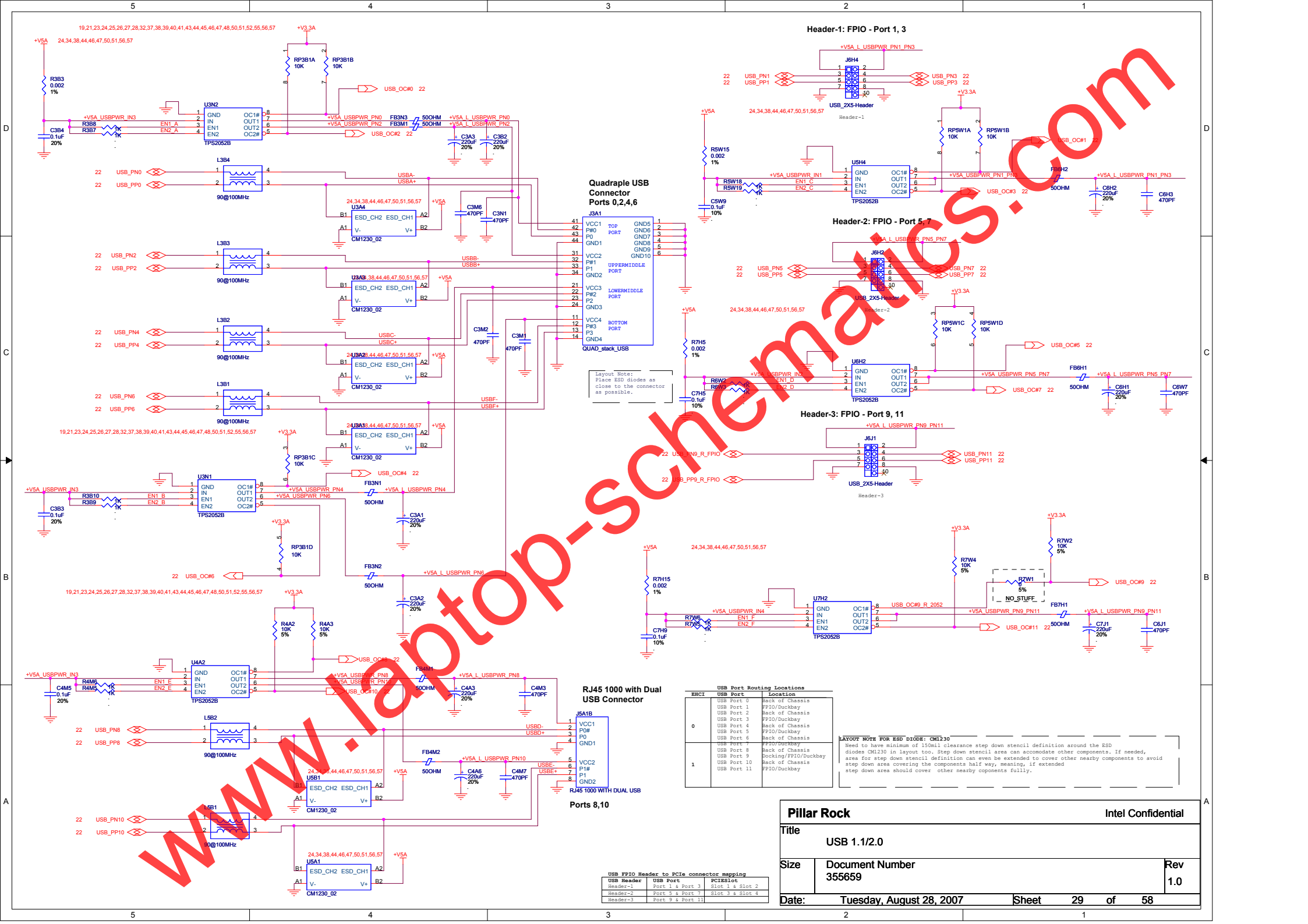
Power Supply for High Definiton Audio



Selection of I/O Voltage for the High Definition Audio



Pillar Rock		Intel Confidential
Title: HDA Power Supply		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 28 of 58	



USB Port Routing Locations

EHCI	USB Port	Location
0	USB Port 0	Back of Chassis
	USB Port 1	FPIO/Duckbay
	USB Port 2	Back of Chassis
	USB Port 3	FPIO/Duckbay
	USB Port 4	Back of Chassis
	USB Port 5	FPIO/Duckbay
	USB Port 6	Back of Chassis
1	USB Port 7	FPIO/Duckbay
	USB Port 8	Back of Chassis
	USB Port 9	Docking/FPIO/Duckbay
	USB Port 10	Back of Chassis
	USB Port 11	FPIO/Duckbay

LAYOUT NOTE FOR ESD DIODE: CM1230

Need to have minimum of 150mil clearance step down stencil definition around the ESD diodes CM1230 in layout too. Step down stencil area can accomodate other components. If needed, area for step down stencil definition can even be extended to cover other nearby components to avoid step down area covering the components half way, meaning, if extended step down area should cover other nearby coponents fullly.

USB FPIO Header to PCIe connector mapping

USB Header	USB Port	PCIESlot
Header-1	Port 1 & Port 3	Slot 1 & Slot 2
Header-2	Port 5 & Port 7	Slot 3 & Slot 4
Header-3	Port 9 & Port 11	

Pillar Rock		Intel Confidential
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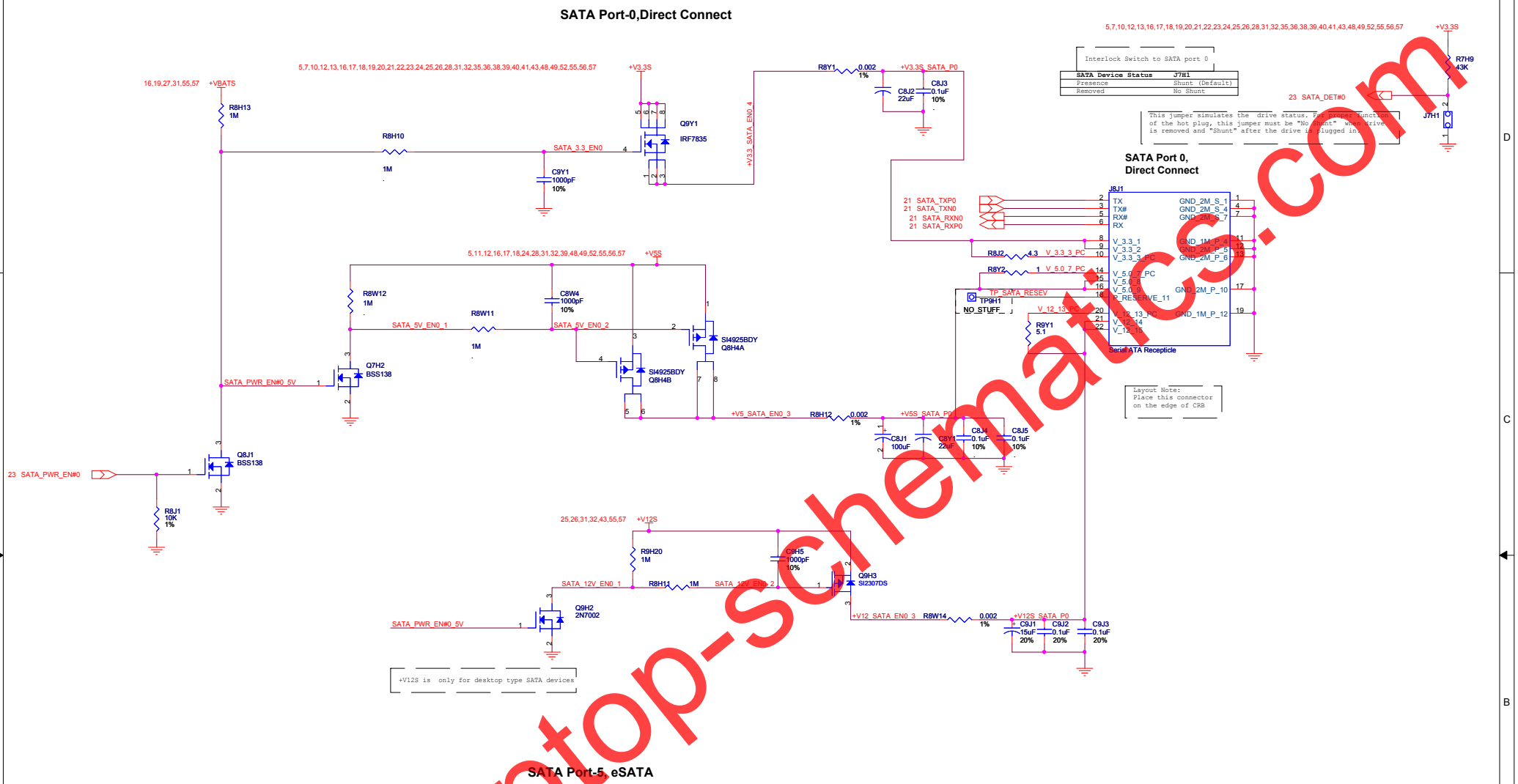

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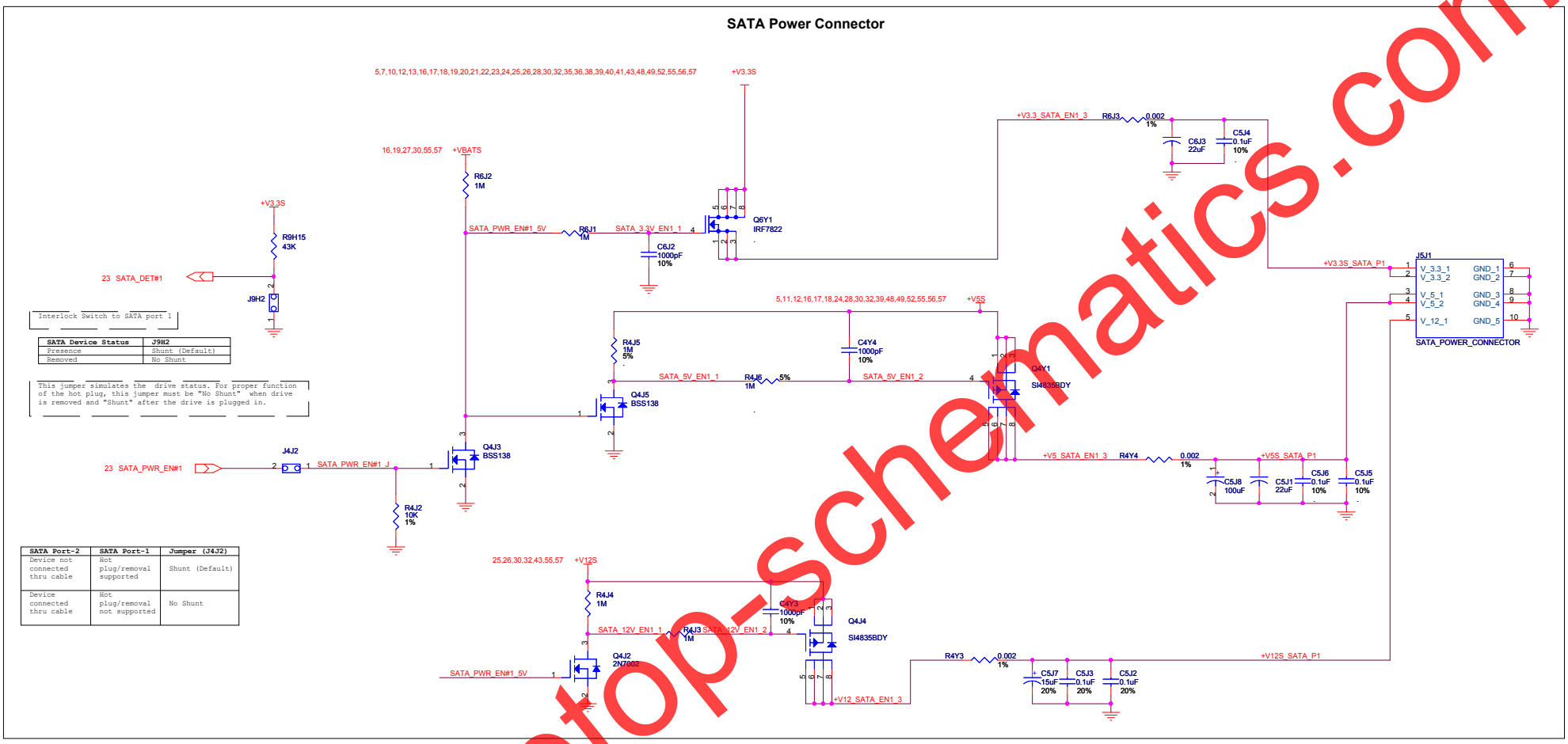
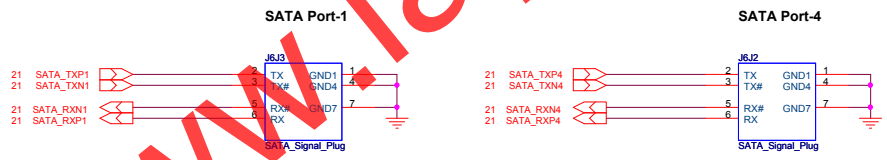
SATA Port-1 and Port-2, Cable Connect

SATA Power Connector

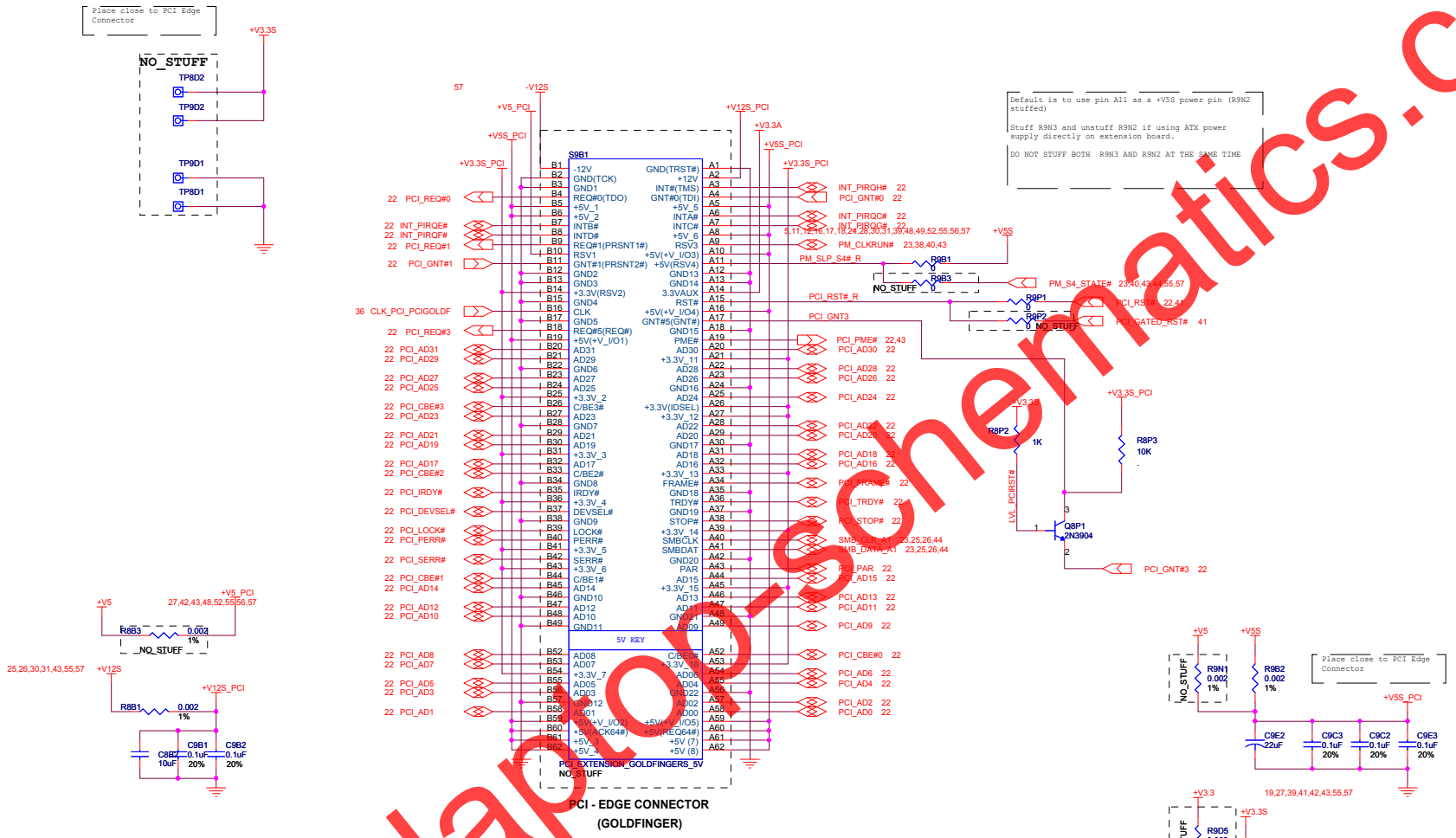


SATA Signal Connectors

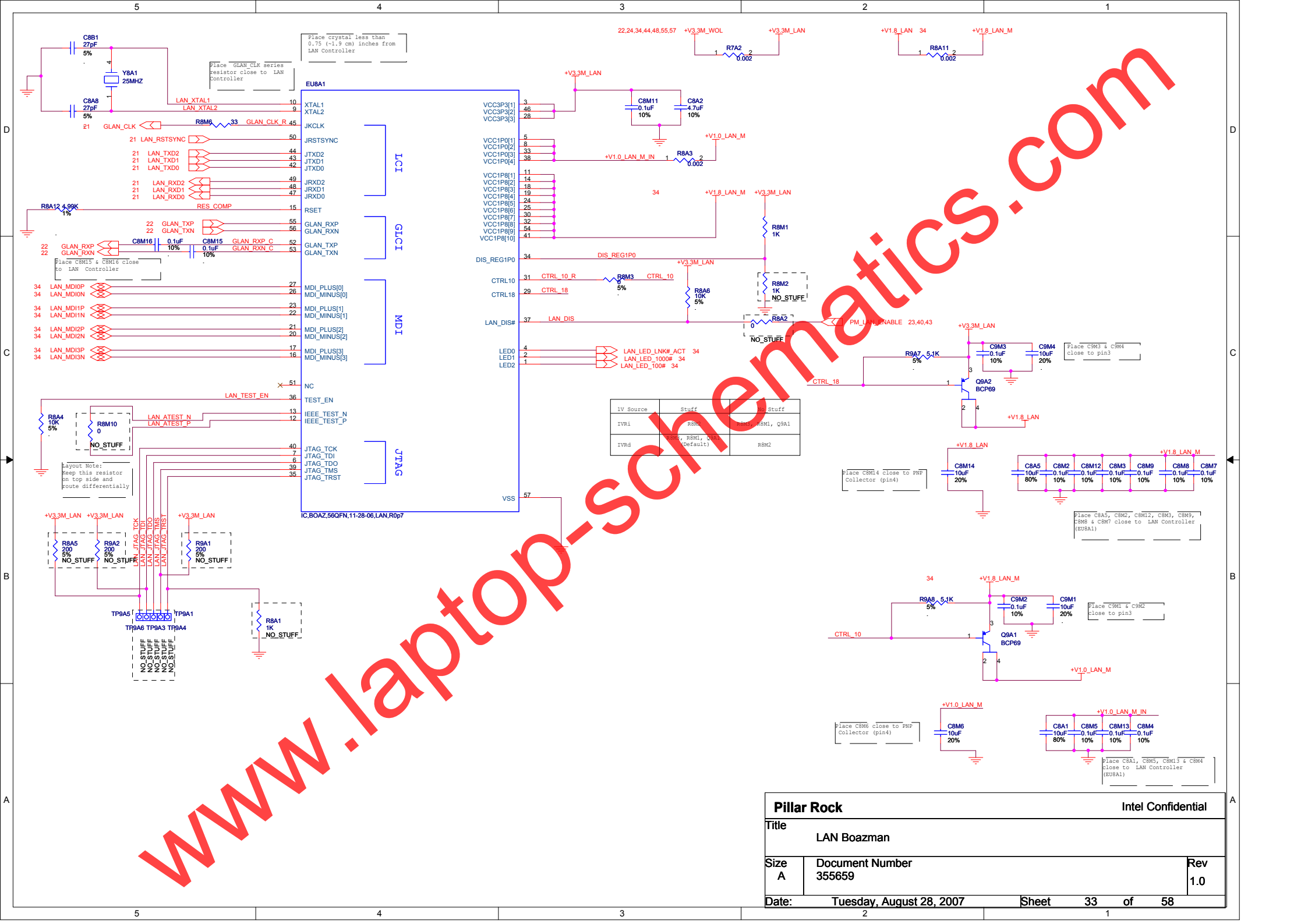


Notes:
-- Both SATA Port-1 and SATA Port-2 share the same power connector, J5J1
-- Use Y-Cable available with Kit to feed the power from J5J1 to SATA device on port-1 and SATA device on port-2.
-- Connect Power cable first before connecting SATA signal cable.

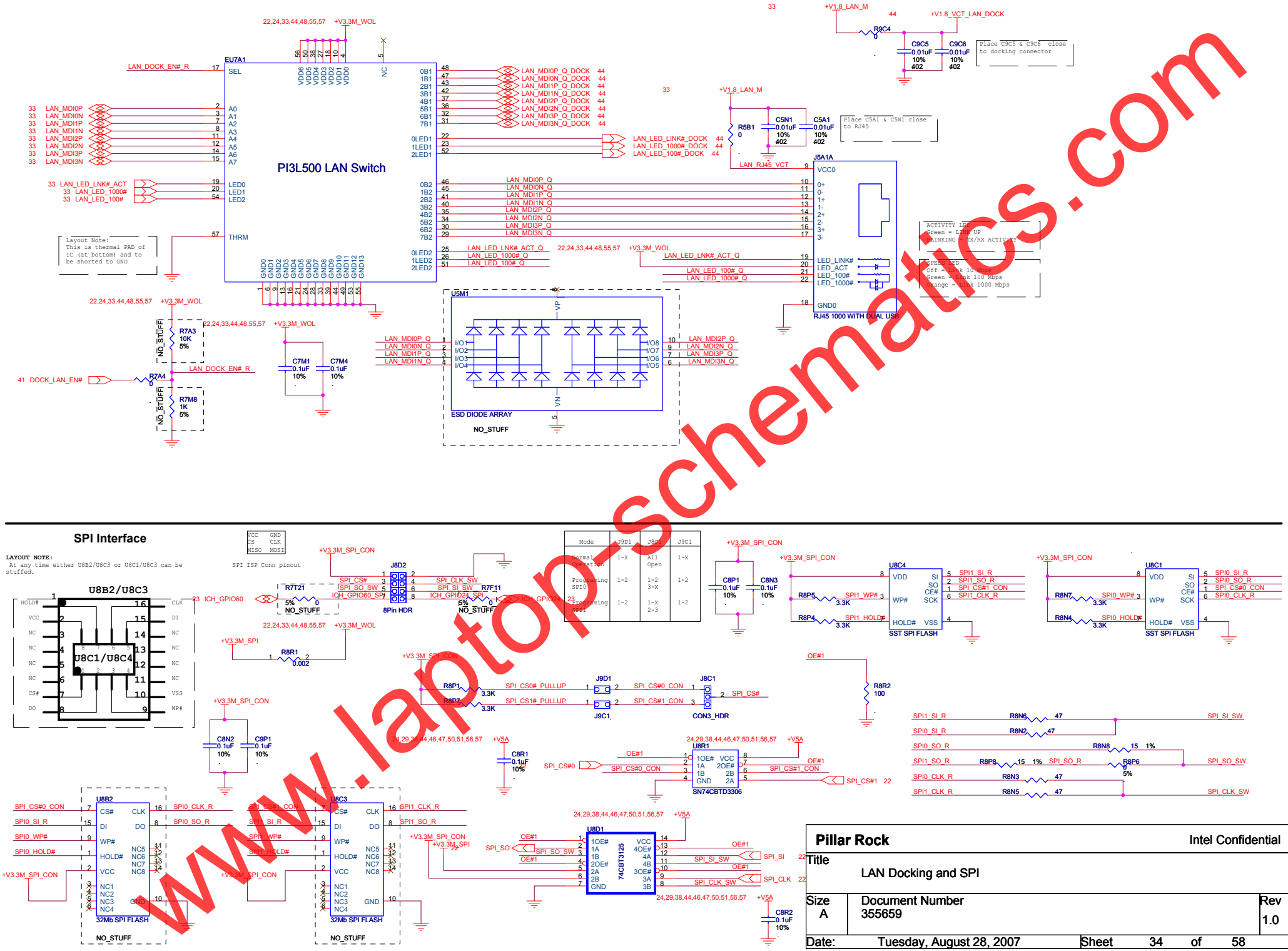
Pillar Rock		Intel Confidential
Title	SATA (2 and 3 of 3)	
Size	Document Number 355659	Rev 1.0
Date: Tuesday, August 28, 2007	Sheet 31 of 58	

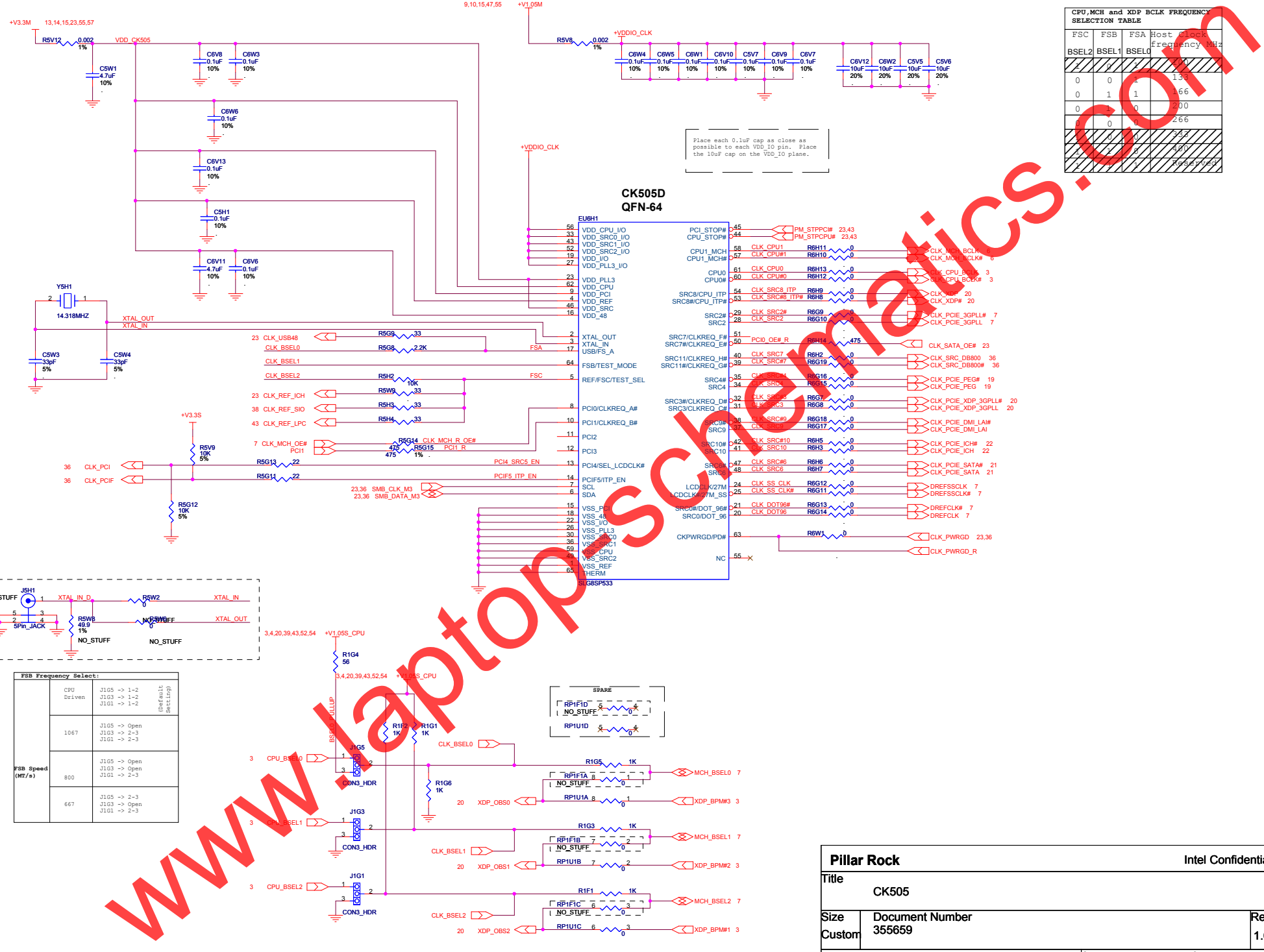


Pillar Rock		Intel Confidential
Title	PCI Edge Connector (Goldfinger)	
Size	Document Number 355659	Rev 1.0
Date: Tuesday, August 28, 2007	Sheet 32 of 58	

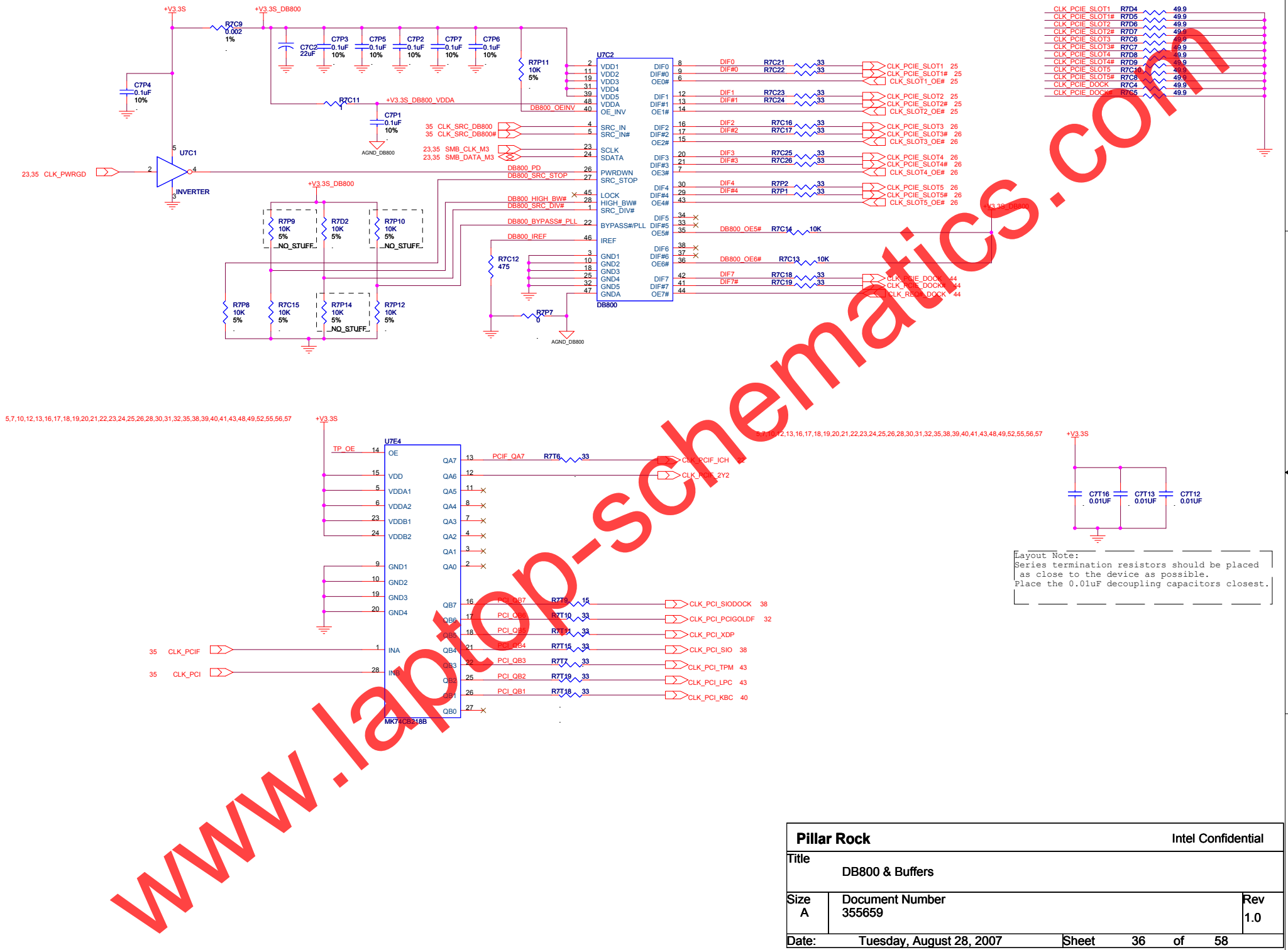


Pillar Rock		Intel Confidential
Title: LAN Boazman		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 33 of 58	



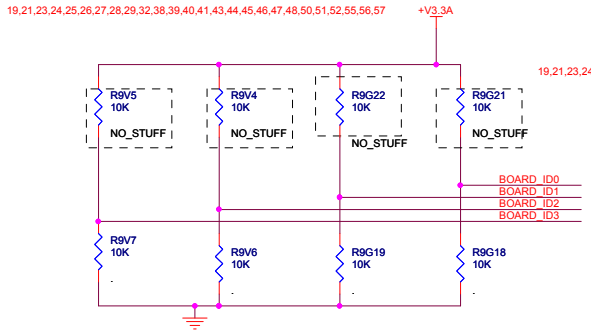


Pillar Rock	Intel Confidential
Title: CK505	
Size: Custom	Document Number: 355659
Rev: 1.0	
Date: Tuesday, August 28, 2007	Sheet 35 of 58

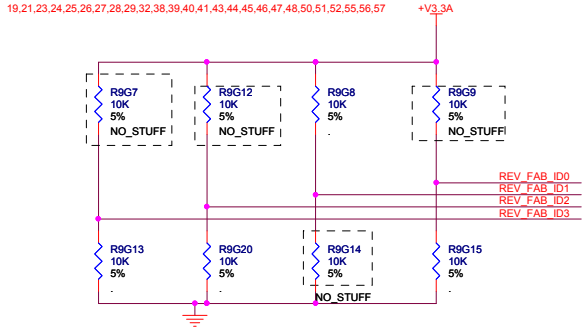


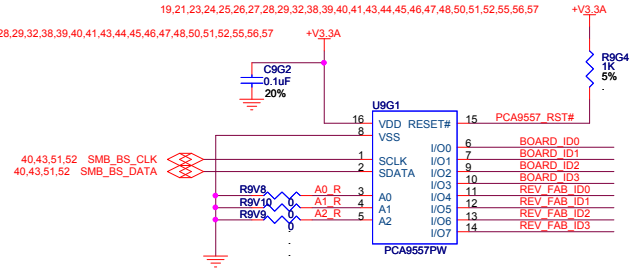
Pillar Rock		Intel Confidential
Title	DB800 & Buffers	
Size A	Document Number 355659	Rev 1.0
Date: Tuesday, August 28, 2007	Sheet 36 of 58	

BOARD REVISION

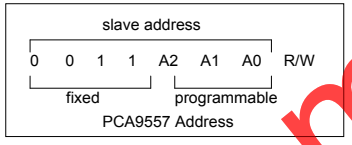


FAB REVISION





8-bit I/O Port Expander



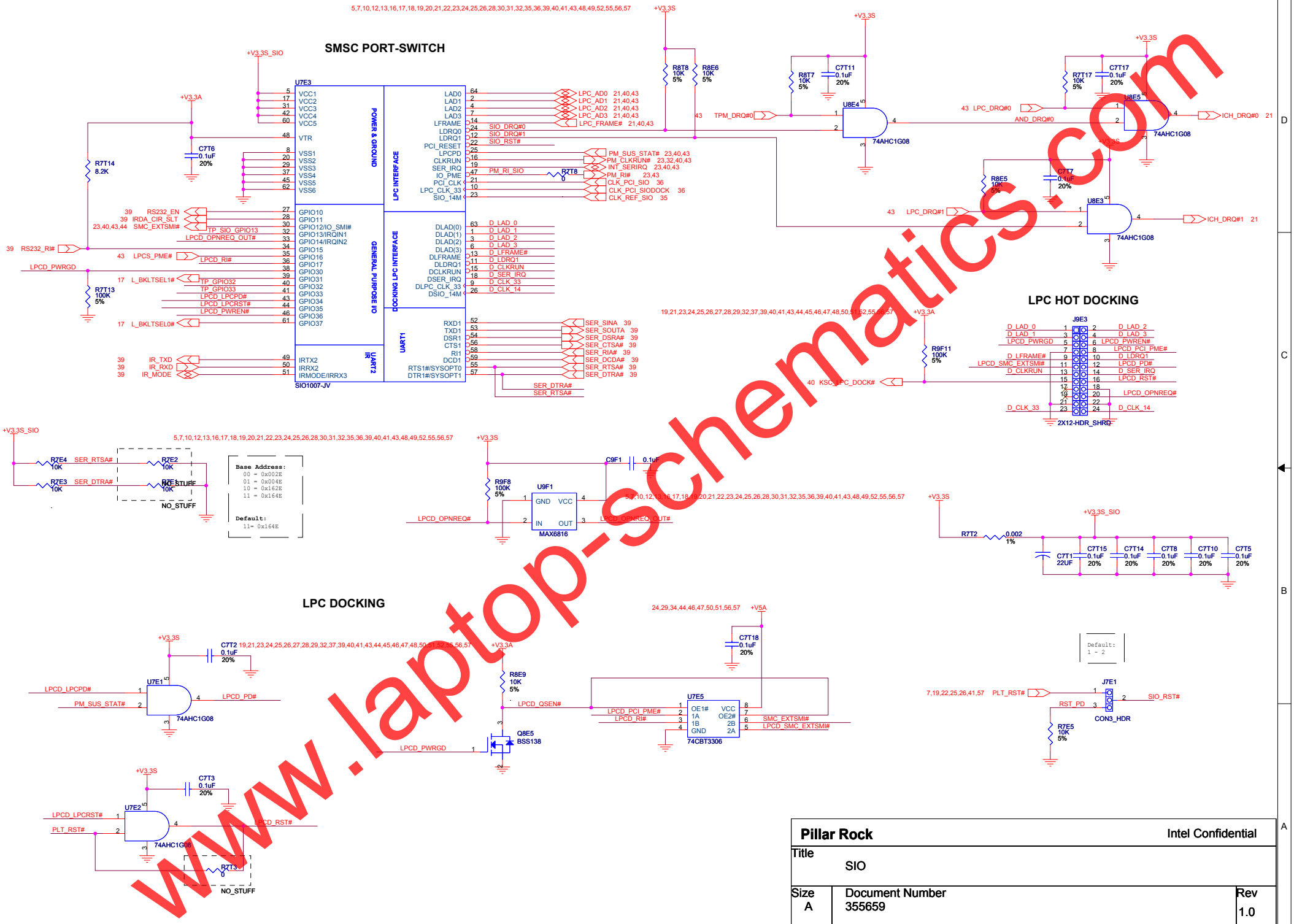
FAB ID Strapping Table

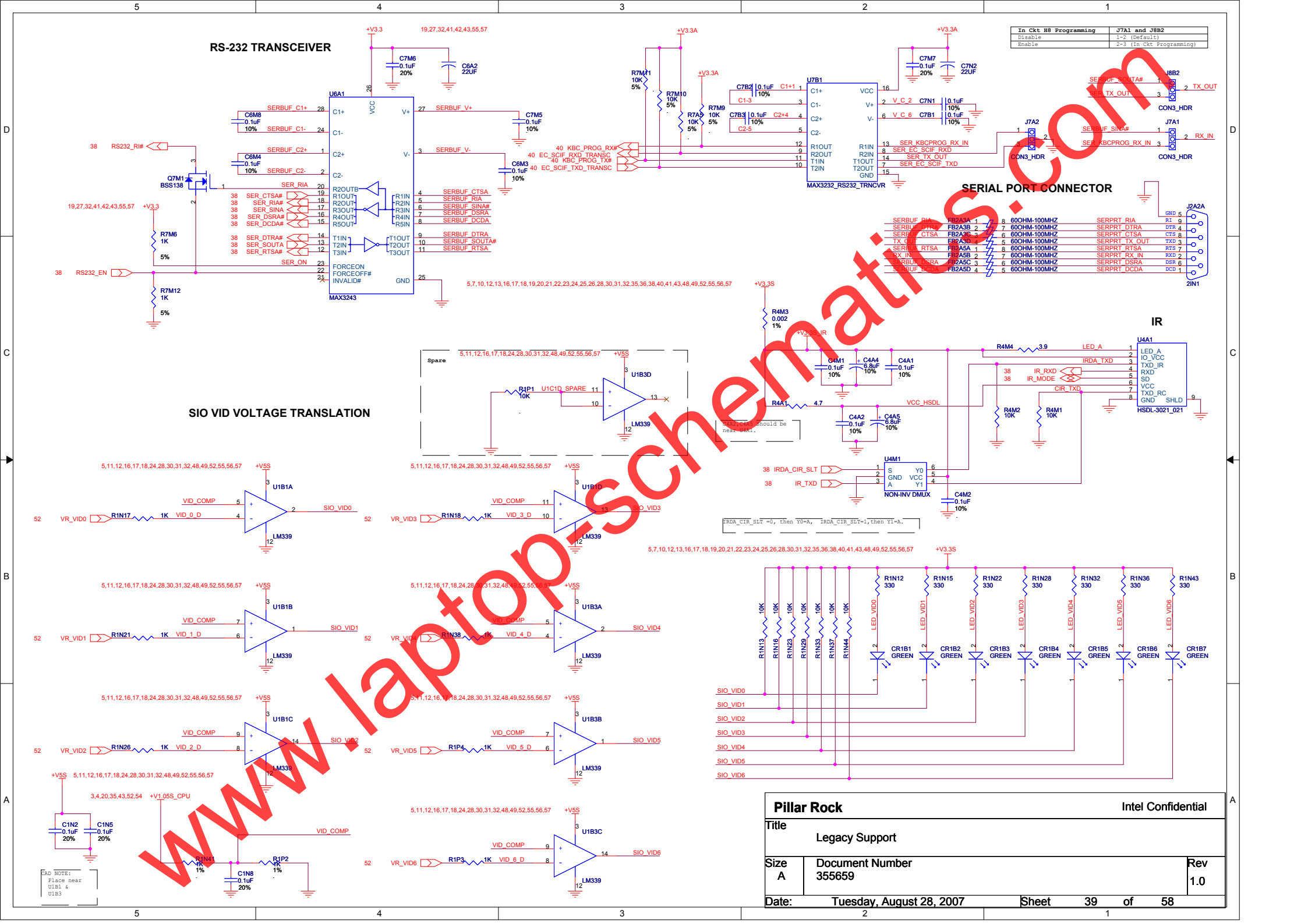
FAB_REV 3	2	1	0	BOARD FAB
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

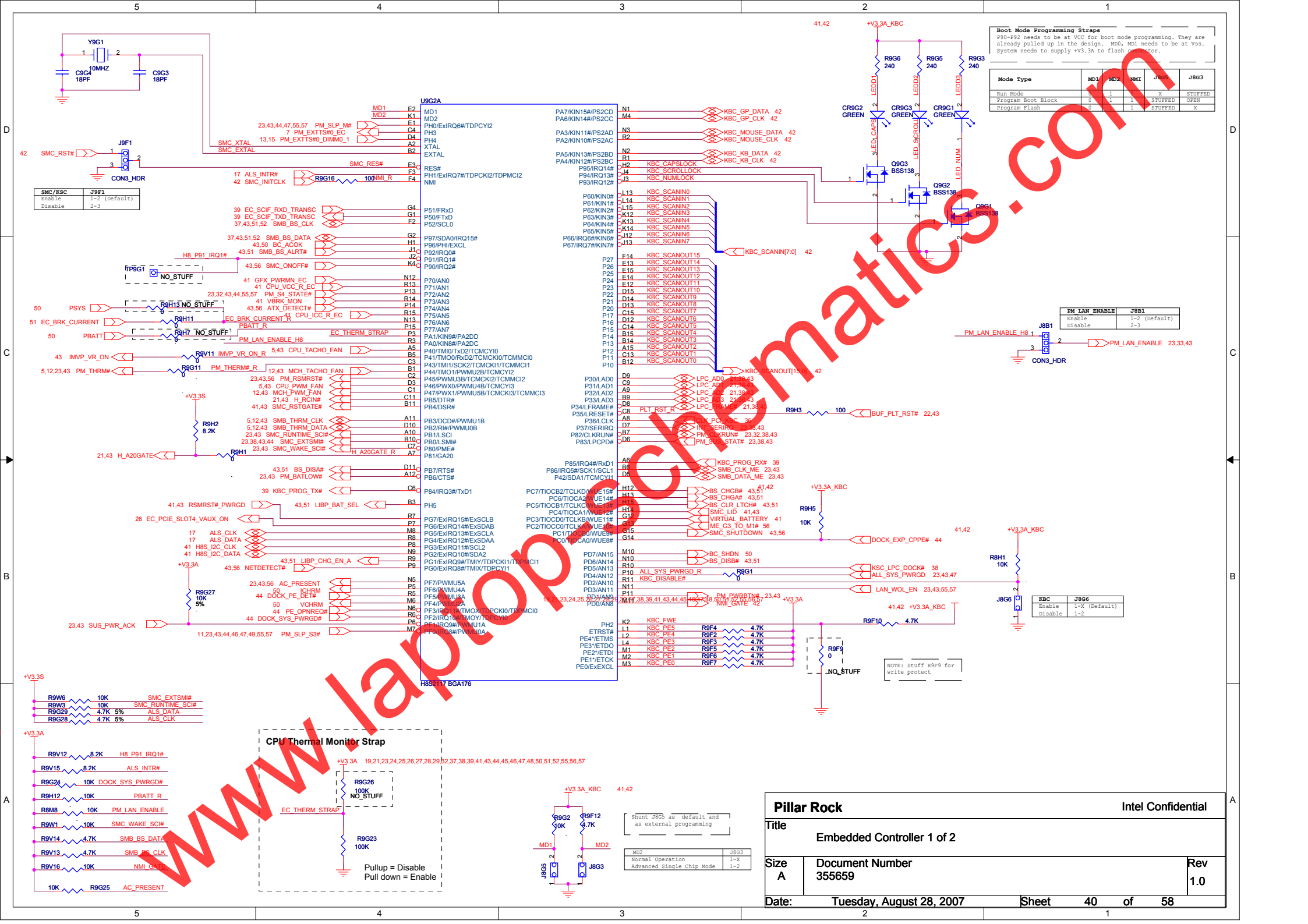
BOARD REVISION Strapping Table

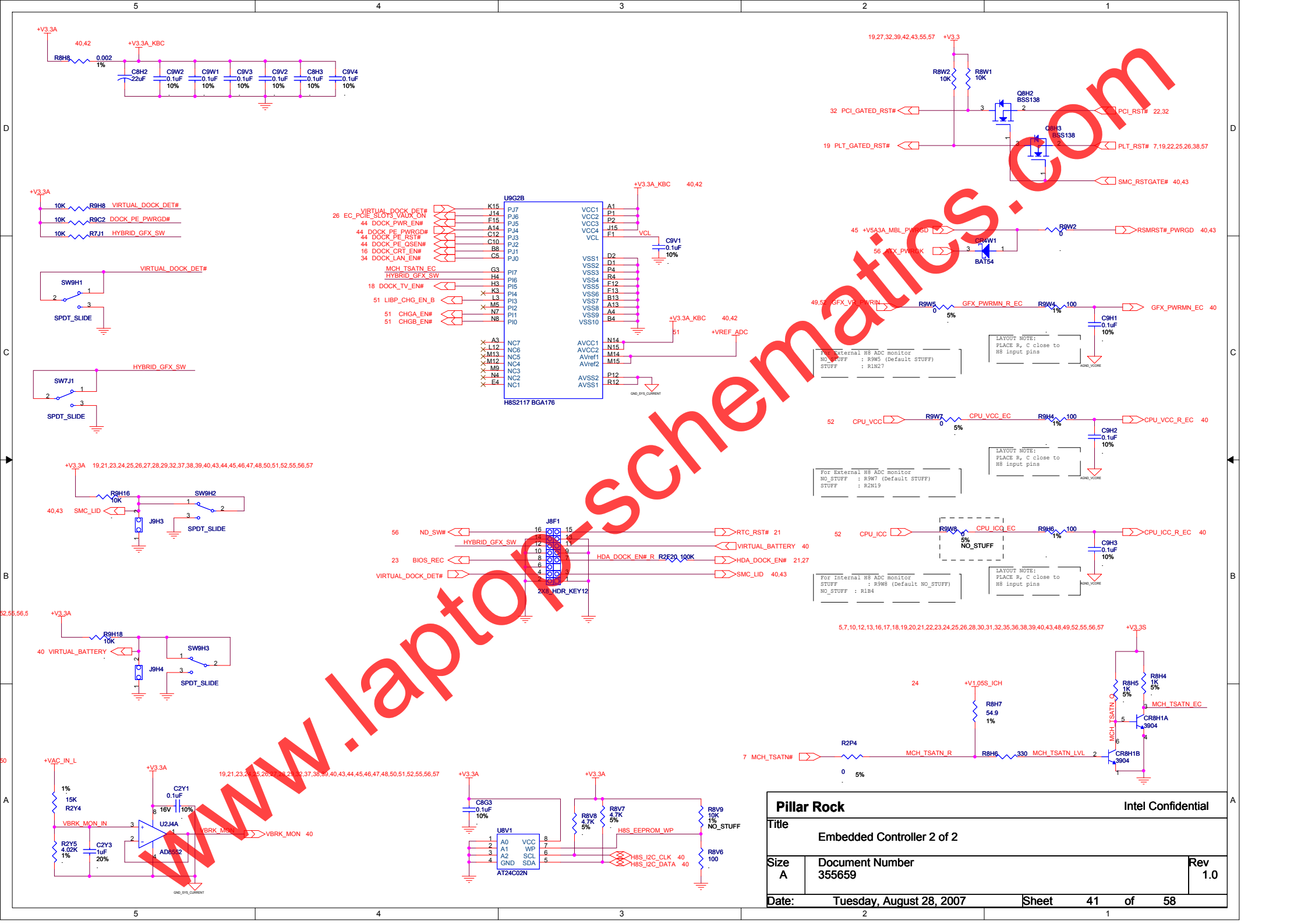
BOARD_REVISION 3	2	1	0	BOARD ID
0	0	0	0	Pillar Rock
0	0	0	1	Silver Cascade
0	0	1	0	Fern Hill
0	0	1	1	STHI CPV-MCH DDR2
0	1	0	0	STHI CPV-MCH DDR3
0	1	0	1	STHI CPV-ICH DDR2
0	1	1	0	STHI PPV-PGA DDR2
0	1	1	1	Sundial
1	0	0	0	TBD
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD

Pillar Rock		Intel Confidential
Title: I/O Port Expander		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 37 of 58	

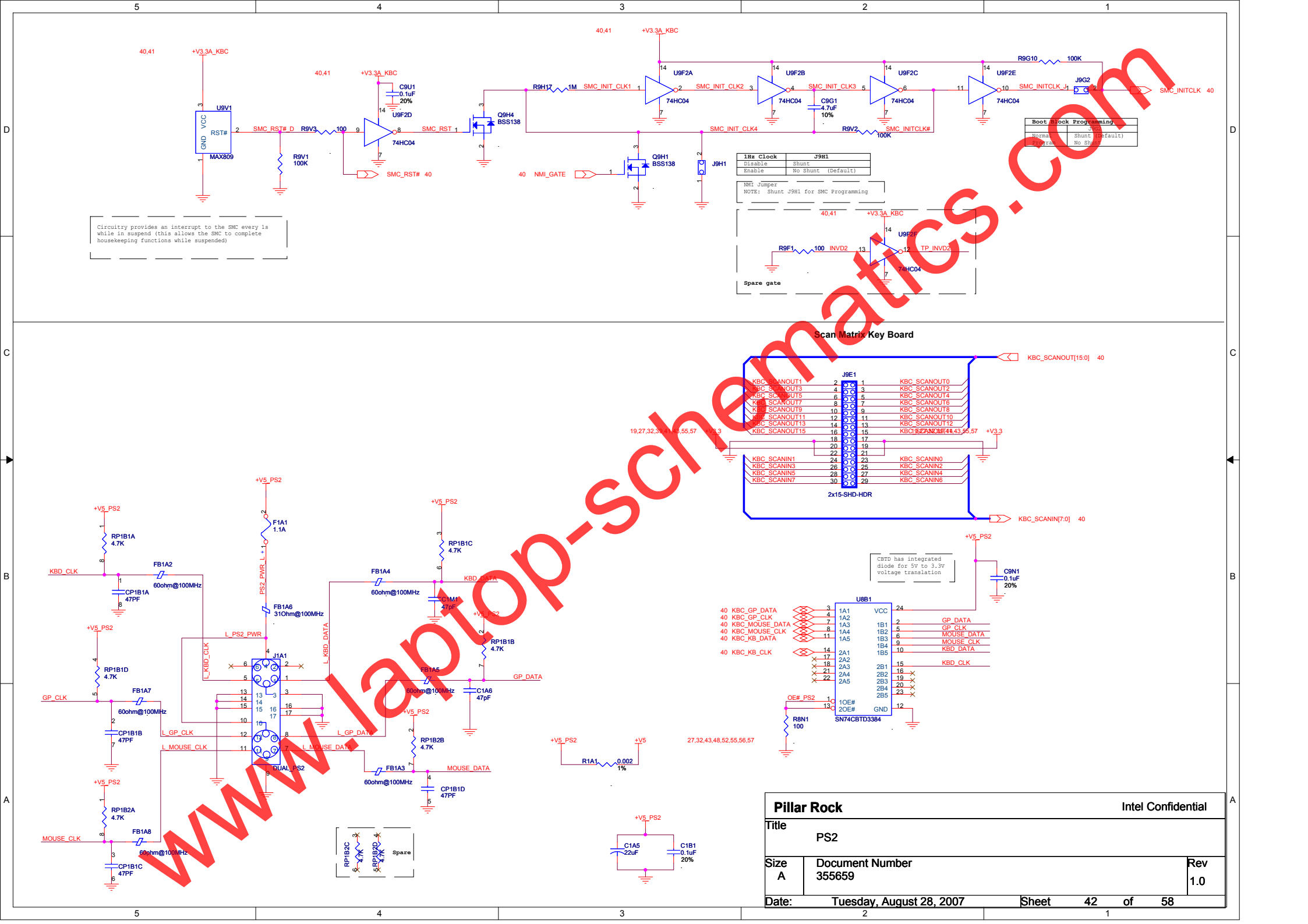


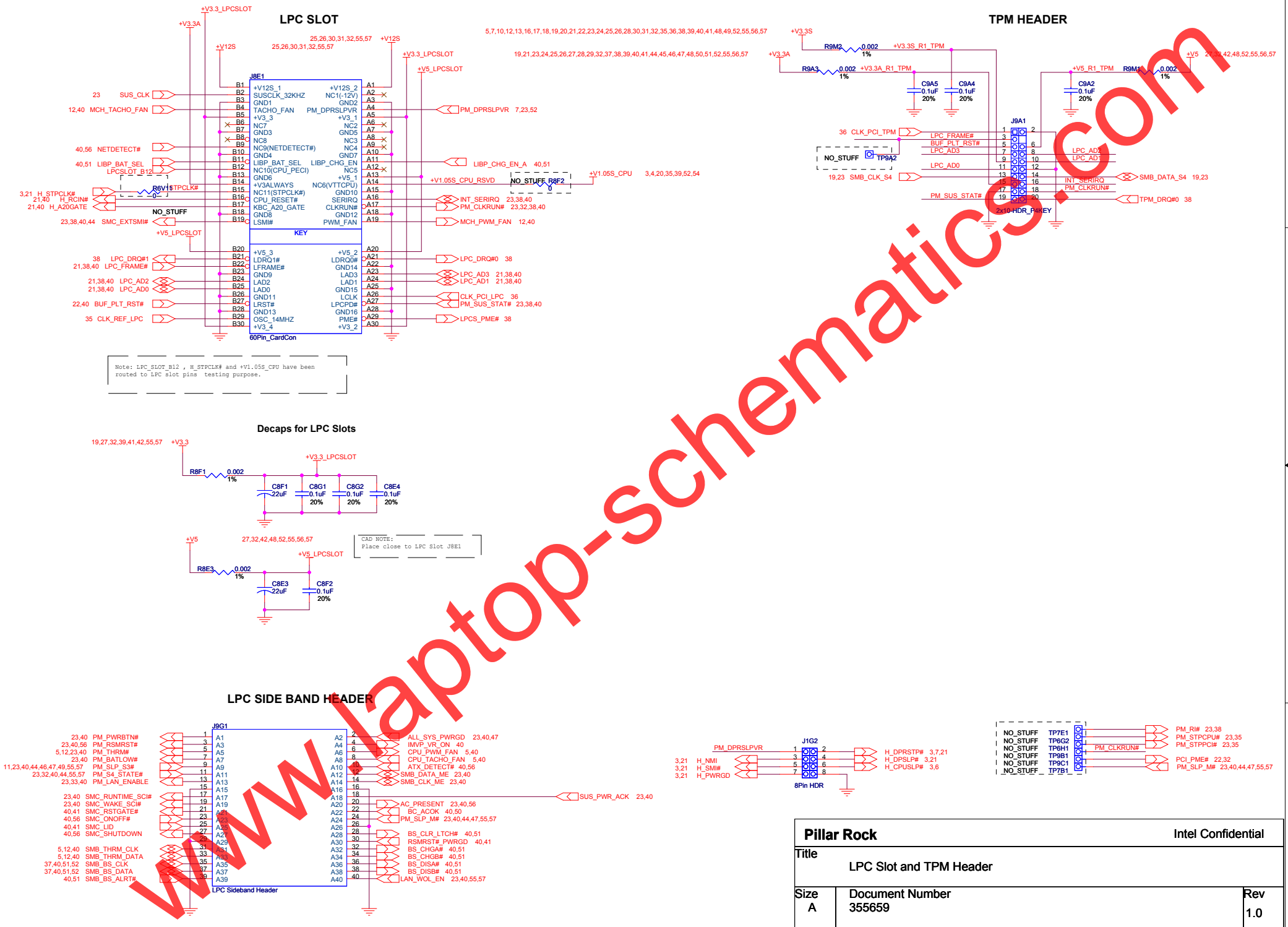






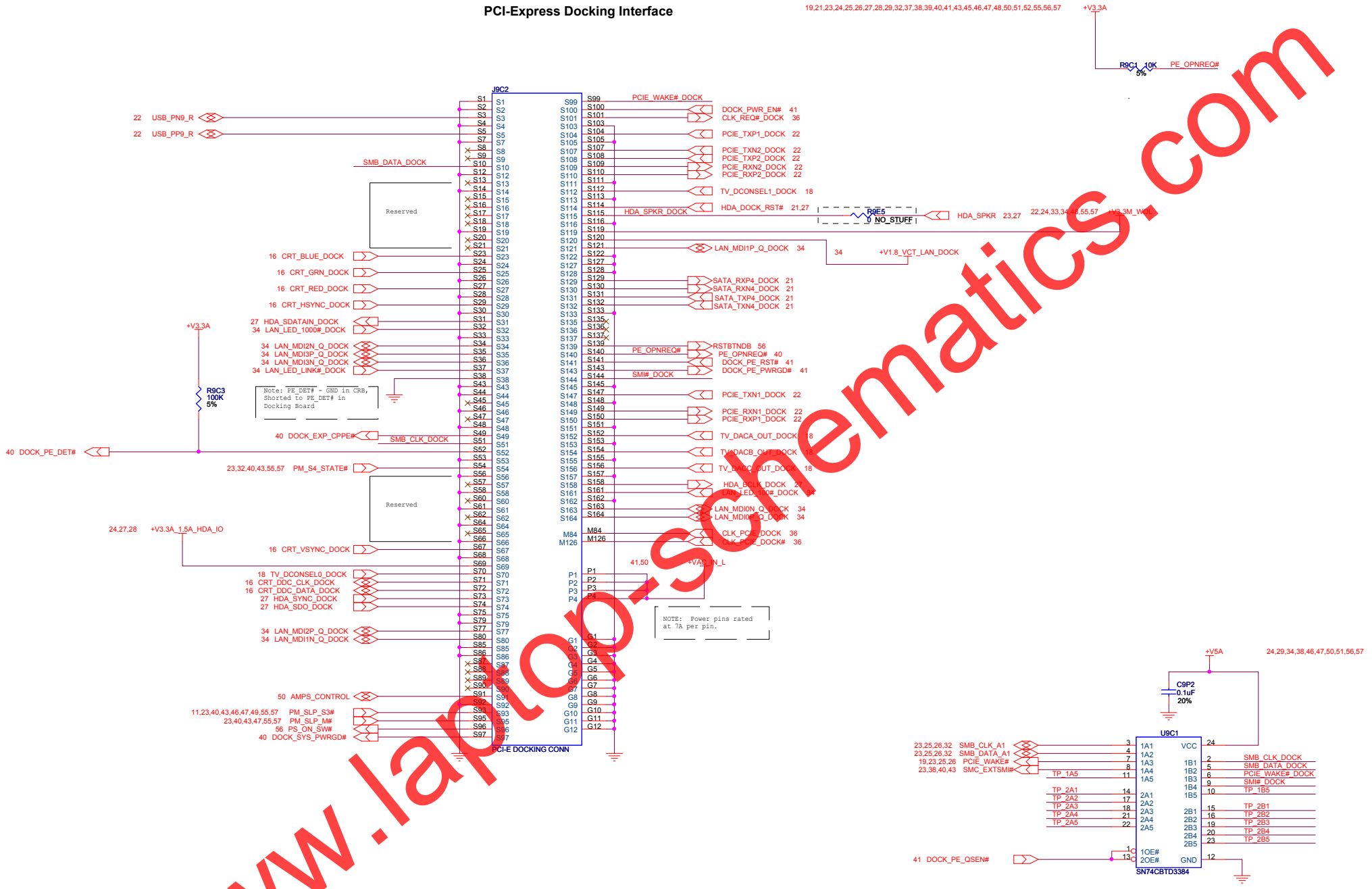
Pillar Rock		Intel Confidential
Title: Embedded Controller 2 of 2		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 41 of 58	



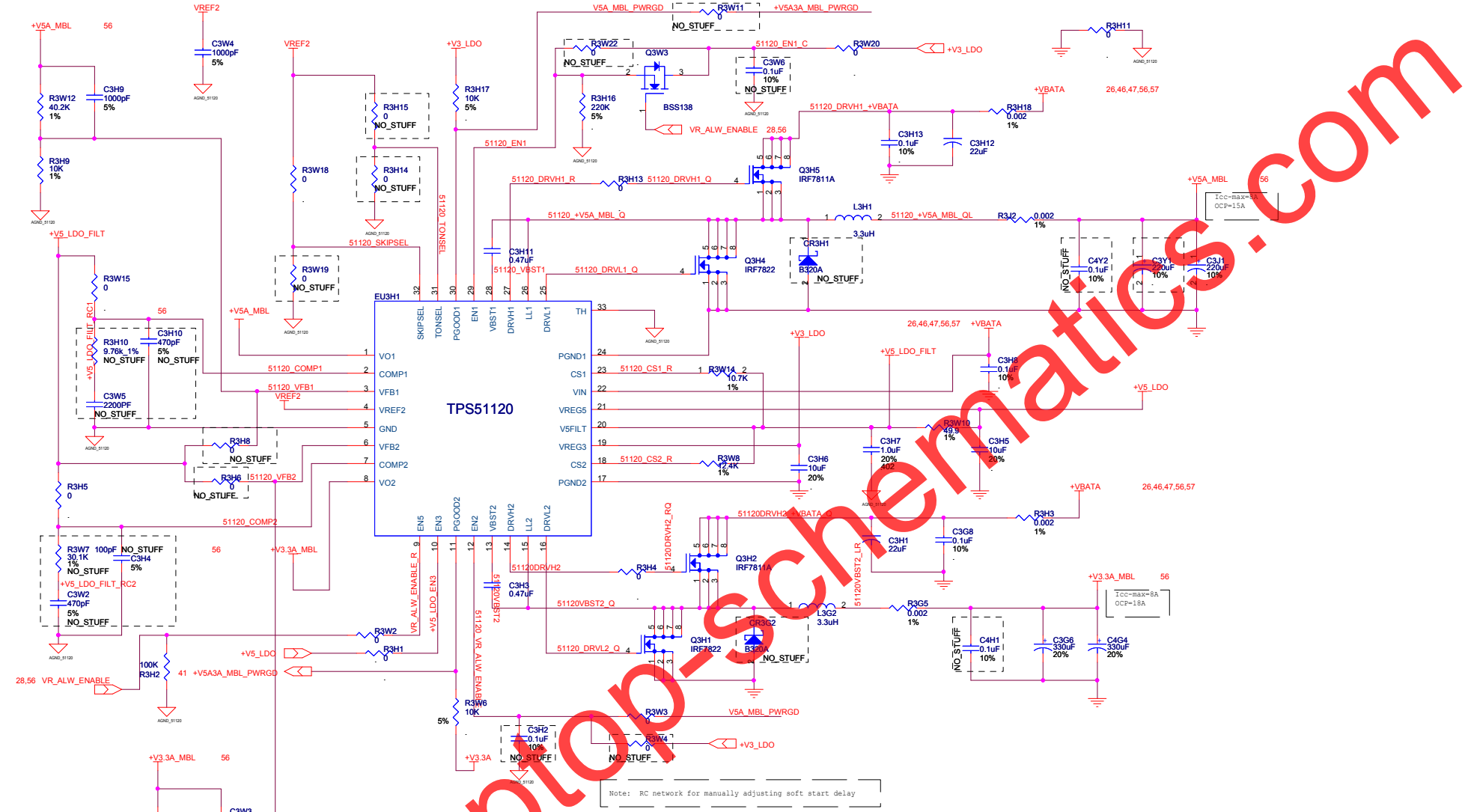


Pillar Rock		Intel Confidential
Title: LPC Slot and TPM Header		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 43 of 58	

PCI-Express Docking Interface



Pillar Rock		Intel Confidential
Title: Docking		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 44 of 58	



PROGRAMMING TABLE				
PIN	AGND	VREF2	FLOAT	+V5_LDO_FILT
SKIPSEL	AUTO-SKIP	AUTO-SKIP FAULTS OFF	PWM FAULTS OFF	PWM
COMP	N/A	N/A	N/A	D-CAP MODE
TONSEL(CH1/2)	380KHz/590KHz	290KHz/440KHz	220KHz/330KHz (DEFAULT)	180KHz/280KHz
VFB1	N/A	SHOULD NOT BE USED	N/A	5V FIXED OUTPUT
VFB2	N/A	SHOULD NOT BE USED	N/A	3.3V FIXED OUTPUT
EN1,EN2	SWITCHER OFF	SHOULD NOT BE USED	N/A	SWITCHER ON
EN3,EN5	LDO OFF	SHOULD NOT BE USED	N/A	LDO ON

V5 Output Mode Selection		
	C3H9, R3W12 & R3H9	R3H8
Fixed Output Mode	NO_STUFF	STUFF
Adjustable Mode (default)	STUFF	NO_STUFF

V3.3 Output Mode Selection		
	C3W3, R3H10 & R3W9	R3H6
Fixed Output Mode	NO_STUFF	STUFF
Adjustable Mode (default)	STUFF	NO_STUFF

V5 Mode Selection		
	R3W15	R3H10, C3H10 & C3W5
Current Mode	NO_STUFF	STUFF
D_CAP Mode (default)	STUFF	NO_STUFF

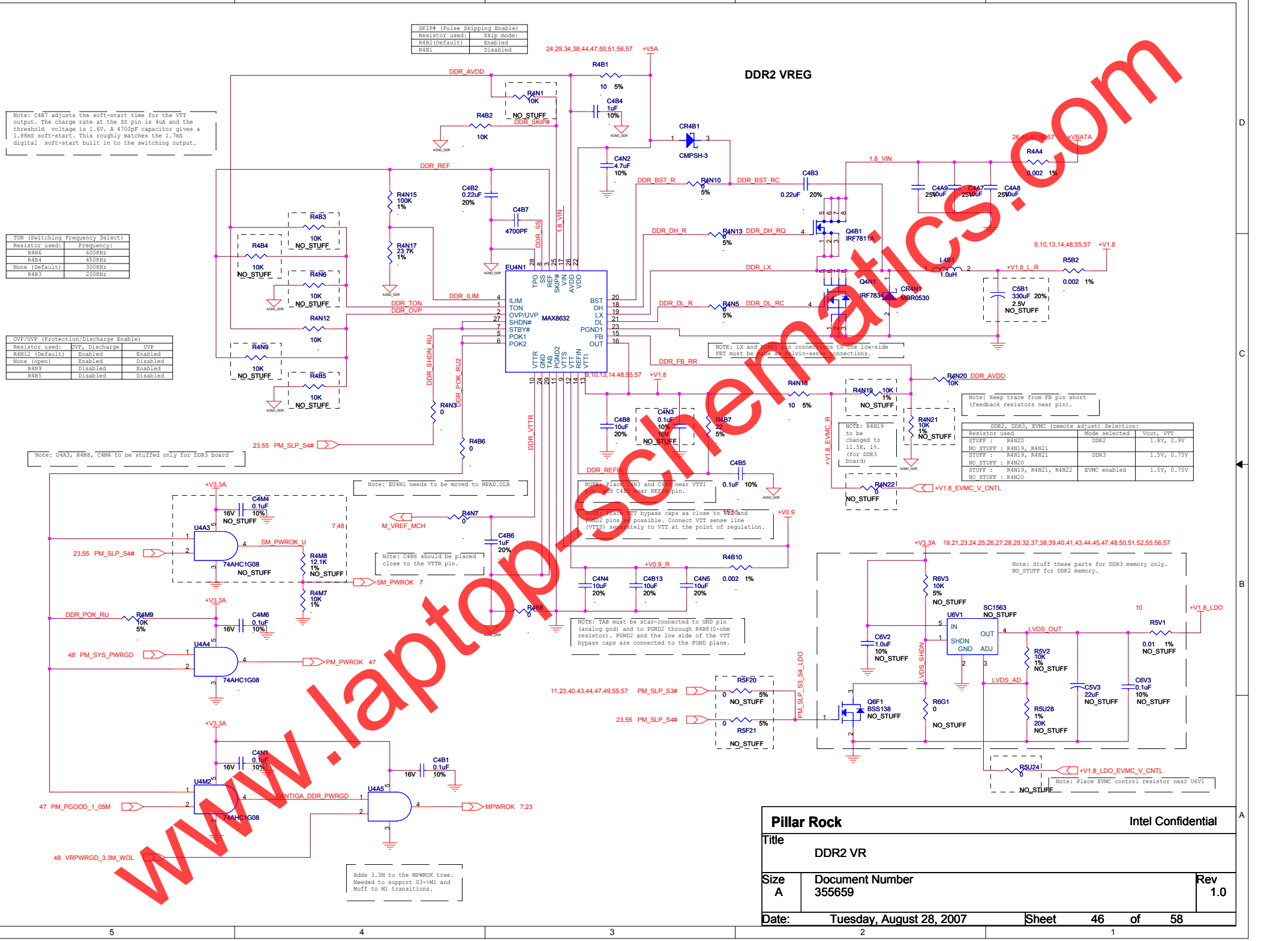
V3.3 Mode Selection		
	R3H5	R3W7, C3H4 & C3W2
Current Mode	NO_STUFF	STUFF
D_CAP Mode (default)	STUFF	NO_STUFF

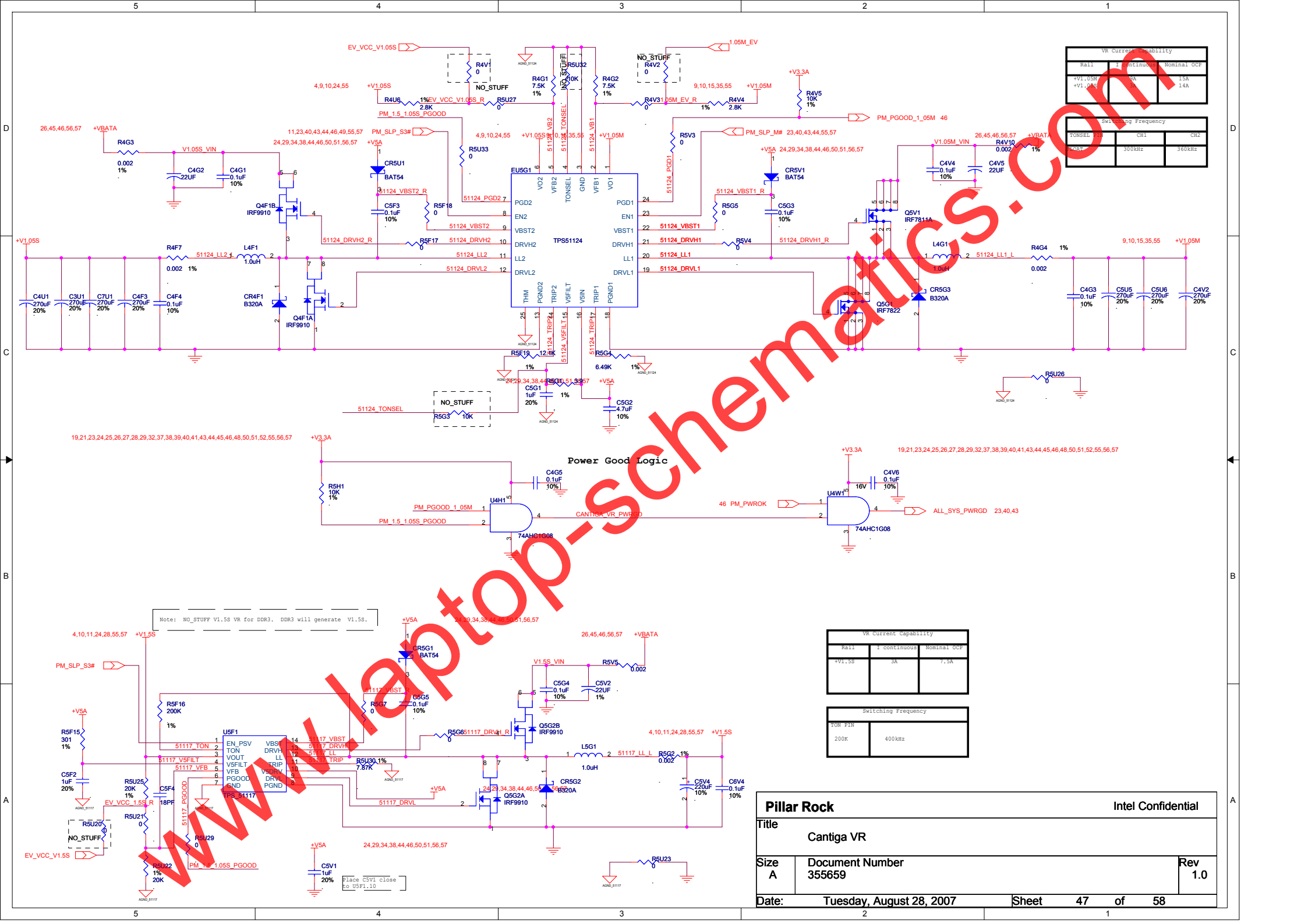
Pillar Rock — Intel Confidential

Title: TPS51120 System Power

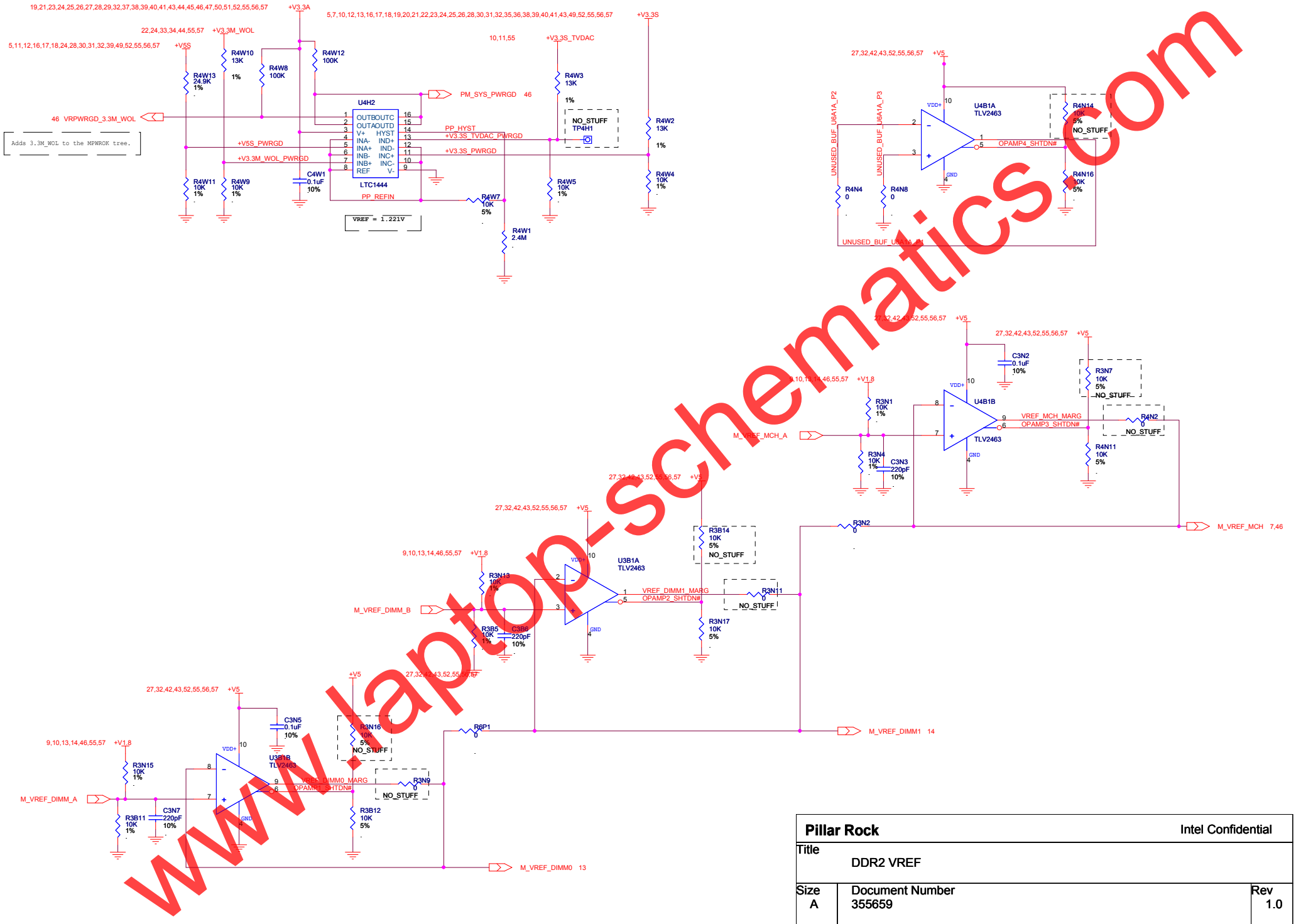
Size	Document Number	Rev
A	355659	1.0

Date: Tuesday, August 28, 2007 — Sheet 45 of 58

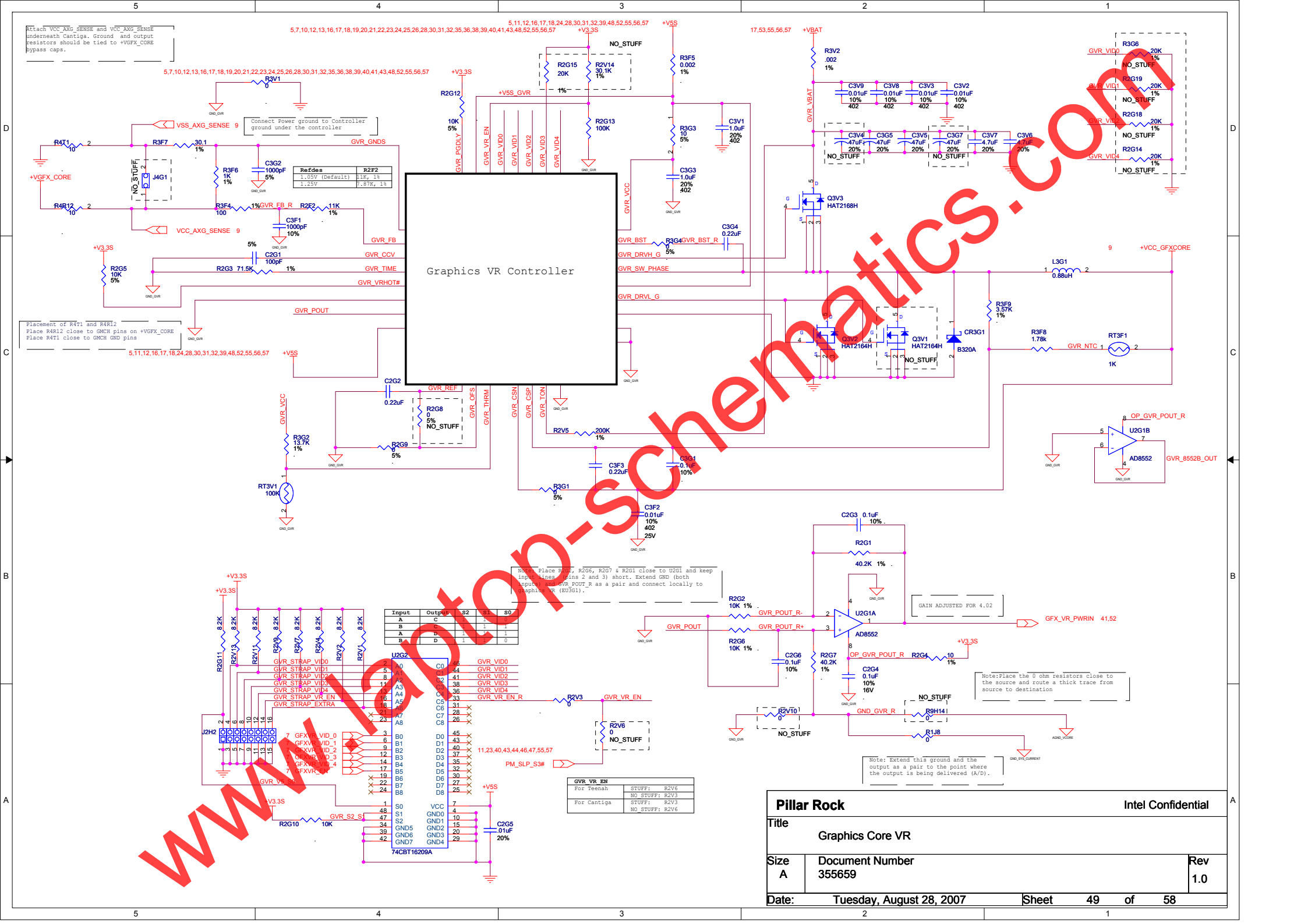


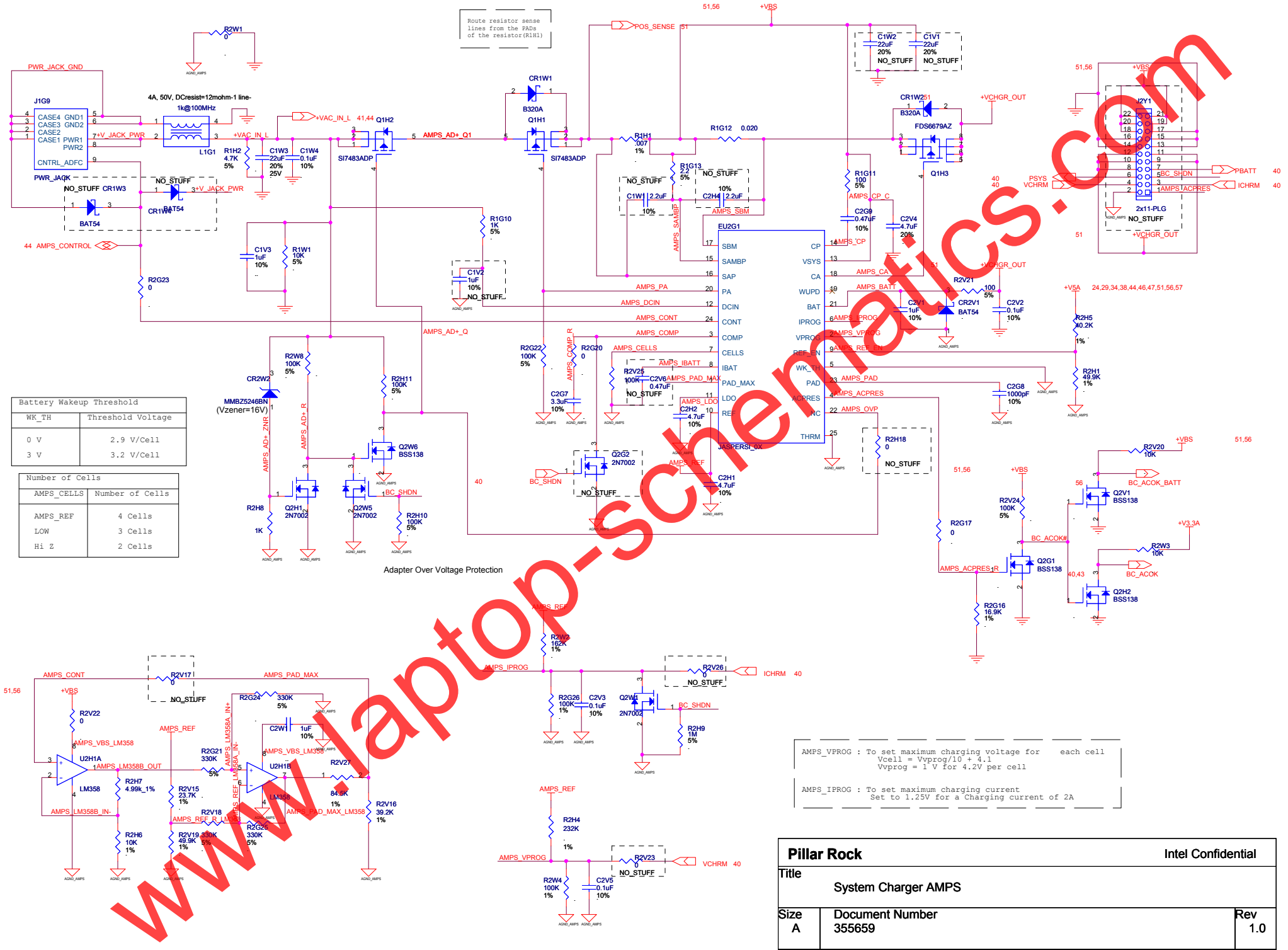


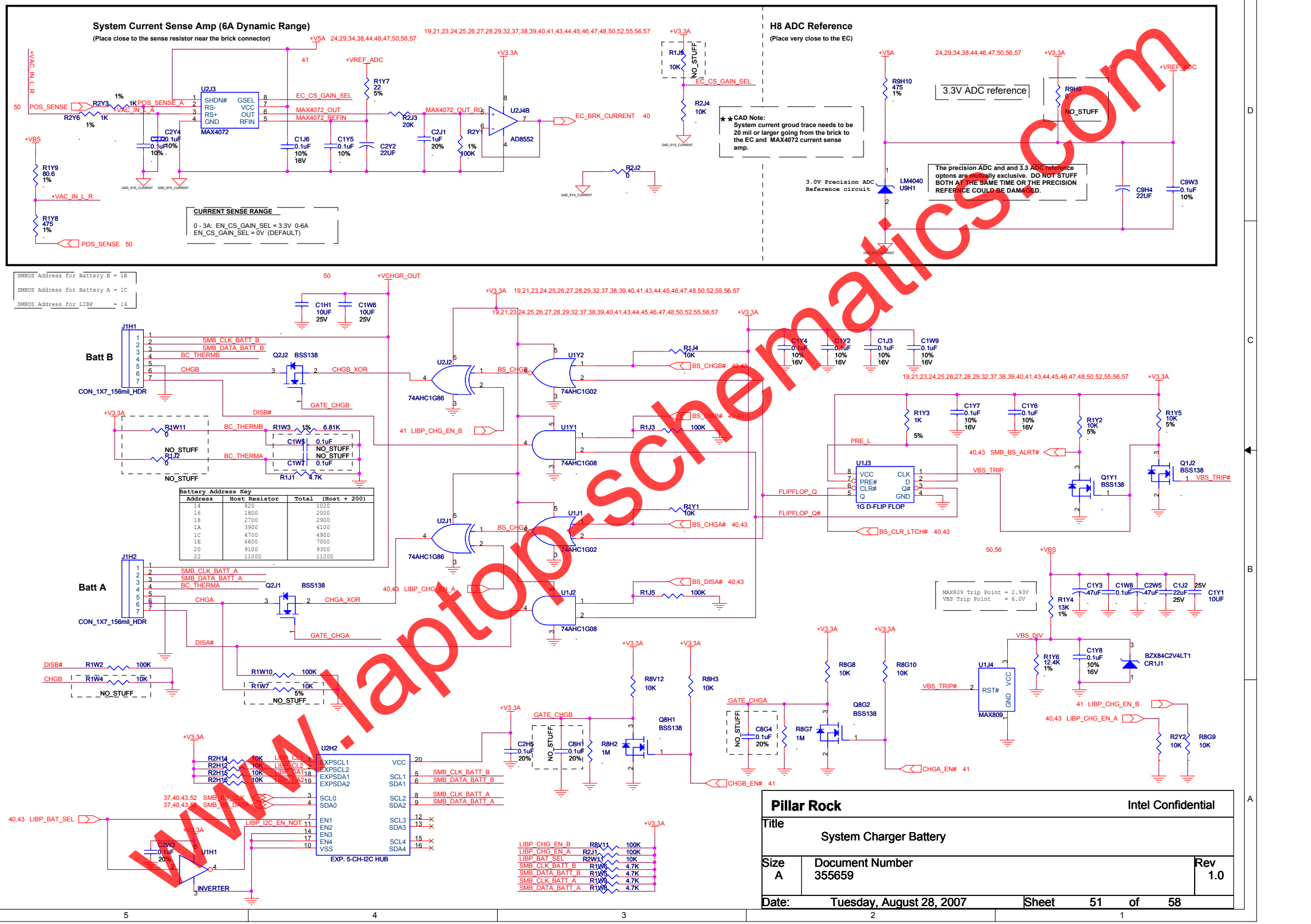
Pillar Rock		Intel Confidential
Title: Cantiga VR		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 47 of 58	



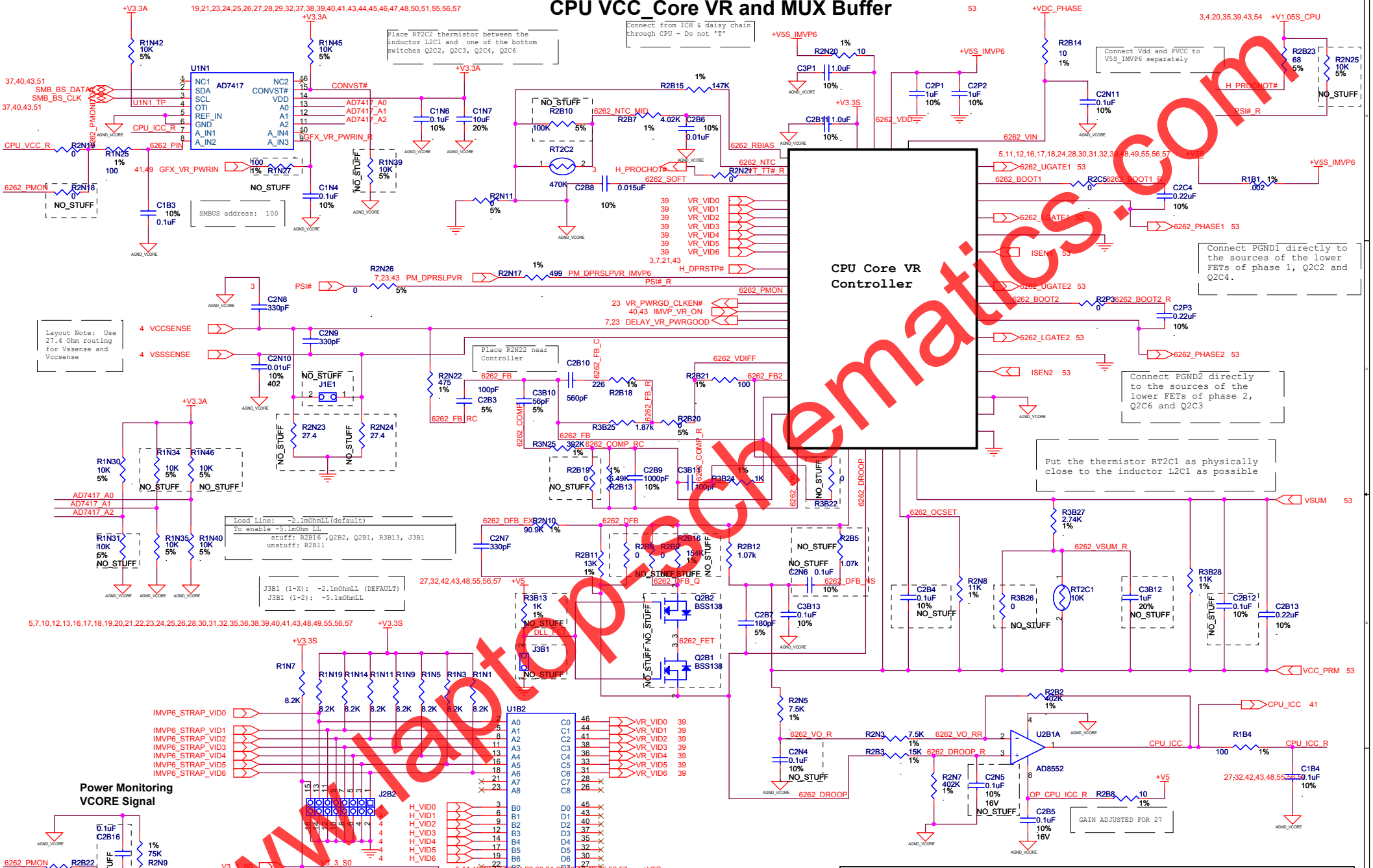
Pillar Rock		Intel Confidential
Title	DDR2 VREF	
Size A	Document Number 355659	Rev 1.0
Date: Tuesday, August 28, 2007	Sheet 48 of 58	





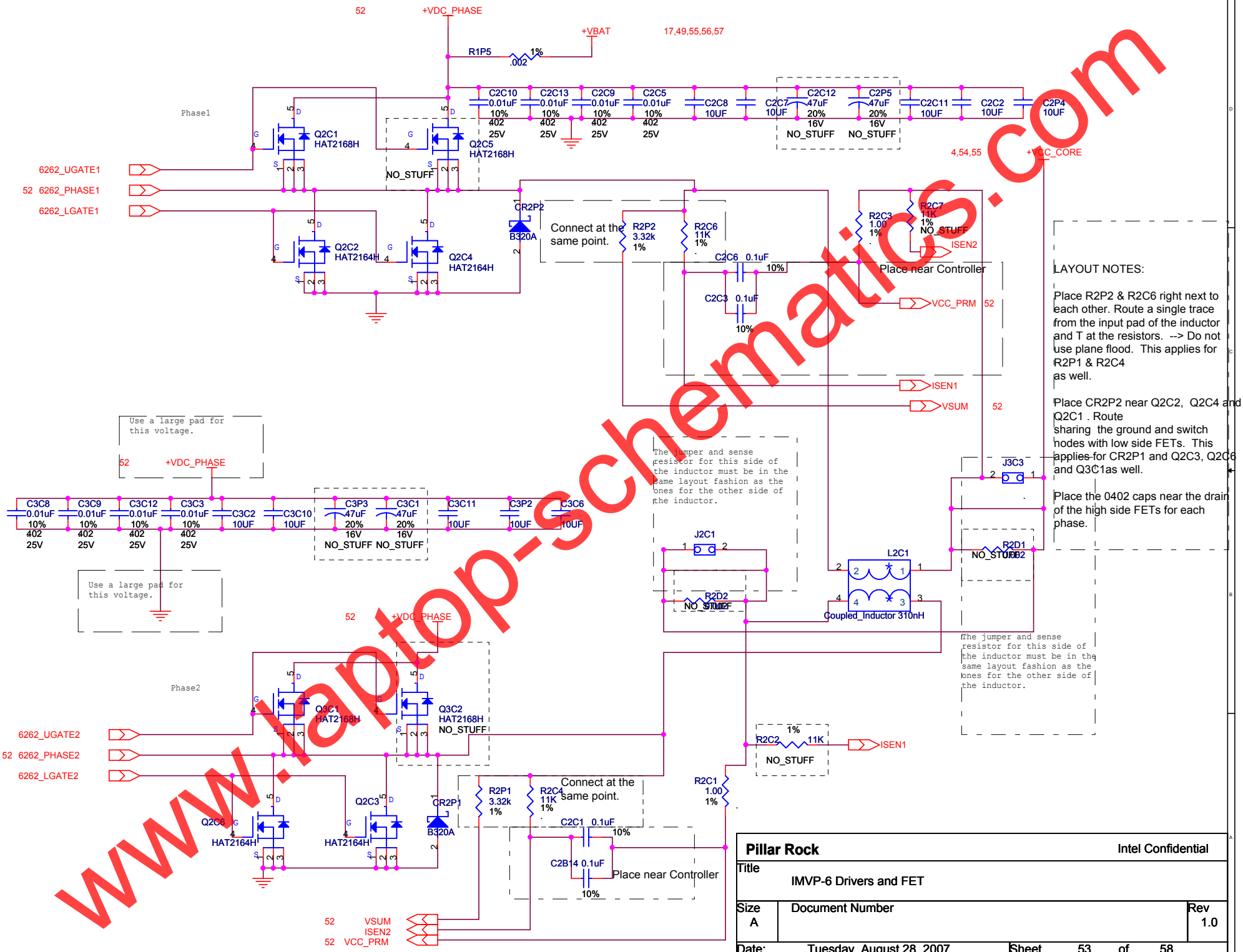


CPU VCC_Core VR and MUX Buffer

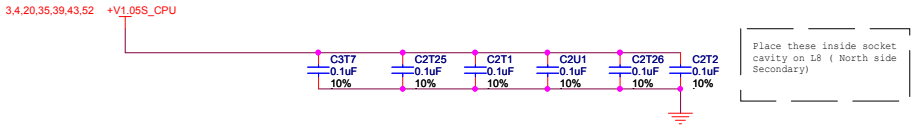


Input	Output	S2	S1	S0
A	C	1	1	0
B	C	1	1	1
A	D	1	1	1
B	D	1	1	0

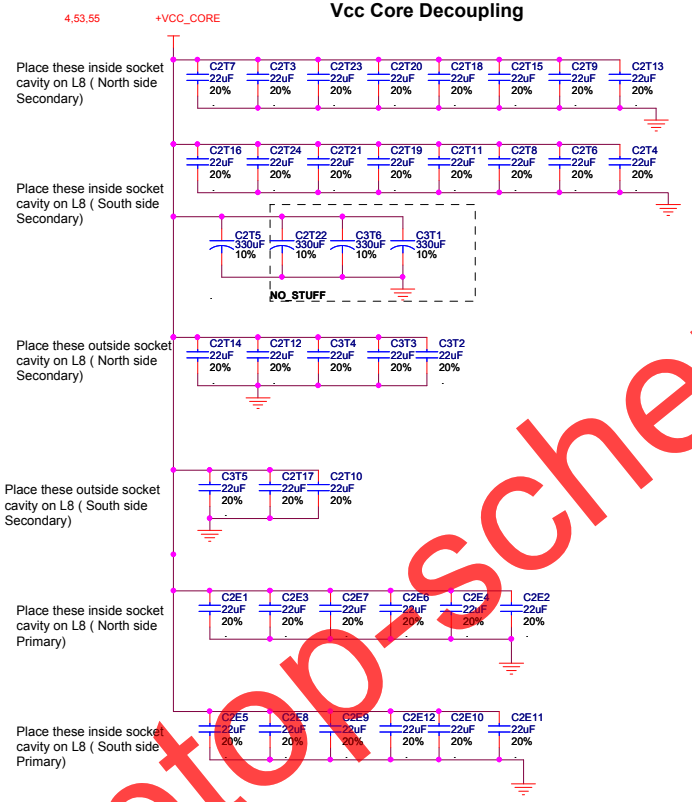
Pillar Rock		Intel Confidential
Title	IMVP-6 Controller	
Size A	Document Number 355659	Rev 1.0
Date: Tuesday, August 28, 2007	Sheet 52 of 58	



Vccp Core Decoupling



Vcc Core Decoupling



Pillar Rock		Intel Confidential
Title: CPU Decoupling		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 54 of 58	

SLP_S3# DISCHARGE CKT DESIGNED FOR ~100ms DISCHARGE ON ALL S3 RAILS.

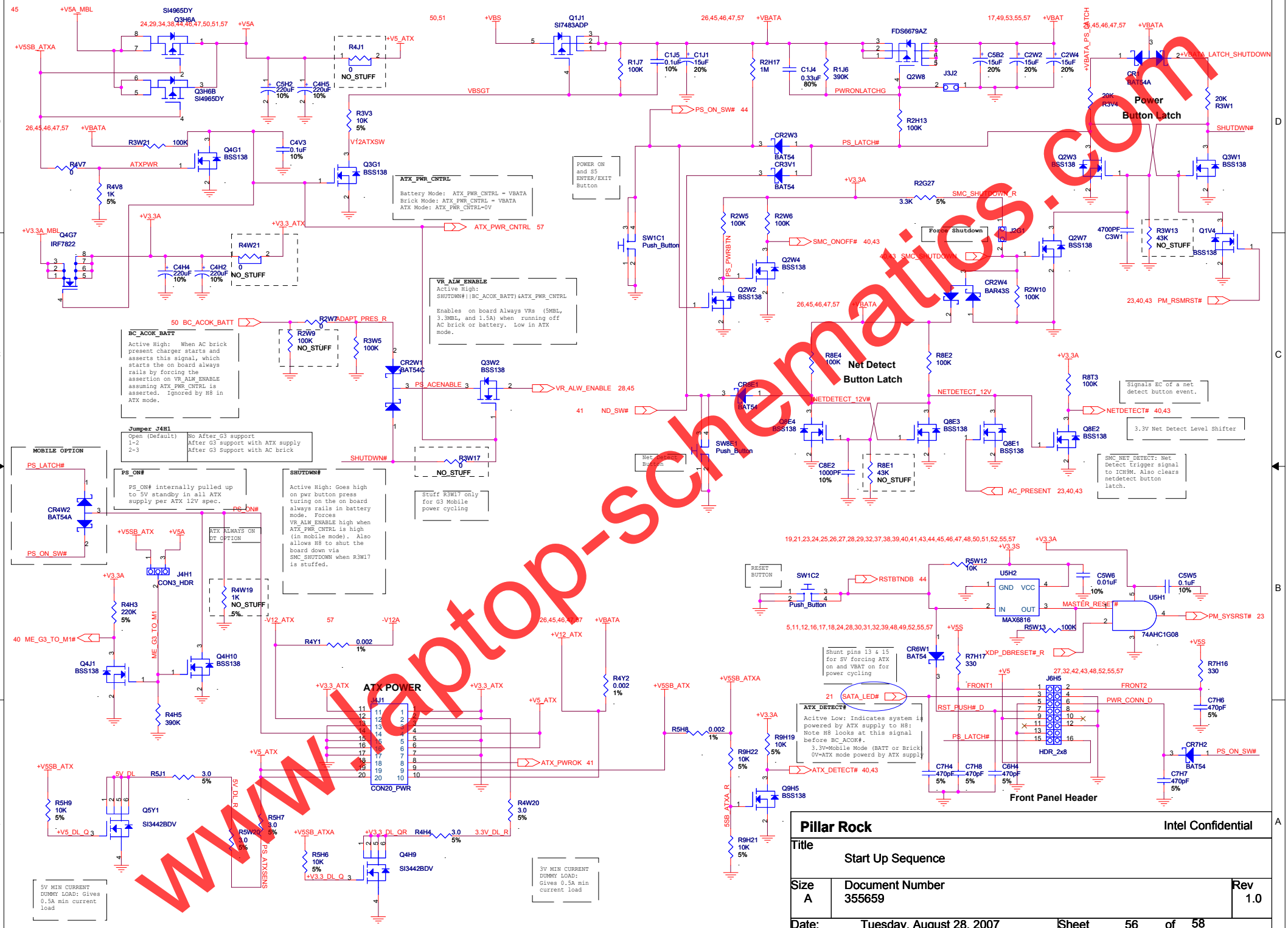
SLP_S4# DISCHARGE CKT DESIGNED FOR ~100ms DISCHARGE ON ALL S4 RAILS.

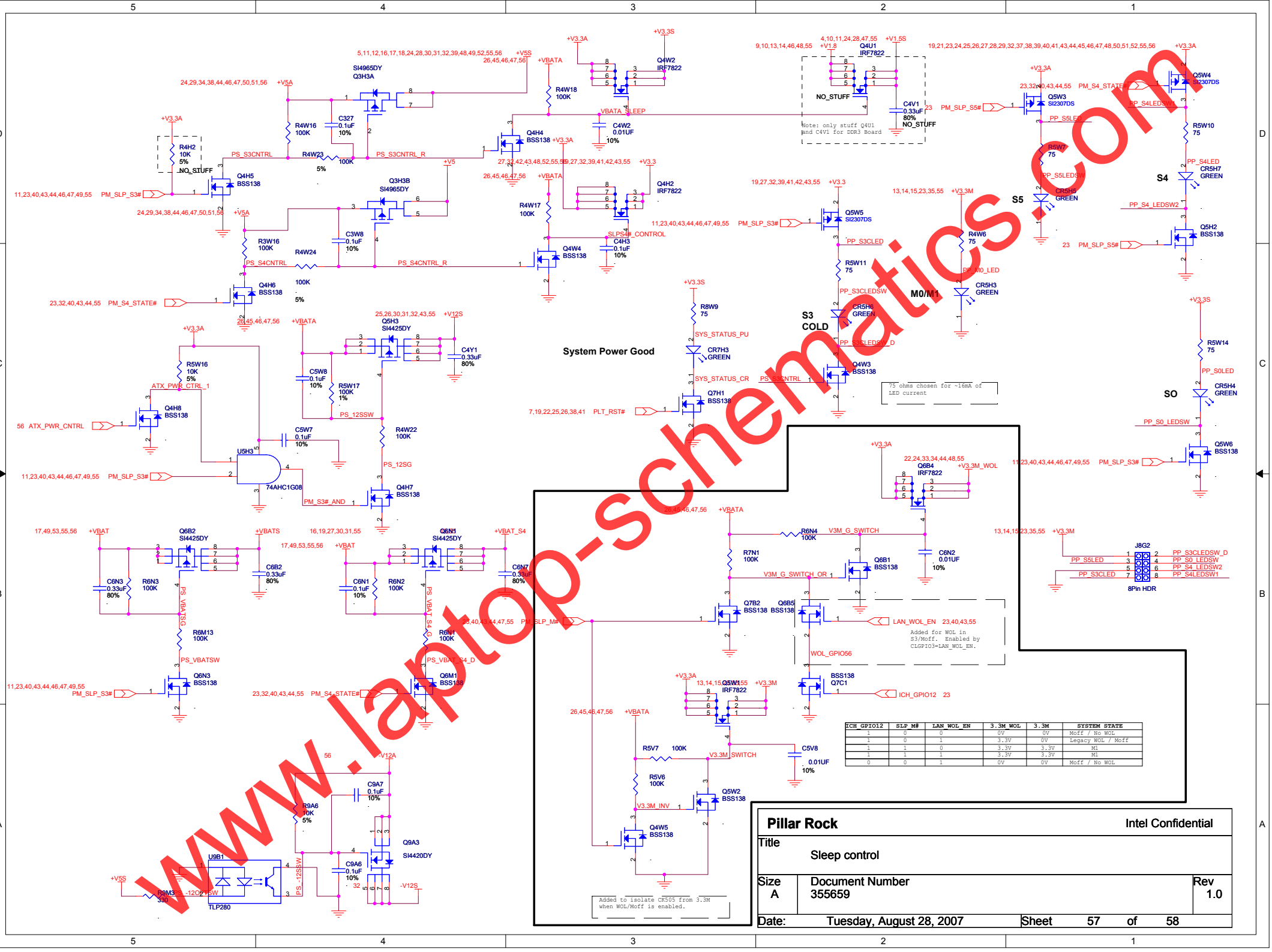
5,7,10,12,13,16,17,18,19,20,21,22,23,24,25,26,28,30,31,32,35,36,38,39,40,41,43,48,49,52,56,57 +V3.3S
25,26,30,31,32,43,57 +V12S
R7B1 180
PP_V12SDIS
Q7B1 BSS138
R4W15 97.6
PP_V3SDIS
Q4H3 BSS138
19,27,32,39,41,42,43,48,49,52,56,57 +V3.3
R5V11 97.6
PP_V3DIS
Q5G3 BSS138
17,49,53,56,57 +VBAT
CR3R1 BAT54
VBATA_DISCHARGE
5,11,12,16,17,18,24,28,30,31,32,39,48,49,52,56,57 +V5S
C3P5 22UF
R3R6 100K
R4W14 97.6
PP_V5SDIS
Q4W1 BSS138
PM_SLP_S3
11,23,40,43,44,46,47,49,57 PM_SLP_S3#
Q3R1 BSS138
R3R5 1M
R3R1 100K
R5W1 97.6
PP_V5SDIS
Q5V2 BSS138
27,32,42,43,48,52,56,57 +V5
+VBAT_S4
R6N5 180
PP_BATS4DIS
Q6N2 BSS138
PP_S4GT
16,19,27,30,31,57 +VBATS
4,10,11,24,28,47,57 +V1.5S
R5H5 100
PP_1.2DIS
Q5H1 BSS138
R4V6 47
PP_V1.5SDIS
Q4V1 BSS138
Q3R2 BSS138
R5V10 1M
R4V14 100K
15,46
+V0.9
R4B9 220
PP_V0.9DIS
Q4B2 BSS138
DDR_DIS
Q4G6 BSS138
9,10,13,14,46,48,57 +V1.8
R5B3 68 5%
PP_V1.8DIS
Q5N1 BSS138
4,9,10,24,47 +V1.05S
+V3.3A
R4D3 100K
R3D3 470 5%
PM_SLP_S3_BUF_R
Q4D1 BSS138
PM_SLP_S3_BUF
11,23,40,43,44,46,47,49,57 PM_SLP_S3#
Q3R5 BSS138
23,32,40,43,44,57 PM_S4_STATE#
23,46 PM_SLP_S4#
10,11,48 +V3.3S_TVDAC
R3R12 4.87K 1%
PP_V3STVDIS
Q3R3 BSS138
22,24,33,34,44,48,57 +V3.3M_WOL
R4V12 97.6
PP_V3MDIS
Q4G4 BSS138
9,10,15,35,47 +V1.05M
R4V13 470 5%
PP_V105M_DIS
Q4G5 BSS138
PP_V33M_DIS
R4G5 100K 5%
Q4G2 BSS138
LAN_WOL_EN 23,40,43,57
13,14,15,23,35,57 +V3.3M
R4H1 470 5%
PP_V33MCKDIS
Q4H1 BSS138
4,53,54 +VCC_CORE
R4R8 47
PP_VIMVPDIS
Q3R4 BSS138
R4V11 10K
PM_SLP_M
23,40,43,44,47,57 PM_SLP_M#
Q4G3 BSS138
R4V9 1M

ATX Mounting Holes

MT1B1 MT1J1 MT1F1 MT5A1 MT9A1 MT9F1 MT9J1 MT5J1
MT_NO_STUFF

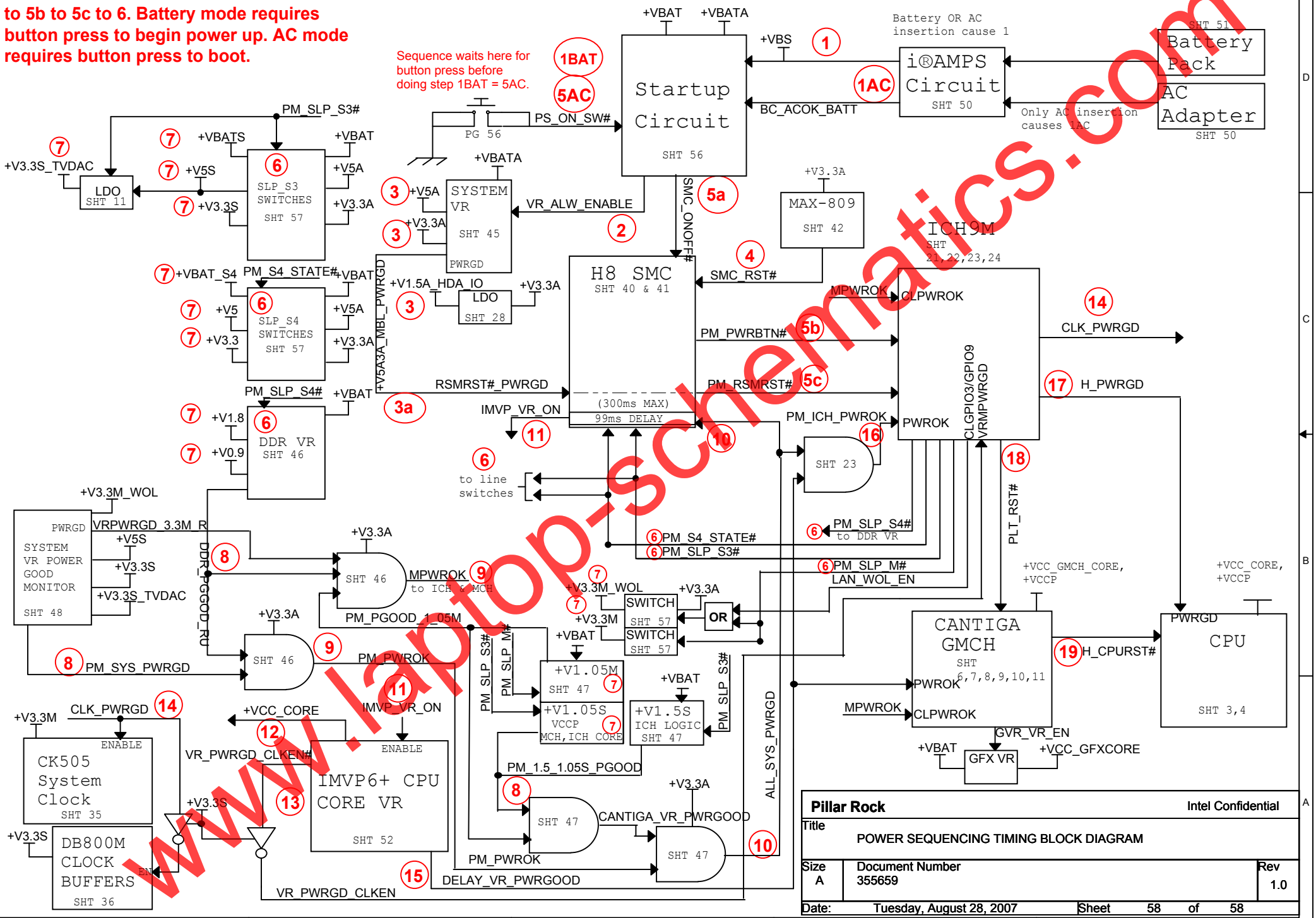
Pillar Rock		Intel Confidential
Title: DISCHARGE CIRCUITS		
Size: A	Document Number: 355659	Rev: 1.0
Date: Tuesday, August 28, 2007	Sheet 55 of 58	





Pillar Rock Mobile Power On Sequence

Steps 1 leads to either 1BAT for battery only mode or 1AC for AC mode. 5AC leads to 5a to 5b to 5c to 6. Battery mode requires button press to begin power up. AC mode requires button press to boot.



Pillar Rock		Intel Confidential
Title	POWER SEQUENCING TIMING BLOCK DIAGRAM	
Size A	Document Number 355659	Rev 1.0
Date: Tuesday, August 28, 2007	Sheet 58 of 58	