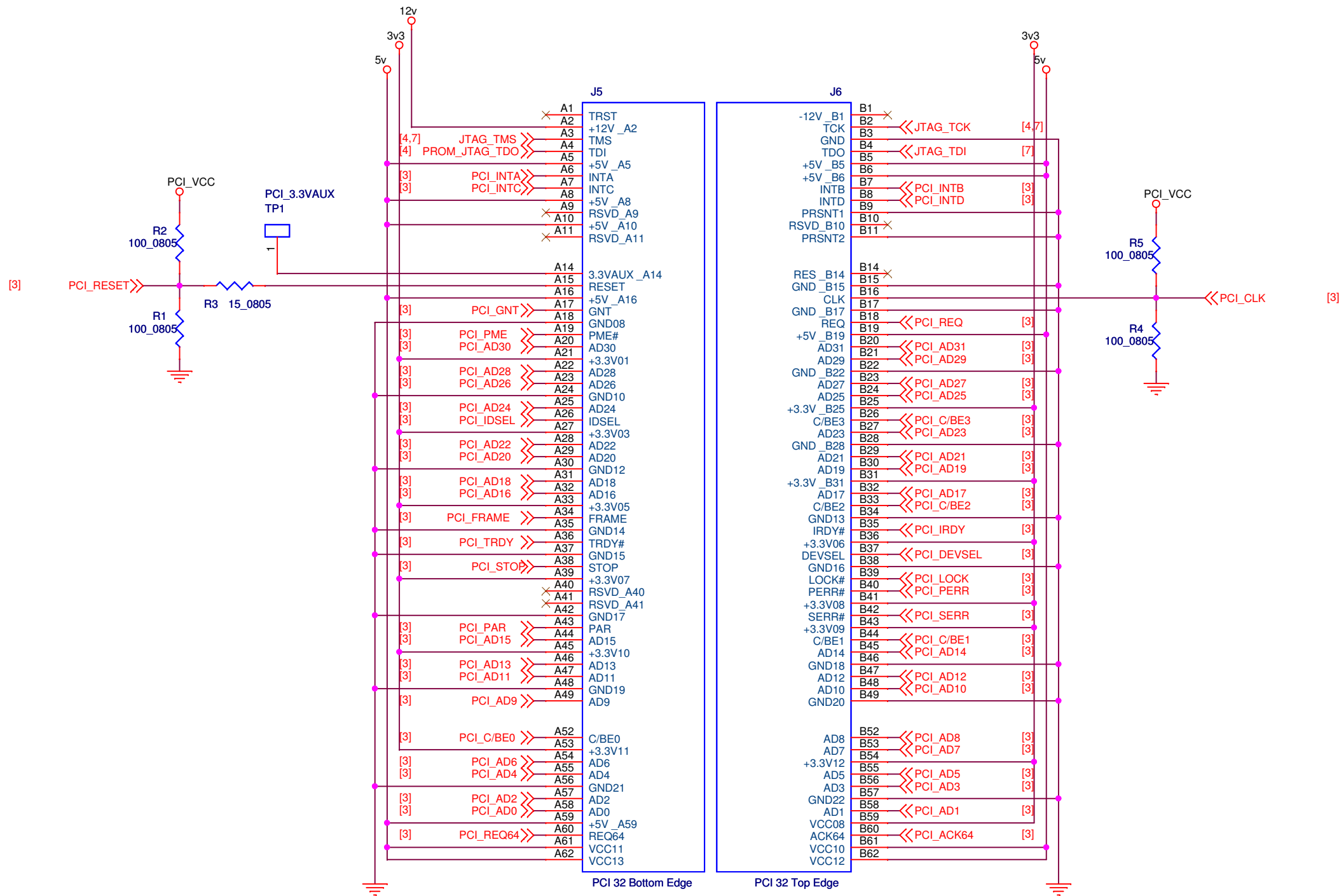
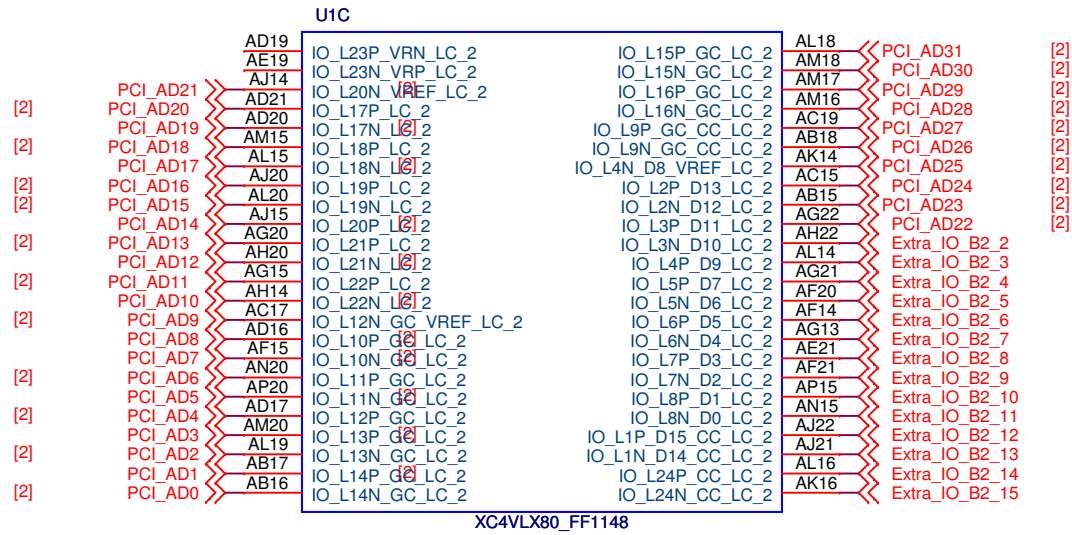
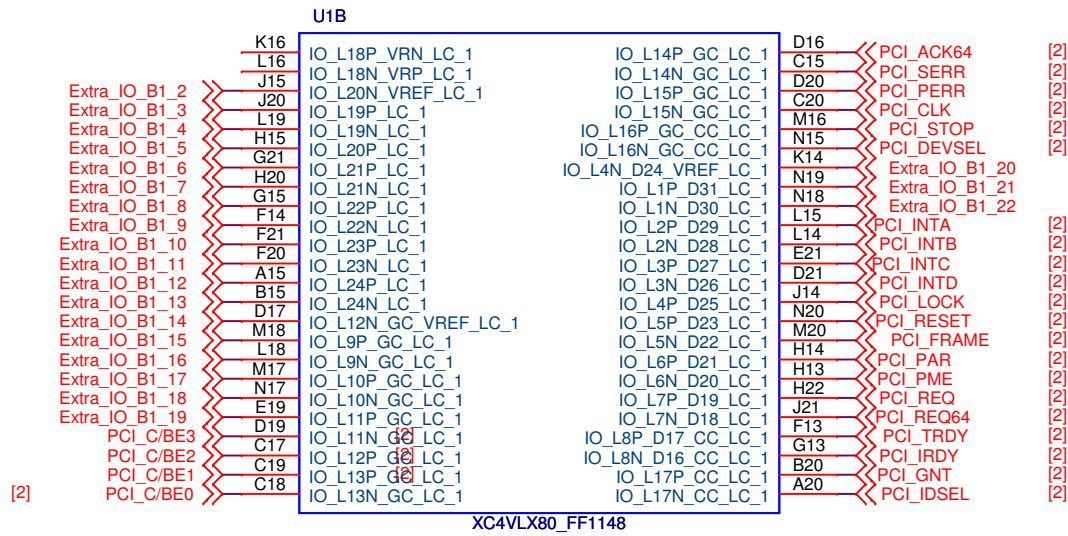


Table of Contents

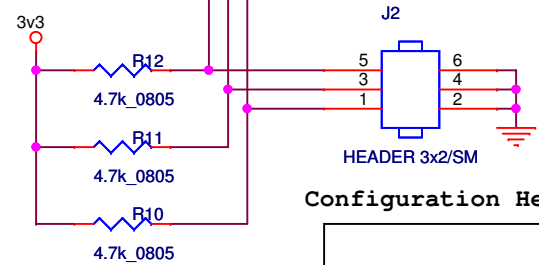
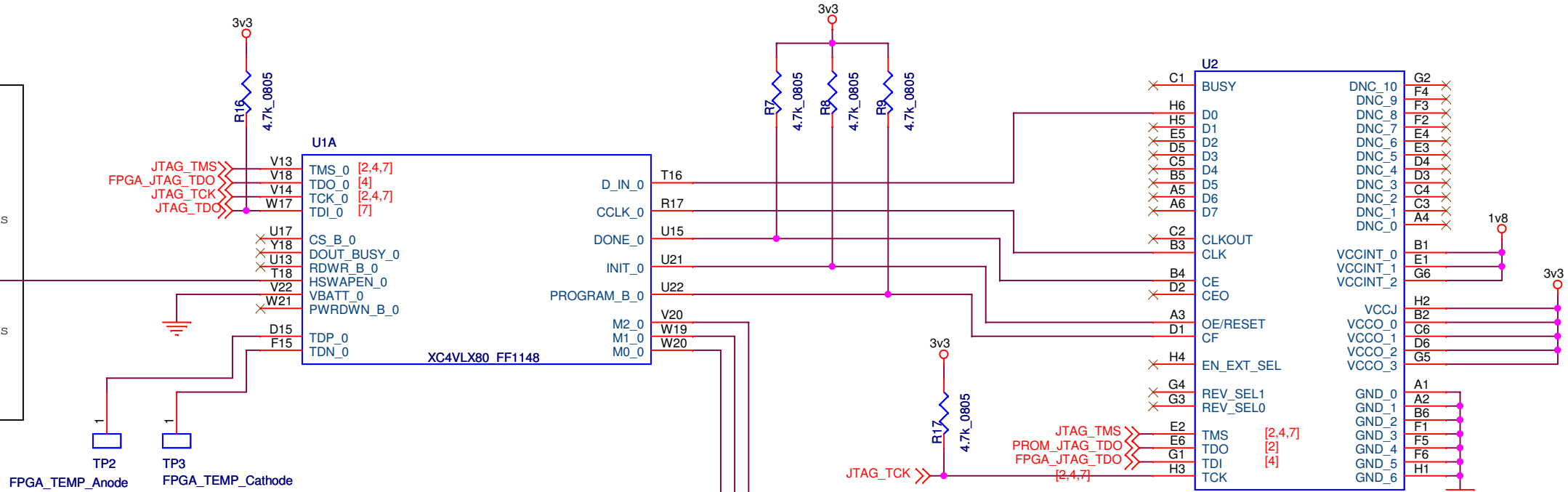
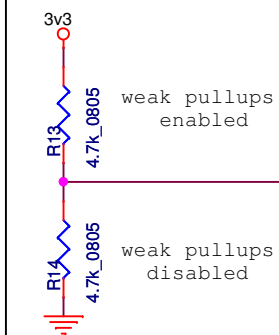
01	Info Page
02	PCI Connector
03	FPGA PCI Banks
04	FPGA Config
05	FPGA GND
06	FPGA Power
07	JTAG
08	FPGA Extra I/O
09	DDR Socket
10	FPGA DDR Banks 5,6
11	FPGA DDR Banks 3,4,7
12	Power Regulation
13	Power Distribution





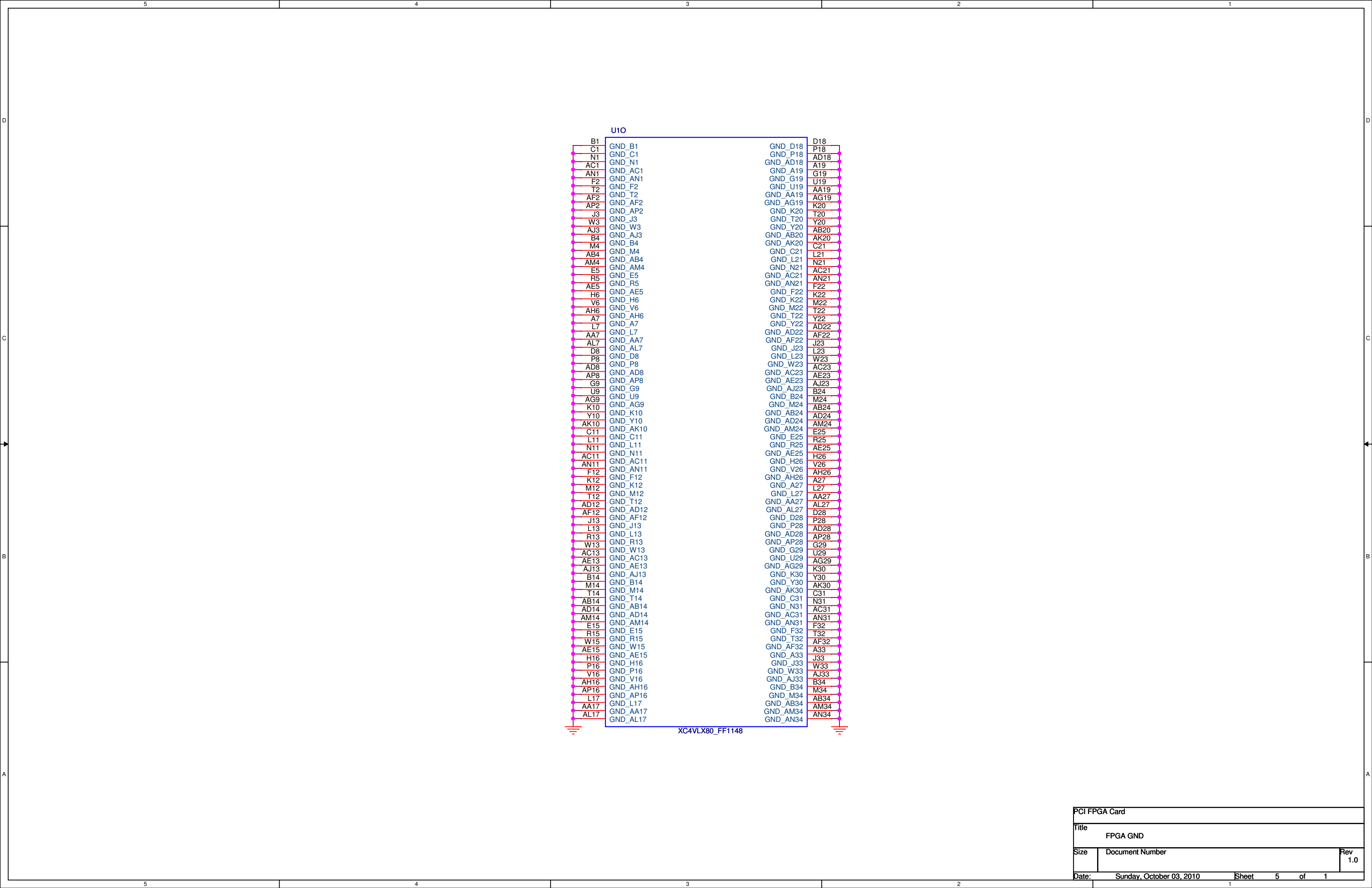
Pullup Config

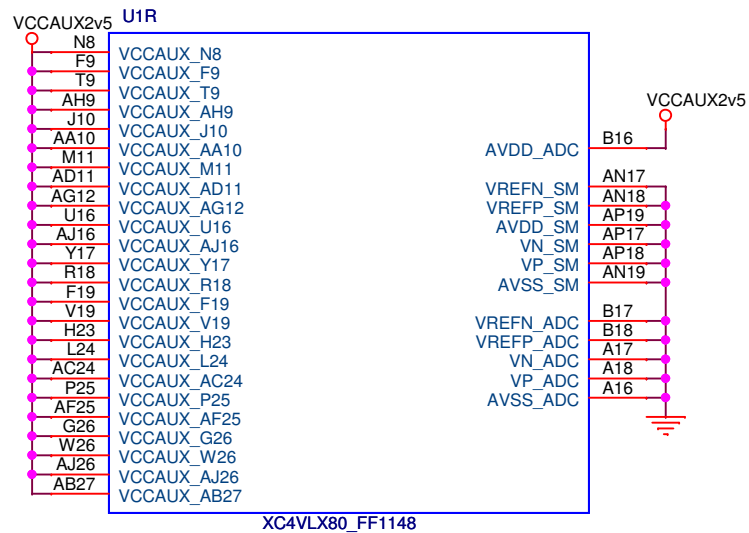
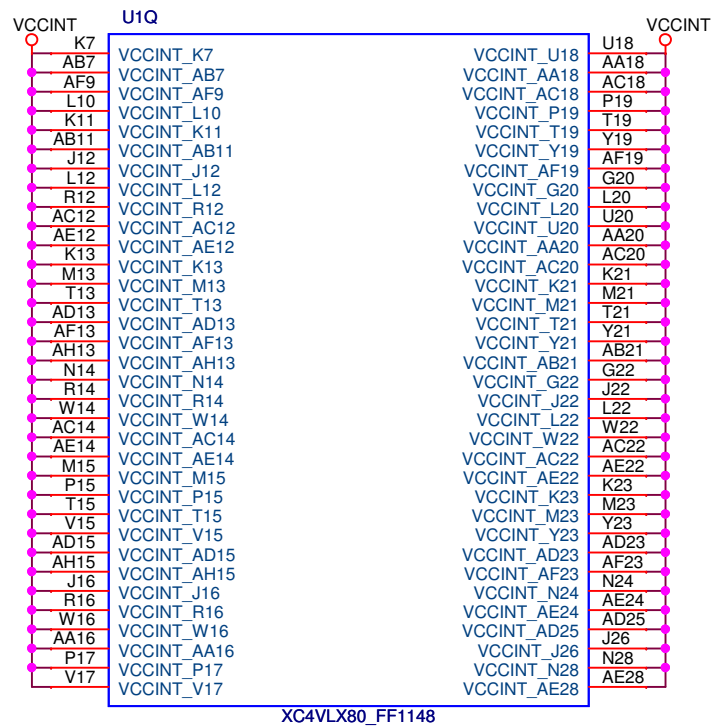
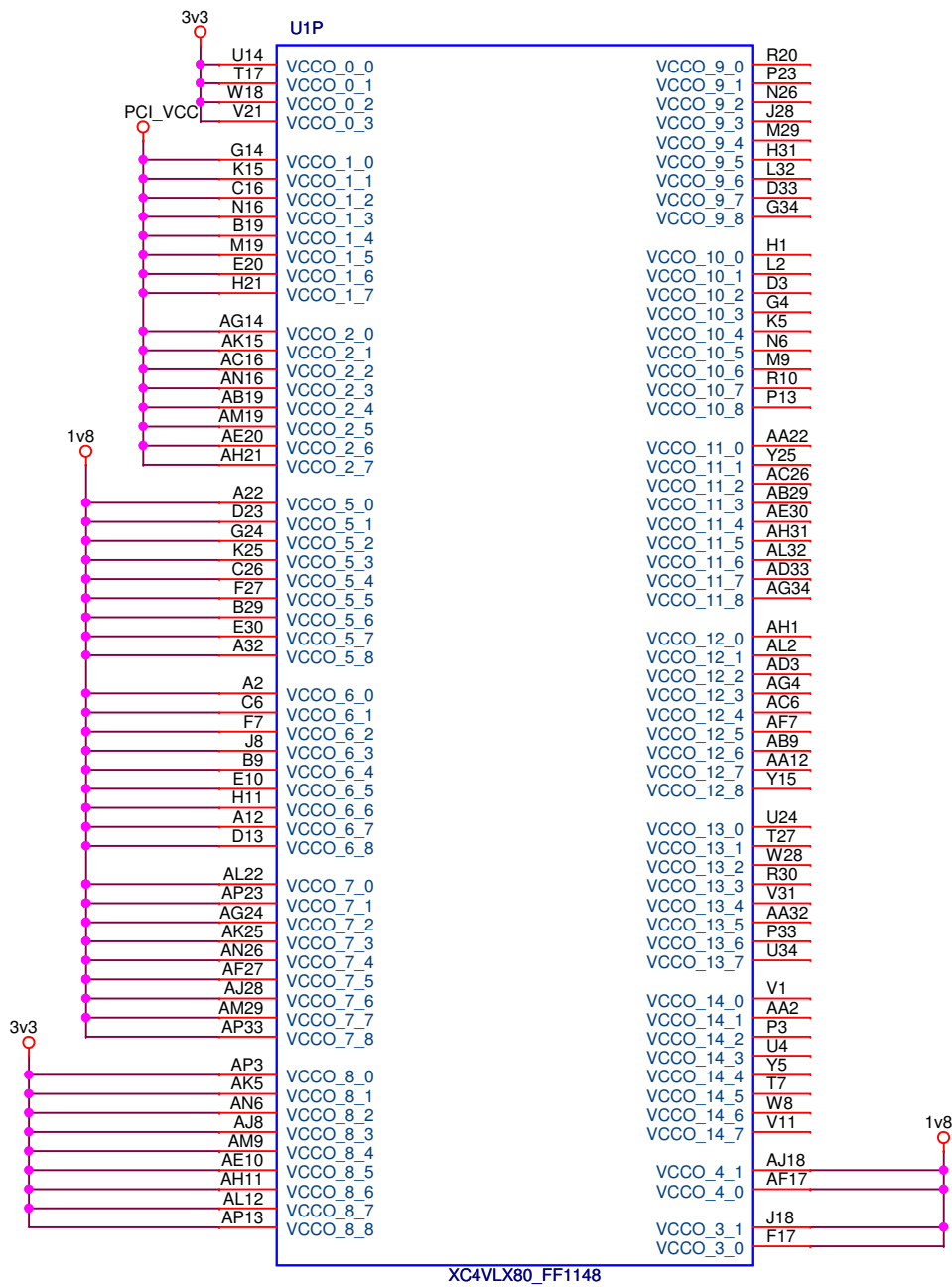
Populate either
R13 or R14
but not both!

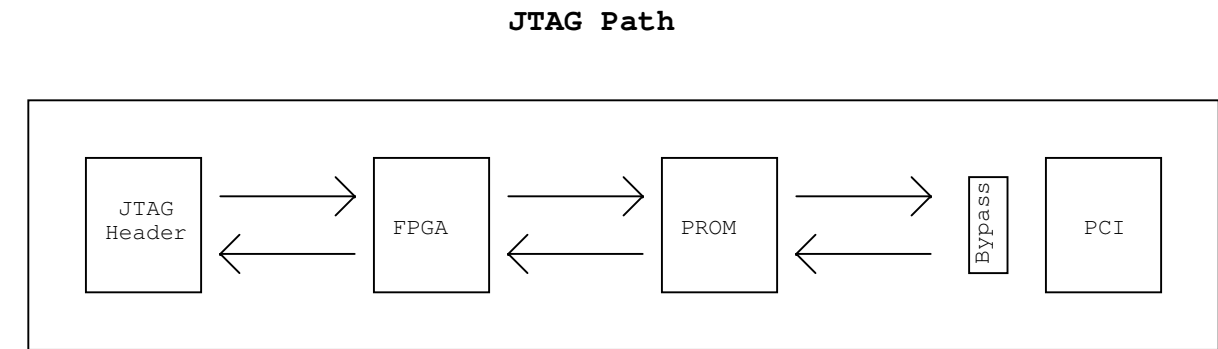
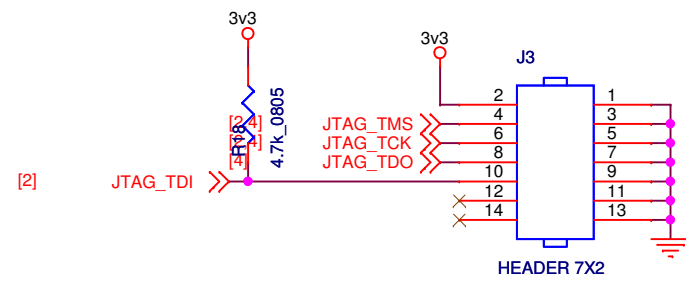


Configuration Header Options

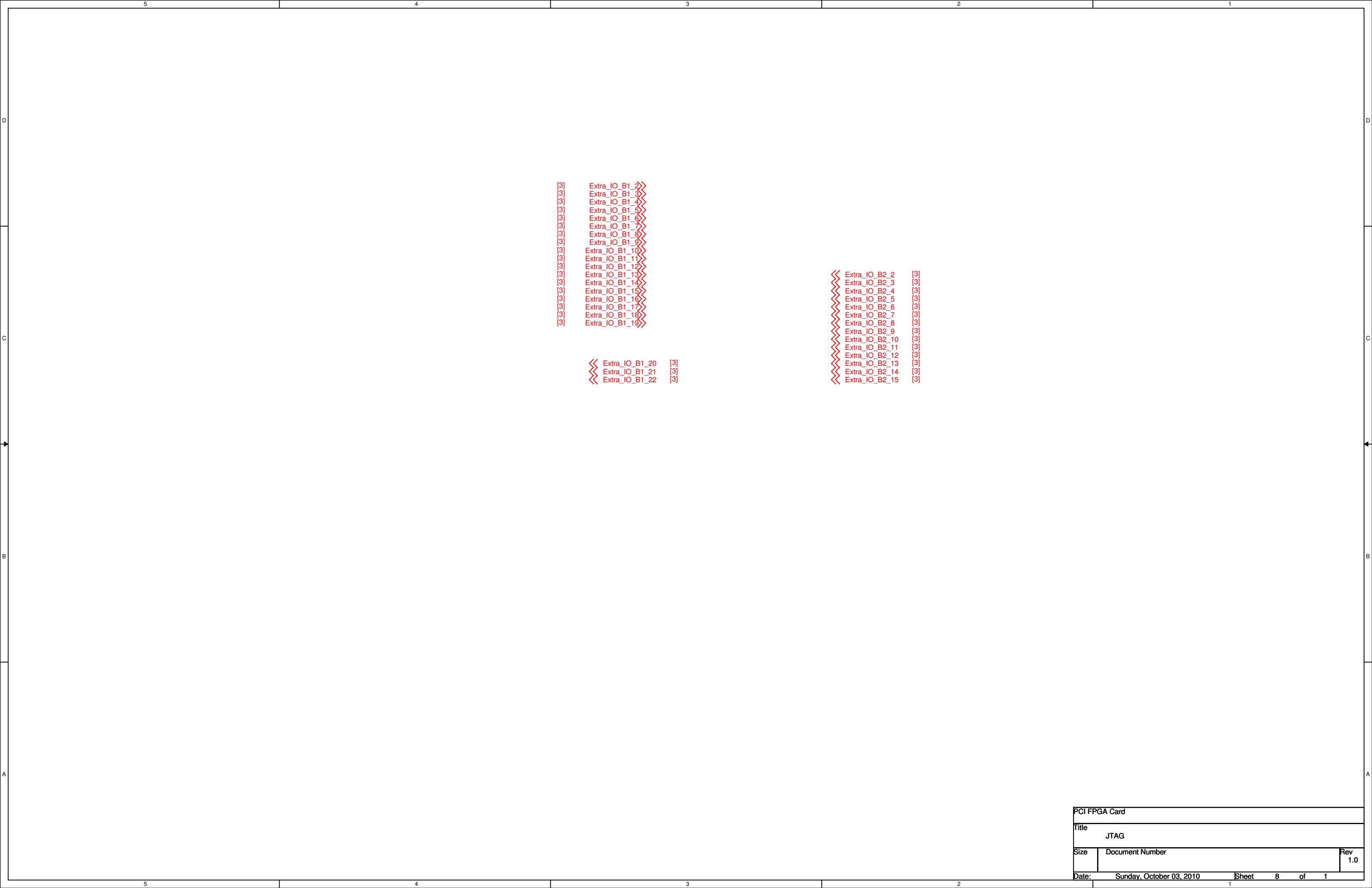
From PROM	From JTAG
1->2 = ON	1->2 = OFF
3->4 = ON	3->4 = ON
5->6 = ON	5->6 = OFF



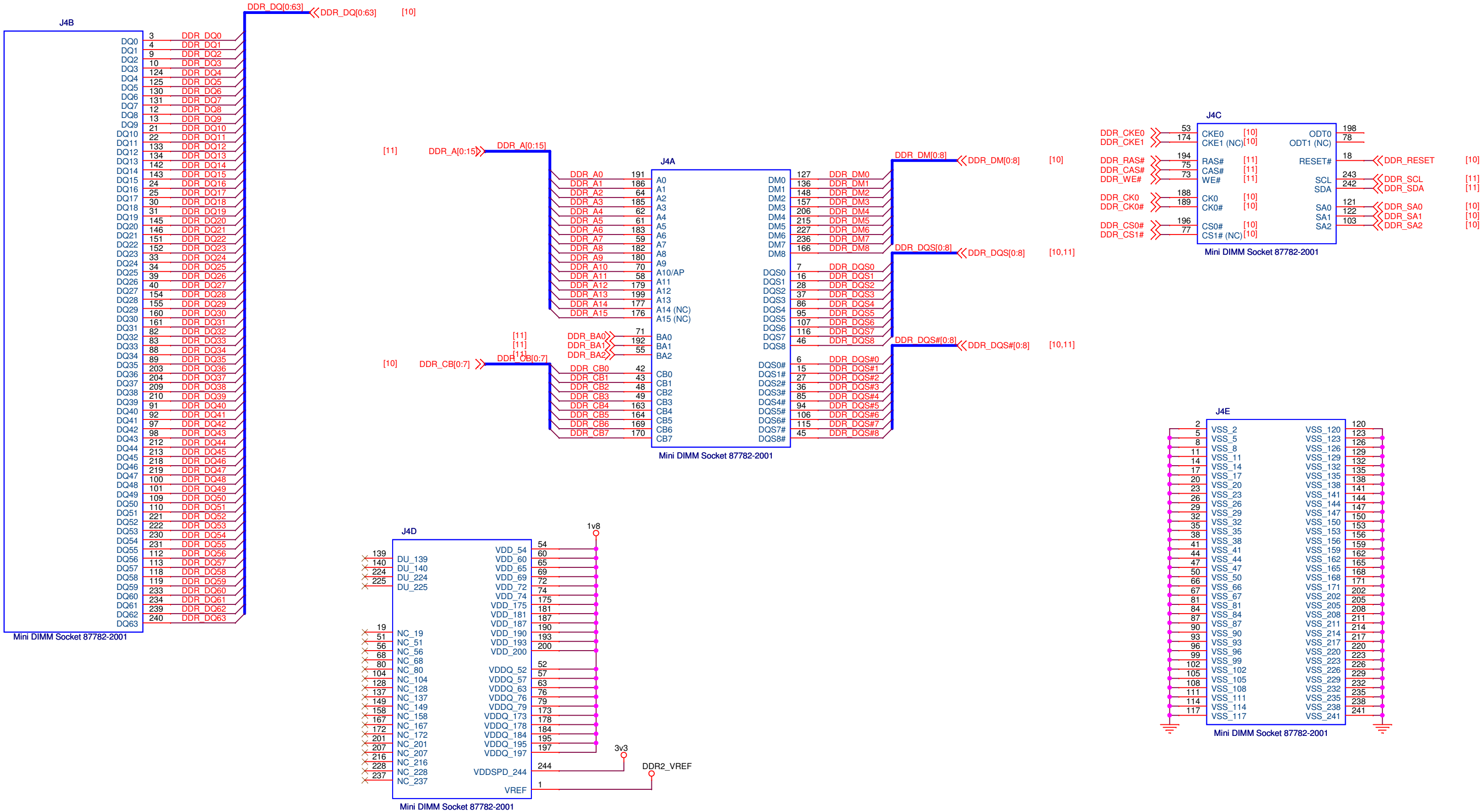


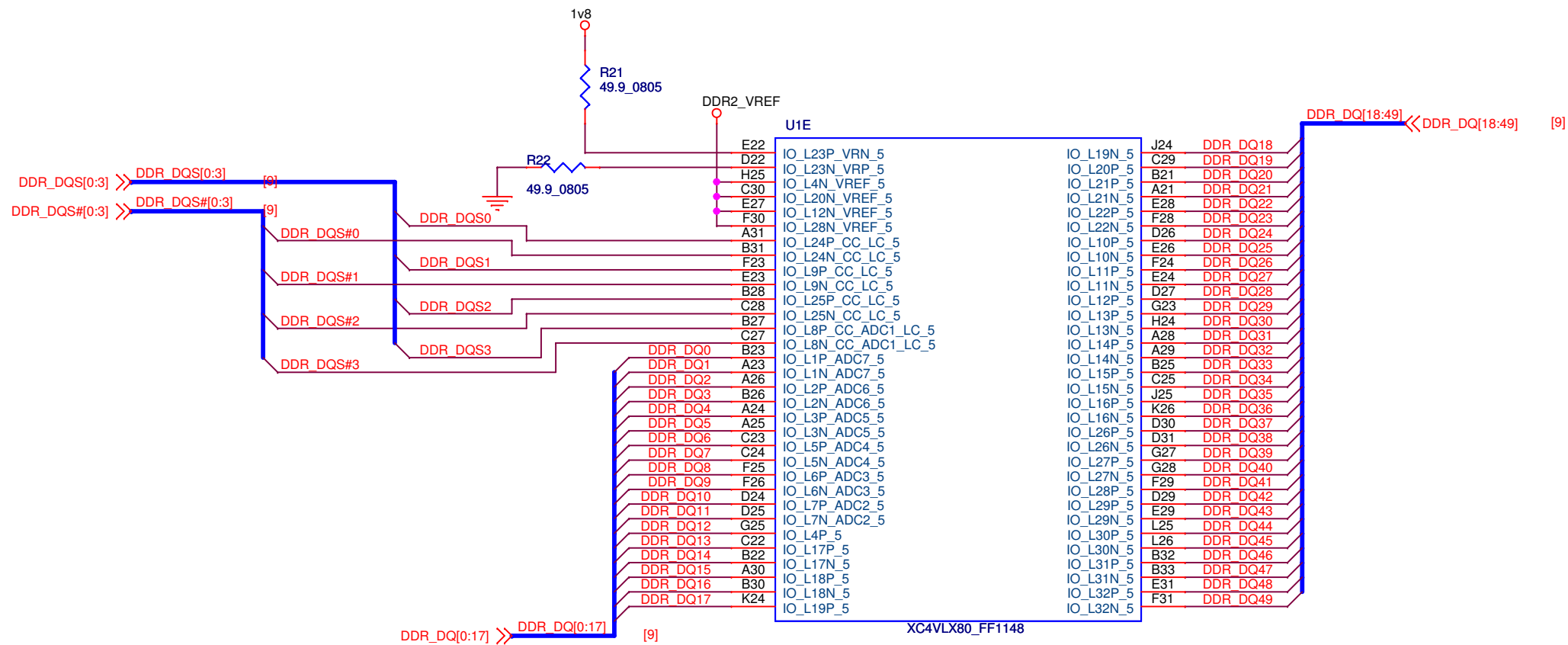
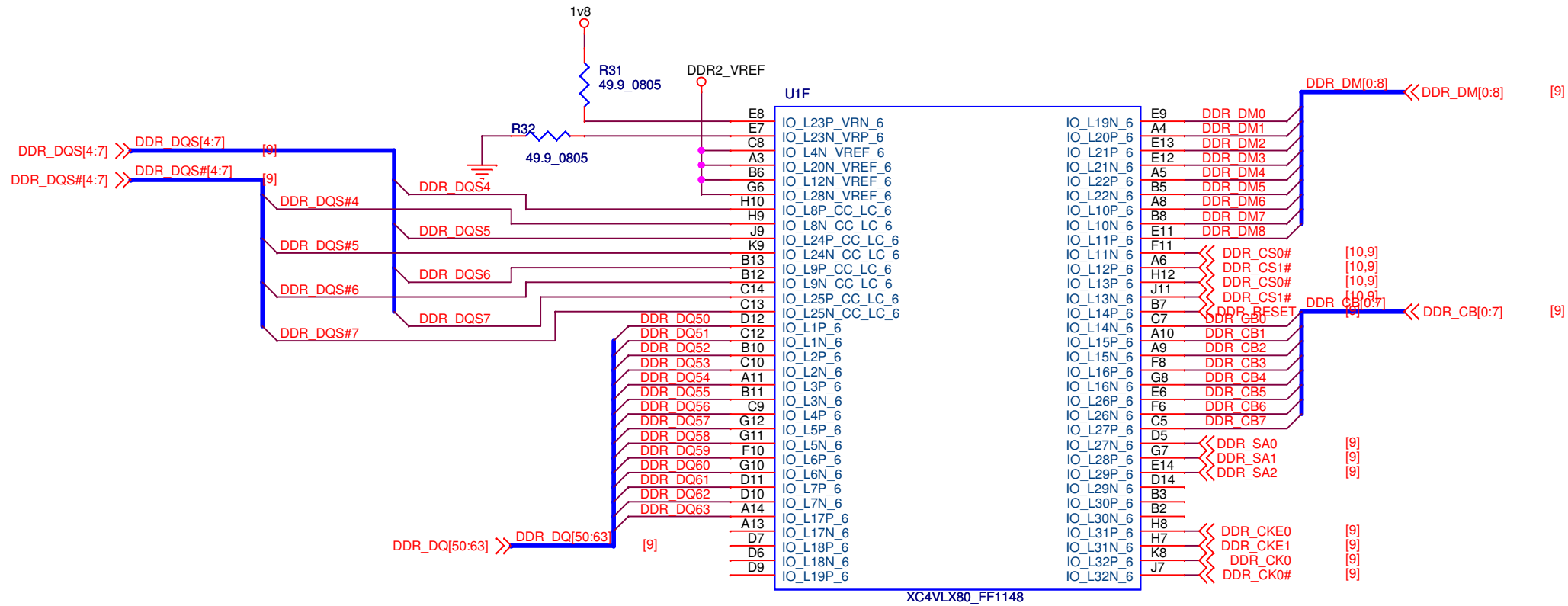


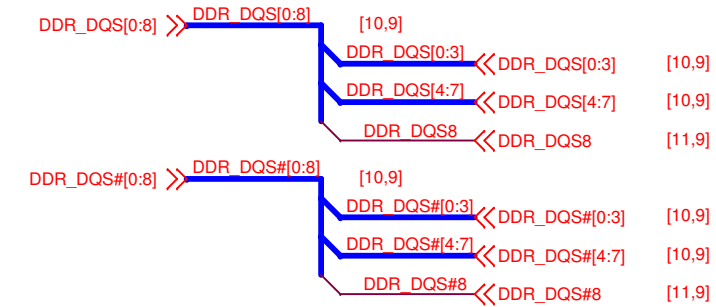
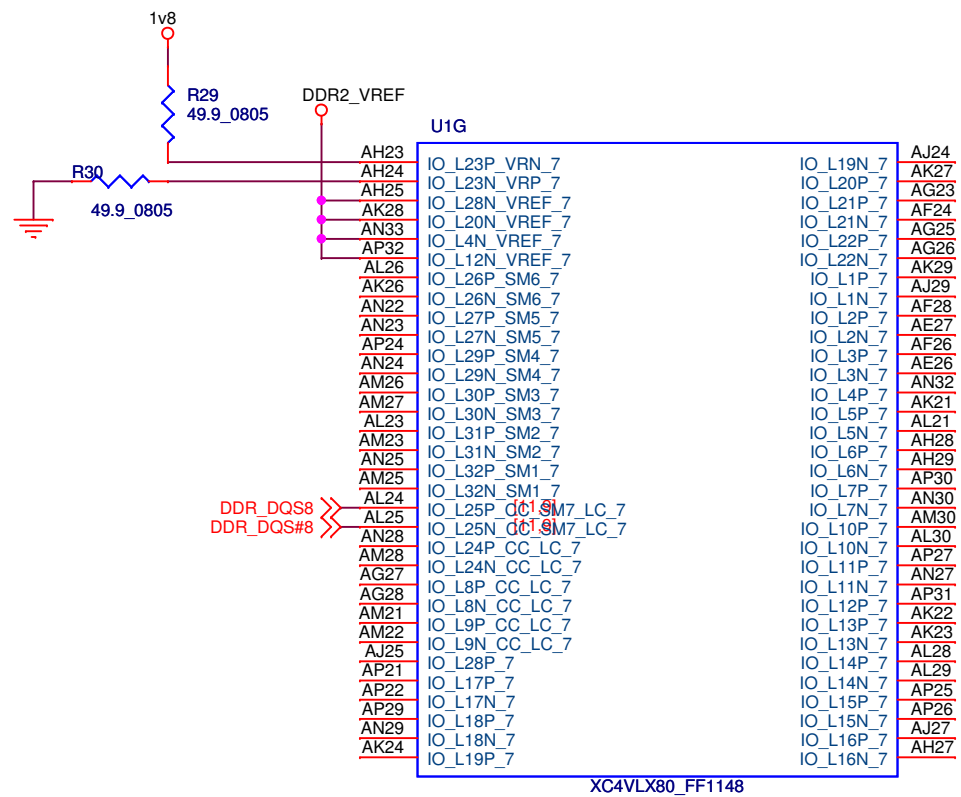
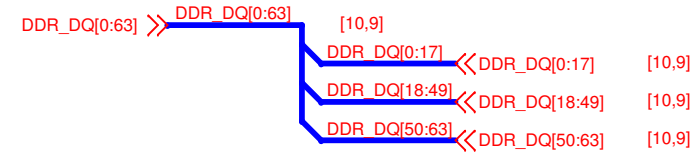
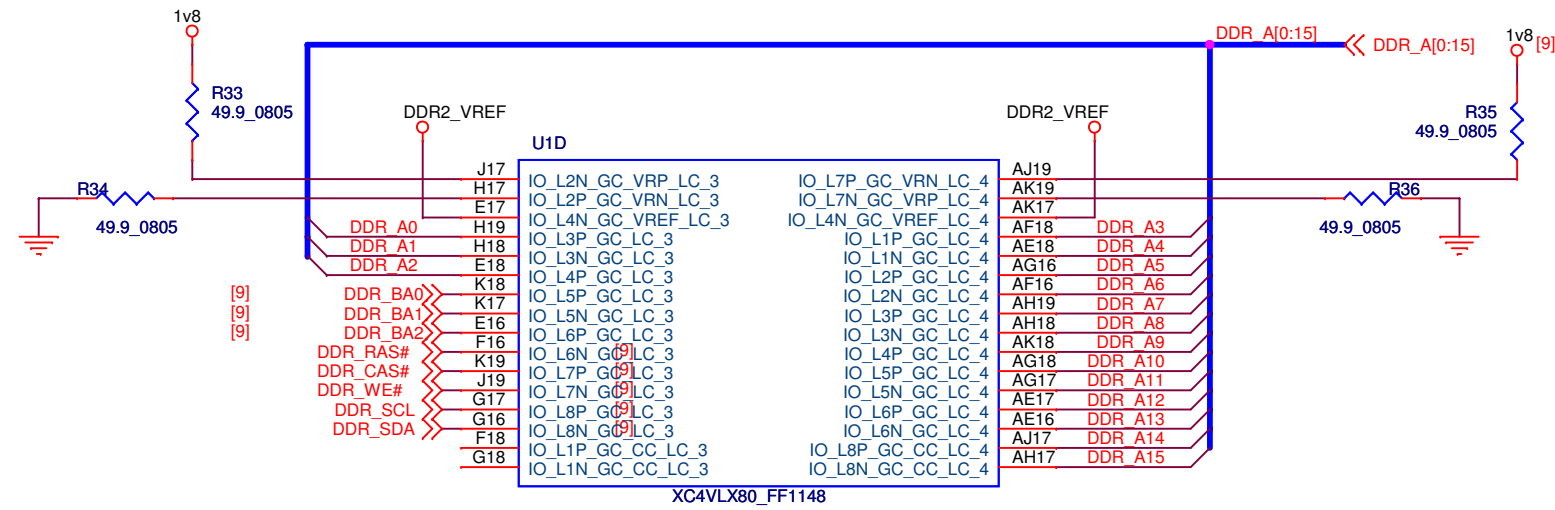
PCI FPGA Card			
Title JTAG			
Size	Document Number		
	Rev 1.0		
Date:	Sunday, October 03, 2010	Sheet	7 of 1

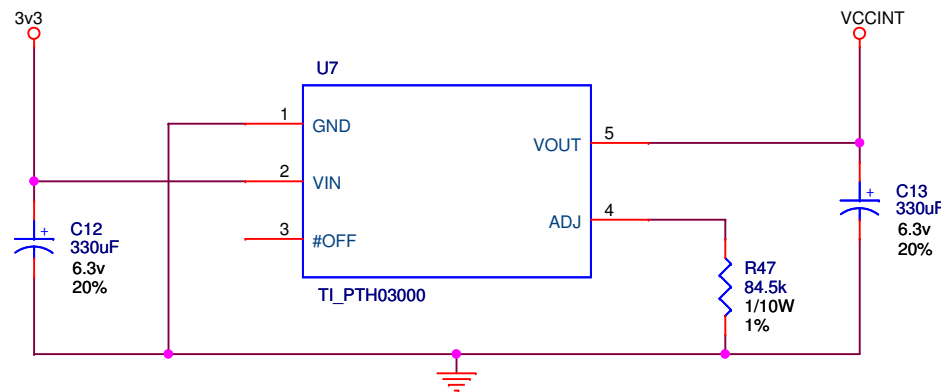
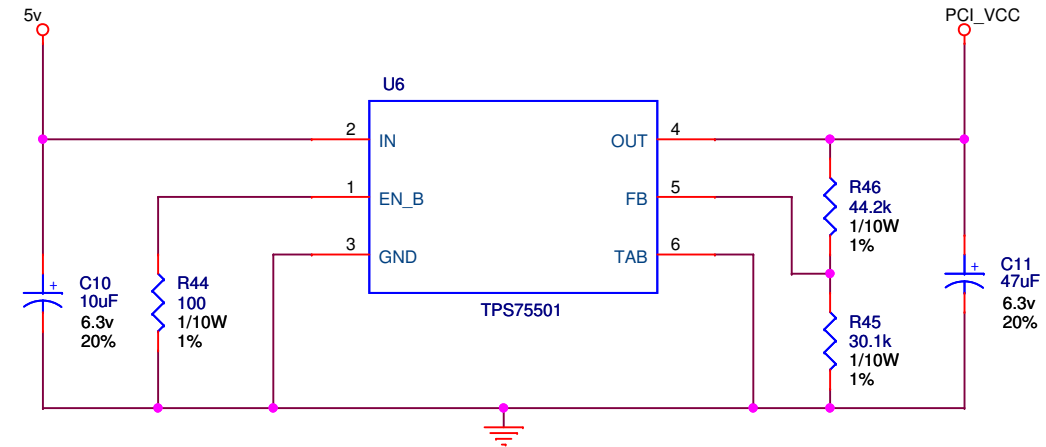
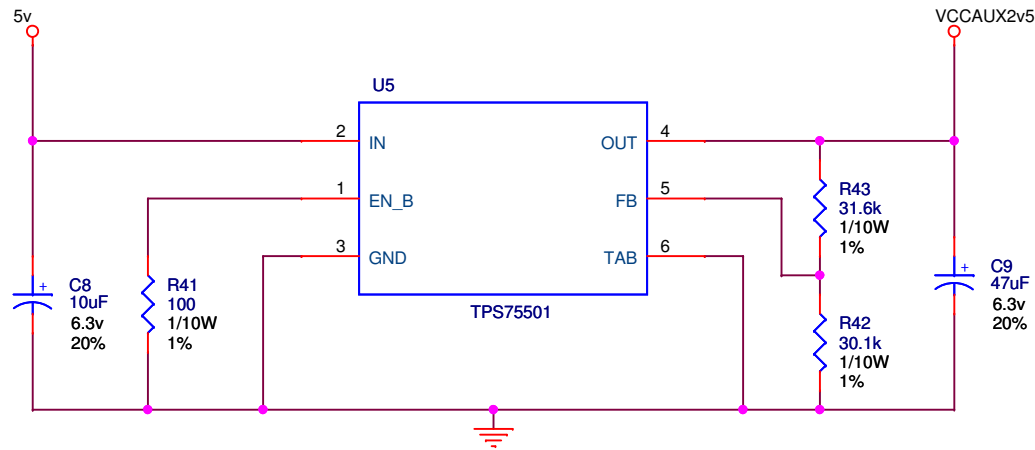
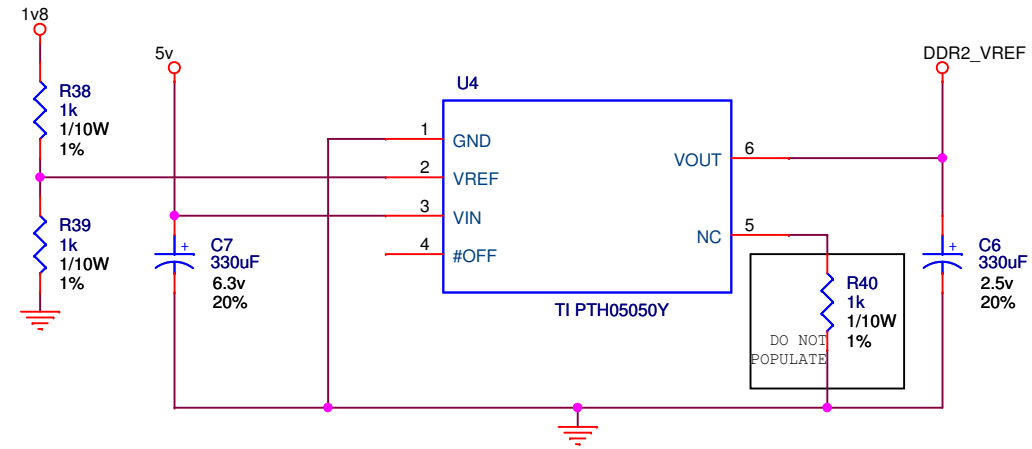
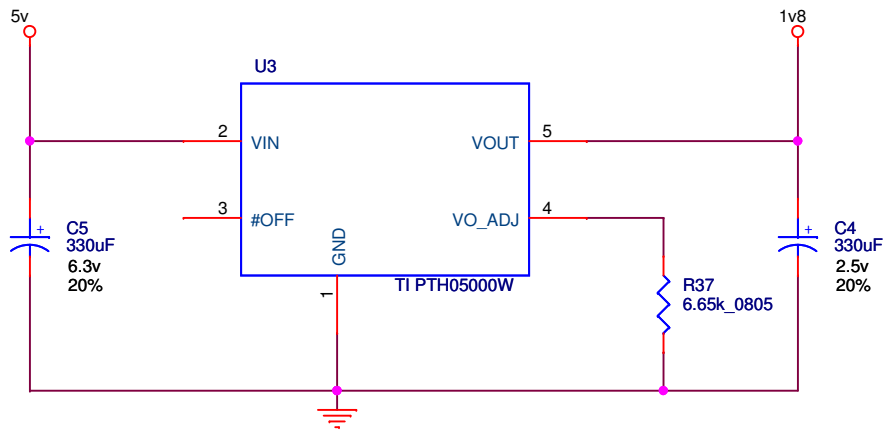


PCI FPGA Card			
Title			
JTAG			
Size	Document Number		Rev
			1.0
Date:	Sunday, October 03, 2010	Sheet	8 of 1









PCI FPGA Card			
Title		Power Regulation	
Size	Document Number		Rev 1.0
Date:	Sunday, October 03, 2010	Sheet 12 of 1	

