Zailesh A R

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EDUCATION

Course	Institute / Board	Aggregate / Year
M.Tech, VLSI Design	Vellore Institute of Technology, Vellore Campus	**8.42, 2027**
B.Tech, Electronics and Communication Engineering	Govt. Model Engineering College, Thrikkakara, Kerala (KTU)	**8.06, 2023**
Class XII	Govt. Model Boys Higher Secondary School, Attingal, Kerala	**97.5%, 2018**
Class X	S.C.V.B.H.S, Chirayinkeezhu, Kerala	**100%, 2016**

SKILLS & INTERESTS

Technical Skills: Cadence Virtuoso, Synopsys Sentaurus TCAD, Design Compiler, Formality, PrimeTime, Atalanta, TetraMAX, Verdi, Intel Quartus Prime, ModelSim, TCL, Verilog, FPGA, Python

Fields of Interest: Low Power Design, Digital and Analog IC Design, TCL Scripting, Design Verification

WORK EXPERIENCE

Embedded Engineer, STEM CADETS Pvt. Ltd. *(1 year)*

Technologies: Proteus Design Suite, ESP boards, C++.

- Executed development and validation of embedded circuits and firmware.
- Built and tested ESP-based IoT prototypes for product development.

PROJECTS

Design of a Telescopic CMOS Amplifier with Gain and Power Constraints

Role: Analog Circuit Designer **Individual Project**

Tools: Cadence Virtuoso, gm/ID Methodology, Spectre

- Designed a telescopic CMOS operational amplifier in 1.8 V supply with power budget of **1 mW** and load capacitance of **5 pF**.
- Achieved midband voltage gain of **21.04 dB ($\approx$ 11.3 V/V)** with -3 dB bandwidth of **20.06 MHz**.
- Obtained unity-gain bandwidth (UGB) of **229.42 MHz** and phase margin of **86.5**$^\circ$, ensuring stable operation.
- Sized transistors using gm/ID methodology with drain current **ID = 555 μA**, bottom NMOS width **48 μm** and top NMOS width **58 μm**.
- Verified performance through DC operating point, AC analysis, pole-zero analysis and transient simulations in Cadence Spectre.

Design and Layout Implementation with Parasitic Extraction of 4-bit Array Multiplier Using CMOS GPDK090 in Cadence Virtuoso

Role: Digital Design Engineer **Individual Project**

Technologies: CMOS GPDK090 (90 nm), Cadence Virtuoso, Spectre, DRC/LVS

- Designed a 4-bit array multiplier using CMOS logic at transistor level with hierarchical gate-based construction.
- Constructed inverter, NAND and XOR gates to build full adders and a 4-bit ripple-carry adder architecture.
- Completed full-custom layout and attained DRC- and LVS-clean verification in GPDK090.
- Performed RC parasitic extraction with **702 MOSFETs** and total extracted capacitance of **1.27 pF**.
- Final layout occupied approximately **2086 μm^2** and consumed about **2 pJ per operation** in post-layout simulation.

Design and ASIC Implementation of RISC-V Processor with UART Peripheral

Role: ASIC Design Engineer **Team Size:** 2

Technologies: Verilog HDL, Synopsys Design Compiler, Formality, PrimeTime, TCL, UART

- Implemented and optimized an RISC-V processor with UART peripheral at RTL level.
- Developed modular Verilog design including datapath, control unit, register file, ALU, and UART controller.
- Verified functional correctness using directed testbenches and waveform-based debugging.
- Performing RTL synthesis using Synopsys Design Compiler with custom TCL scripts.

Timing-Constrained Implementation of Non-Restoring Square Root Algorithm

Role: Digital Design Engineer **Team Size:** 3

Technologies: Verilog HDL, ModelSim, Intel Quartus Prime, DE2-115 FPGA, SDC

- RTL Design and Timing-Constrained Implementation of Non-Restoring Square Root Unit.
- Delivered fully synthesizable Verilog modules for control FSM and arithmetic datapath.
- Verified functionality using ModelSim testbench with input vectors.
- Implemented the design on DE2-115 FPGA with real-time output on 7-segment display.
- Applied timing constraints and performed static timing analysis using Quartus Timing Analyzer.
- Realized timing closure with positive setup, hold, recovery, and pulse-width slack.
- Tabulated results and validated correctness for all inputs from 0 to 15.

Multi-feed Instant Home Automation IoT System

Role: Hardware Designer, Developer **Team Size:** 4

Technologies: ESP8266, C++, IoT, Blynk

- Built a multi-feed home automation system with bi-directional control.

Peltier-based Thermodynamic Cold Cap for Cancer Patients

Role: Hardware Designer, Developer **Team Size:** 4

Technologies: Peltier Modules, SMPS, ESP8266

- Built a prototype to reduce chemotherapy-induced hair loss.

COURSES & CERTIFICATIONS

- Programming with Python — Internshala (Certificate received)

POSITIONS OF RESPONSIBILITY

- **Chief Content Officer, IEDC MEC** – Managed a team of 24 members and coordinated a national-level Techno-Managerial event.
- **Content Manager, IEEE MEC Student Branch** – Led a team of 20+ members and coordinated multiple events, including overnight hackathons.
- **Communications Coordinator, IETE MEC** – Handled official communications and supported coordination of student-led technical events.

ACTIVITIES & ACHIEVEMENTS

- Core Coordinator — MAGIC 2.0
- Core Coordinator — Technopreneur 2023
- Delegate — Model United Nations MEC 2020
- Awards: Third prize (District), First prize (Sub-district)