Zailesh A R

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EDUCATION

Course	Institute / Board	Aggregate / Year
M.Tech, VLSI Design	Vellore Institute Of Technology, Vellore Campus	**Ongoing, 2027**
B.Tech, Electronics and Communication Engineering	Govt. Model Engineering College, Thrikkakara, Kerala (KTU)	**8.06, 2023**
Class XII	Govt. Model Boys Higher Secondary School, Attingal, Kerala	**97.5%, 2018**
Class X	S.C.V.B.H.S, Chirayinkeezhu, Kerala	**100%, 2016**

SKILLS & INTERESTS

Tools: Cadence Virtuoso, Synopsys Sentaurus TCAD, Intel Quartus Prime, ModelSim
Technical Skills: Analog and Digital IC Design, TCAD, Verilog, FPGA, Python, C++, HTML5
Fields of Interest: Low Power Design, Digital and Analog IC Design, Design Verification
Soft Skills: Leadership, Multi-tasking, Creative Thinking, Fast Learner, Teamwork, Critical Thinking, Time Management

WORK EXPERIENCE

Embedded Engineer, STEM CADETS Pvt. Ltd. *(1 year)*
Technologies: Proteus Design Suite, ESP boards, C++.
- Designed and debugged embedded circuits and firmware.
- Hands-on experience with ESP-based IoT prototypes and product development.

PROJECTS

Design of a Telescopic CMOS Amplifier with Gain and Power Constraints
Role: Analog Circuit Designer **Individual Project**
Tools: Cadence Virtuoso, Lookup Table-based Design Methodology, Power Distribution Method
- Designed a telescopic CMOS operational amplifier to meet specific gain and power constraints using Cadence Virtuoso.
- Optimized biasing and transistor sizing through lookup table-based analytical modeling.
- Verified amplifier performance through DC, AC, Pole Zero and transient analyses in Virtuoso.

Design of a Low-Power Multiplier in Cadence Virtuoso
Role: Digital Design Engineer **Individual Project**
Tools: Cadence Virtuoso
- Designing a low-power, high-speed digital multiplier optimized for MAC units and neural network accelerators.
- Performing delay analysis on various blocks.

Design and Simulation of a Memory Module using Verilog on FPGA
Role: RTL Designer **Individual Project**
Tools: Verilog, ModelSim, Intel Quartus Prime, Cyclone IV EP4CE11529C7
- Designed and simulated a parameterized memory module supporting both read and write operations.
- Verified functionality and timing behavior using testbench-based simulations.

Multi-feed Instant Home Automation System
Role: Hardware Designer, Developer **Team Size:** 4
Technologies: ESP8266, C++, IoT, Blynk, Multiplexer, Sensors
- Built a multi-feed home automation system with bi-directional control and cloud communication.

IoT Based Sanitizer Dispenser
Role: Hardware Designer **Team Size:** 6
Technologies: ESP8266, Diaphragm Pump, Wi-Fi, SMPS
- Designed an automatic sanitizer dispenser with usage logging to the Blynk server.

Peltier-based Thermodynamic Cold Cap for Cancer Patients
Role: Hardware Designer, Developer **Team Size:** 4
Technologies: Peltier Modules, SMPS, ESP8266
- Developed a prototype to reduce chemotherapy-induced hair loss with a Peltier-based cooling cap.

COURSES & CERTIFICATIONS

- Programming with Python — Internshala (Certificate received)

POSITIONS OF RESPONSIBILITY

- Chief Content Officer, IEDC MEC
- Content Manager, IEEE MEC Student Branch
- Communications Coordinator, IETE MEC

ACTIVITIES & ACHIEVEMENTS

- Core Coordinator — MAGIC 2.0 (IEEE MEC SB)
- Core Coordinator — Technopreneur 2023 (IEDC MEC)
- Delegate — Model United Nations MEC 2020
- Awards: Third prize (District) — Improvised Experiments, State Science Fair 2018; First prize (Sub-district) — Improvised Experiments (2016–2018)

EXTRA-CURRICULAR

Karate, Yoga, Poem Writing, Playing Guitar, Blogging, Podcasting, Quizzing, Video Editing.

REFERENCES

- **Prof. Dr. Jacob Thomas V**, Principal, Govt. Model Engineering College, Thrikkakara
  `principal@mec.ac.in`
- **Prof. Dr. Mini M. G**, HOD, ECE, Govt. Model Engineering College, Thrikkakara
  `hodec@mec.ac.in`