```
`timescale 1ns / 1ps
module ram(address,clk,write,read,data_in,data_out);
///////////////  RAM I/O DELECATRIONS //////////////
reg [31:0] ram [0:31];
input write,clk;
input read;
input [31:0] data_in;
output reg[31:0] data_out;
input [4:0] address;
integer i;
///////////////  RAM OPERATION //////////////
always@(posedge clk)
begin
if(write)
ram[address] <= data_in;
else if (read)
data_out <=  ram[address];
end
////////////////////// RAM INITAL VALUES /////////
initial
begin
for(i=0;i<32;i=i+1)
ram[i]= 32'd1;
end
endmodule
```