```
`timescale 1ns / 1ps

module redaddress(alu_address,ram_address);
input  [31:0] alu_address;
output reg [4:0] ram_address;
////////////////////// Reduce Address of 32 bit to 5 bit
always@(*)
begin
casex(alu_address)
32'hxx00: ram_address = 5'd0;
32'hxx01: ram_address = 5'd1;
32'hxx02: ram_address = 5'd2;
32'hxx03: ram_address = 5'd3;
32'hxx04: ram_address = 5'd4;
32'hxx05: ram_address = 5'd5;
32'hxx06: ram_address = 5'd6;
32'hxx07: ram_address = 5'd7;
32'hxx08: ram_address = 5'd8;
32'hxx09: ram_address = 5'd9;
32'hxx0A: ram_address = 5'd10;
32'hxx0B: ram_address = 5'd11;
32'hxx0C: ram_address = 5'd12;
32'hxx0D: ram_address = 5'd13;
32'hxx0E: ram_address = 5'd14;
32'hxx0F: ram_address = 5'd15;
32'hxx10: ram_address = 5'd16;
32'hxx11: ram_address = 5'd17;
32'hxx12: ram_address = 5'd18;
32'hxx13: ram_address = 5'd19;
32'hxx14: ram_address = 5'd20;
32'hxx15: ram_address = 5'd21;
32'hxx16: ram_address = 5'd22;
32'hxx17: ram_address = 5'd23;
32'hxx18: ram_address = 5'd24;
32'hxx19: ram_address = 5'd25;
32'hxx1A: ram_address = 5'd26;
32'hxx1B: ram_address = 5'd27;
32'hxx1C: ram_address = 5'd28;
32'hxx1D: ram_address = 5'd29;
32'hxx1E: ram_address = 5'd30;
32'hxx1F: ram_address = 5'd31;
default: ram_address = 5'bZZZZZ;
endcase
end

endmodule
```