```
`timescale 1ns / 1ps
module RiscV_tb;

reg clock,reset;
wire [31:0] pc,IR,Data1,Data2;
wire [6:0] op_code;

data_path
dut(.clock(clock),.pc(pc),.reset(reset),.IR(IR),.op_code(op_code),.Data1(Data1),.Data
2(Data2));

initial
begin
reset = 1'b0;
clock = 1'b0;
#20 reset = 1'b1;
end
always
#20 clock = !clock;

endmodule
```