Faculty of Engineering and Technology Department of Electrical and Computer Engineering

ENCS 2110

Digital Electronics and Computer Organization Lab Experiment No. 4- Digital Circuits Implementation using Breadboard (POST Lab)

Name:	**Zainab murad ismail**
ID:	**1211020**
Instructor:	**Ashraf Al-Rimawi**
Section:	**4**

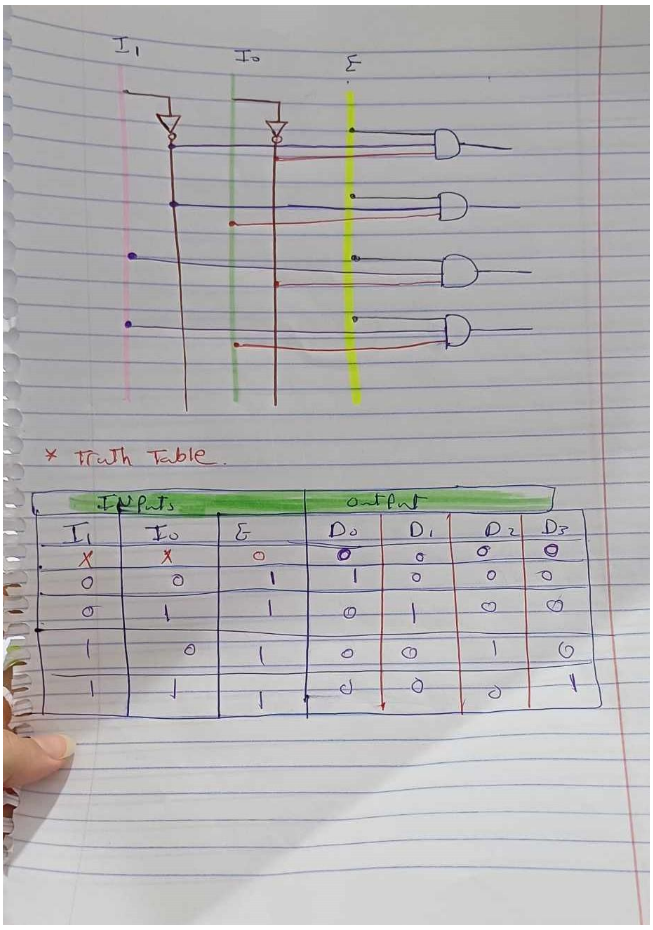
1. How do you go about adding an Enable (E) signal to the decoder in Figure 4.7? Modify the implementation to show that. (Design Only using chips in Figure 1).

We can do this By adding a third Input to the AND gates which will be the Enable.

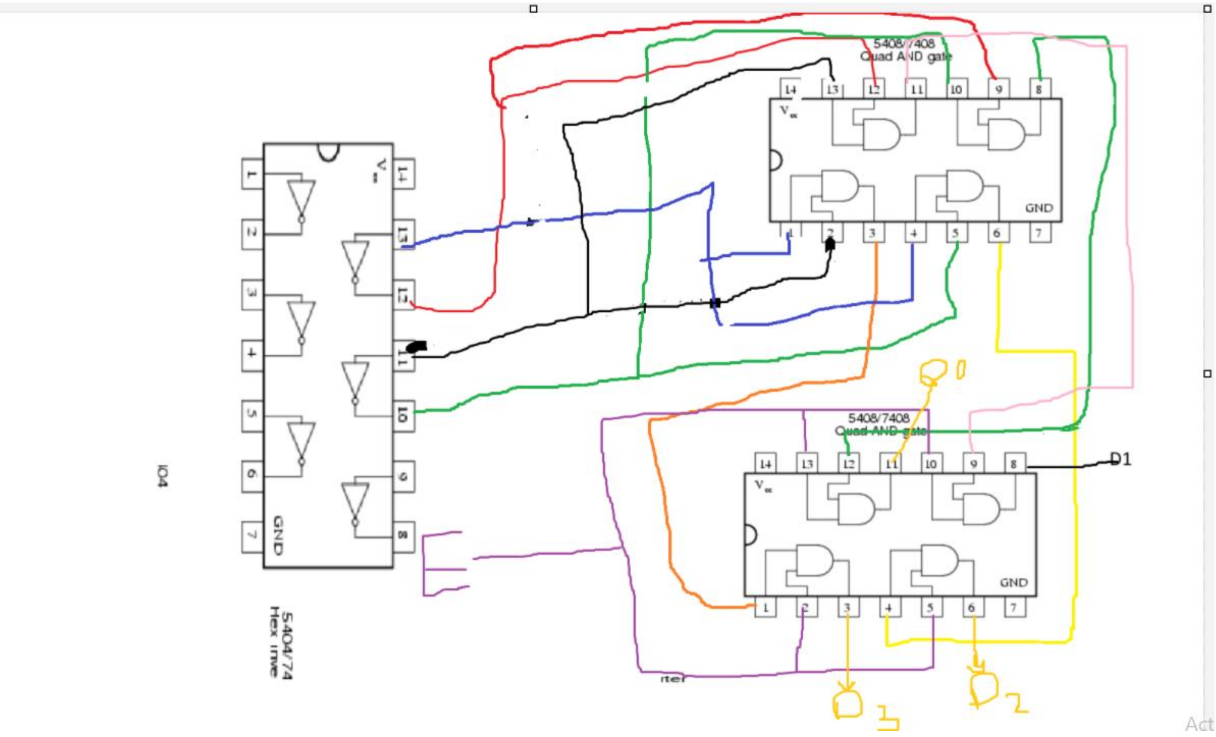
If the Enable =0 all the outputs will be zero no matter the inputssince all the AND Gates won't work.

If the Enable equals One it will work like a normal Decoder Since the Enable won't affect anything.

When using the IC there is no 3 input AND gate so what we Do is use two AND gates instead of a Three input AND Gate.



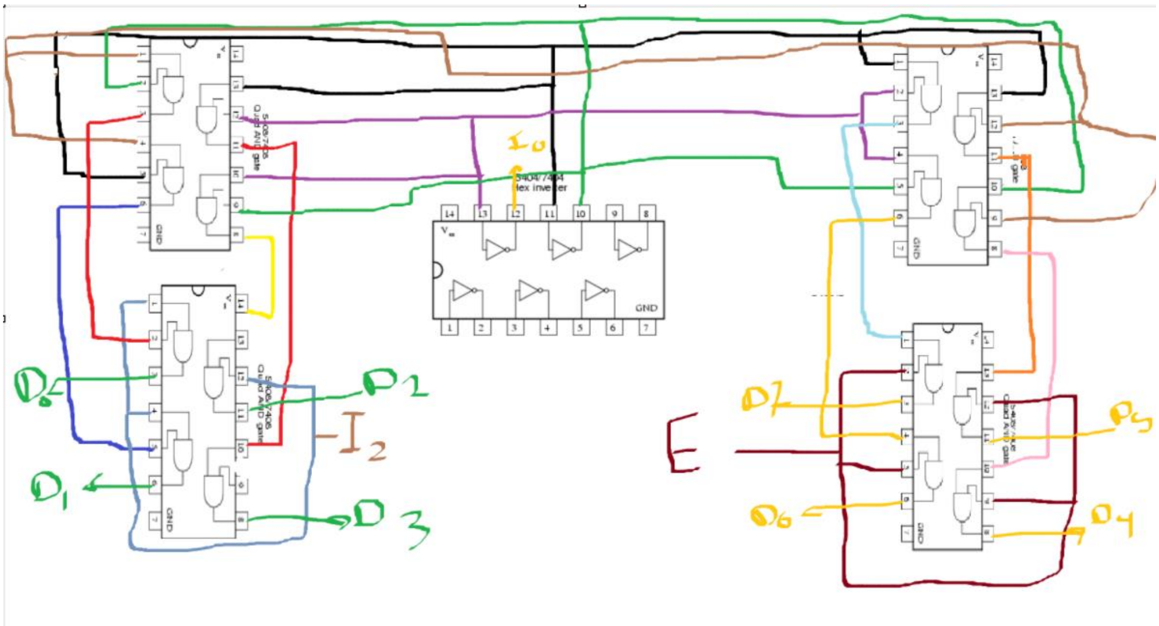
I_1	I_0	E	D_0	D_1	D_2	D_3
X	X	0	0	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1



5408/7408
Quad AND gate
GND
D1
5404/74
Hex inve
GND

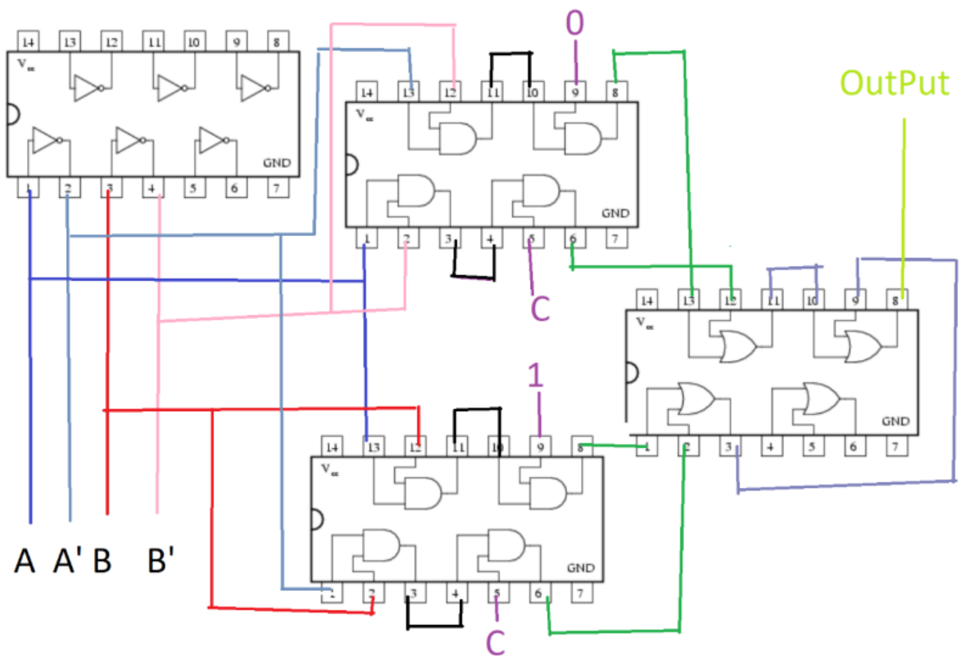
2. How to use that to implement a 3x8 decoder using chips in Figure 1.

We make I2 the enable of both decoders, and use I1 and I0 as the inputs of the decoders.



3. Use the just constructed 4x1 multiplexer to design a three-input network that gives 1 if the majority of its inputs are 1 and outputs a zero otherwise (Design Only using chips in Figure 1).

A	B	C	OUTPUT	Output Equivalent : to
0	0	0	0	0
0	0	1	0	0
0	1	0	0	C
0	1	1	1	C
1	0	0	0	C
1	0	1	1	C
1	1	0	1	1
1	1	1	1	1



4. Implement f(x, y, z) = m(0, 1, 4, 6, 7), using 4x1 MUX using chips in Figure 1.

X	Y	Z	F	Output Equivalent : to
0	0	0	1	1
0	0		1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	’Z
1	0	1	0	’Z
1	1	0	1	1
1	1	1	1	1