Faculty of Engineering and Technology Department of Electrical and Computer Engineering

ENCS 2110

Digital Electronics and Computer Organization Lab Experiment No. 1 - Combinational Logic Circuits (POST Lab)

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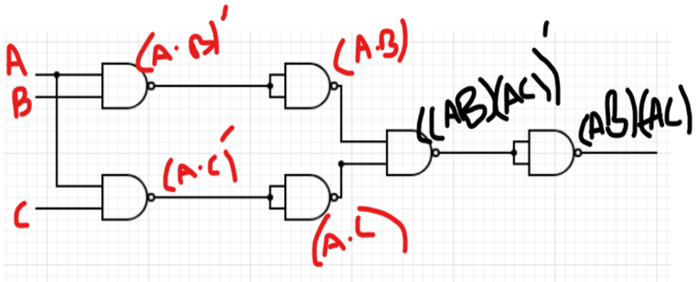
Section:	**4**

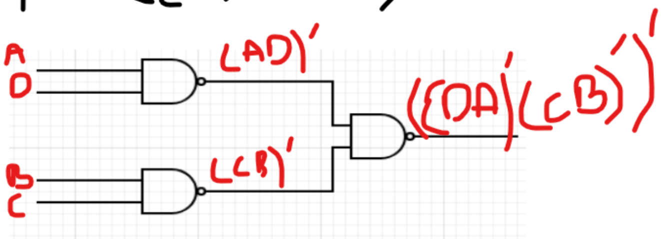
- Draw the logic diagram showing the implementation of the following Boolean equation using "NAND" gates:

a) F = AB (CA)

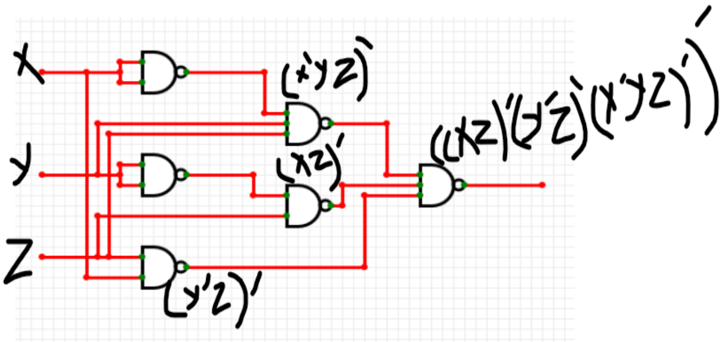


b) F= (D.A) + (C.B) =

$$F' = (DA)'(CB)'$$
$$F'' = ((DA)'(CB)')'$$



c) F = XZ + Y’Z + X’YZ

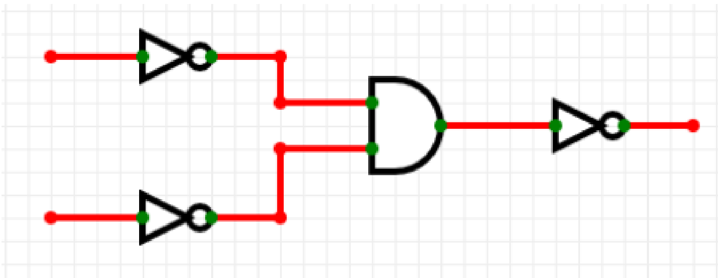


•Implement the OR operation using AND, NOT gate. Draw the logic diagram and write the Boolean equation:

F=A+B

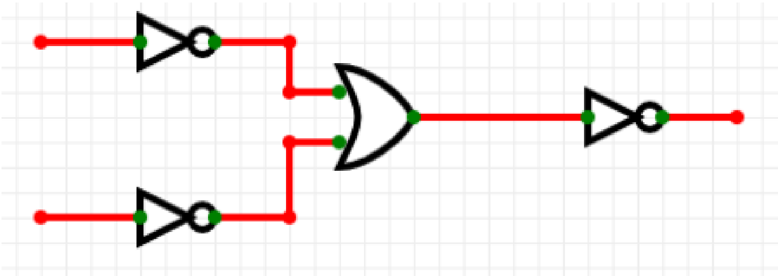
= (A+B)"

=’(’A’.B)



• implement the AND gate using OR, NOT gate. Draw the logic diagram and write the Boolean equation.

F=A.B =(A.B)’’ =(A’+B’)’



Prove that the equality operation F1=AB+A’B’ is the inverse of exclusive OR operation F2=AB’+A’B. (use Demerger’s theorem):

F2’ = (AB’+A’B)’ complement to find inverse

=(AB’)’ . (A’B)’ By DeMorgan’s law

= (A’+B) . (A+B’) By DeMorgan’s

=A’.A + A’.B’+B.A+B.B’ By Distribution law

F2’ = 0 + A’.B’+B.A + 0 By Complement law

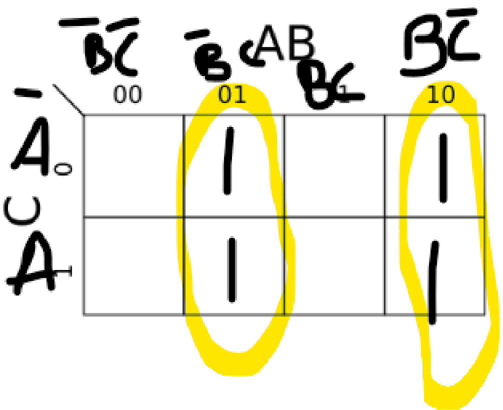
F2’ = A’.B’ +B.A By Identity law

F2’ = AB+A’B’=F1 By commutative law

• Show how is it possible to reduce Boolean expressions using the

Karnaugh map

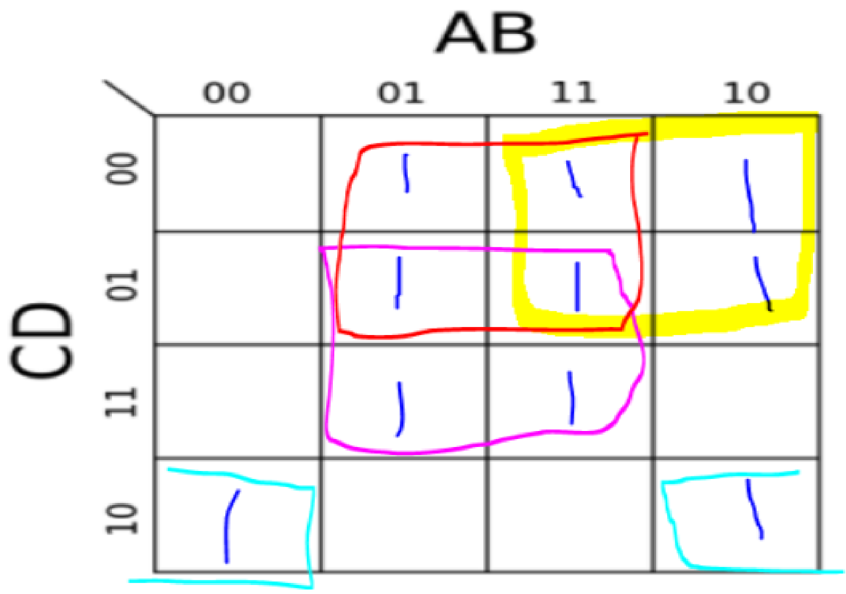
a) F1 = A’B’C + ABC’ + A’BC’ + AB’C



F1=B’C+BC’=B XOR C

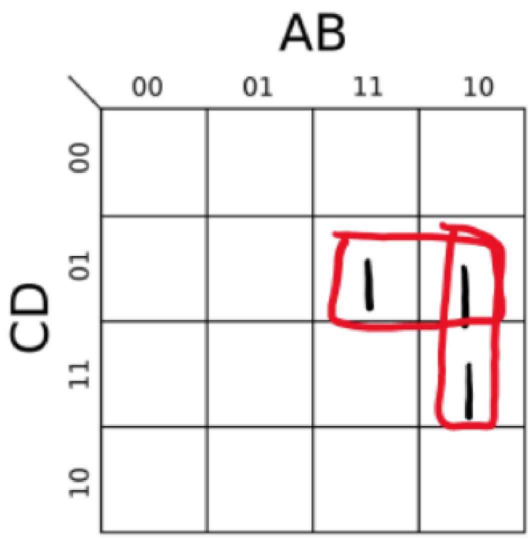
b) F2=A’D+A’C+BD+AB’D’:

F2=A’(B+B’)(C+C’)D+A’ (B+B’)C(D+D’)+(A+A’)B(C+C’)D+AB’(C+C’)D’
F2=A’BCD+A’B’CD+A’B’C’D+A’BC’D+A’BCD+A’B’CD+A’B’CD’+A’BCD’+ABCD
+A’B CD+A’BC’D+ABC’D+AB’CD’+AB’C’D’



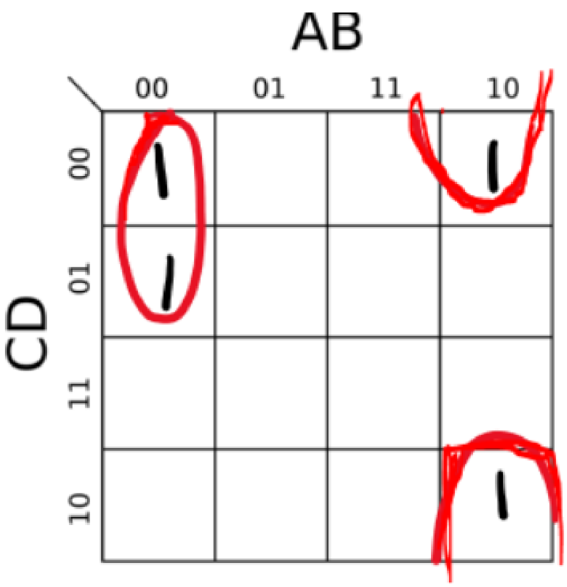
F2=A’D+A’C+BD+AB’D’

c) F3= A'BCD + ABCD' + A'BCD' + ABCD':



F3=A’BC+BCD'

d) F4= A'B'C'D' + AB'CD' + A'B'CD' + A'BC'



F4=A’C’D’+B’CD’=D’(A’C’+B’C)