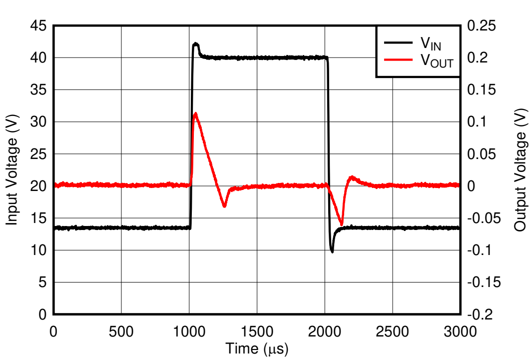
TPS7B86-Q1 500-mA, 40-V, Adjustable, Low-Dropout Regulator With Power-Good

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Input voltage range: 3 V to 40 V (42 V max)
- Output voltage range:
  - Adjustable output 1.2 V to 18 V
  - Fixed 3.3-V and 5-V output
- Maximum output current: 500 mA
- Output voltage accuracy: ±0.85% (max)
- Low dropout voltage:
  - 475 mV (max) at 450 mA (V_{OUT} ≥ 3.3 V)
- Low quiescent current:
  - 17 µA (typ) at light loads
  - 5 µA (max) when disabled
- Excellent line transient response:
  - ±2% V_{OUT} deviation during cold-crank
  - ±2% V_{OUT} deviation (1-V/µs V_{IN} slew rate)
- Power-good with programmable delay period
- Stable with a 2.2-µF or larger capacitor
- Package options:
  - 5-pin TO-252 package: 29.7°C/W $R_{θJA}$
  - 8-pin HSOIC-8 package with thermal pad: 41.8°C/W $R_{θJA}$

2 Applications

- Reconfigurable instrument clusters
- Body control modules (BCM)
- Always-on battery-connected applications:
  - Automotive gateways
  - Remote keyless entries (RKE)



Line Transient Response (3-V/µs V_{IN} Slew Rate)

3 Description

The TPS7B86-Q1 is a low-dropout linear regulator designed to connect to the battery in automotive applications. The device has an input voltage range extending to 40 V, which allows the device to withstand transients (such as load dumps) that are anticipated in automotive systems. With only a 17-µA quiescent current at light loads, the device is an optimal solution for powering always-on components such as microcontrollers (MCUs) and controller area network (CAN) transceivers in standby systems.

The device has state-of-the-art transient response that allows the output to quickly react to changes in load or line (for example, during cold-crank conditions). Additionally, the device has a novel architecture that minimizes output overshoot when recovering from dropout. During normal operation, the device has a tight DC accuracy of ±0.85% over line, load, and temperature.

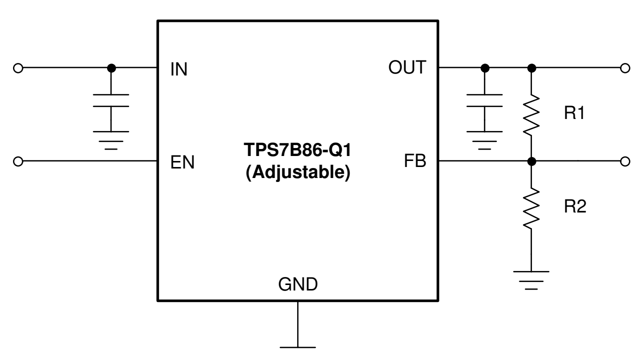
The power-good delay can be adjusted by external components, allowing the delay time to be configured to fit application-specific systems.

The device is available in thermally conductive packaging to allow the device components to efficiently transfer heat to the circuit board.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7B86-Q1	HSOIC (8)	4.89 mm × 3.90 mm
	TO-252 (5)	6.60 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Adjustable Output Voltage

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (December 2020)	Page
• Changed document status from advanced information to production data	1

5 Pin Configuration and Functions

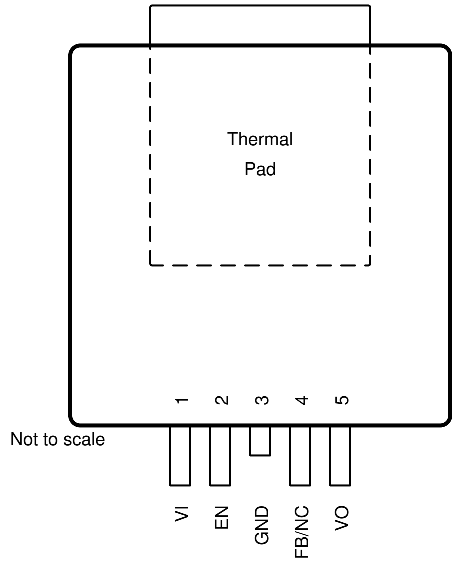


Figure 5-1. KVU Package, 5-Pin TO-252, Top View

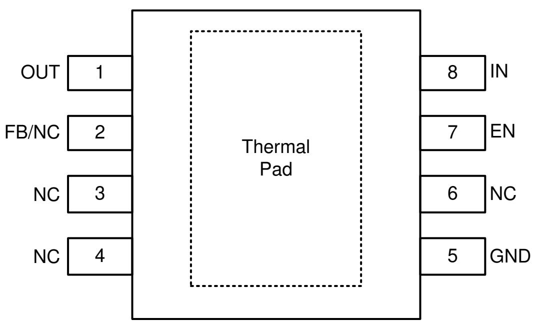


Figure 5-2. DDA Package (Without PG), 8-Pin HSOIC, Top View

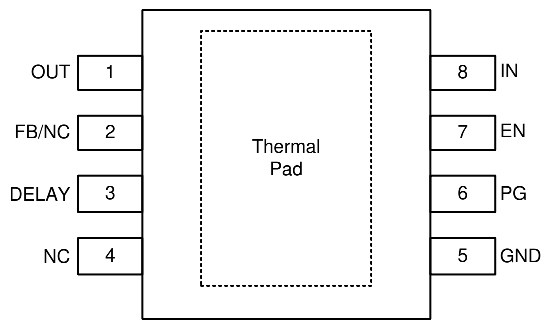


Figure 5-3. DDA Package (With PG), 8-Pin HSOIC, Top View

Table 5-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	KVU	DDA (Without PG)	DDA (With PG)		
DELAY	—	—	3	O	Power-good delay adjustment pin. Connect a capacitor from this pin to GND to set the PG reset delay. Leave this pin floating for a default ($t_{(DLY\_FIX)}$) delay. See the *Power-Good (PG)* section for more information. If this functionality is not desired, leave this pin floating because connecting this pin to GND causes a perminant increase in the GND current.
EN	2	7	7	I	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). Do not leave this pin floating because this pin is high impedance. If left floating, this pin may cause the device to enable or disable.
FB/NC	4	2	2	I	This pin is a feedback pin when using an external resistor divider or an NC pin when using the device with a fixed output voltage. When using the adjustable device, this pin must be connected through a resistor divider to the output for the device to function. If using a fixed output this pin can either be left floating or connected to GND.
GND	3	4, 5	4, 5	G	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.

Table 5-1. Pin Functions (continued)

PIN				TYPE	DESCRIPTION
NAME	KVU	DDA (Without PG)	DDA (With PG)		
IN	1	8	8	P	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND as listed in the *Recommended Operating Conditions* table and the *Input Capacitor* section. Place the input capacitor as close to the input of the device as possible.
NC	—	3, 6	3, 6	—	No internal connection. This pin can be left floating or tied to GND for best thermal performance.
OUT	5	1	1	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to GND; see the *Recommended Operating Conditions* table and the *Output Capacitor* section. Place the output capacitor as close to output of the device as possible. If using a high equivalent series resistance (ESR) capacitor, decouple the output with a 100-nF ceramic capacitor.
PG	—	—	6	O	Power-good pin. This pin has an internal pullup resistor. Do not connect this pin to V_{OUT} or any other biased voltage rail. V_{PG} is logic level high when V_{OUT} is above the power-good threshold. See the *Power-Good (PG)* section for more information.
Thermal pad	Pad	Pad	Pad	—	Thermal pad. Connect the pad to GND for best possible thermal performance. See the *Layout* section for more information.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input	–0.3	42	V
EN	Enable input	–0.3	42	V
V_{OUT}	Regulated output	–0.3	V_{IN} + 0.3 V(2)	V
FB	Feedback	–0.3	20	V
Delay	Reset delay input, power-good adjustable threshold	–0.3	6	V
PG	Power-good outupt	–0.3	20	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. Theseare stress ratings only and functional operation of the device at these or any other conditionsbeyond those indicated under *recommended operating conditions* isnot implied. Exposure to absolute-maximum-rated conditions for extended periods may affect devicereliability.
(2) The absolute maximum rating is VIN + 0.3 V or 20 V, whichever is smaller

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	3		40	V
V_{OUT}	Output voltage	1.2		18	V
I_{OUT}	Output current	0		500	mA
F_{EN}	Enable pin frequency(1)			5	kHz
V_{EN}	High voltage (I/O)	0		40	V
V_{Delay}	Delay pin voltage, power-good adjustable threshold	0		5.5	V
V_{PG}	Power-good outupt pin	0		18	V
C_{OUT}	Output capacitor(3)	2.2		220	µF
ESR	Output capacitor ESR requirements	0.001		2	Ω
C_{IN}	Input capacitor(2)	0.1	1		µF
C_{Delay}	Power-good delay capacitor			1	µF
T_J	Operating junction temperature	–40		150	°C

(1) Minimum pulse time on the EN pin is 100 µs.
(2) For robust EMI performance the minimum input capacitance is 500 nF.
(3) Effective output capacitance of 1 µF minimum required for stability.

6.4 Thermal Information

THERMAL METRIC[1] [2]		TPS7B86-Q1		UNIT
		KVU	DDA	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.7	41.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.2	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.6	17.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.9	4.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.5	17.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.5	5.7	°C/W

(1) The thermal data is based on the JEDEC standard high K profile,JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered tothe thermal land pattern. Also, correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics,see the Semiconductor and IC PackageThermal Metrics application report.

6.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		Test Conditions	MIN	TYP	MAX	UNIT
V_{OUT}	Regulated output (DDA package)	$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 100 µA to 450 mA, T_J = 25ºC[1]	–0.75		0.75	%
		$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 100 µA to 500 mA, T_J = 25ºC[1]	–0.75		0.75	
		$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 100 µA to 450 mA[1]	–0.85		0.85	
		$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 100 µA to 500 mA[1]	–0.85		0.85	
V_{OUT}	Regulated output (KVU Package)	$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 100 µA to 450 mA, T_J = 25ºC[1]	–0.85		0.85	%
		$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 100 µA to 500 mA, T_J = 25ºC[1]	–0.85		0.85	
		$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 100 µA to 450 mA[1]	–1.15		1.15	
		$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 100 µA to 500 mA[1]	–1.15		1.15	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	$V_{IN} = V_{OUT}$ + 1 V, I_{OUT} = 100 µA to 450 mA , V_{OUT} ≥ 3.3 V			0.425	%
		$V_{IN} = V_{OUT}$ + 1 V, I_{OUT} = 100 µA to 500 mA , V_{OUT} ≥ 3.3 V			0.45	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation (adjustable output only)	$V_{IN} = V_{OUT}$ + 1 V, I_{OUT} = 100 µA to 450 mA , V_{OUT} < 3.3 V			0.625	%
		$V_{IN} = V_{OUT}$ + 1 V, I_{OUT} = 100 µA to 500 mA , V_{OUT} < 3.3 V			0.65	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 100 µA			0.2	%
ΔV_{OUT}	Load transient response settling time	$t_R = t_F$ = 1 µs; C_{OUT} = 10 µF, V_{OUT} ≥ 3.3V			100	µs
ΔV_{OUT}	Load transient response overshoot, undershoot[2]	$t_R = t_F$ = 1 µs; C_{OUT} = 10 µF, V_{OUT} ≥ 3.3V; I_{OUT} = 150 mA to 350 mA	–2%			$\%V_{OUT}$
		I_{OUT} = 350 mA to 150 mA			10%	
		I_{OUT} = 0 mA to 500 mA	–10%			
ΔV_{OUT}	Load transient response overshoot, undershoot[2]	$t_R = t_F$ = 1 µs; C_{OUT} = 10 µF, V_{OUT} < 3.3V; I_{OUT} = 150 mA to 350 mA	–2.5%			$\%V_{OUT}$
		I_{OUT} = 350 mA to 150 mA			10%	
		I_{OUT} = 0 mA to 500 mA	–10%			
I_Q	Quiescent current	$V_{IN} = V_{OUT}$ + 1 V to 40V, I_{OUT} = 0 mA, T_J = 25ºC[3]		17	21	µA
		$V_{IN} = V_{OUT}$ + 1 V to 40 V, I_{OUT} = 0 mA[3]			26	
		I_{OUT} = 500 µA			35	
$I_{SHUTDOWN}$	Shutdown supply current (I_{GND})	V_{EN} = 0 V, T_J = 25ºC			2.5	µA
		V_{EN} = 0 V			4	
V_{DO}	Dropout voltage fixed output voltages (DDA Package)	I_{OUT} ≤ 1 mA, V_{OUT} ≥ 3.3 V, $V_{IN} = V_{OUT(NOM)}$ x 0.95			43	mV
		I_{OUT} = 315 mA, V_{OUT} ≥ 3.3 V, $V_{IN} = V_{OUT(NOM)}$		260	360	
		I_{OUT} = 450 mA, V_{OUT} ≥ 3.3 V, $V_{IN} = V_{OUT(NOM)}$		335	475	
		I_{OUT} = 500 mA, V_{OUT} ≥ 3.3 V, $V_{IN} = V_{OUT(NOM)}$		360	535	
V_{DO}	Dropout voltage adjustable output	I_{OUT} ≤ 1 mA, V_{FB} = 0.61 V, V_{IN} = 3 V			43	mV
		I_{OUT} = 315 mA, V_{FB} = 0.61 V, V_{IN} = 3 V			400	
		I_{OUT} = 450 mA, V_{FB} = 0.61 V, V_{IN} = 3 V			525	
		I_{OUT} = 500 mA, V_{FB} = 0.61 V, V_{IN} = 3 V			570	
V_{DO}	Dropout voltage fixed output voltages (KVU Package)	I_{OUT} ≤ 1 mA, V_{OUT} ≥ 3.3 V, $V_{IN} = V_{OUT(NOM)}$ x 0.95			46	mV
		I_{OUT} = 315 mA, V_{OUT} ≥ 3.3 V, $V_{IN} = V_{OUT(NOM)}$		275	400	
		I_{OUT} = 450 mA, V_{OUT} ≥ 3.3 V, $V_{IN} = V_{OUT(NOM)}$		360	525	
		I_{OUT} = 500 mA, V_{OUT} ≥ 3.3 V, $V_{IN} = V_{OUT(NOM)}$		390	575	

6.5 Electrical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		Test Conditions	MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage	Reference voltage for FB	0.644	0.65	0.656	V
I_{FB}	Feedback current	Current into FB pin	-10		10	nA
I_{EN}	EN pin current	V_{EN} = V_{IN} = 13.5 V			50	nA
$V_{UVLO(RISING)}$	Rising input supply UVLO	V_{IN} rising	2.6	2.7	2.82	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO	V_{IN} falling	2.38	2.5	2.6	V
$V_{UVLO(HYST)}$	$V_{UVLO(IN)}$ hysteresis			230		mV
V_{IL}	Enable logic input low level				0.7	V
V_{IH}	Enable logic input high level		2			V
I_{CL}	Output current limit	V_{IN} = V_{OUT} + 1 V, V_{OUT} short to 90% x $V_{OUT(NOM)}$	540		780	mA
PSRR	Power supply rejection ratio	V_{IN} - V_{OUT} = 1 V, frequency = 1 kHz, I_{OUT} = 450 mA		70		dB
R_{PG}	Power-good internal pull up resistor		10	30	50	kΩ
$V_{PG(OL)}$	PG pin low level output voltage	V_{OUT} ≤ 0.83 x V_{OUT}			0.4	V
$V_{PG(TH,RISING)}$	Default power-good threshold	V_{OUT} rising	85		95	%V_{OUT}
$V_{PG(TH,FALLING)}$	Default power-good threshold	V_{OUT} falling	83		93	%V_{OUT}
$V_{PG(HYST)}$	Power-good hysteresis			2		%V_{OUT}
$V_{DLY(TH)}$	Threshold to release power-good high	Voltage at DELAY pin rising	1.17	1.21	1.25	V
$I_{DLY(CHARGE)}$	Delay capacitor charging current	Voltage at DELAY pin = 1 V	1	1.5	2	µA
T_J	Junction temperature		–40		150	°C
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			20		°C

(1) Power dissipation is limited to 2 W for device production testing purposes. The power dissipation can be higher during normal operation. See the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150℃.
(2) Specified by design.
(3) For the adjustable output this is tested in unity gain and resistor current is not included.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(DLY\_FIX)}$	Power-good propagation delay	No capacitor connect at DELAY pin		100		µs
$t_{(Deglitch)}$	Power-good deglitch time	No capacitor connect at DELAY pin		90		µs
$t_{(DLY)}$	Power-good propagation delay	Delay capacitor value: $C_{(DELAY)}$ = 100 nF		80		ms

6.7 Typical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)

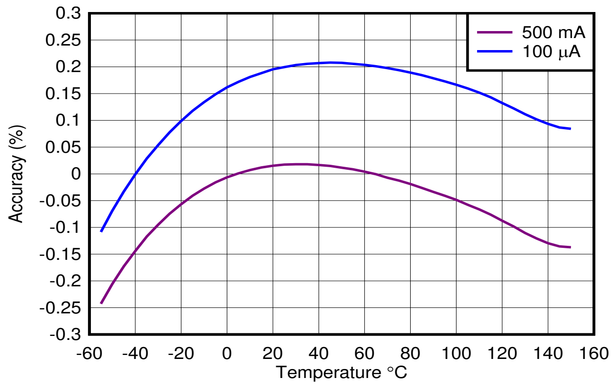
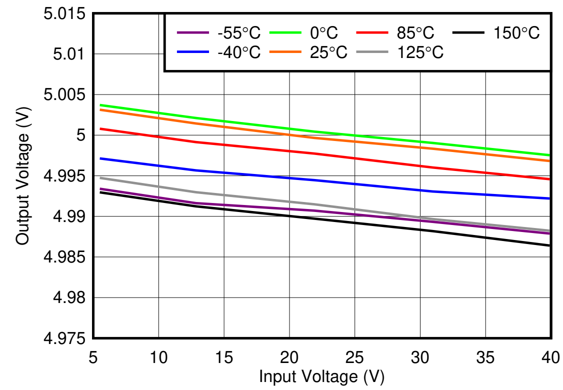
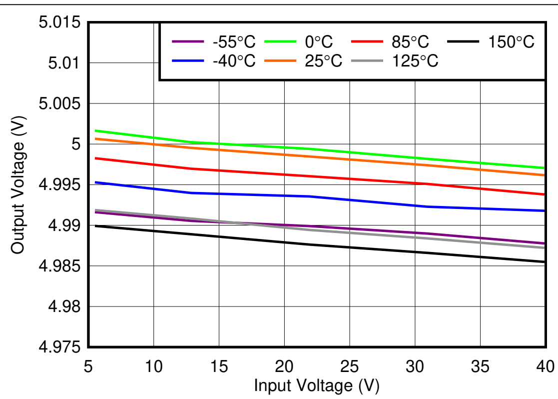


Figure 6-1. Accuracy vs Temperature



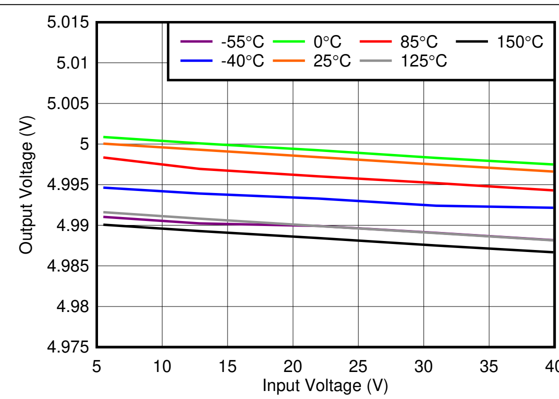
V_{OUT} = 5 V, I_{OUT} = 150 mA

Figure 6-2. Line Regulation vs V_{IN}



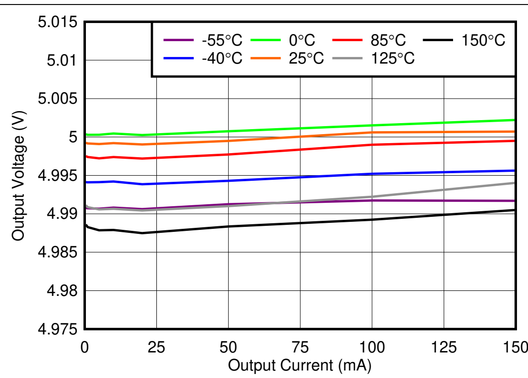
V_{OUT} = 5 V, I_{OUT} = 5 mA

Figure 6-3. Line Regulation vs V_{IN}



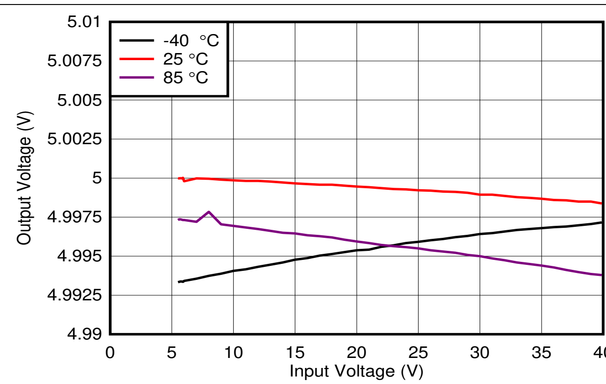
V_{OUT} = 5 V, I_{OUT} = 1 mA

Figure 6-4. Line Regulation vs V_{IN}



V_{OUT} = 5 V

Figure 6-5. Load Regulation vs I_{OUT}

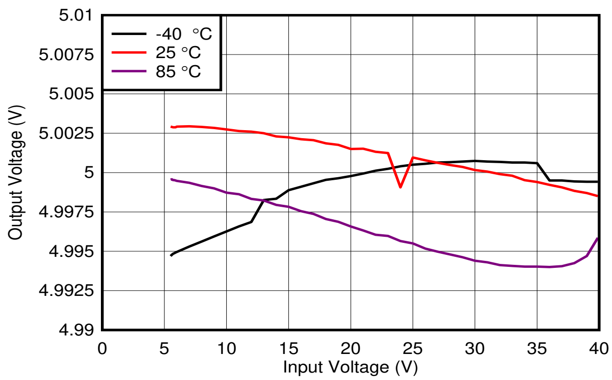


C_{OUT} = 10 µF, V_{OUT} = 5 V

Figure 6-6. Line Regulation at 50 mA

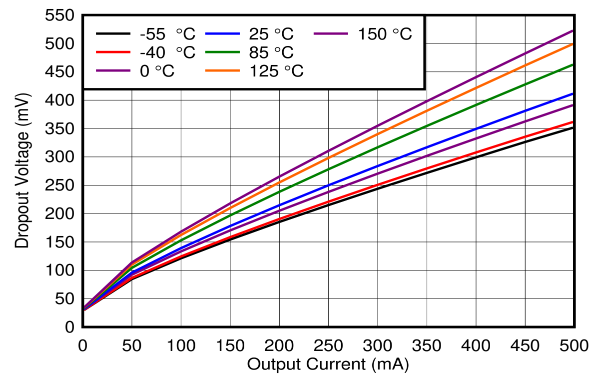
6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



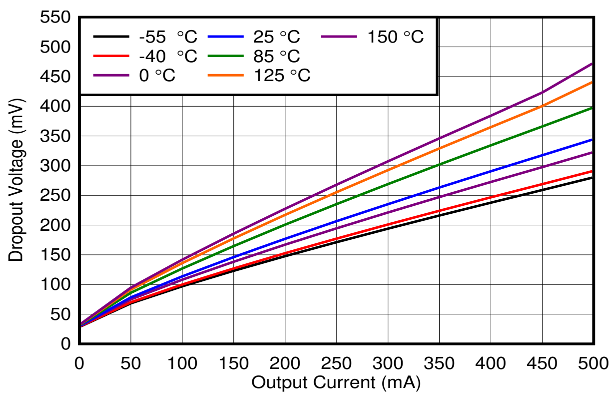
C_{OUT} = 10 µF, V_{OUT} = 5 V

Figure 6-7. Line Regulation at 100 mA



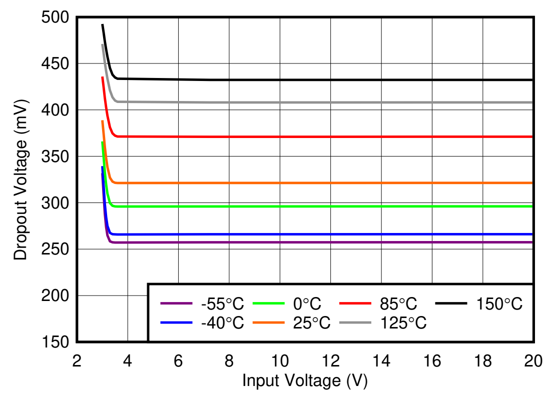
V_{IN} = 3 V

Figure 6-8. Dropout Voltage (V_{DO}) vs I_{OUT}



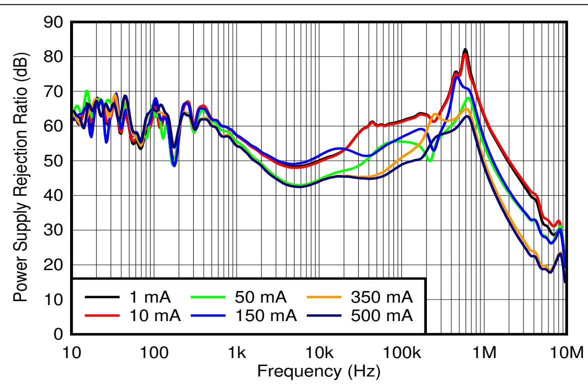
V_{IN} = 20 V

Figure 6-9. Dropout Voltage (V_{DO}) vs I_{OUT}



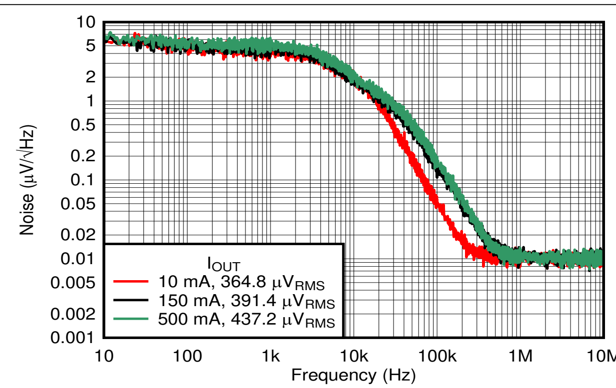
I_{OUT} = 450 mA

Figure 6-10. Dropout Voltage (V_{DO}) vs V_{IN}



C_{OUT} = 10 µF (X7R 50 V), V_{OUT} = 5 V

Figure 6-11. PSRR vs Frequency and I_{OUT}

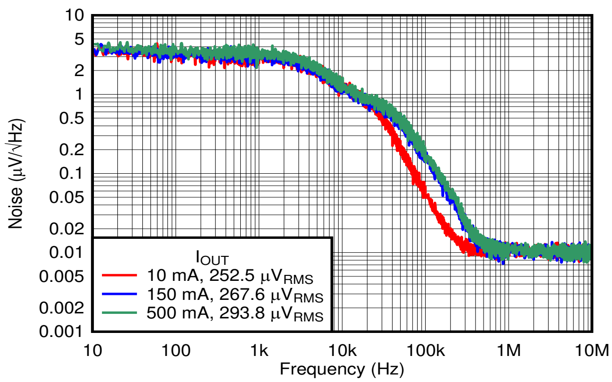


C_{OUT} = 10 µF (X7R 50 V), V_{OUT} = 5 V

Figure 6-12. Noise vs Frequency

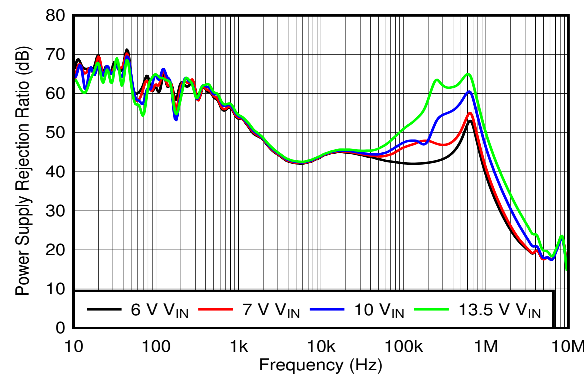
6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



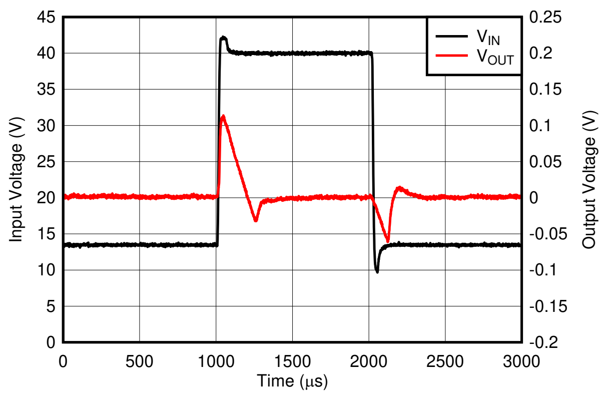
C_{OUT} = 10 µF (X7R 50 V), V_{OUT} = 3.3 V

Figure 6-13. Noise vs Frequency



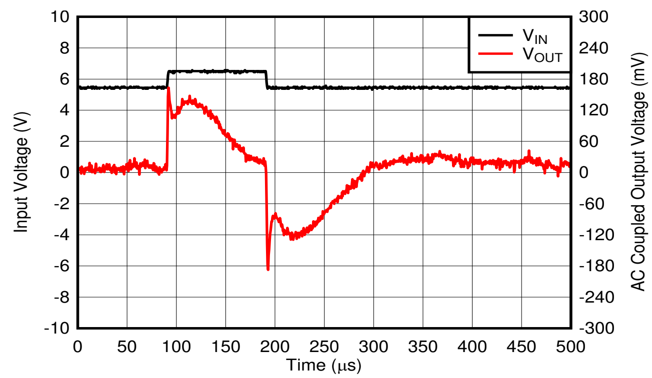
C_{OUT} = 10 µF (X7R 50 V), I_{OUT} = 500 mA, V_{OUT} = 5 V

Figure 6-14. PSRR vs Frequency and V_{IN}



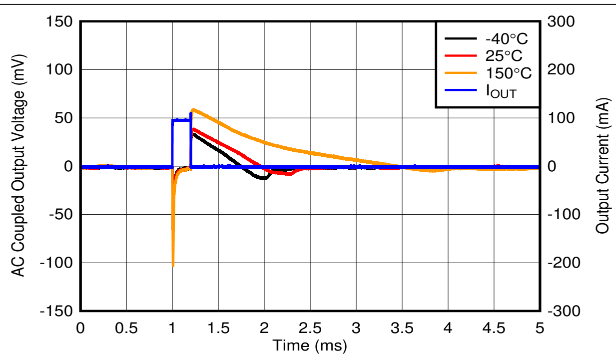
V_{OUT} = 5 V, I_{OUT} = 1 mA, V_{IN} = 13.5 V to 45 V, slew rate = 2.7 V/µs, V_{EN} = 3.3 V

Figure 6-15. Line Transients



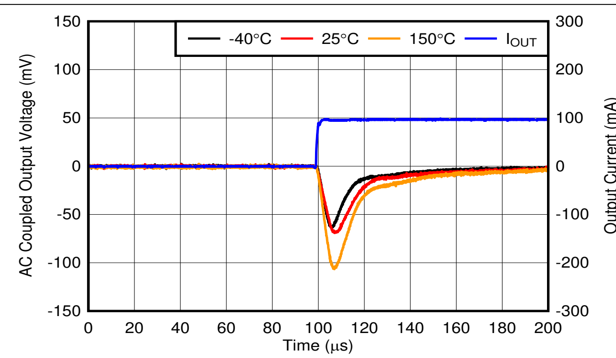
V_{OUT} = 5 V, I_{OUT} = 100 mA, V_{IN} = 5.5 V to 6.5 V, rise time = 1 µs, V_{EN} = 3.3 V

Figure 6-16. Line Transients



V_{OUT} = 5 V, I_{OUT} = 0 mA to 100 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-17. Load Transient, No Load to 100 mA

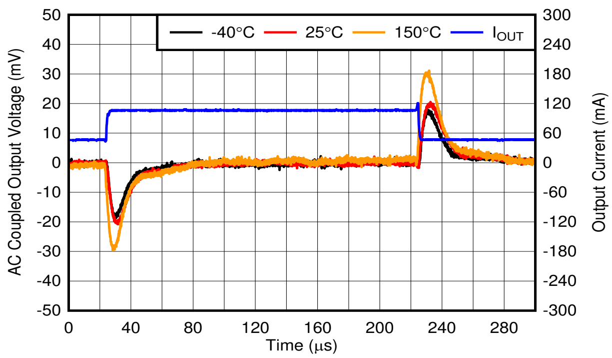


V_{OUT} = 5 V, I_{OUT} = 0 mA to 100 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-18. Load Transient, No Load to 100-mA Rising Edge

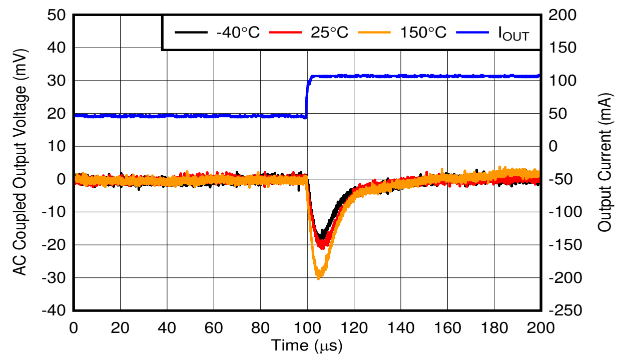
6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



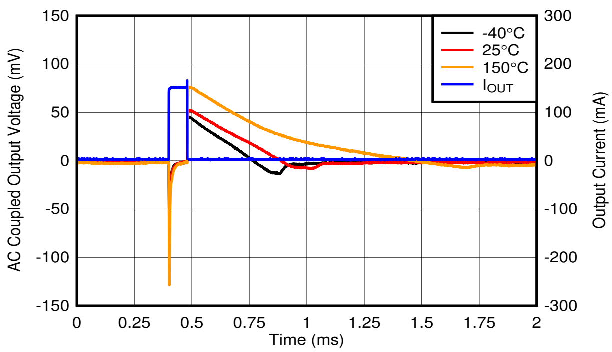
V_{OUT} = 5 V, I_{OUT} = 45 mA to 105 mA, slew rate = 0.1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-19. Load Transient, 45 mA to 105 mA



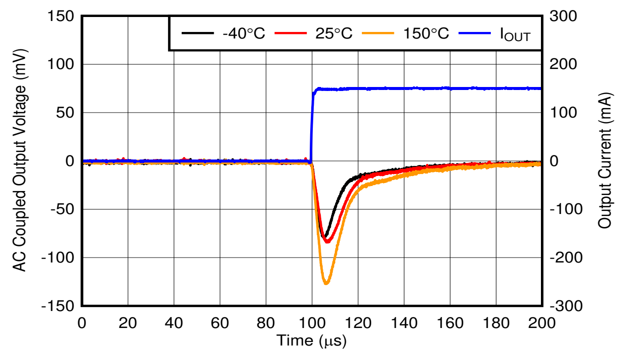
V_{OUT} = 5 V, I_{OUT} = 45 mA to 105 mA, slew rate = 0.1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-20. Load Transient, 45-mA to 105-mA Rising Edge



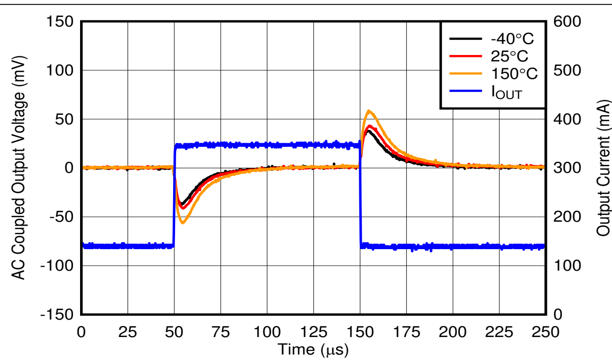
V_{OUT} = 5 V, I_{OUT} = 0 mA to 150 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-21. Load Transient, No Load to 150-mA



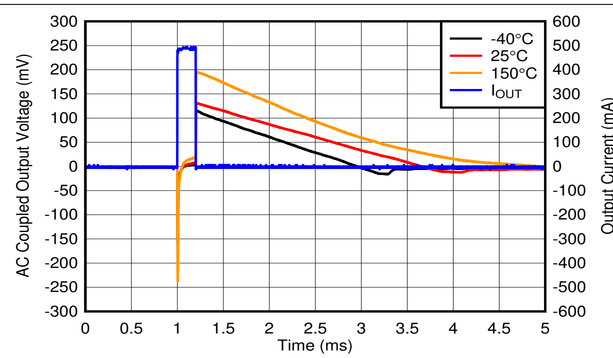
V_{OUT} = 5 V, I_{OUT} = 0 mA to 150 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-22. Load Transient, No Load to 150-mA Rising Edge



V_{OUT} = 5 V, I_{OUT} = 150 mA to 350 mA, slew rate = 0.1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-23. Load Transient, 150-mA to 350-mA

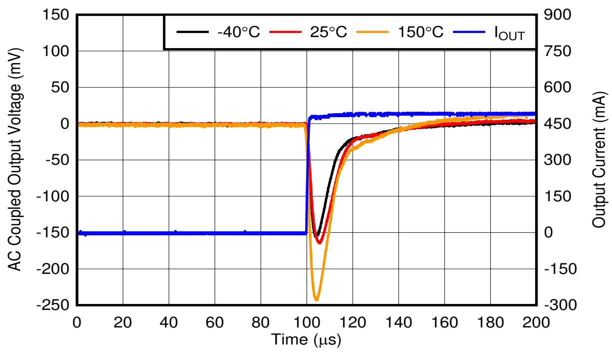


V_{OUT} = 5 V, I_{OUT} = 0 mA to 500 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-24. Load Transient, No Load to 500 mA

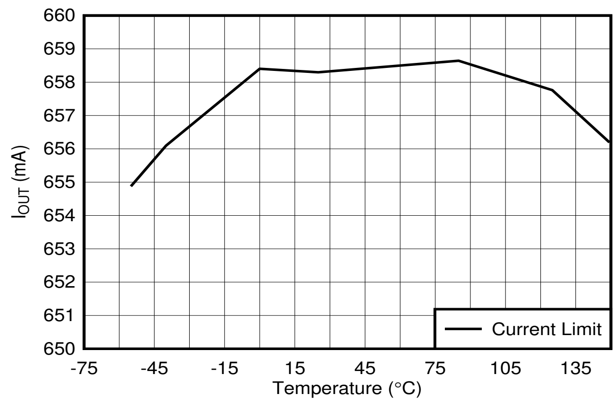
6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)



V_{OUT} = 5 V, I_{OUT} = 0 mA to 500 mA, slew rate = 1 A/µs, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-25. Load Transient, No Load to 500-mA Rising Edge



V_{IN} = V_{OUT} + 1 V, V_{OUT} = 90% × $V_{OUT(NOM)}$

Figure 6-26. Output Current Limit vs Temperature

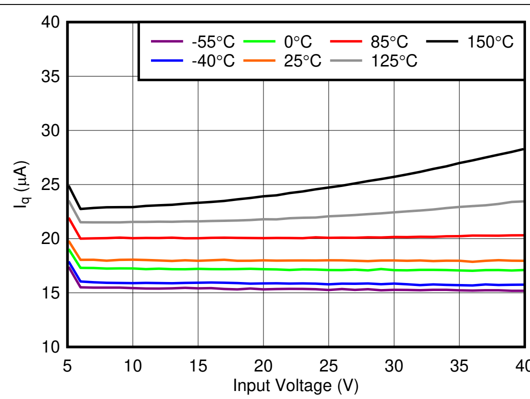
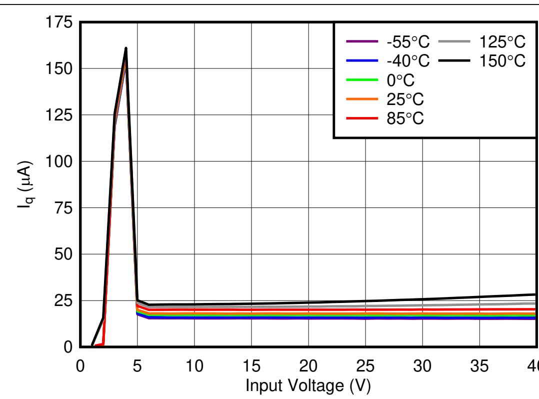


Figure 6-27. Quiescent Current (I_Q) vs V_{IN}



V_{OUT} = 5 V

Figure 6-28. Quiescent Current (I_Q) vs V_{IN}

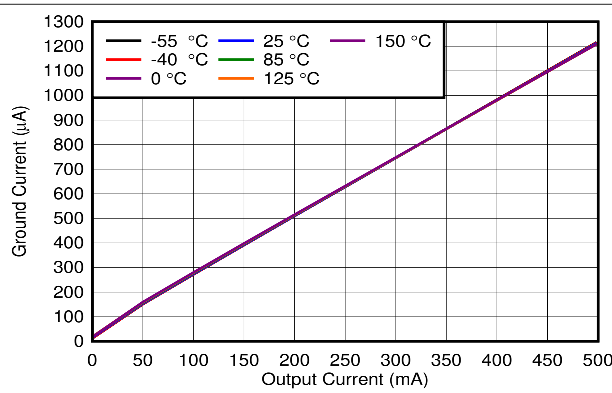


Figure 6-29. Ground Current (I_{GND}) vs I_{OUT}

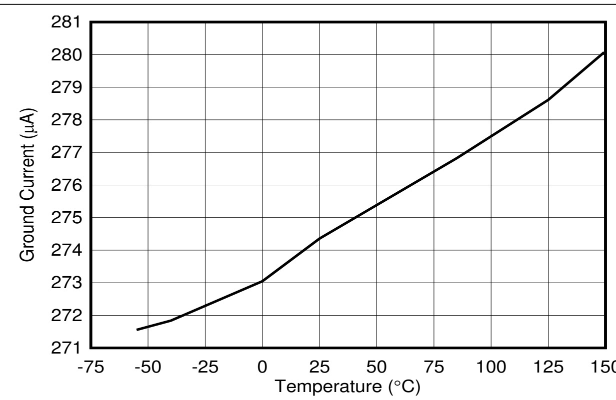


Figure 6-30. Ground Current at 100 mA

6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)

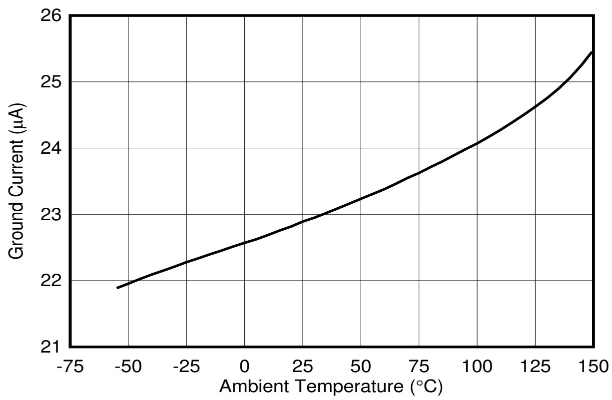


Figure 6-31. Ground Current at 500 µA

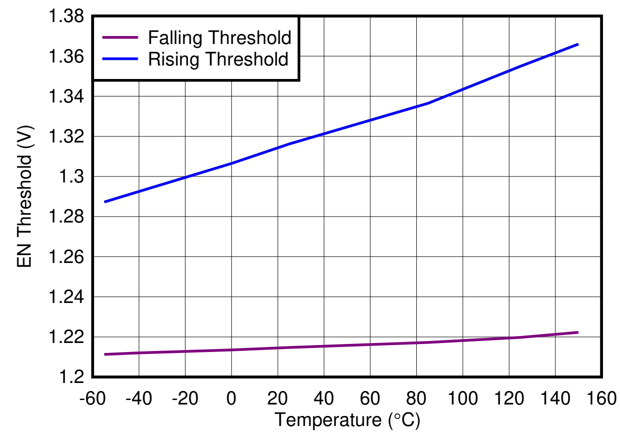


Figure 6-32. EN Threshold vs Temperature

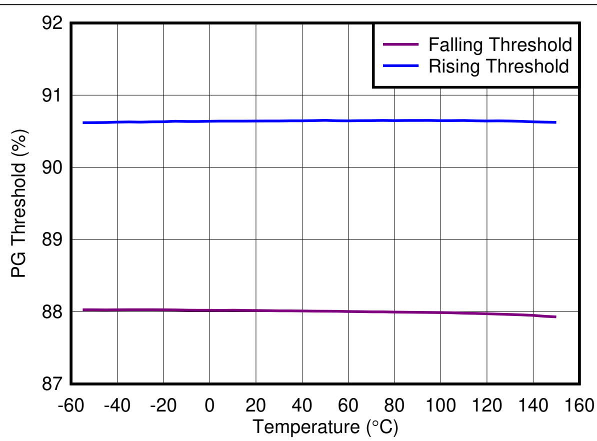
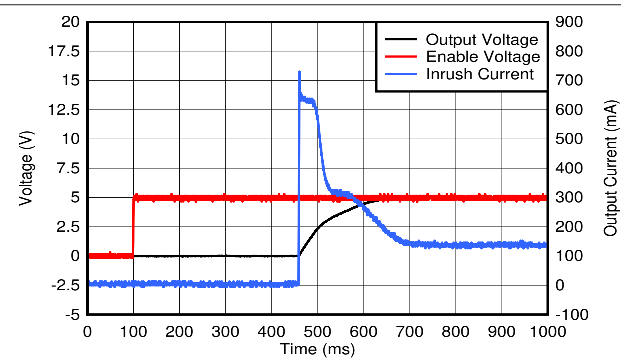


Figure 6-33. PG Threshold vs Temperature



V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 150 mA, V_{EN} = 3.3 V, C_{OUT} = 10 µF

Figure 6-34. Startup Plot Inrush Current

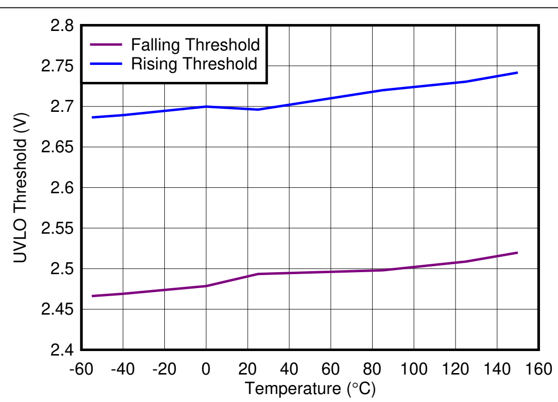
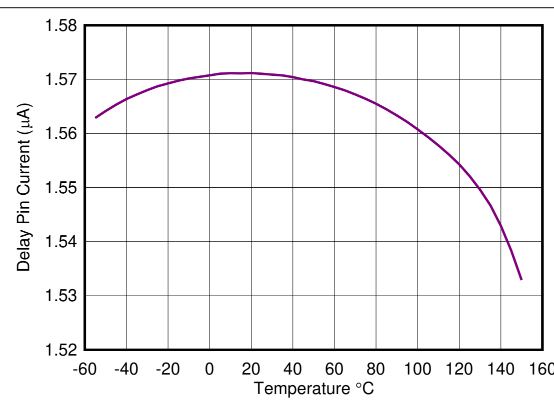


Figure 6-35. Undervoltage Lockout (UVLO) Threshold vs Temperature



V_{DELAY} = 1 V

Figure 6-36. Delay Pin Current vs Temperature

6.7 Typical Characteristics (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 2.2 µF, 1 mΩ < C_{OUT} ESR < 2 Ω, C_{IN} = 1 µF, and V_{EN} = 2 V (unless otherwise noted)

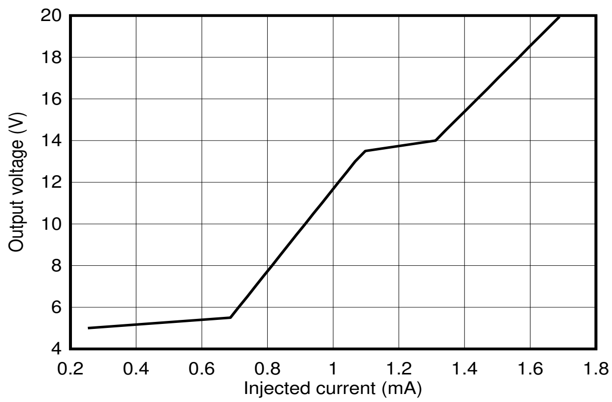


Figure 6-37. Output Voltage vs Injected Current

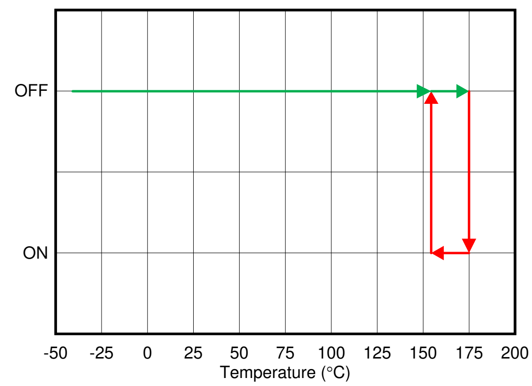


Figure 6-38. Thermal Shutdown

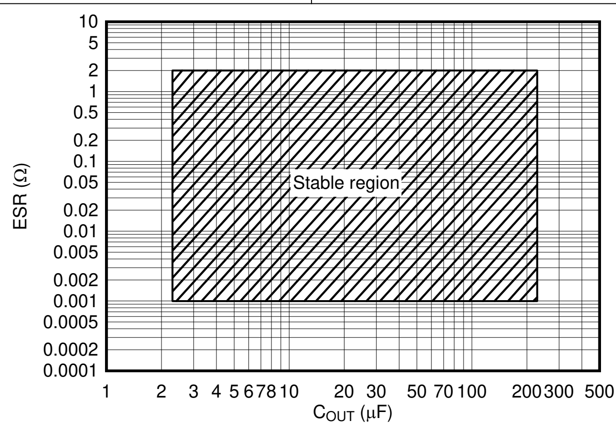


Figure 6-39. Stability, ESR vs C_{OUT}

7 Detailed Description

7.1 Overview

The TPS7B86-Q1 is a low-dropout linear regulator (LDO) with improved transient performance that allows for quick response to changes in line or load conditions. The device aslo features a novel output overshoot reduction feature that minimizes output overshoot during cold-crank conditions.

The integrated power-good and delay features allow for the system to notify down-stream components when the power is good and assist in sequencing requirements.

During normal operation, the device has a tight DC accuracy of ±0.85% over line, load, and temperature. The increased accuracy allows for the powering of sensitive analog loads or sensors.

7.2 Functional Block Diagrams

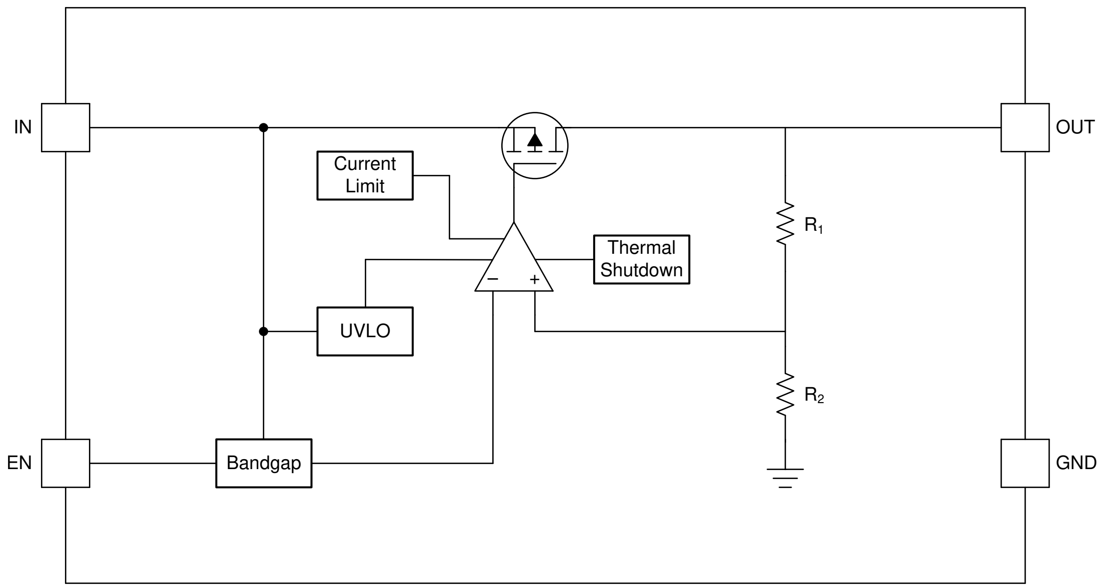


Figure 7-1. TPS7B86-Q1 Fixed Output Without PG

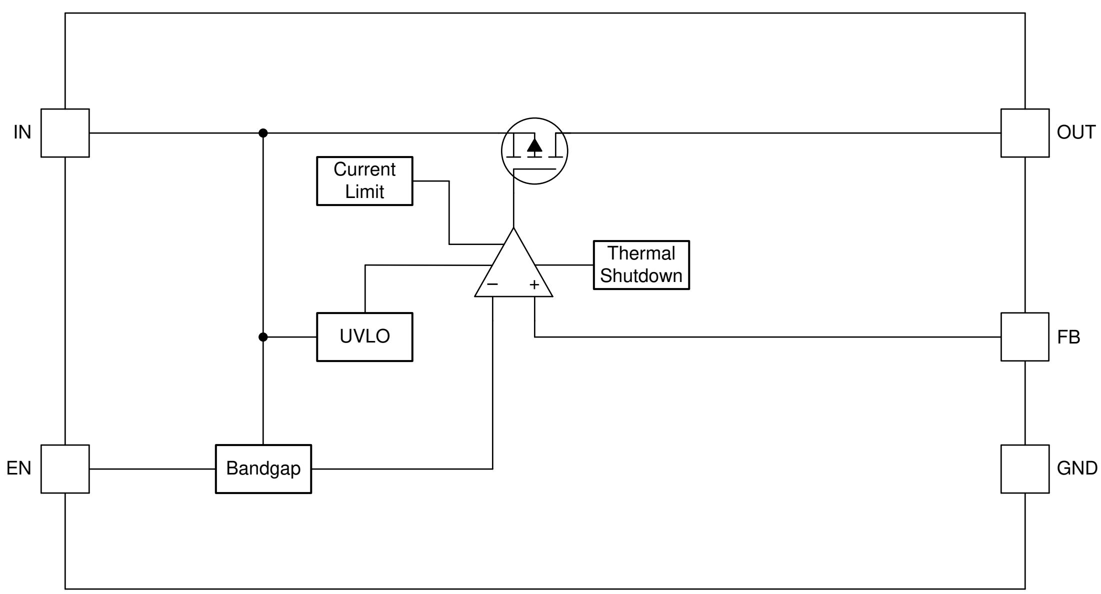


Figure 7-2. TPS7B86-Q1 Adjustable Output Without PG

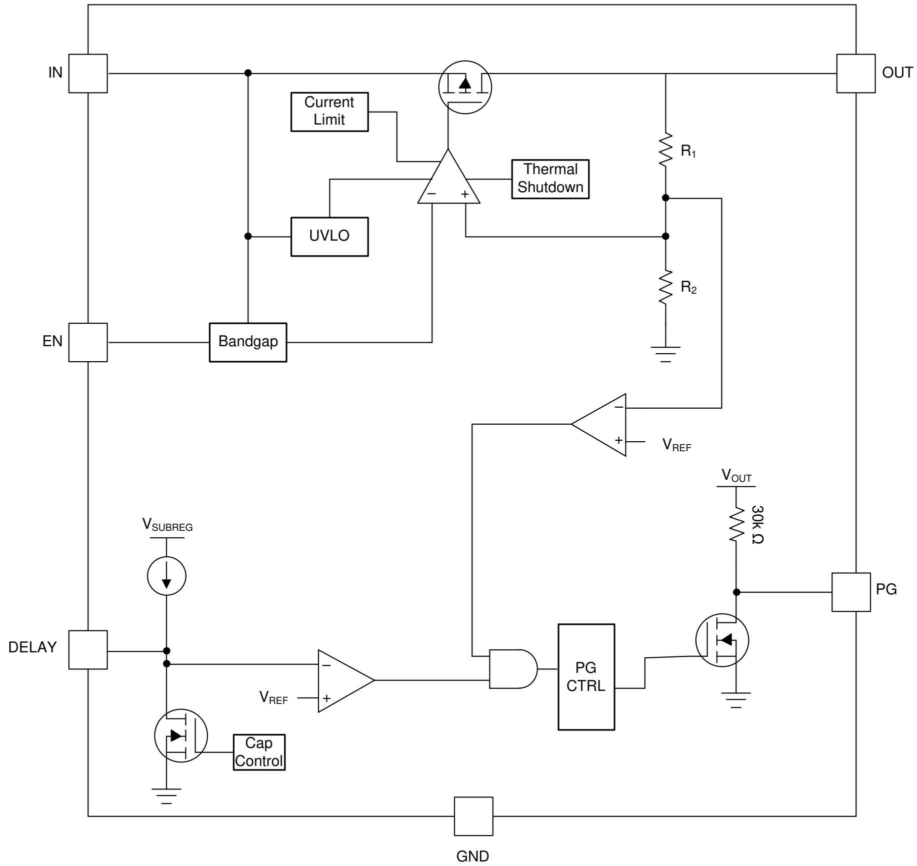


Figure 7-3. TPS7B86-Q1 With PG

7.3 Feature Description

7.3.1 Enable (EN)

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

7.3.2 Power-Good (PG)

The PG signal provides an easy solution to meet demanding sequencing requirements because PG alerts when the output nears its nominal value. PG can be used to signal other devices in a system when the output voltage is near, at, or above the set output voltage ($V_{OUT(nom)}$). Figure 7-4 shows a simplified schematic. The PG signal is an internal pullup resistor to the nominal output voltage and is active high. The PG circuit sets the PG pin into a high-impedance state to indicate that the power is good.

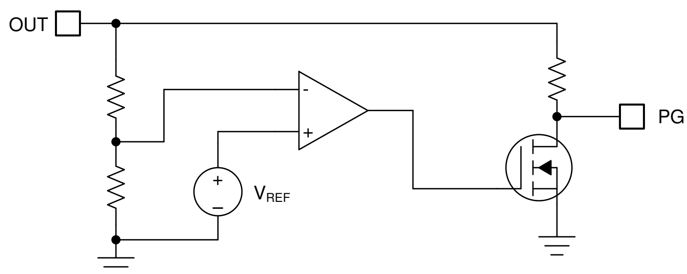
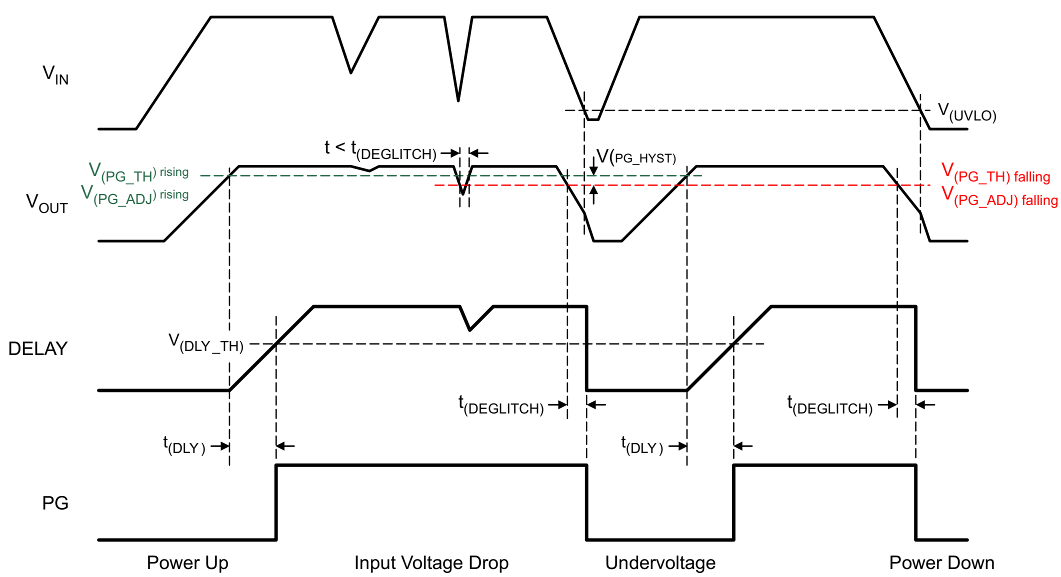


Figure 7-4. Simplified Power-Good Schematic

7.3.3 Adjustable Power-Good Delay Timer (DELAY)

The power-good delay period is a function of the external capacitor on the DELAY pin. The adjustable delay configures the amount of time required before the PG pin becomes high. This delay is configured by connecting an external capacitor from this pin to GND. Figure 7-5 shows the typical timing diagram for the power-good delay pin. If the DELAY pin is left floating, the power-good delay is $t_{(DLY\_FIX)}$. For more information on how to program the PG delay, see the *Setting the Adjustable Power-Good Delay* section.



$V_{(PG\_TH)\ falling} = V_{(PG\_TH)\ rising} – V_{(PG\_HYST)}$.

Figure 7-5. Typical Power-Good Timing Diagram

7.3.4 Undervoltage Lockout

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.6 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brickwall scheme. In a high-load current fault, the brickwall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 7-6 shows a diagram of the current limit.

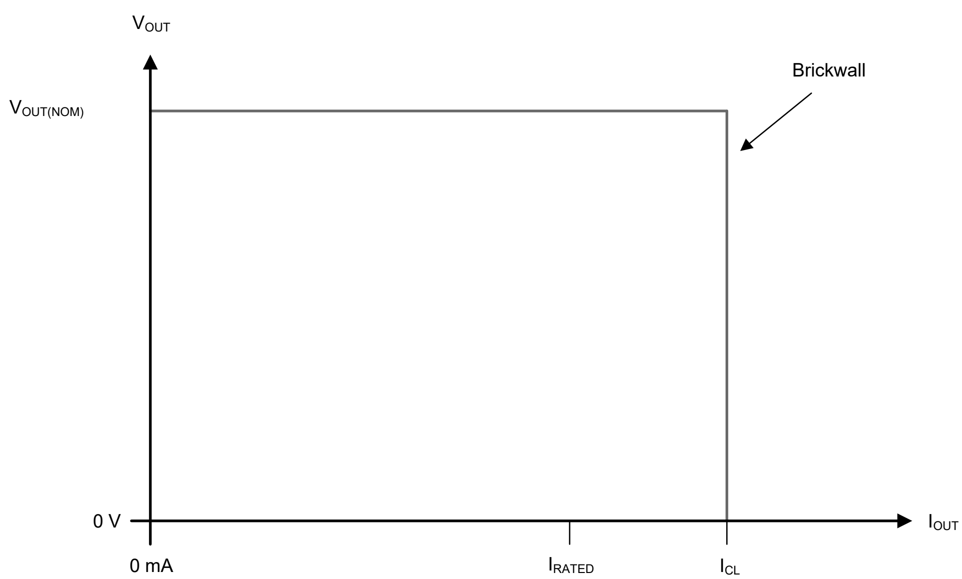


Figure 7-6. Current Limit

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shutdown.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Selection

The TPS7B86-Q1 requires an output capacitor of 2.2 µF or larger (1 µF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001 Ω and 2 Ω. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.1.2 Adjustable Device Feedback Resistor Selection

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (1)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \le V_{OUT} / (I_{FB} \times 100) \quad (2)$$

8.1.3 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the startup time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (3)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \,||\, R_2)) \quad (4)$$

8.1.4 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{5}$$

8.1.5 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

8.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \tag{6}$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{7}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.6.1 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table in the *Specifications* section is determined by the JEDEC standard (as shown in Figure 8-1), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

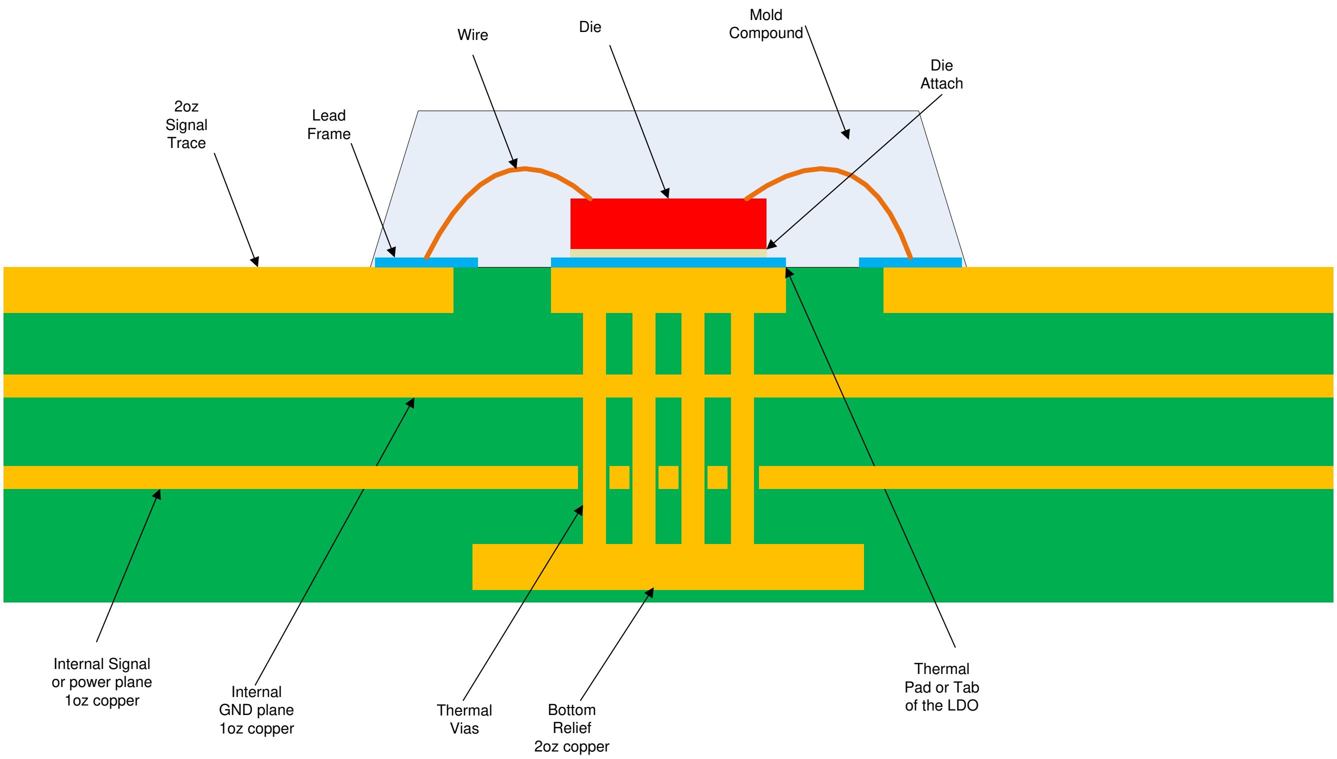


Figure 8-1. JEDEC Standard 2s2p PCB

Figure 8-2 through Figure 8-5 illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness. These plots are generated with a 101.6-mm x 101.6-mm x 1.6-mm PCB of two and four layers. For the 4-layer board, inner planes use 1-oz copper thickness. Outer layers are simulated with both 1-oz and 2-oz copper thickness. A 2x3 (DDA package) or a 3x4 (KVU package) array of thermal vias with a 300-µm drill diameter and 25-µm copper plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

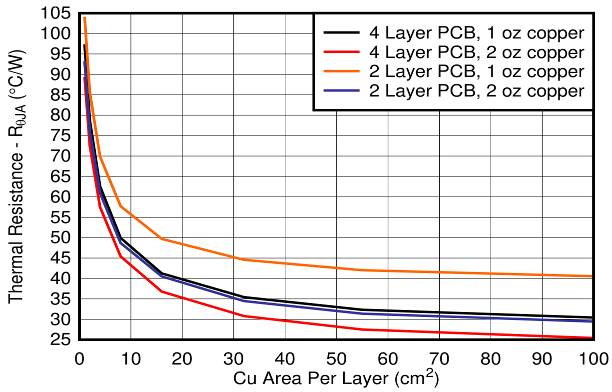


Figure 8-2. $R_{\theta JA}$ vs Copper Area (DDA Package)

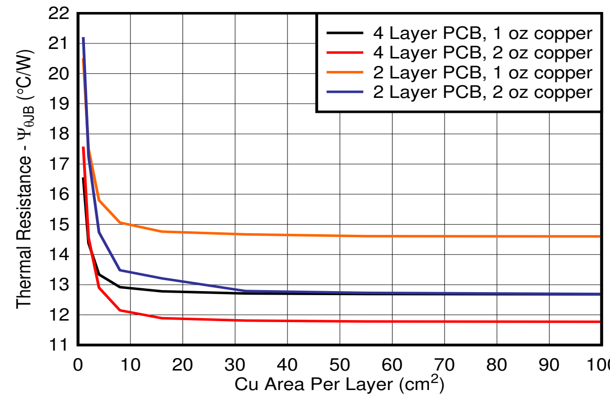


Figure 8-3. Ψ_{JB} vs Copper Area (DDA Package)

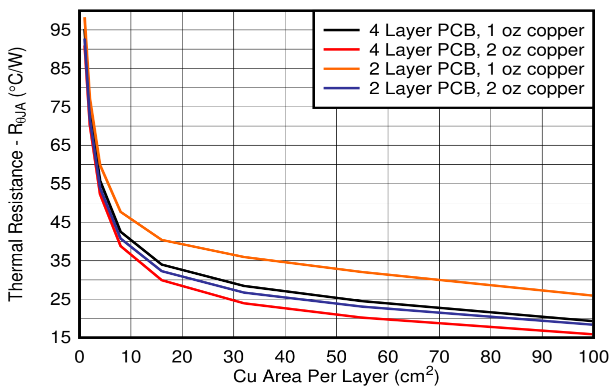


Figure 8-4. $R_{\theta JA}$ vs Copper Area (KVU Package)

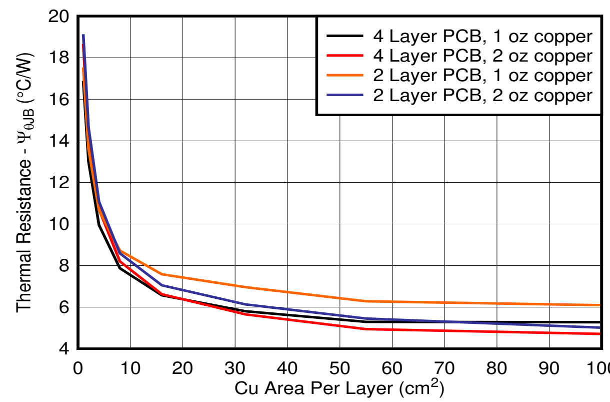


Figure 8-5. Ψ_{JB} vs Copper Area (KVU Package)

8.1.6.2 Power Dissipation Versus Ambient Temperature

Figure 8-6 is based off of a JESD51-7 4-layer, high-K board. The allowable power dissipation was estimated using the following equation. As disscussed in the *An empirical analysis of the impact of board layout on LDO thermal performance* application report, thermal dissipation can be improved in the JEDEC high-K layout by adding top layer copper and increasing the number of thermal vias. If a good thermal layout is used, the allowable thermal dissipation can be improved by up to 50%.

$$T_A + R_{\theta JA}\, x\, P_D \leq 150\ °C \tag{8}$$

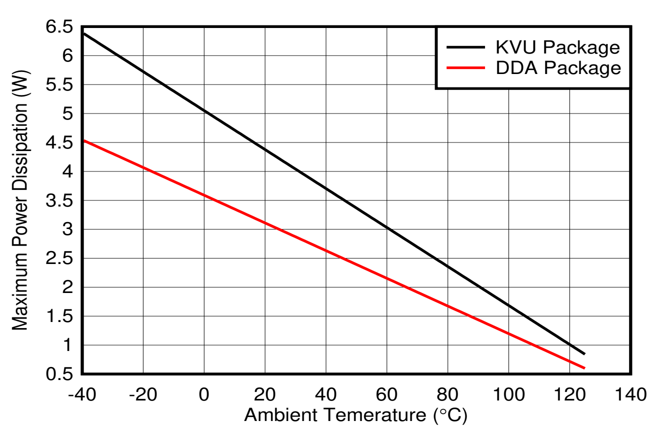


Figure 8-6. TPS7B86-Q1 Allowable Power Dissipation

8.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.1.8 Pulling Up the PG Pin to a Different Voltage

Because the power-good (PG) pin is pulled up internally to the output rail, this pin cannot be pulled up to any voltage or wire AND'd like a typical open-drain PG output can be. If this signal must be pulled up to another logic level then an external circuit can be implemented using a PMOS transistor and a pullup resistor. Implementing the circuit shown in Figure 8-7 allows the outputs to be pulled up to any logic rail. If a PMOS transistor is used make sure to pick a transistor with a low threshold voltage as this will determine the output low voltage. this can also be done with a NMOS transistor, but it inverts the logic. This implementation also allows the outputs to be AND'd together like the traditional power-good pins.

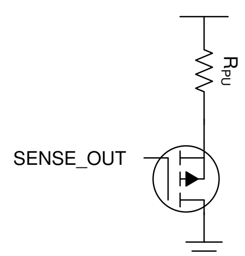


Figure 8-7. Additional Components for the PG Pin to be Pulled Up to Another Rail

8.1.9 Power-Good

8.1.9.1 Setting the Adjustable Power-Good Delay

The power-good delay time can be set in two ways: either by floating the DELAY pin or by connecting a capacitor from this pin to GND. When the DELAY pin is floating, the time defaults to $t_{(DLY\_FIX)}$. The delay time is set by the following equation if a capacitor is connected between the DELAY pin and GND.

$$t = t_{(DLY\_FIX)} + C_{DELAY}\left(\frac{V_{DLY(TH)}}{I_{DLY(CHARGE)}}\right) \quad (11)$$

8.2 Typical Application

Figure 8-8 shows a typical application circuit for the TPS7B86-Q1. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

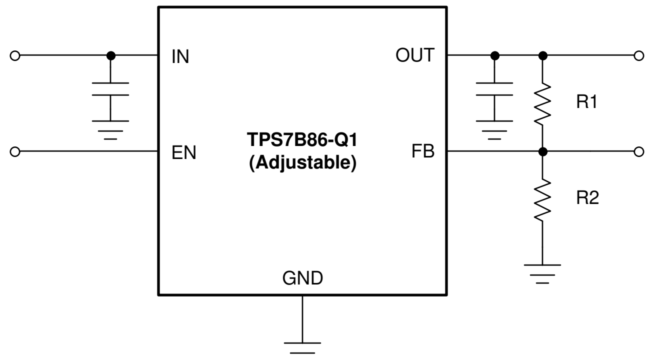


Figure 8-8. Typical Application Schematic for the TPS7B86-Q1

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6 V to 40 V
Output voltage	5 V
Output current	350 mA
Output capacitor	10 µF

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 1 µF. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value must be between 2.2 µF and 200 µF and the ESR range must be between 1 mΩ and 2 Ω. For this design, a low ESR, 10-µF ceramic capacitor was used to improve transient performance.

8.2.3 Application Curves

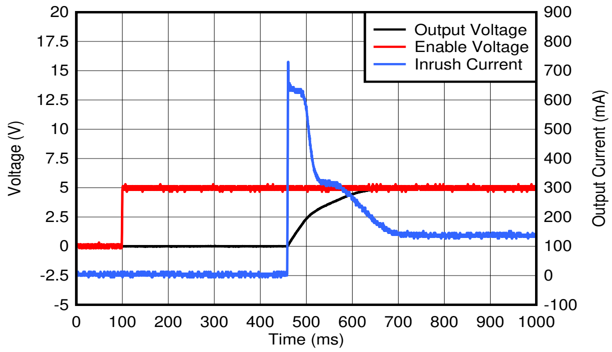


Figure 8-9. Power-Up Waveform With EN

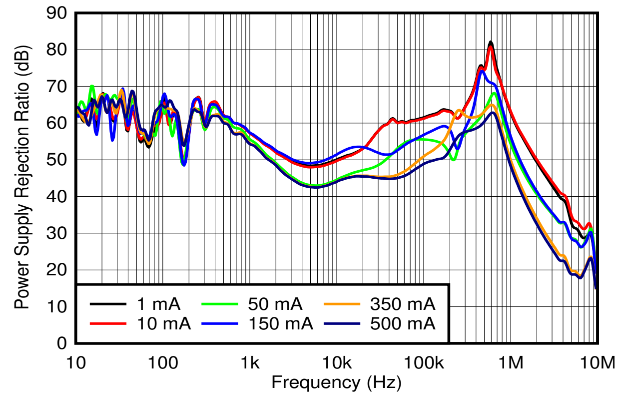


Figure 8-10. PSRR

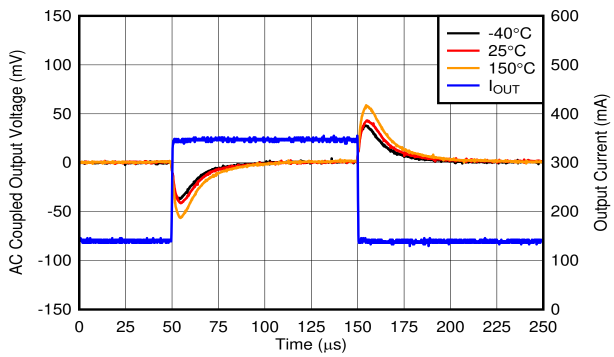


Figure 8-11. Transient Response

9 Power Supply Recommendations

This device is designed for operation from an input voltage supply with a range between 3 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B86-Q1, add an electrolytic capacitor with a value of 22 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. TI also recommends a ground reference plane either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

10.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7B86-Q1 are available at the end of this document and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

As depicted in Figure 10-1 and Figure 10-2 , place the input and output capacitors close to the device for the layout of the TPS7B86-Q1. In order to enhance the thermal performance, place as many vias as possible around the device. These vias improve the heat transfer between the different GND planes in the PCB.

To improve AC performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place each capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces to connect the capacitors because may negatively affect system performance and even cause instability.

If possible, and to ensure the maximum performance specified in this document, use the same layout pattern used for the TPS7B86-Q1 evaluation board, available at www.ti.com.

10.2 Layout Examples

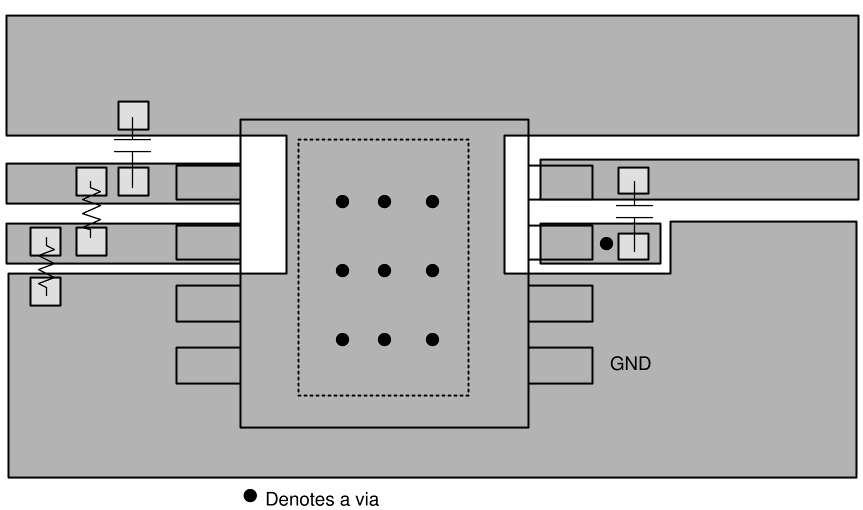
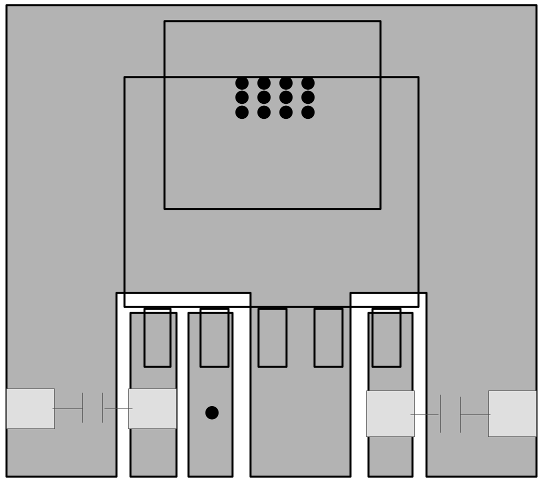


Figure 10-1. DDA Package Adjusable Output



● Denotes a via

Figure 10-2. KVU Package Fixed Outupt

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Table 11-1. Device Nomenclature (1)

PRODUCT	V_{OUT}
TPS7B86**xx** **z**Q**yyy**RQ1	**xx** is the nominal output voltage (for example, 33 = 3.3 V V; 50 = 5.0 V; 01 = adjustable). **z** indicates the version of the device no letter here indicates a device without power-good. B indicates a device with power-good. **yyy** is the package designator. **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

11.1.2 Development Support

For the PSpice model, see the TPS7B4250 PSpice Transient Model.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Various Applications for Voltage-Tracking LDO* application report
- Texas Instruments, *TPS7B4250 Evaluation Module* user's guide
- Texas Instruments, *TPS7B5250-Q1 Pin FMEA* application report

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B8601QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	7B8601	Samples
TPS7B8633QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	7B8633	Samples
TPS7B8633QKVURQ1	ACTIVE	TO-252	KVU	5	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	7B8633	Samples
TPS7B8650QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	7B8650	Samples
TPS7B8650QKVURQ1	ACTIVE	TO-252	KVU	5	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	7B8650	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

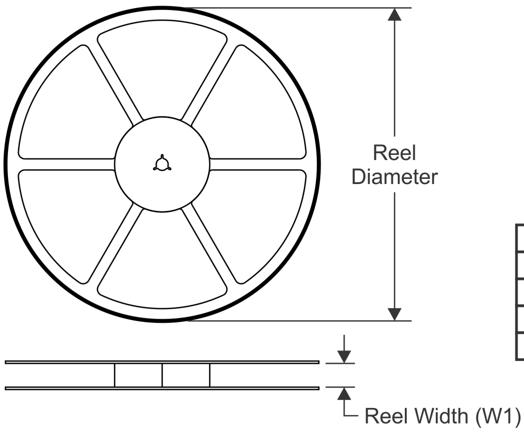
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

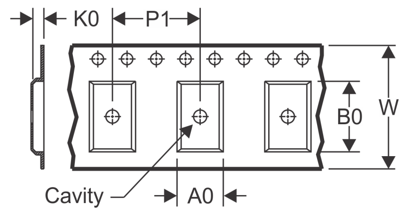
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

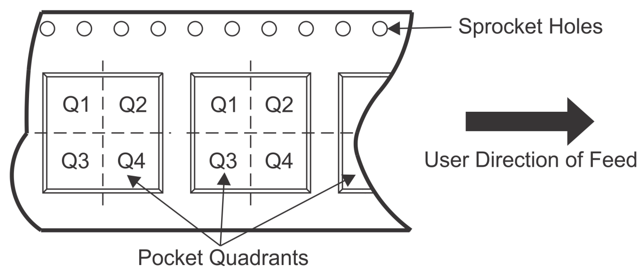


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

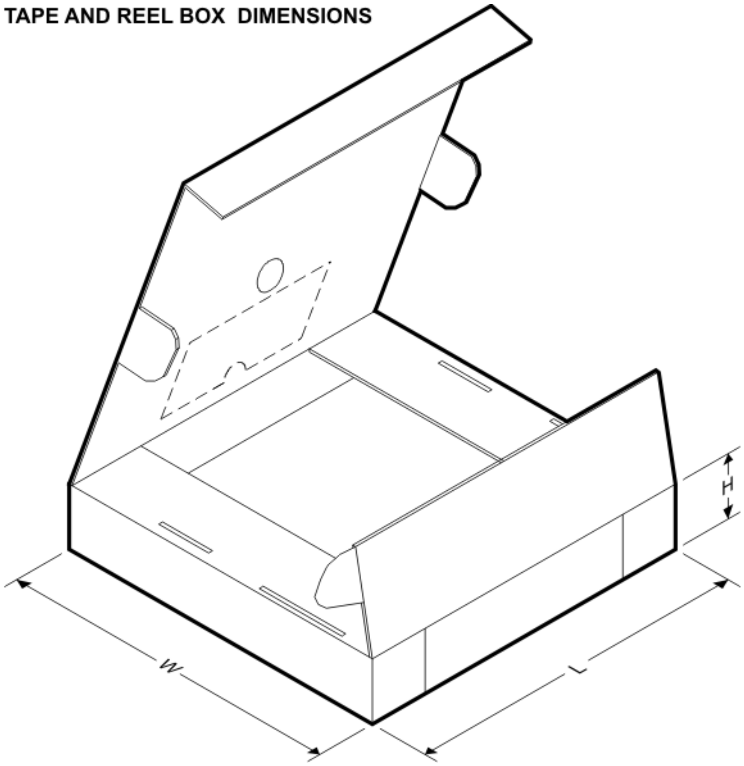
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8601QDDARQ1	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS7B8633QDDARQ1	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS7B8650QDDARQ1	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

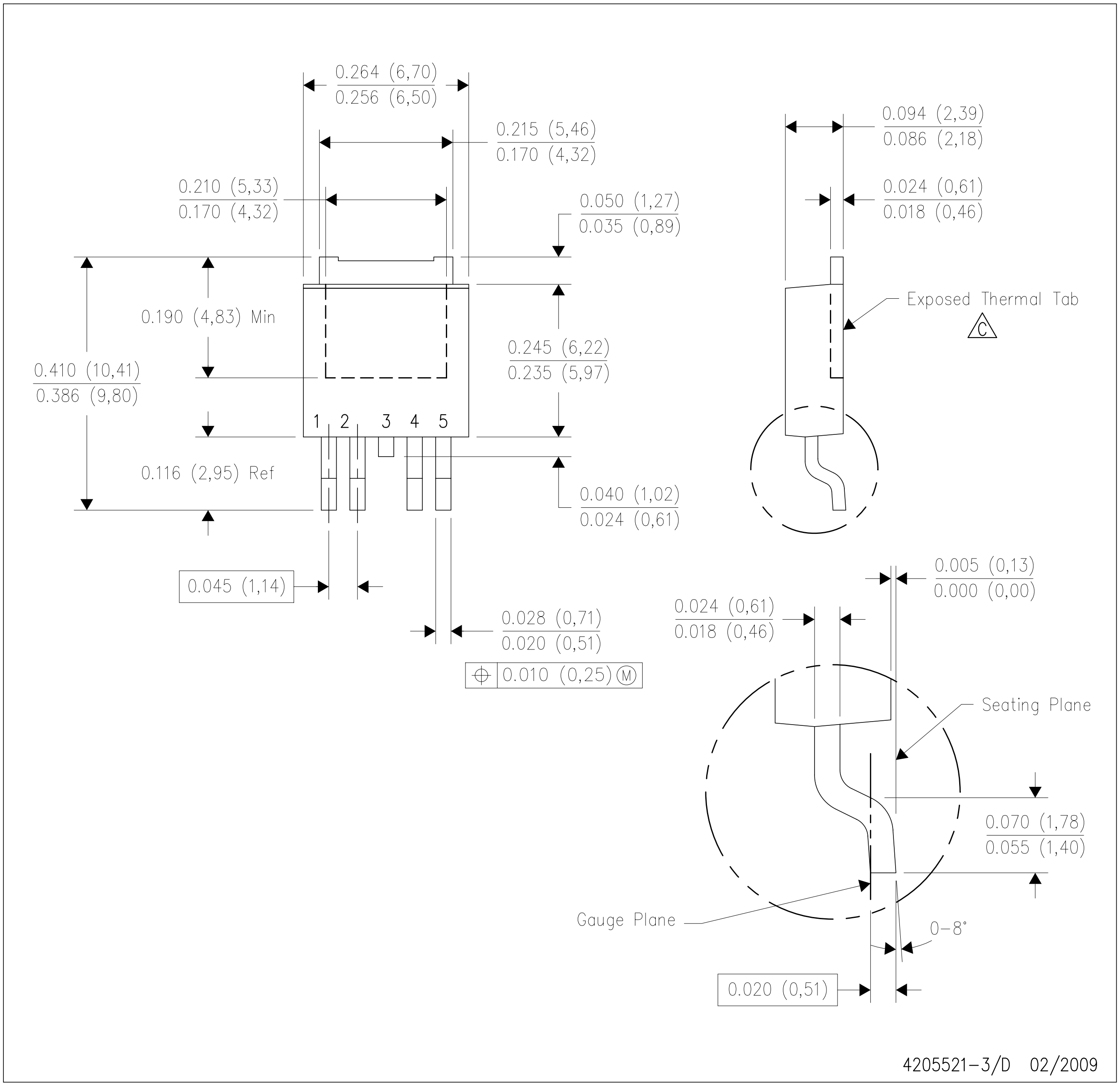
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

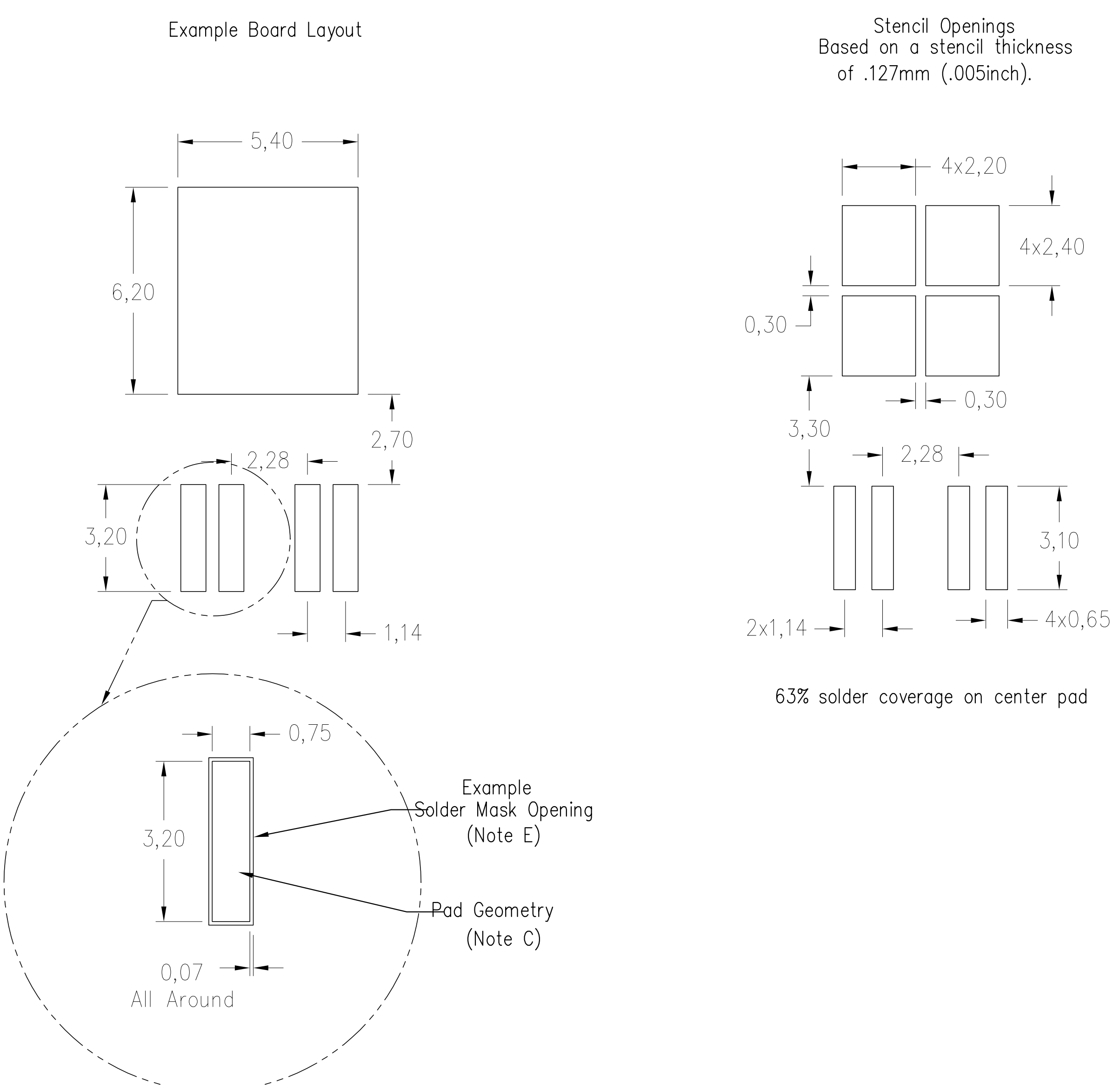
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8601QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS7B8633QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS7B8650QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

KVU (R-PSFM-G5) PLASTIC FLANGE-MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. The center lead is in electrical contact with the exposed thermal tab.
- D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
- E. Falls within JEDEC TO-252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

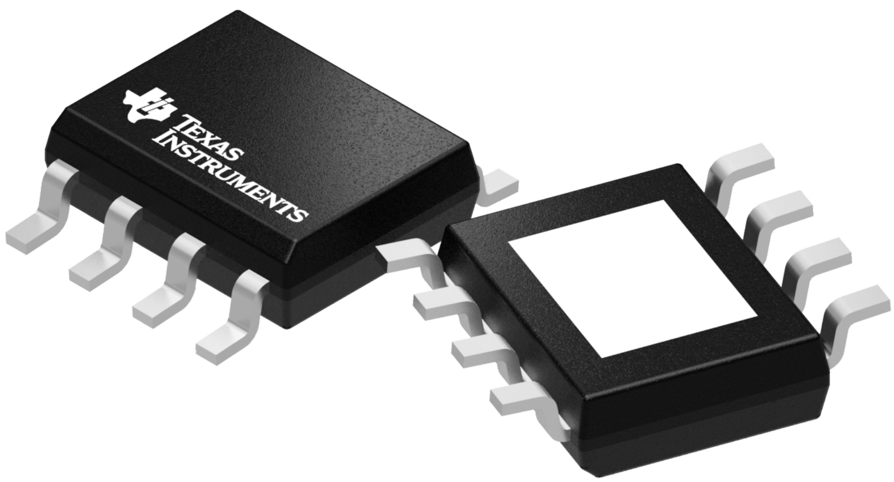


4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

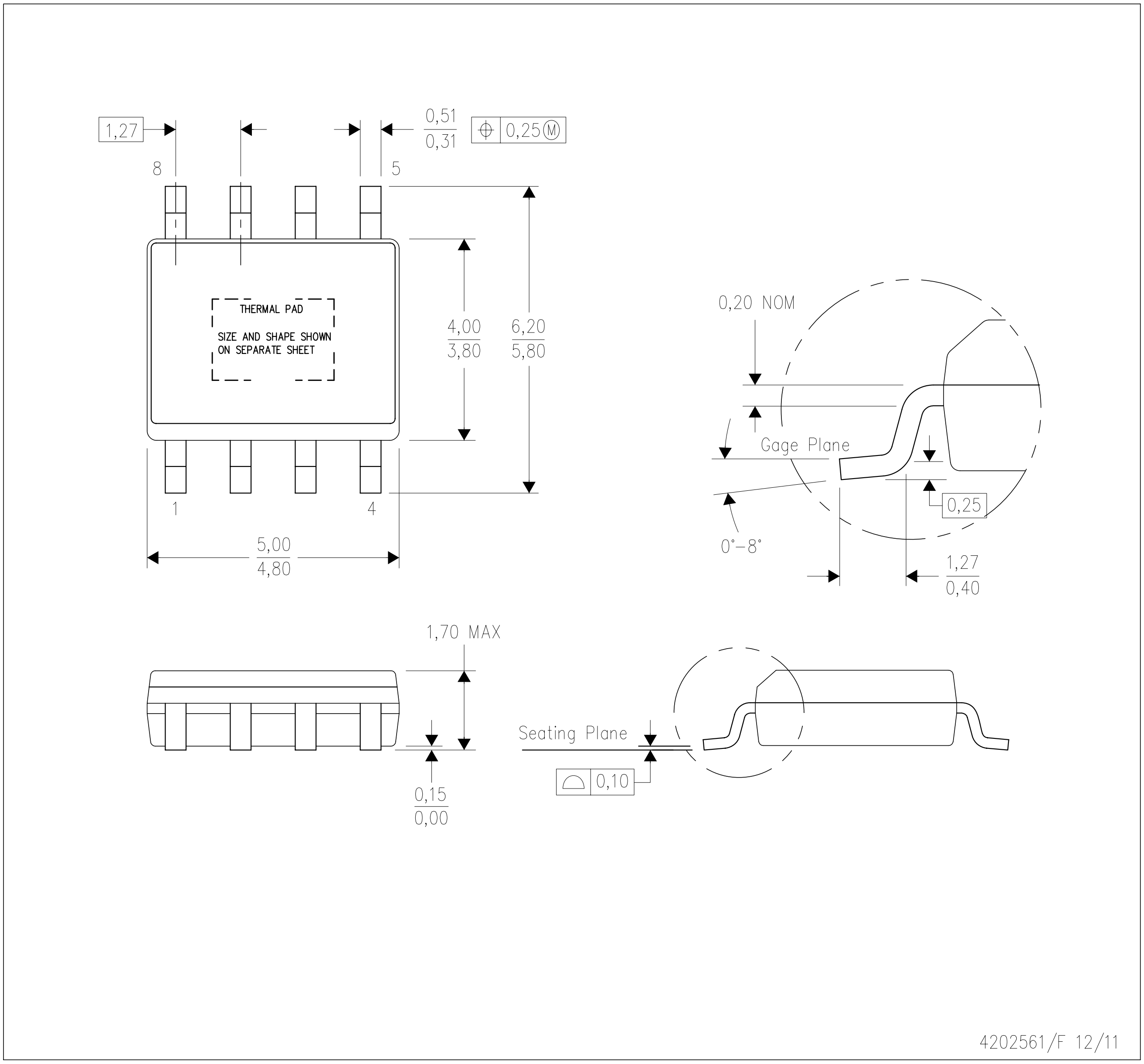
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4202561/G

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

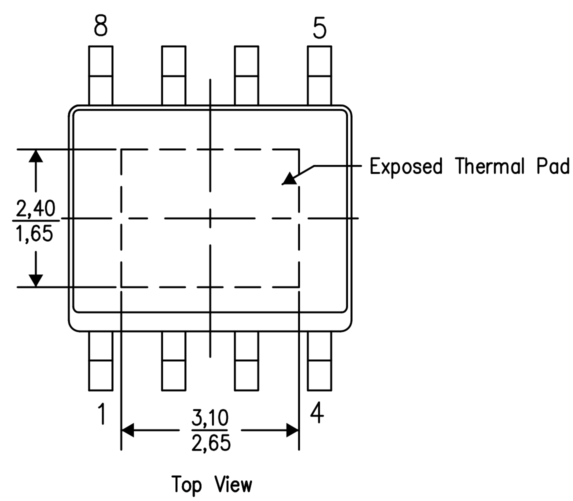
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

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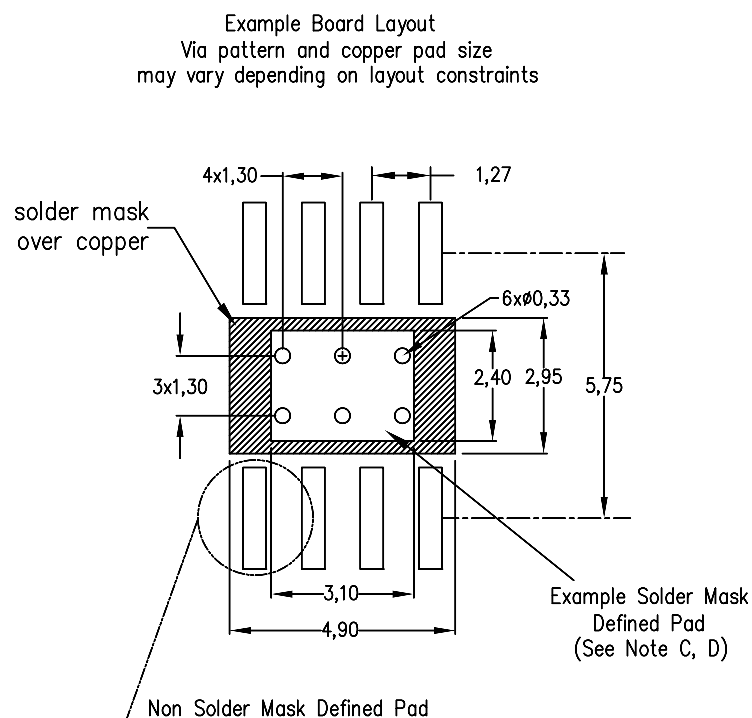
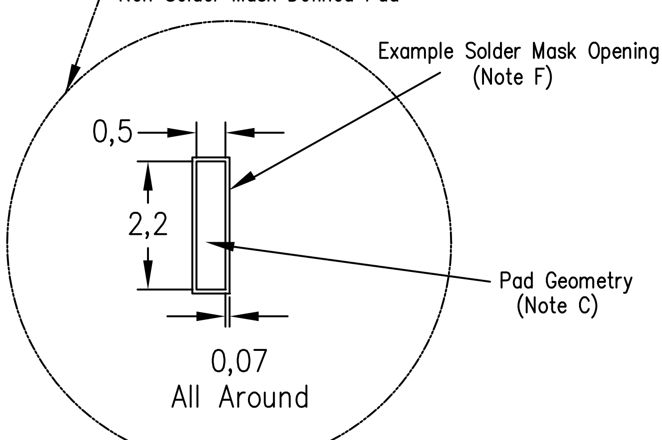
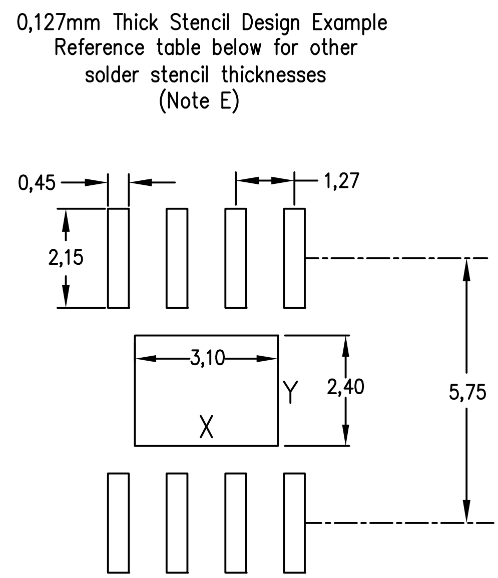
NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE







Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

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