



PEOPLE'S DEMOCRATIC REPUBLIC OF ALGERIA  
UNIVERSITY OF M'HEMED BOUGARA BOUMERDES  
INSTITUTE OF ELECTRICAL AND ELECTRONICS  
ENGINEERING

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**Advanced Digital Systems**

LAB #2

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# 1 Introduction

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## 2 Tools and Software

1. First itemtext
2. Second itemtext
3. Last itemtext
4. First itemtext

## 3 Part I: bla bla bla

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This is some VHDL code:

```
0  -- import std_logic from the IEEE library
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3  entity ANDGATE is
4      port (
5          I1 : in std_logic;
6          O  : out std_logic);
7  end entity ANDGATE;
8
9  architecture RTL of ANDGATE is
10 begin
11     O <= I1 ; -- this is a comment
12 end architecture RTL;
```

"Title here"

```

0  library IEEE;
1  Use IEEE.std_logic_1164.all;
2  Use IEEE.numeric_std.all;
3
4  entity FSM_Mealy is
5      port (
6          w, clk, rst : in std_logic;
7          y           : out std_logic
8      );
9  end FSM_Mealy;
10
11
12  architecture logic of FSM_Mealy is
13      TYPE state_type is (A,B,C,D,E);
14      signal current_state : state_type;
15  begin
16
17      FSM_PROC1 : process(clk, w, rst)
18      begin
19          if rst = '1' then current_state <= A;
20          elsif falling_edge(clk) then
21              case current_state is
22                  when A => if w = '0' then current_state <= B;
23                           else current_state <= A end if;
24                  when B => if w = '0' then current_state <= B;
25                           else current_state <= C end if;
26                  when C => if w = '0' then current_state <= D;
27                           else current_state <= A end if;
28                  when D => if w = '0' then current_state <= B;
29                           else current_state <= E end if;
30                  when E => if w = '0' then current_state <= D;
31                           else current_state <= A end if;
32              end if;
33          end process;
34
35          y <= '1' when (current_state = E and w = '1') else '0';
36
37  end architecture;

```

"Mealy FSM"

## 4 Conclusion

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