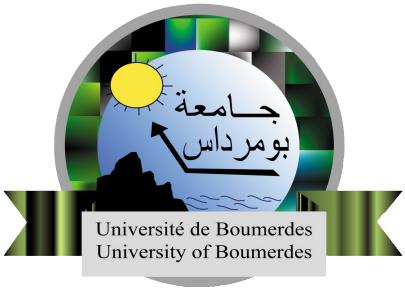

PEOPLE'S DEMOCRATIC REPUBLIC OF ALGERIA
UNIVERSITY OF M'HEMED BOUGARA BOUMERDES

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERING

Advanced Digital Systems

LAB #2

OCTOBER 30, 2021

Authors

Madaoui Zakaria	Group 2
Lariane Sidali	Group 2

Instructor: Dr. A. benzekri

Contents

1 Introduction

Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Ut purus elit, vestibulum ut, placerat ac, adipiscing vitae, felis. Curabitur dictum gravida mauris. Nam arcu libero, nonummy eget, consectetuer id, vulputate a, magna. Donec vehicula augue eu neque. Pellentesque habitant morbi tristique senectus et netus et malesuada fames ac turpis egestas. Mauris ut leo. Cras viverra metus rhoncus sem. Nulla et lectus vestibulum urna fringilla ultrices. Phasellus eu tellus sit amet tortor gravida placerat. Integer sapien est, iaculis in, pretium quis, viverra ac, nunc. Praesent eget sem vel leo ultrices bibendum. Aenean faucibus. Morbi dolor nulla, malesuada eu, pulvinar at, mollis ac, nulla. Curabitur auctor semper nulla. Donec varius orci eget risus. Duis nibh mi, congue eu, accumsan eleifend, sagittis quis, diam. Duis eget orci sit amet orci dignissim rutrum.

2 Tools and Software

1. First itemtext
2. Second itemtext
3. Last itemtext
4. First itemtext

3 Part I: bla bla bla

Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Ut purus elit, vestibulum ut, placerat ac, adipiscing vitae, felis. Curabitur dictum gravida mauris. Nam arcu libero, nonummy eget, consectetuer id, vulputate a, magna. Donec vehicula augue eu neque. Pellentesque habitant morbi tristique senectus et netus et malesuada fames ac turpis egestas. Mauris ut leo. Cras viverra metus rhoncus sem. Nulla et lectus vestibulum urna fringilla ultrices. Phasellus eu tellus sit amet tortor gravida placerat. Integer sapien est, iaculis in, pretium quis, viverra ac, nunc. Praesent eget sem vel leo ultrices bibendum. Aenean faucibus. Morbi dolor nulla, malesuada eu, pulvinar at, mollis ac, nulla. Curabitur auctor semper nulla. Donec varius orci eget risus. Duis nibh mi, congue eu, accumsan eleifend, sagittis quis, diam. Duis eget orci sit amet orci dignissim rutrum.

This is some VHDL code:

```
0  -- import std_logic from the IEEE library
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3  entity ANDGATE is
4    port (
5      I1 : in std_logic;
6      O  : out std_logic);
7  end entity ANDGATE;
8
9  architecture RTL of ANDGATE is
10 begin
11   O <= I1 ; -- this is a comment
12 end architecture RTL;
13
```

"Title here"

```
library IEEE;
Use IEEE.std_logic_1164.all;
Use IEEE.numeric_std.all;

entity FSM_Mealy is
    port (
        w, clk, rst : in std_logic;
        y      : out std_logic
    );
end FSM_Mealy;


architecture logic of FSM_Mealy is
    TYPE state_type is (A,B,C,D,E);
    signal current_state : state_type;
begin

    FSM_PROC1 : process(clk, w, rst)
    begin
        if rst = '1' then current_state <= A;
        elsif falling_edge(clk) then
            case current_state is
                when A => if w = '0' then current_state <= B;
                          else current_state <= A end if;
                when B => if w = '0' then current_state <= B;
                          else current_state <= C end if;
                when C => if w = '0' then current_state <= D;
                          else current_state <= A end if;
                when D => if w = '0' then current_state <= B;
                          else current_state <= E end if;
                when E => if w = '0' then current_state <= D;
                          else current_state <= A end if;
        end if;
    end process;

    y <= '1' when (current_state = E and w = '1') else '0';

end architecture;
```

"Mealy FSM"

4 Conclusion

Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Ut purus elit, vestibulum ut, placerat ac, adipiscing vitae, felis. Curabitur dictum gravida mauris. Nam arcu libero, nonummy eget, consectetuer id, vulputate a, magna. Donec vehicula augue eu neque. Pellentesque habitant morbi tristique senectus et netus et malesuada fames ac turpis egestas. Mauris ut leo. Cras viverra metus rhoncus sem. Nulla et lectus vestibulum urna fringilla

ultrices. Phasellus eu tellus sit amet tortor gravida placerat. Integer sapien est, iaculis in, pretium quis, viverra ac, nunc. Praesent eget sem vel leo ultrices bibendum. Aenean faucibus. Morbi dolor nulla, malesuada eu, pulvinar at, mollis ac, nulla. Curabitur auctor semper nulla. Donec varius orci eget risus. Duis nibh mi, congue eu, accumsan eleifend, sagittis quis, diam. Duis eget orci sit amet orci dignissim rutrum.