SAKINDER ALI

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Firmware Engineer with 8 years of experience working with FPGA's, CPLD's and Zynq technologies. Significant experience with implementation of digital systems. Excellent interpersonal and communication abilities, and possess a wide range of technical skills. Enjoys being part of a team, as managing, motivating and training a productive team and thrives in high pressure and challenging working environments.

Experience

Principal Engineer Mar 2020 - Present
Northrop Grumman, Baltimore, MD (US)

Created custom bus agent in uvm environment which verify dut through coverage reports.
Updated RTL design for Microsemi Igloo2 FPGA and migrated traditional vhdl testbench into uvm environment (System Verilog) and verified it through coverage reports. Updated verification plan document according to verification requirement vs met coverages.

Verified various design with help of team members.

Specialist Electrical Engineer May 2019 - Feb 2020
L3Harris, Columbia, MD (US)

Worked on cryptographic transmission security (TRANSEC) verification using System Verilog and Universal Verification Methods (UVM).
Wrote verification design document for the TRANSEC component of provided waveform.

Senior Electrical Engineer Nov 2017 - May 2019
Raytheon Missiles & Defense, Tucson, AZ (US)

Design, verification and implementation of VHDL modules.
RTL design and development from the concept to production for Microsemi Igloo2 FPGA.
System integration test and verification from CCA down to the FPGA design.

Participated daily Scrum meeting.

Senior Firmware Engineer Jul 2017 - Nov 2017
FAST FIT TECHNOLOGIES, CONSULTANT

Rewrite and add features to already developed algorithms for Kernel [FPGA based accelerator] using OpenCL on Intel-Altera Platform. Debug for functionality, performance and optimize for OpenCL acceleration design, provide demonstrations and proofs of concepts.

Senior Electrical Engineer Sep 2016 - Jul 2017
LYNNTECH, COLLEGE STATION

Wrote technical proposal "Network Isolation of Industrial Control System (ICS) Devices via Permanent Host Identifiers" Solicitation Number OSD172-DI4. Endorsed by Raytheon IDS.

Developed external memory [QDR] Interface through MIG for imaging/video-based technology to improve detection algorithms and performance for small maritime targets for both commercial and military applications. Designed and development various AXI-interface IPS and test software for local (PL) and arm (PS)

communications within the ZYNQ chip. Implemented and tested camera [FLIR] interface to VDMA which includes node map address mapping core/pixel buffer sync core/camera link buffer core/camera link buffer core functional and hardware test.

Customized LWIP TCP/IP stack protocol library and created raw and socket mode applications for webserver on ZYNQ [ZC7020 Ethernet interface and the PS-DDR]. Developed client user interface and controls with the hardware server platform, which visualized the adc data results in real time. Further application was used for testing and debugging the hardware and software.

Prepared daily status, weekly and monthly reports related to firmware development to management and customer. Proposed various solutions for new designs from concept to implantation.

ELECTRONIC DESIGN ENGINEER, ENGINEER Jan 2012 - Sep 2016
GENERAL ELECTRIC, ERIE

Prepared and implemented test protocols and test cases based on product specifications. Provided support to other departments, performed troubleshoots and identified the cause of malfunction. Coordinated with the ohv team members and ensured that the tests were performed per the specification given for the product. Tested, assessed, and modified existing software system to improve performance. Prepared the test software and ensured that it was compatible with the product certification requirements. Checked the components and identified the cause of malfunction and resolved them. Developed generic test cases and debugged the functional failures.

Completed RTL implementation, timing improvement of new design for FPGA[Kintex]. Completed axi4 drivers for communication between FPGA and ARM[A9]. Created a detailed test-plan to verify the analog channels timing from FPGA to arm through axi4lite bus per the test plan. Created ADS8568 model in RTL using VHDL for test software written in C for ZYNQ design. Participated in verification of compliance processes of all VHDL products. Conducted system, unit and integration testing for VHDL products. Written assertions, code coverage modules, functional coverage modules and toggle coverage modules to ensure 100% verification.

Completed SPI, UART and AXI4 low-level drivers. Completed analog filtering, detection and proposed algorithms application's in C ARM- CORTEX-A9[ZYNQ]. Performed software integration and conducted software code reviews, as required. Designed specification of generic interrupt request (IRQ) controller.

Created and implemented test software for automated testing and validation. Created panel test to ensure proper backplane communication between Zynq card and master card. Implemented software requirements and proposed algorithms for system functionality. Prepared and implemented test protocols and test cases based on product specifications. Provided support to other departments, performed troubleshoots and iden

Electrical Engineer Part-time Aug 2011 - Oct 2011
Howard Hughes Medical Institute, Ashburn, VA (US)

Designed new PC boards and created Component Libraries used in schematic and printed circuit board development utilizing Eagle Layout and Eagle Capture tools. Developed and documented test plans and procedures - Designed test fixtures. Redesigned & modified numerous existing products to improve performance. Development of test hardware interfaces to final products. Performed different type of testing on hardware to ensure that hardware is error free.

Electrical Engineer Part-time Jan 2009 - Dec 2009

Axis Engineering Technologies, College Park, MD (US)

Designed and development of various HDL modules using Xilinx Spartan III FPGA board Transforming Matlab algorithmic code into FPGA Design Test benches were written for top level module as well all the sub modules to carry out functional as well as timing simulation. Designed up to date digital circuit board and interface to attain high quality diagnostics of the system.

Electrical Engineer Coop Jan 2008 - Aug 2008

Chesapeake Sciences Corporation, Millersville, MD (US)

Developed block diagrams, schematics and printed circuit boards of digital designs. Models and simulates VHDL designs; validates designs with test benches. Performed basic circuit simulation. Worked on CAD design tools (Cadence design suite)/bills of materials (BOMs) and maintain CAD libraries. Worked with software and hardware engineers to integrate the work of different disciplines. Designed printed circuit boards using OrCADs Capture and Layout software for prototype Designs Electrical circuit testing to ensure quality level of performance. Debugged analog and digital circuits and designed troubleshooting systems for circuit board malfunctions. Created schematics and process flow diagrams for control units and communication systems. Review bug reports from the test technicians for errors prior to them being entered into the tracking hardware.

Skills & Specialization

RTOS, Motorola, PL, Layout, Simulation, Vhdl, Type, LANGUAGES, Controller, Specification, Debugging, C TOOLS, COM, CA, Software Design, Logic, Flash, Troubleshoot, Hardware, Features, JavaScript, Quality, Technical Manuals, Risk Management, OrCAD, Process Improvement, Transportation, Schematics, C, DOCUMENTATION, Basic, Matlab, Proposal, TCL, Real Time, Designing, Ethernet, Content, Video, Quality Improvement, Written, Functional, User Interface, IP, CAD, System Design, PROGRAMMING, Concept, Validation, Client, Camera, Embedded Systems, Cost Reduction, TCP/IP, Technical Support, Network, Imaging, VHDL, ADS, Intel, Troubleshooting, Processes, Cadence, Materials, Memory, VIDEO, Drivers, Protocols

Education

University of Maryland Aug 2010

Electrical Engineering

College Park