SAKINDER ALI
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SUMMARY
Logical Design and its verification with 12+ years of experience working with FPGA's, CPLD's and Zynq technologies. Enjoys being part of a team, as managing, motivating and training a productive team and thrives in high pressure and challenging working environments.

EDUCATION
AS General Engineering, May 2007, Montgomery College, Rockville, MD
BS Electrical Engineering, August 2010, University of Maryland, College Park, MD

HONORS AND ACTIVITIES
Dean's List awarded for three semesters.
Awarded the 2007-2008 Arnold A. Korab Endowed Scholarship.
Awarded the 2008-2009, 2009-2010 The Dollenberg Family Scholarship.
Awarded the 2009-2010 The David Scholarship.
Academy of Academic Excellence Award 2009-2010.

TRAININGS
ARM Cortex-A9 for ZYNQ System Design (Doulos, CA)
ARM Cortex-M3/M4 Software Design (Doulos, CA)
Advanced Embedded Systems Hardware and Software Design (Doulos, CA)
Zynq SOC Architecture and Embedded Systems Software (Via Logic, PA)
Vivado Design Suite STA and Xilinx Design Constraints (Via Logic, PA)
Zynq Ultrascale+ (Via Logic, PA)
Designing Embedded systems with Yockto (Doulos, CA)
Designing for Performance (Bottom Line Technology, MD)
Comprehensive VHDL (Doulos, CA)
SystemVerilog UVM

SKILLS
Embedded Systems Development: CPLDs, FPGAs, SoC
Logic Devices: Xilinx Zynq [Zc7010, Zc7020, Zc7030 And Zc7045]/Artix/Kintex/Spartan/Cpld/Microsemi
FPGA design tools: Xilinx [Vivado, Ise, Planeahead, SDAccel], Intel-Altera [OpenCL SDK, Quartus Prime]
Tools: Waveformer Pro, Chipscope, Matlab and ModelSim/QuestaSim
Programming: Vhdl, System Verilog, Tcl, Batch, Assembly, C and Opencl
Communication protocols: TRANSEC, RS232, RS422, UART, SPI and I2C
Hardware debugging: Signal Generator, Logic Analyzer, Digital Oscilloscope and FPGA Debugging tools

WORK EXPERIENCE

NORTHROP GRUMMAN - Mission Systems (Linthicum, MD)
Principal Engineer (03/27/2020- 01/04/2024)

Created reusable master custom bus agent in UVM environment testbench which verify DUT through coverage reports. Imported design verification requirements into Questa test plan. Implemented functional coverage points and tracked to complete the FV through verification management tracker. Updated RTL design for Microsemi Igloo2 FPGA and migrated traditional VHDL testbench into UVM environment (System Verilog) and verified it through coverage reports. Updated verification plan document according to verification requirement vs met coverages. Wrote test case to initialize DDR calibration routine. Created specific test scenarios to write/read

transections to DDR memory controller through Serdes interfaces. Verified various design with help of team members.

L3HARRIS - Communication Systems (Columbia, MD)
Specialist Electrical Engineer (05/13/2019- 02/20/2020)

Worked on cryptographic transmission security (TRANSEC) verification using System Verilog and Universal Verification Methods (UVM).
Wrote test cases to inject errors and validate it according to verification test matrix.
Wrote verification design document for the TRANSEC component of provided waveform.

RAYTHEON - Missile System (Tucson, AZ)
Senior Electrical Engineer (11/2017 - 05/09/2019)

Design, verification and implementation of VHDL modules.
RTL design and development from the concept to production for Microsemi Igloo2 FPGA.
System integration test and verification from CCA down to the FPGA design.

Participated daily Scrum meeting.

FAST FIT TECHNOLOGIES CONTRACT/ CONSULTANT (Remote)
Senior Firmware Engineer (7/2017 - 11/2017)

Rewrite and add features to already developed algorithms for Kernel [FPGA based accelerator] using OpenCL on Intel-Altera Platform. Debug for functionality, performance and optimize for OpenCL acceleration design, provide demonstrations and proofs of concepts.

LYNNTECH (College Station, TX)
Senior Electrical Engineer (9/2016 - 7/2017)

Wrote technical proposal "Network Isolation of Industrial Control System (ICS) Devices via Permanent Host Identifiers" Solicitation Number OSD172-DI4. Endorsed by Raytheon IDS.

Developed external memory [QDR] Interface through MIG for imaging/video-based technology to improve detection algorithms and performance for small maritime targets for both commercial and military applications. Designed and development various AXI-interface IPS and test software for local (PL) and arm (PS) communications within the ZYNQ chip. Implemented and tested camera [FLIR] interface to VDMA which includes node map address mapping core/pixel buffer sync core/camera link buffer core/camera link buffer core functional and hardware test.

Customized LWIP TCP/IP stack protocol library and created raw and socket mode applications for webserver on ZYNQ [ZC7020 Ethernet interface and the PS-DDR]. Developed client user interface and controls with the hardware server platform, which visualized the adc data results in real time. Further application was used for testing and debugging the hardware and software.

Conduct DTAG Training Sessions to US Border Patrol Agents at Naco/Brian Station AZ and Campo Station CA locations.

GENERAL ELECTRIC - TRANSPORTATION (Erie, PA)
Engineer/Technologist Firmware (01/2012 - 09/2016)

Prepared and implemented test protocols and test cases based on product specifications. Provided support to other departments, performed troubleshoots and identified the cause of malfunction. Coordinated with the ohv team members and ensured that the tests were performed per the specification given for the product. Tested, assessed, and

modified existing software system to improve performance. Prepared the test software and ensured that it was compatible with the product certification requirements. Checked the components and identified the cause of malfunction and resolved them. Developed generic test cases and debugged the functional failures.

Completed RTL implementation, timing improvement of new design for FPGA[Kintex]. Completed axi4 drivers for communication between FPGA and ARM[A9]. Created a detailed test-plan to verify the analog channels timing from FPGA to arm through axi4lite bus per the test plan. Created ADS8568 model in RTL using VHDL for test software written in C for ZYNQ design. Participated in verification of compliance processes of all VHDL products. Conducted system, unit and integration testing for VHDL products. Written assertions, code coverage modules, functional coverage modules and toggle coverage modules to ensure 100% verification.

Completed SPI, UART and AXI4 low-level drivers. Completed analog filtering, detection and proposed algorithms applications in C ARM- CORTEX-A9[ZYNQ]. Performed software integration and conducted software code reviews, as required. Designed specification of generic interrupt request (IRQ) controller.

Created and implemented test software for automated testing and validation. Created panel test to ensure proper backplane communication between Zynq card and master card. Implemented software requirements and proposed algorithms for system functionality. Prepared and implemented test protocols and test cases based on product specifications. Provided support to other departments, performed troubleshoots and identified the cause of malfunction.

Coordinated with the ohv team members and ensured that the tests were performed per the specification given for the product. Tested, assessed, and modified existing software system to improve performance. Prepared the test software and ensured that it was compatible with the product certification requirements. Checked the components and identified the cause of malfunction and resolved them. Developed verification plan for generic IRQ controller. Developed generic test cases and debugged the functional failures.

Assembled all the customer requirements and coordinated with the customer's engineers. Detected, assessed, documented, and eliminated technical problems. Collected the data and participated in the design review and related activities. Provided support to the production [GET Locomotive Plant-Erie PA] and design team, developed the Zynq- card hardware test procedure for OHV [320-ton and 360-ton haul truck Off-Highway Vehicles] truck. Performed troubleshoot on the master control systems with the help of electrical components. Ensured that all preventative actions were maintained in the facility along with stable production process. Assisted the customer in all technical and program issues, resolved all problems by reviewing the data. Provided technical support to the development of the product and conducted production tests. Verified the existing designs and initiated ways to improve the product and reduce the costs. Coordinated with the suppliers and provided support to the production team. Maintained the production designs and worked toward cost reduction and quality improvement. Supported and participated in process improvement and risk management activities.

Created, documented, and maintained embedded system components and software. Prepared all documents for technical requirements of the project and designed the test plans. Assisted the other departments and prepared validation document such as validation test plans. Prepared technical manuals provided technical content for the same. Documented all the software solutions and created system level test plans. Organized the procedure per the required product verification and validation. Documented all changes and updated the reports accordingly. Documented the test procedures and ensured that the technicians followed the procedures and installed accordingly.

Consistently worked on debugging and troubleshooting issues affecting product level. Completed Abel- code to VHDL for use in Arcnet protocol communication system. Tasks include: VHDL RTL design of a microcontroller (Motorola 68302), COM20020 chip, sram and flash interface, CPLD and FPGA device selection and pinout, synthesis, layout, RTL/Gate level simulation and debugging, and timing analysis. Tools used include Modelsim, Xilinx ISE for synthesis, and Xilinx Alliance for place and route. Coordinated with the hardware and software engineers and developed Arcnet firmware and applications. Assisted the other engineers and integrated and

performed tests on the system. Determined and documented project specifications and requirements, in an efficient manner.

HOWARD HUGHES MEDICAL INSTITUTE (Ashburn, VA)
Electrical Engineer - Internship (08/2011 - 10/2011)

Designed new pc boards and created component libraries used in schematic and printed circuit board development utilizing eagle layout and eagle capture tools. Developed and documented test plans and procedures - Designed test fixtures. Redesigned & modified numerous existing products to improve performance. Development of test hardware interfaces to final products. Performed different type of testing on hardware to ensure that hardware is error free.

AXIS ENGINEERING TECHNOLOGIES (College Park, MD)
Electrical Engineer - PartTime (01/2009 - 12/2009)

Designed and developed various HDL modules using Xilinx Spartan III FPGA board and transformed Matlab algorithmic code into FPGA design. Designed up to date digital circuit board interface logic to attain high quality diagnostics of the system.

CHESAPEAKE SCIENCES CORPORATION-L3 (Millersville, MD)
Electrical Engineer - Coop (01/2008 - 08/2008)

Developed block diagrams, schematics and printed circuit boards of digital designs. Models and simulates VHDL designs; validates designs with test benches. Performed basic circuit simulation. Worked on CAD design tools (Cadence design suite)/bills of materials (BOMs) and maintain cad libraries. Worked with software and hardware engineers to integrate the work of different disciplines. Designed printed circuit boards using OrCAD's capture and layout software for prototype designs electrical circuit testing to ensure quality level of performance. Debugged analog and digital circuits and designed troubleshooting systems for circuit board malfunctions. Created schematics and process flow diagrams for control units and communication systems. Reviewed bug reports from the test technicians for errors and issues.