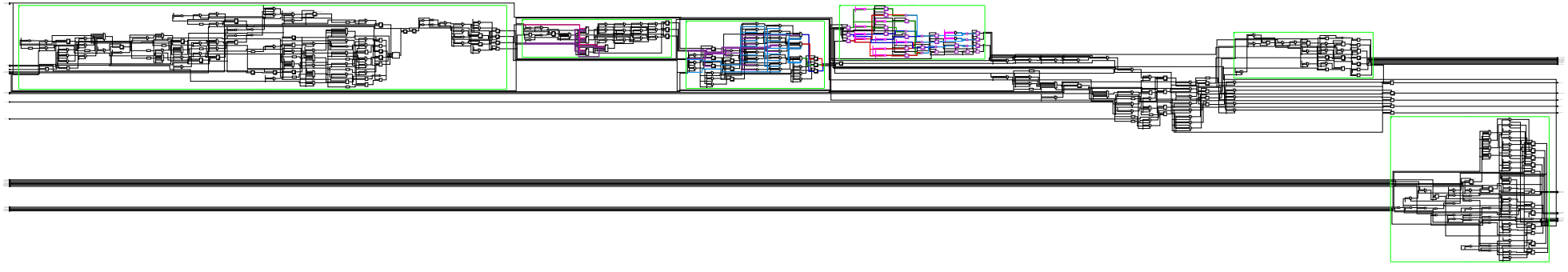
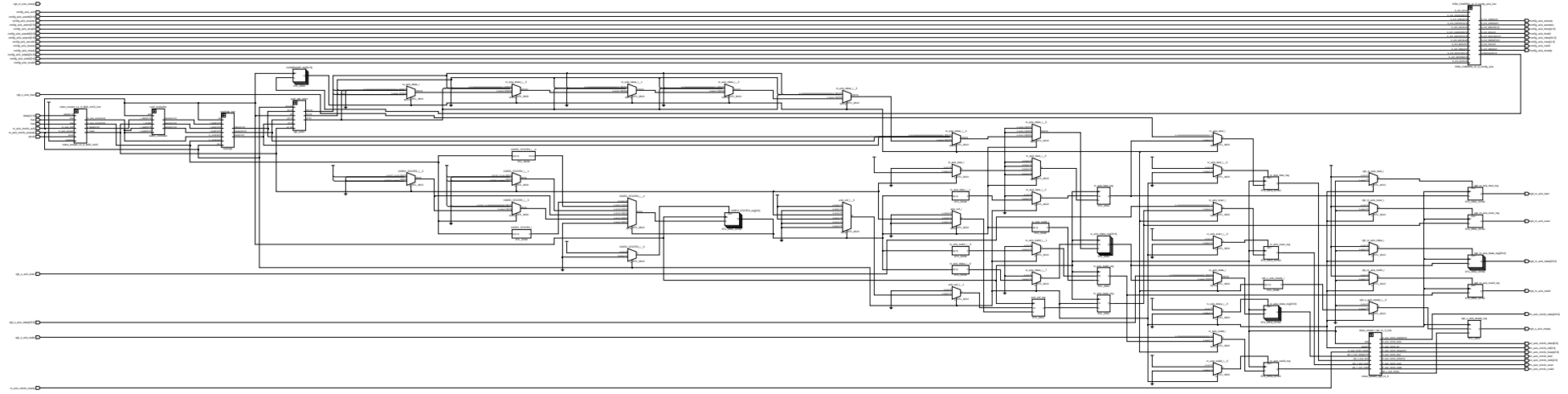
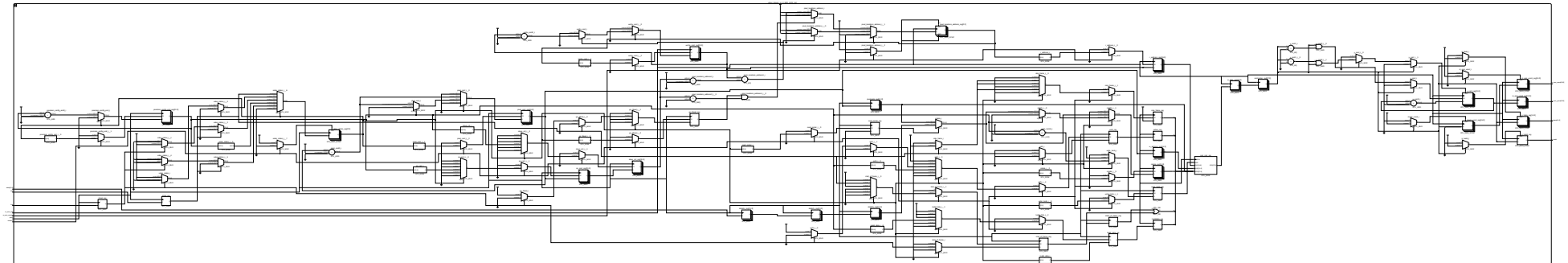
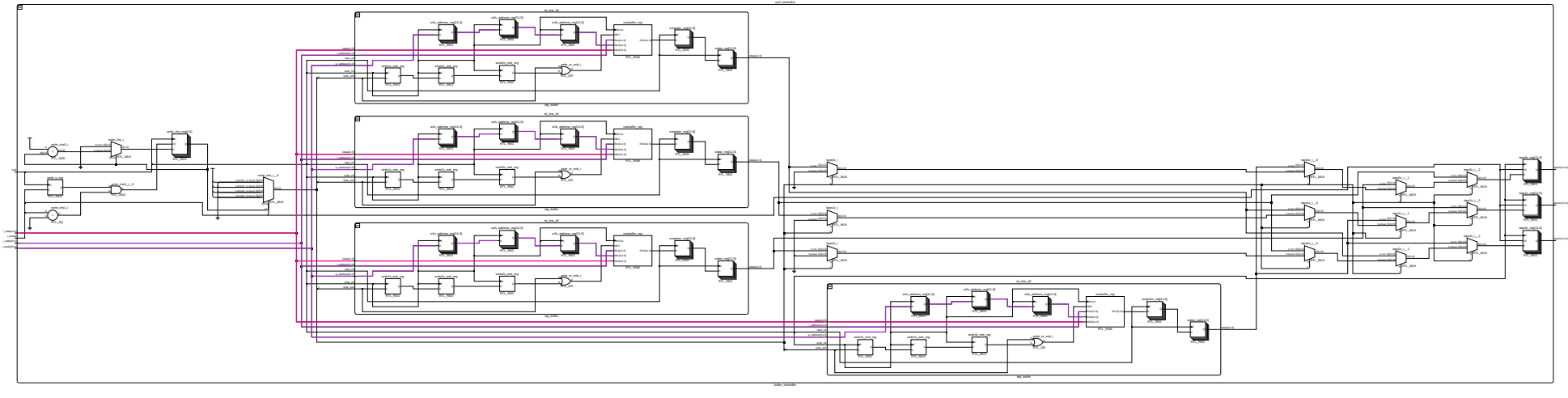
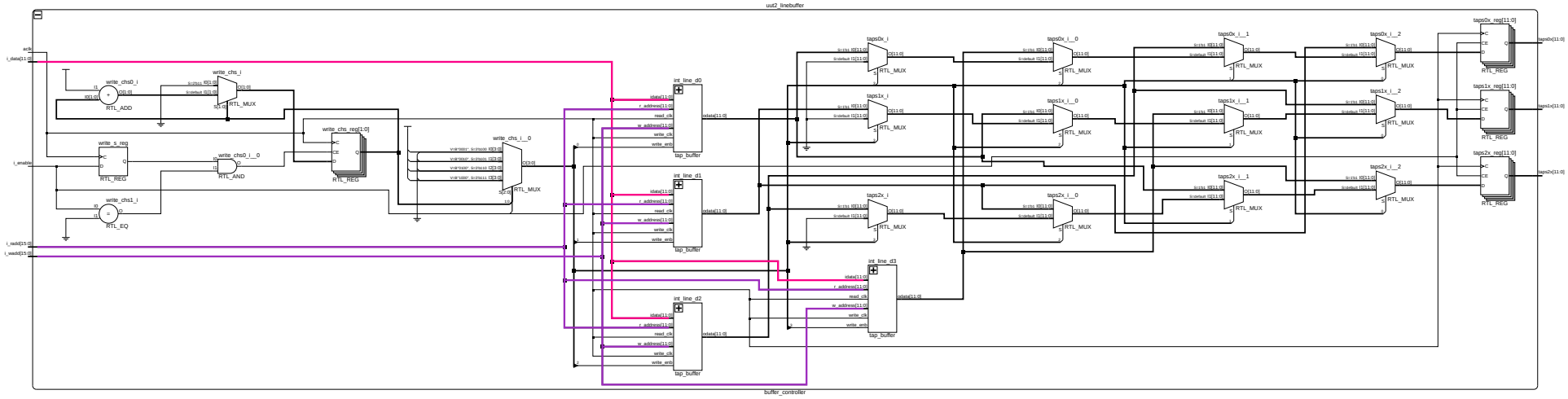
D5M CAMERA RAW TO RGB TO YCBCR VIDEO FRAMES
D5M_AXI_STREAM_OUT

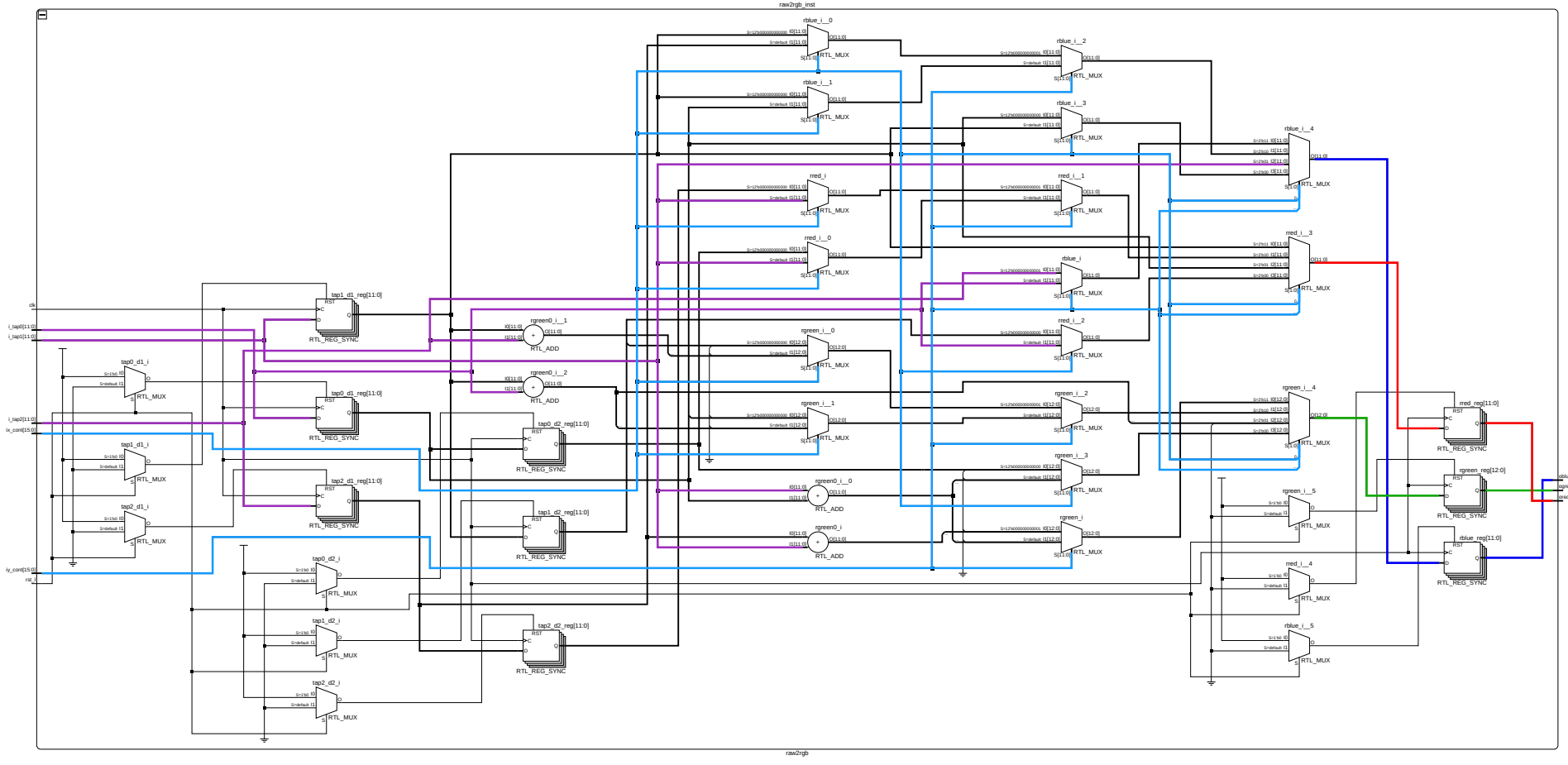


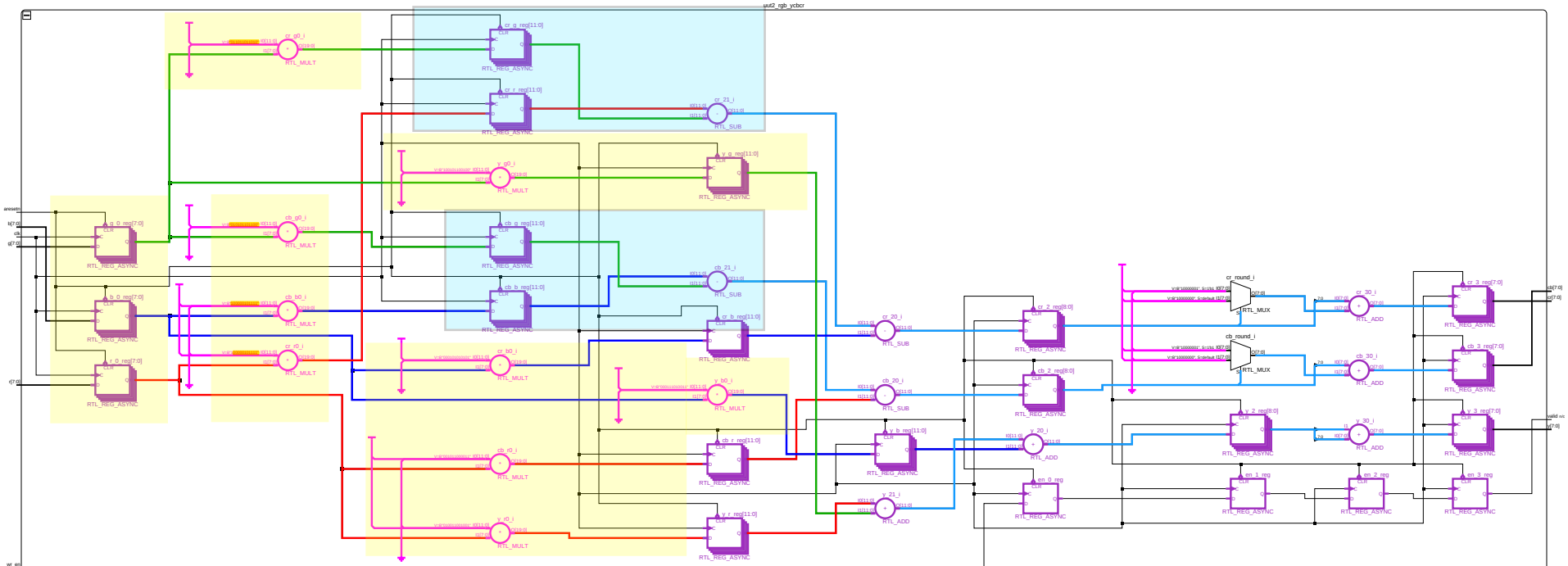







uut2_linebuffer
buffer_controller
write_chs0_i
write_chs_i
RTL_ADD
RTL_MUX
write_s_reg
write_chs0_i__0
RTL_REG
RTL_AND
write_chs_reg[1:0]
write_chs1_i
RTL_EQ
write_chs_i__0
int_line_d0
int_line_d1
int_line_d2
int_line_d3
tap_buffer
taps0x_i
taps0x_i__0
taps0x_i__1
taps0x_i__2
taps1x_i
taps1x_i__0
taps1x_i__1
taps1x_i__2
taps2x_i
taps2x_i__0
taps2x_i__1
taps2x_i__2
taps0x_reg[11:0]
taps1x_reg[11:0]
taps2x_reg[11:0]
i_data[11:0]
i_enable
i_raddr[15:0]
i_waddr[15:0]


raw2rgb_inst
rblue_i__0
rblue_i__1
rblue_i__2
rblue_i__3
rblue_i__4
rblue_i
rred_i
rred_i__0
rred_i__1
rred_i__2
rred_i__3
rred_i__4
rgreen0_i__0
rgreen0_i__1
rgreen0_i__2
rgreen0_i
rgreen_i__0
rgreen_i__1
rgreen_i__2
rgreen_i__3
rgreen_i__4
rgreen_i
rgreen_i__5
rblue_i__5
RTL_MUX
RTL_ADD
RTL_REG_SYNC
tap0_d1_reg[11:0]
tap1_d1_reg[11:0]
tap2_d1_reg[11:0]
tap0_d2_reg[11:0]
tap1_d2_reg[11:0]
tap2_d2_reg[11:0]
tap0_d1_i
tap1_d1_i
tap2_d1_i
tap0_d2_i
tap1_d2_i
tap2_d2_i
rred_reg[11:0]
rgreen_reg[12:0]
rblue_reg[11:0]
clk
i_tap0[11:0]
i_tap1[11:0]
i_tap2[11:0]
ix_con[15:0]
iy_con[15:0]
rst_n
rblue[11:0]
rgreen[12:0]
rred[11:0]
raw2rgb


uut2_rgb_ycbcr
rgb_ycbcr
RTL_REG_ASYNC
RTL_MULT
RTL_SUB
RTL_ADD
RTL_MUX
cr_g_reg[11:0]
cr_r_reg[11:0]
cr_g0_i
cr_r0_i
cr_21_i
cr_20_i
y_g_reg[11:0]
y_g0_i
cb_g_reg[11:0]
cb_b_reg[11:0]
cb_g0_i
cb_b0_i
cb_21_i
cb_20_i
cr_b_reg[11:0]
cr_b0_i
y_b_reg[11:0]
y_b0_i
cb_r_reg[11:0]
cb_r0_i
y_r_reg[11:0]
y_r0_i
y_21_i
y_20_i
cr_2_reg[8:0]
cb_2_reg[8:0]
y_2_reg[8:0]
en_0_reg
en_1_reg
en_2_reg
en_3_reg
cr_round_i
cb_round_i
cr_30_i
cb_30_i
y_30_i
cr_3_reg[7:0]
cb_3_reg[7:0]
y_3_reg[7:0]
r_0_reg[7:0]
b_0_reg[7:0]
g_0_reg[7:0]
aresetn
b[7:0]
r[7:0]
g[7:0]
wr_en
valid
cb[7:0]
cr[7:0]