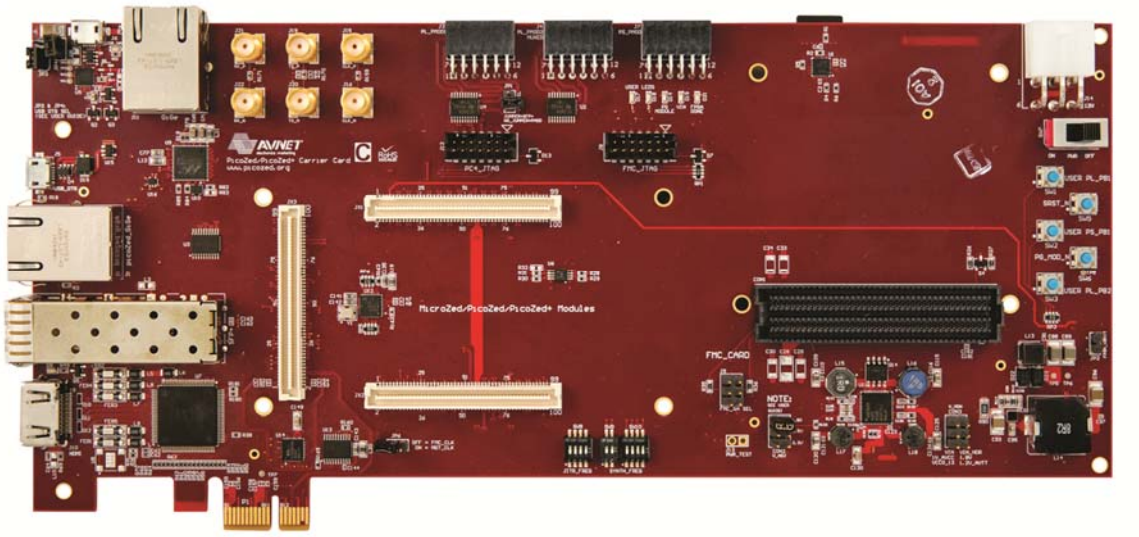
# PicoZed FMC Carrier Card

## PZCC-FMC, Revision C

### Hardware User Guide



**Revision 1.1**
**09 SEP 2015**

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# 1 Introduction

The PicoZed FMC Carrier Card (PZCC-FMC) is a development board designed for customers to easily evaluate the Avnet PicoZed System On Module (SOM) boards. This board provides an I/O breakout platform for the PicoZed SOMs. The PZCC-FMC provides all necessary SOM power, reset control and SoC I/O pin accessibility through the JX1, JX2, and JX3 microheaders.

This document details the specific features, operation and configuration of the PZCC-FMC board.

## Glossary

| Term | Definition |
|---|---|
| MIO | Multiplexed Input Output – the dedicated I/O available on the PS |
| PL | Programmable Logic |
| POR | Power On Reset |
| PS | Processing System |
| SOM | System On Module |
| SoC | System On Chip – Xilinx Zynq-7000 |

## Additional Documentation

Additional information and documentation on Xilinx's Zynq®-7000 All Programmable SoCs can be found at www.xilinx.com/zynq. Additional information and documentation on PicoZed can be found at www.picozed.org. Please refer to the appropriate PicoZed User's Guide for specific SOM features.

## 1.1 PZCC-FMC Features:

- **Interfaces:**
  - FMC LPC (72 differential, 4 single ended)
  - Xilinx PC4 Header for programming
    - Accesses PL JTAG
  - FMC JTAG
    - Accesses the JTAG chain on the FMC connector
  - 3 Digilent Pmod™ compatible interfaces:
    - One connected to PS MIO (muxed with eMMC)
    - One connected to Bank 13 PL (7Z015/20/30 only)
    - One muxed to Bank 13 PL (7Z015/30 only) - muxed with a SFP+ connection
  - uSD Card slot
  - Three 100-pin JX MicroHeaders for SOM insertion
  - SFP+ Interface - muxed with a Pmod™ connection
  - HDMI 1080p Output
  - PCIe x 1 Gen 2 Interface pairs:
    - PCIE-RX0 P/N
    - PCIE-TX0 P/N
    - PCIE-REFCLK P/N
  - SMA connector pairs:
    - SMA-TX P/N
    - SMA-RX P/N
    - SMA-MGTCLK P/N
  - 10/100/1000 Mb RJ45 Ethernet connector (connected to PicoZed SOM PHY) – J1
  - 10/100/1000 Mb RJ45 Ethernet PHY and connector – J11
  - Clock Synthesizer configuration switches
  - USB UART - Micro USB connector and transceiver
  - USB 2.0 OTG - Micro USB connector
  - 1 PS User Push Button
  - 2 PL User Push Buttons
  - 2 Configuration Push Buttons (CARRIER_RST_N, PG_MODULE_N)
  - 1 Jumper for Pmod™ or SFP+ MUX select
  - 2 PL Red User LEDs
  - 1 PS Red User LED
  - 3 Status LEDs (VIN_HDR, FPGA DONE & PG_MODULE)
  - 1 100 mil header for FPGA_VBAT_TEST
  - 1 Voltage Monitor pads 0.100” pads
  - 1 VADJ User Selectable Header: 1.8V, 2.5V, 3.3V selection; defaults to 1.8V
  - 1 slide switch for main power

- **Power**
  - On Board
    - One single channel SMPS IC:
      - Generates the primary board 5V power supply.
        - 5V @ 10 Amp capable.
    - One 5 channel SMPS IC:
      - 1.0V_AVCC @ 3.2A
      - 3.3V VCCO_13 and board logic @ 3.0A
      - 1.8V, 2.5V, 3.3V VADJ @ 1.2A (user selectable value)
      - 1.2V_AVTT @ 1.2A
      - 1.8V LDO@ 200mA
  - Wall Adapter
    - Primary 12V ≥ 5.0A, 2x3 connector
      - NOTE: not an ATX compatible power supply.

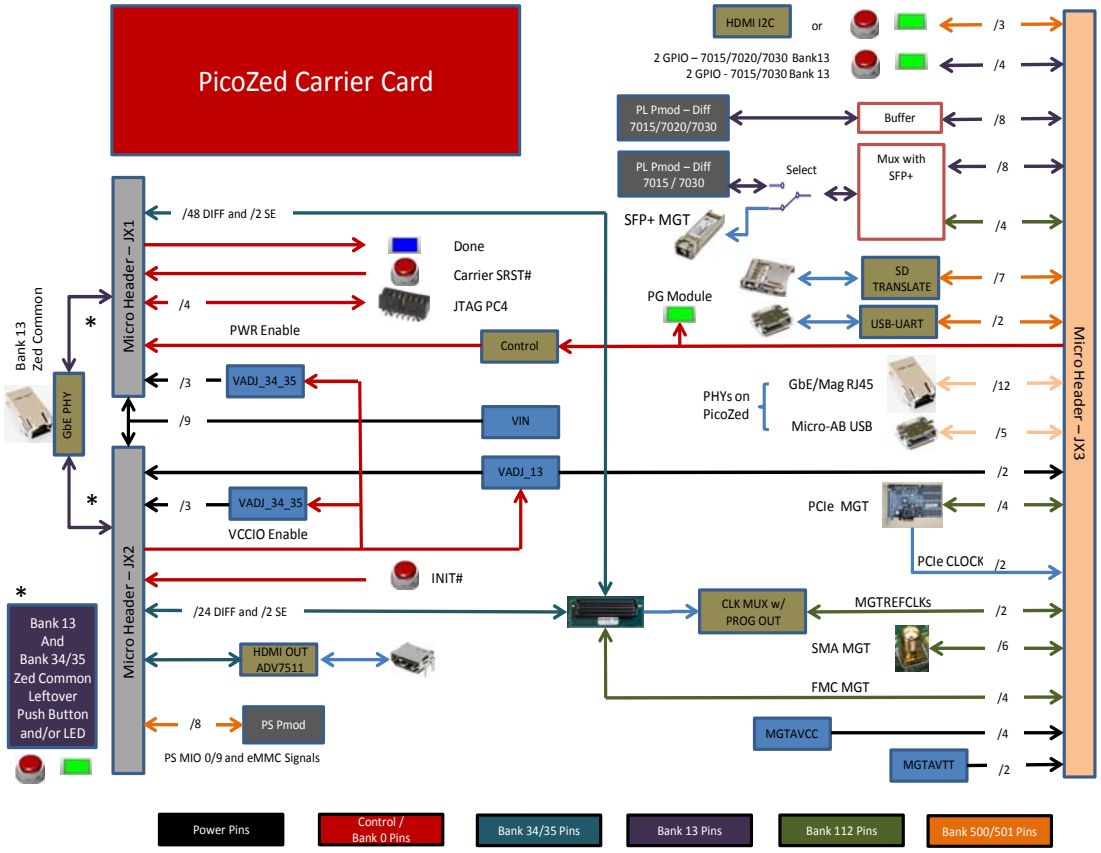



**Figure 1 – PZCC-FMC Block Diagram**

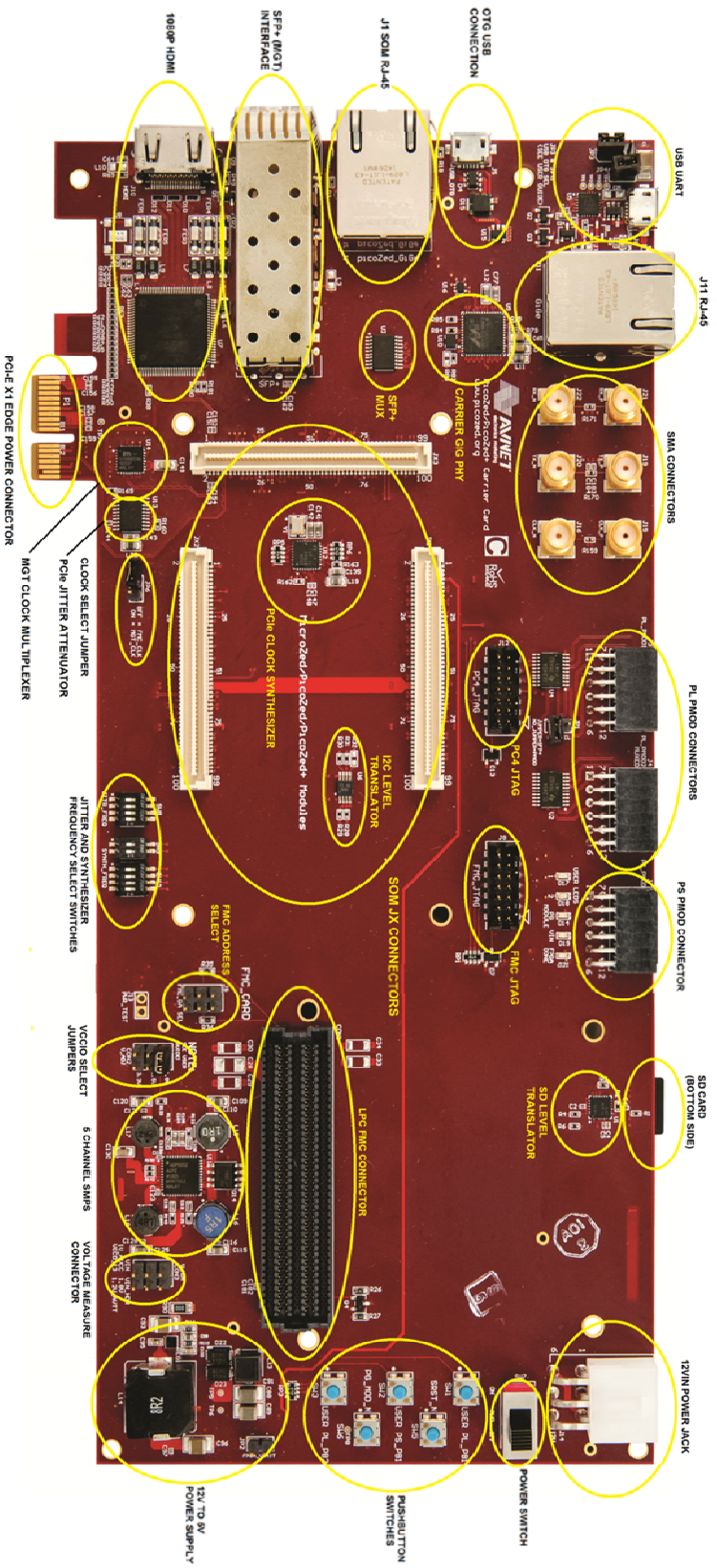



**Figure 2 – PZCC-FMC Component Overview**

# 2 Functional Description

The PZCC-FMC Carrier is an expansion board for the PicoZed SOMs. The FMC is the primary means of exposing the additional I/O although there are a few Pmod connectors as well. The board also features additional MGT lanes for PCIe and SFP+. The PZCC-FMC bridges Avnet's PicoZed SOM products to common high speed interfaces.

In addition to the LPC FMC connector, the PZCC-FMC also has 3 Digilent Pmod™ compatible interfaces (one is muxed with the SFP+ interface), a SFP+ connector, a Micro SD card, 2 JTAG ports (FMC & PC4), an HDMI port, 2 USB ports (UART and 2.0), PCIe x1 Gen 2.0 edge connector and 2 Ethernet ports (one with an on-carrier PHY and the other a connector interface for the PHY on the SOM).

The board includes user adjustable operational features to aid in product design and development. Such features include switch configurable MGT clock synthesizer and PCIe jitter attenuator, SMA clock and MGT (TX/RX) data inputs and a user adjustable VADJ power plane.

**NOTE:** While the PZCC-FMC board can support a MicroZed, the MicroZed SOM's I/O is limited and the user will find more value in using the MicroZed-centric MBCC-FMC board.

## 2.1 Reset sources

### 2.1.1 System Power Reset: PG_MODULE_N – SW6

The PG_MODULE signal is an active high 2.75V signal indicating both the carrier and SOM power supply are determined to be functional. LED D14 will illuminate when this signal is high, indicating both the SOM and carrier power supplies are functional.

When low the signal resets the SOM's USB UART, USB OTG circuit and turns off the FMC-CC VCCIO_34/35 power supplies. The carrier's Ethernet PHY is also reset while low. This signal is used to invoke a carrier card and SOM total system power reset. The PS and PL are reset to power on default settings and the selected boot process is initiated.

**Table 1 – PG_MODULE Connection**

| Carrier Net Name | MicroHeader Connection | Zynq AP SoC Connection |
|---|---|---|
| PG_MODULE | JX2, pin 11 | PG_MODULE |

### 2.1.2 Processor Subsystem Reset: CARRIER_SRST_N – SW5

The SYS_RST# button provides an active low signal to net CARRIER_SRST_N which allows the user to reset all of the functional logic within the SOM SoC device without disturbing the debug environment. For example, the previous breakpoints set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the OCM. The PL is also reset in system reset. Upon de-assertion of this signal, the SoC does not re-sample the boot mode strapping pins.

**Table 2 – CARRIER_SRST_N Connection**

| Carrier Net Name | MicroHeader Connection | Zynq AP SoC Connection |
|---|---|---|
| CARRIER_SRST_N | JX1, pin 6 | CARRIER_SRST_N |

## 2.2 User I/O – Switches and LEDs

### 2.2.1 User Push Buttons: SW1 – SW3

The Carrier provides 3 user GPIO push buttons to the Zynq-7000 AP SoC. Pull-down resistors provide a known low default state and a decoupling capacitor helps to filter out excessive noise on the signal. When pushed the button provides a logic high on the net.

**Table 3 – Push Button Connections**

| Carrier Net Name | MicroHeader Connection | PicoZed 7010/7020 Bank-Pin # | PicoZed 7015/7030 Bank-Pin # |
|---|---|---|---|
| PL_PB1 | JX2, pin 100 | 13 - V5 | 13 – T16 |
| PL_PB2 | JX3, pin 88 | N/A | 13-V14 |
| PS_PB1 | JX3, pin 64 | 501 – B9 | 501 – C13 |

### 2.2.2 User LEDs

The Carrier has 3 SOM driven user LEDs -- two from the PL and one from the PS. A logic high from the Zynq-7000 AP SoC I/O turns the LED on. LED's are sourced from the PZCC-FMC's 3.3V rail.

**Table 4 – User LED Connections**

| Carrier Net Name | MicroHeader Connection | PicoZed 7010/7020 Bank-Pin # | PicoZed 7015/7030 Bank-Pin # |
|---|---|---|---|
| PL_LED1 | JX3.73 | 13-Y7 | 13-Y18 |
| PL_LED2 | JX3.75 | 13-Y6 | 13-Y19 |
| PS_LED1 | JX3.40 | 501 - B14 | 501 - B13 |

### 2.2.3 PCIe Clock Synthesizer

The PZCC-FMC contains a Texas Instruments CDCM61002 user programmable clock synthesizer, U12, to afford maximum user clocking flexibility. The table below reflects the typical operating modes expected with the appropriate switch positions listed. Please be aware this is not an exhaustive list of all possible frequency selections; please refer to the Texas Instruments datasheet for the full table:

www.ti.com → Search CDCM61002

The default frequency factory configured is 62.5 MHz, used for GiGE interfacing.

**Table 5 – PCIe Clock Synthesizer Selection via SW9 & SW10**

| CDCM61002 SW9, SW10 FREQ SELECTION TABLE | | | | | | | |
|---|---|---|---|---|---|---|---|
| FREQ - MHz: | SW9.1 (PR1): | SW9.2 (PR0): | SW10.1 (CE): | SW10.2 (OD2): | SW10.3 (OD1): | SW10.4 (OD0): | Interface USE: |
| 62.5000 | OFF | OFF | OFF | OFF | OFF | OFF | GigE |
| 100.0000 | ON | ON | OFF | OFF | ON | OFF | PCI Exp |
| 125.0000 | OFF | OFF | OFF | ON | OFF | OFF | GigE |
| 156.2500 | OFF | ON | OFF | ON | OFF | OFF | 10 GigE |
| 200.0000 | ON | ON | OFF | ON | OFF | ON | PCI Exp |
| 250.0000 | OFF | OFF | OFF | ON | ON | OFF | GigE |
| NOTE: For all other frequencies please see the TI datasheet | | | | | | | |
| Note: "ON" position labeled on switch; "ON" = a logic low on CDCM pin | | | | | | | |
| Note: "OFF" position = a logic high on CDCM pin | | | | | | | |

## 2.3 Interface Connections

### 2.3.1 PCIe x1 Interface

***The PCIe interface is only available on the PZCC-FMC when a PicoZed 7015 or 7030 SOM is plugged into the carrier.***

- The PCIe x1 interface is **not** required for normal operation. However, it has been provided to assist in the development of PCIe based SOM products if desired. When inserted into a PCIe slot, 12V power from the host PCIe slot can be used to power the PZCC-FMC in lieu of the wall adapter power supply. The PCIe interface includes a 12V power circuit, control signals and a single data lane (differential TX and RX) and a single differential PCIe clock.

- The PCIe interface on the PZCC-FMC is one lane wide. The PRSNT1# and PRSNT2# signals for Lane 0 are hard wired together in hardware. The PRSNT2# on the host connector is pulled-up on the host motherboard. There is a single PRSNT1# pin that is pulled-low or tied to GND on the host motherboard. The add-in card connects the PRSNT1# pin to the PRSNT2# pin for the widest lane option in most applications, which effectively pulls the corresponding PRSNT2# pin low. This indicates to the host controller the lane width supported by the add-in card. In this application, the widest lane option is lane 0, and the corresponding PRSNT2# signal is use to connect to PRSNT1#.

**2.3.1.1** The PCIe reference clocks are passed through a jitter attenuator and conditioner, U13, prior to be routed to the JX3 header. The output frequency can be selected using SW8 per the table below. The factory shipped default output frequency is 250 MHz, with all Switch 8 positions “off”. Position 4 of switch 8 is a no connect. Please note the green highlighted position is what Avnet used for initial testing.

**Table 6 – SW8 PCIe Jitter Attenuator Frequency Table**

| SW8 FREQUENCY SELECTION (WITH 100MHz IN) | | | |
|---|---|---|---|
| OUT – MHz: | SW1: | SW2: | SW3: |
| 100 – DEFAULT | OFF | OFF | ON |
| 125 | OFF | ON | OFF |
| 250 | OFF | OFF | OFF |
| • NOTE: ICS has an internal 5x multiplier | | | |
| • NOTE: “ON” position is labeled on the switch | | | |

The PCI Express transmit lanes are AC coupled (DC blocking capacitors are included in the signal path) on the development board as required by the PCI Express specification.

**Table 7 – GTP Pin Locations for PCI Express**

| Carrier Net Name | MicroHeader Connection | PicoZed 7015/7030 Bank-Pin # |
|---|---|---|
| PCIE_RX0P | JX3.8 | 112 – AA7 |
| PCIE_RX0N | JX3.10 | 112 – AB7 |
| PCIE_TX0P | JX3.13 | 112 – AA3 |
| PCIE_TX0N | JX3.15 | 112 – AB3 |
| PCIE_REFCLK_P | JX3.1 | 112 – U9 |
| PCIE_REFCLK_N | JX3.3 | 112 – V9 |
| PCIE_RST_N | JX3.86 | 13 - V13 |

### 2.3.2 FMC LPC Connector

A single Low Pin Count (LPC) FMC connector is implemented on the carrier board to support FMC plug-in modules. The block diagram shows the MicroHeader connections to the FMC LPC connectors. See Figure **3 – FMC Connections** for topology overview. See **Section 2.5** for the FMC MicroHeader (JX) connections.

There are four mounting holes in the FMC card area to facilitate secure FMC module mounting.

The following guidelines have been observed in the layout of the FMC interface:

- **CLK_#_M2C**
  - 50 ohm single-ended impedance
  - Less than 10mil skew in P/N pair
  - Connected to MRCC (Multi-Region)
  - No length matching to any other feature
- **LA bus**
  - 50 ohm single-ended impedance
  - Less than 10mil skew in P/N pair
  - Less than 100mil length skew across all bits in a bus
  - LA Bus 0:16 located in bank 34
  - LA Bus 17:33 located in bank 35
  - CC Pairs 0, 17 on MRCC pins
  - CC Pairs 1, 18 on SRCC pins
- To conserve SoC pins, GA[1:0] pins are connected to header J9 – see **Section 3.1.1** for address selection.

### 2.3.3 Layout Routing Guidelines

- The signals for each header follow FMC routing tolerances and guidelines. Each of the P/N pairs have 50Ω single-ended impedance (100Ω differential) with less than 10 mil skew between all P/N pairs on each header.

- There is less than 200 mil length skew across all bits in a bus or byte group, including DQ and DQS pins in each bank.

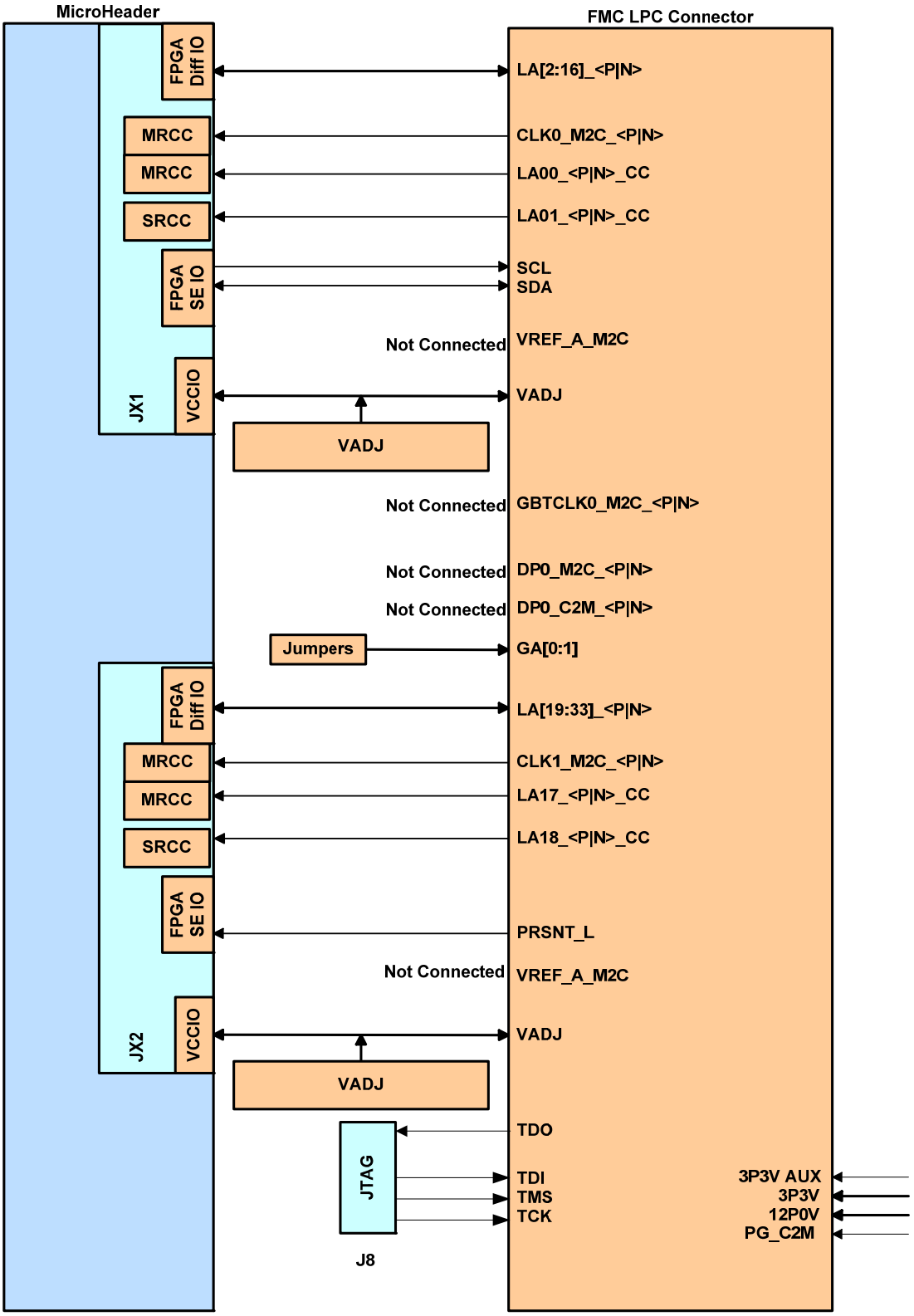



**Figure 3 – FMC Connections**

**Note**: The FMC slot SDA, SCL, and FMC_PRSNT signals are 3.3V levels. For this reason, level translation is implemented to follow the VADJ level.

## 2.4 SFP+ and PS/PL PMOD™ Interfaces

The carrier has 3 Digilent Pmod™ right angle 0.1" female sockets (2x6). Two connectors are for the SoC's PL, and one for the SoC's PS. These connections include eight GPIO and on the PL connections an adjustable voltage provided by the onboard VADJ power supply. VADJ is jumper selectable to provide 1.8V, 2.5V or 3.3V to the SoC bank.

**NOTE**: VADJ must be set to 1.8V on the PZCC-FMC when a PicoZed 7030 SOM is plugged in. Setting VADJ to 2.5V or 3.3V with the PicoZed 7030 will damage the Zynq device!

- Pmod™ Connections based on board type:
  - PicoZed 7010: PS Pmod only
  - PicoZed 7020: PS & PL1 Pmod
  - PicoZed 7015/30: PS, PL1 & PL2 Pmods

- Both PL Pmod connections are voltage level translated on the PZCC-FMC to ensure Pmod compliance and SOM connectivity, regardless of the SoCs I/O bank voltage selection (1.8V, 2.5V or 3.3V).

- PL1 Pmod1 (PL1) is available when using a 7015/7020/7030 SOM module and is routed differentially. In the event the user wants to use both PL1 and PL2 Pmod™ interfaces simultaneously, PL1 features a propagation delay buffer (U4) to better match the delays through PL 2's mux IC (U2).

- PL2 Pmod2 (PL2) is only accessible when a 7015/30 SOM is used. This interface is multiplexed with the Gigabit SFP+ connector. The user can choose via JP1 which interface to use: PL2 Pmod 2 interface **or** the SFP+ Interface.

  - JP1 open selects PL2 Pmod interface (default)
  - JP1 closed selects the SFP+ interface

- The PL Pmod data rates, based on the TI TX0108EPWR translator datasheet :
  - Push-Pull: 60 Mb/s

- PS Pmod is attached to bank 500 and can be used as a general Pmod interface, Processor (PJTAG) access or other hardened MIO peripherals (SPI, GPIO, CAN, I2C, UART, SD, QSPI, Trace, Watchdog).

- **NOTE:** The PicoZed 7015, 7020, or 7030 can access both the PS and PL Pmod interface(s), but a PicoZed 7010 can only access the PS Pmod.

### 2.4.1 Muxed Pmod and SFP+ interface diagram

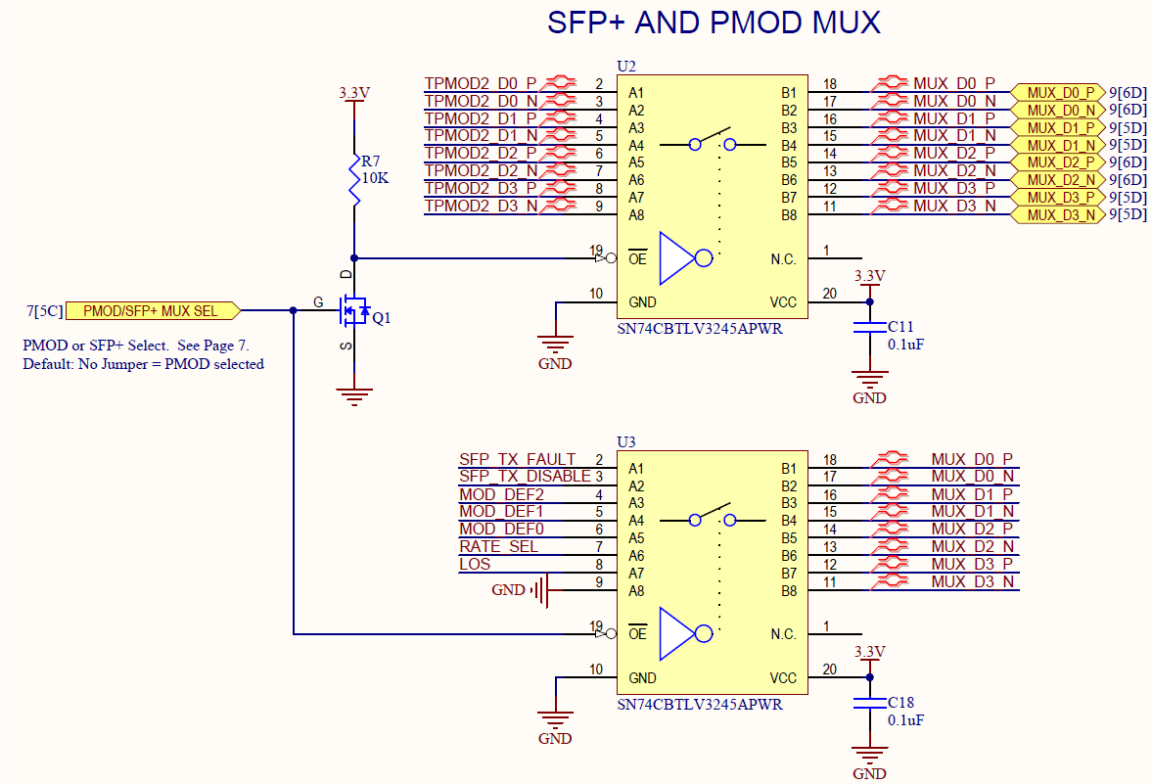



**Figure 4 – SFP+ or Pmod Multiplexer**

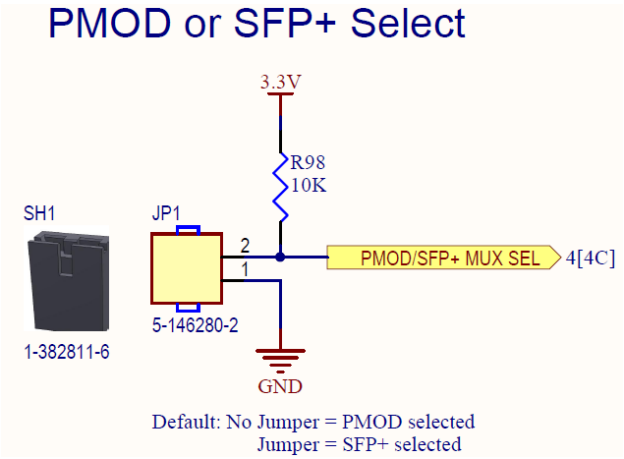



**Figure 5 – SFP+ or PMOD Selection**

**Table 8 – Digilent Pmod™ Compatible Interface Connections**

| PL1 Pmod™ | Carrier Net Name | J7 Pin Number | PicoZed Net Name | MicroHeader Connection | PicoZed 7020 Bank & Pin # | PicoZed 7015/30 Bank & Pin # |
|---|---|---|---|---|---|---|
| J3 | CPMOD1_D0_P | Pin 1 | BANK13_LVDS_8_P | JX3, pin 74 | 13-Y9 | 13-AA16 |
| | CPMOD1_D0_N | Pin 2 | BANK13_LVDS_8_N | JX3, pin 76 | 13-Y8 | 13-AA17 |
| | CPMOD1_D1_P | Pin 3 | BANK13_LVDS_9_P | JX3, pin 79 | 13-W10 | 13-AA11 |
| | CPMOD1_D1_N | Pin 4 | BANK13_LVDS_9_N | JX3, pin 81 | 13-W9 | 13-AB11 |
| | CPMOD1_D2_P | Pin 7 | BANK13_LVDS_10_P | JX3, pin 80 | 13-U9 | 13-Y12 |
| | CPMOD1_D2_N | Pin 8 | BANK13_LVDS_10_N | JX3, pin 82 | 13-U8 | 13-Y13 |
| | CPMOD1_D3_P | Pin 9 | BANK13_LVDS_11_P | JX3, pin 85 | 13-W11 | 13-V11 |
| | CPMOD1_D3_N | Pin 10 | BANK13_LVDS_11_N | JX3, pin 87 | 13-Y11 | 13-W11 |

| PL2 Pmod™ | Carrier Net Name | J7 Pin Number | PicoZed Net Name | MicroHeader Connection | PicoZed 7015/30 Bank & Pin # | SFP+ Net Name & P2 Pin # |
|---|---|---|---|---|---|---|
| J4 | PMOD2_D0_P | Pin 1 | BANK13_LVDS_14_P | JX3, pin 92 | 13-R17 | SFP_TX_Fault, 2 |
| | PMOD2_D0_N | Pin 2 | BANK13_LVDS_14_N | JX3, pin 94 | 13-T17 | SFP_TX_Disable, 3 |
| | PMOD2_D1_P | Pin 3 | BANK13_LVDS_13_P | JX3, pin 91 | 13-W12 | MOD_DEF2, 4 |
| | PMOD2_D1_N | Pin 4 | BANK13_LVDS_13_N | JX3, pin 93 | 13-W13 | MOD_DEF1, 5 |
| | PMOD2_D2_P | Pin 7 | BANK13_LVDS_16_P | JX3, pin 98 | 13-V16 | MOD_DEF0, 6 |
| | PMOD2_D2_N | Pin 8 | BANK13_LVDS_16_N | JX3, pin 100 | 13-W16 | RATE_SEL, 7 |
| | PMOD2_D3_P | Pin 9 | BANK13_LVDS_15_P | JX3, pin 97 | 13-V15 | LOS, 8 |
| | PMOD2_D3_N | Pin 10 | BANK13_LVDS_15_N | JX3, pin 99 | 13-W15 | GND |

| PS Pmod™ | Carrier Net Name | J7 Pin Number | MIO # | MicroHeader Connection | PicoZed 7010/20 Bank & Pin # | PicoZed 7015/30 Bank & Pin # |
|---|---|---|---|---|---|---|
| J7 | PSPMOD_D0 | Pin 1 | MIO10 | JX2, pin 1 | 500 - E8 | 500 - G16 |
| | PSPMOD_D1 | Pin 2 | MIO13 | JX2, pin 2 | 500 - E9 | 500 - A17 |
| | PSPMOD_D2 | Pin 3 | MIO14 | JX2, pin 3 | 500 - C6 | 500 - B17 |
| | PSPMOD_D3 | Pin 4 | MIO15 | JX2, pin 4 | 500 - D9 | 500 - E17 |
| | PSPMOD_D4 | Pin 7 | MIO12 | JX2, pin 5 | 500 - E6 | 500 - C18 |
| | PSPMOD_D5 | Pin 8 | MIO11 | JX2, pin 6 | 500 - B5 | 500 - B19 |
| | PSPMOD_D6 | Pin 9 | MIO0 | JX2, pin 7 | 500 - C5 | 500 - G17 |
| | PSPMOD_D7 | Pin 10 | MIO9 | JX2, pin 8 | 500 - C8 | 500 - C19 |

## 2.5 JX1, JX2 and JX3 SOM Interface Microheaders

The PicoZed Carrier has three 100-pin Micro Headers (FCI, 61082-101400LF) for connection to the SOMs.

The JX1 and JX2 connectors interface power control signals, SOM reset, JTAG, PL (FMC data/control, PB), PS Pmod, Ethernet, and HDMI signals to the SOM target.

The JX3 connector interfaces SOM Ethernet, PCIe TX/RX/CLKs, microSD Card, USB OTG, PL I/O, USB UART, Gigabit transceivers data and clocks (MGT/GTX), and the MUXed SFP+/PL PMOD2 signals.

The connectors are FCI 0.8mm Bergstak®, 100 Position, Dual Row, BTB Vertical Receptacles. These have variable stack heights from 5mm to 16mm, making it easy to connect to a variety of carrier or system boards. Each pin can carry 500mA of current. The 5mm stack height used on the PZCC-FMC, and PicoZed SOMs support I/O speeds up to 8 Gbps as shown in the following FCI customer presentation:

*BergStak® 0.8mm Mezzanine Connectors*
*Customer Presentation*
June 2014

http://portal.fciconnect.com/Comergent/fci/documentation/customerpresentation/bergstak_customerpresentation.pdf

The fastest supported rate in the PicoZed family exists with the 7030 member, whose Zynq device/package can achieve 6.6 Gbps. This is within the operating rate of the Bergstak connectors.

The carrier card powers the PicoZed PL VCCIO banks. This gives the carrier card the flexibility to control the I/O bank voltages. On the PZCC-FMC, both VCCO_34 and VCCO_35 are powered from a single supply.

One signal in a Bank 34differential pair (JX1_LVDS_2_P on 7010/20, JX2_LVDS_2_P on 7015/30) is shared with PUDC_B.

**Table 9 – Micro Header JX1 and JX2 Overview**

| Micro Header #1 (JX1) | | | | Micro Header #2 (JX2) | | | |
|---|---|---|---|---|---|---|---|
| Signal Name | | Source | Pins | Signal Name | | Source | Pins |
| PL | JX1 I/Os, for 7010/20: PUDC on JX1.17 | Zynq Bank 34 or Zynq Bank 35 | 49 ## | PL | JX2 I/Os for 7015/30: PUDC is on JX2.23 | Zynq Bank 35 or Zynq Bank 34 | 50 ++ |
| | Bank 13 I/Os | Zynq Bank 13 | 8 ** | | Bank 13 I/Os | Zynq Bank 13 | 7 ** |
| JTAG | TMS_0 | Zynq Bank 0 | 5 4 | PS | PS MIO [0,9-15] | Zynq Bank 500 | 8 |
| | TDI_0 | Zynq Bank 0 | | C | Init_B_0 | Zynq Bank 0 | 1 1 |
| | TCK_0<br>TDO_0 | Zynq Bank 0<br>Zynq Bank 0 | | | VCCIO_EN | Module/Carrier | |
| | Carrier_SRST# | Carrier | | Power | PG_MODULE | Module/Carrier | 1 |
| | VP_0 | Zynq Bank 0 | | | Vin | Carrier | 5 |
| Analog | VN_0 | Zynq Bank 0 | 2 | | GND | Carrier | 23 |
| | DXP_0 | Zynq Bank 0 | | | VCCO_13 | Carrier | 1 |
| | DXN_0 | Zynq Bank 0 | | | VCCO_35 | Carrier | 3 |
| | PUDC_B / IO | Zynq Bank 34 | | | | | |
| C | DONE | Zynq Bank 0 | | Total | | | 100 |
| Power | PWR_Enable | Carrier | 1 | | | | |
| | Vin | Carrier | 4 | | | | |
| | GND | Carrier | 23 | | | | |
| | VCCO_34 | Carrier | 3 | | | | |
| | VBATT | Carrier | 1 | | | | |
| TOTAL | | | 100 | | | | |

** PicoZed 7015/7020/7030
## PicoZed 7010/7020 Bank 34 and PicoZed 7015/7030 Bank 35
++ PicoZed 7010/7020 Bank 35 and PicoZed 7015/7030 Bank 34

**Table 10 – Micro Header JX3 Overview**

| MicroHeader #3 (JX3) | | | |
|---|---|---|---|
| **Signal Name** | | **Source** | **Pin Count** |
| PL | Bank 13 I/Os | Zynq Bank 13 | 20 ** |
| XCVR | MGTTX I/Os | Zynq Bank 112 | 20 ## |
| | MGTRX I/Os | Zynq Bank 112 | |
| | MGTREFCLK I/Os | Zynq Bank 112 | |
| PS | MIO[40-51] | Zynq Bank 501 | 26 |
| | ETHERNET | Zynq Bank 501 | |
| | USB 2.0 | Zynq Bank 500 | |
| Power | USB_VBUS_OTG | Carrier | 1 |
| | VCCO_13 | Carrier | 2 |
| | MGTAVCC | Carrier | 4 |
| | MGTAVTT | Carrier | 2 |
| | GND | Carrier | 25 |
| **TOTAL** | | | 100 |

** PicoZed 7020 has 10 I/O and PicoZed 7015/7030 adds 20 I/O
## PicoZed 7015/7030 only

**Table 11 – JX1 Connections**

| PicoZed 7015/7030 Bank-Pin # | PicoZed 7010/7020 Bank-Pin # | Net Name | JX1 Pin # | JX1 Pin # | Net Name | PicoZed 7010/7020 Bank-Pin # | PicoZed 7015/7030 Bank-Pin # |
|---|---|---|---|---|---|---|---|
| 0 – H11 | 0 - F9 | JTAG_TCK | 1 | 2 | JTAG_TMS | 0 - J6 | 0 – H10 |
| 0 – G9 | 0 - F6 | JTAG_TDO | 3 | 4 | JTAG_TDI | 0 - G6 | 0 – H9 |
| N/A | N/A | PWR_ENABLE | 5 | 6 | CARRIER_SRST# | 501 - B10 | 501 – C14 |
| 0 – G14 | 0 - F11 | **FPGA_VBATT** | 7 | 8 | FPGA_DONE | 0 - R11 | 0 – T10 |
| 35 – H6 | 34 - R19 | FMC_SCL | 9 | 10 | FMC_SDA | 34 - T19 | 35 – H5 |
| 35 – H4 | 34 - T11 | LA03_P | 11 | 12 | LA02_P | 34 - T12 | 35 – F5 |
| 35 – H3 | 34 - T10 | LA03_N | 13 | 14 | LA02_N | 34 - U12 | 35 – E5 |
| N/A | N/A | **GND** | 15 | 16 | **GND** | N/A | N/A |
| 35 – G3 | 34 - U13 | LA08_P | 17 | 18 | LA04_P | 34 - V12 | 35 – F2 |
| 35 – G2 | 34 - V13 | LA08_N | 19 | 20 | LA04_N | 34 - W13 | 35 – F1 |
| N/A | N/A | **GND** | 21 | 22 | **GND** | N/A | N/A |
| 35 – G4 | 34 - T14 | LA12_P | 23 | 24 | LA07_P | 34 - P14 | 35 – E4 |
| 35 – F4 | 34 - T15 | LA12_N | 25 | 26 | LA07_N | 34 - R14 | 35 – E3 |
| N/A | N/A | **GND** | 27 | 28 | **GND** | N/A | N/A |
| 35 – G6 | 34 - Y16 | LA16_P | 29 | 30 | LA11_P | 34 - W14 | 35 – B2 |
| 35 – F6 | 34 - Y17 | LA16_N | 31 | 32 | LA11_N | 34 - Y14 | 35 – B1 |
| N/A | N/A | **GND** | 33 | 34 | **GND** | N/A | N/A |
| 35 – E8 | 34 - T16 | LA20_P | 35 | 36 | LA15_P | 34 - V15 | 35 – H1 |
| 35 – D8 | 34 - U17 | LA20_N | 37 | 38 | LA15_N | 34 - W15 | 35 – G1 |
| N/A | N/A | **GND** | 39 | 40 | **GND** | N/A | N/A |
| 35 – C6 | 34 - U14 | LA01_CC_P | 41 | 42 | LA00_CC_P | 34 - U18 | 35 – D5 |
| 35 – C5 | 34 - U15 | LA01_CC_N | 43 | 44 | LA00_CC_N | 34 - U19 | 35 – C4 |
| N/A | N/A | **GND** | 45 | 46 | **GND** | N/A | N/A |
| 35 – B4 | 34 - N18 | CLK0_C2M_P | 47 | 48 | LA19_P | 34 - N20 | 35 – D3 |
| 35 – B3 | 34 - P19 | CLK0_C2M_N | 49 | 50 | LA19_N | 34 - P20 | 35 – C3 |
| N/A | N/A | **GND** | 51 | 52 | **GND** | N/A | N/A |
| 35 – D1 | 34 - T20 | LA22_P | 53 | 54 | LA21_P | 34 - V20 | 35 – A2 |
| 35 – C1 | 34 - U20 | LA22_N | 55 | 56 | LA21_N | 34 - W20 | 35 – A1 |
| N/A | N/A | **VIN_HDR** | 57 | 58 | **VIN_HDR** | N/A | N/A |
| N/A | N/A | **VIN_HDR** | 59 | 60 | **VIN_HDR** | N/A | N/A |
| 35 – E2 | 34 - Y18 | LA25_P | 61 | 62 | LA24_P | 34 - V16 | 35 – D7 |
| 35 – D2 | 34 - Y19 | LA25_N | 63 | 64 | LA24_N | 34 - W16 | 35 – D6 |
| N/A | N/A | **GND** | 65 | 66 | **GND** | N/A | N/A |
| 35 – F7 | 34 - R16 | LA29_P | 67 | 68 | LA28_P | 34 - T17 | 35 – A5 |
| 35 – E7 | 34 - R17 | LA29_N | 69 | 70 | LA28_N | 34 - R18 | 35 – A4 |
| N/A | N/A | **GND** | 71 | 72 | **GND** | N/A | N/A |
| 35 – G8 | 34 - V17 | LA31_P | 73 | 74 | LA30_P | 34 - W18 | 35 – A7 |
| 35 – G7 | 34 - V18 | LA31_N | 75 | 76 | LA30_N | 34 - W19 | 35 – A6 |
| N/A | N/A | **GND** | 77 | 78 | **VCCO_34** | N/A | N/A |
| N/A | N/A | **VCCO_34** | 79 | 80 | **VCCO_34** | N/A | N/A |
| 35 – B7 | 34 - N17 | LA33_P | 81 | 82 | LA32_P | 34 - P15 | 35 – C8 |
| 35 – B6 | 34 - P18 | LA33_N | 83 | 84 | LA32_N | 34 - P16 | 35 – B8 |
| N/A | N/A | **GND** | 85 | 86 | **GND** | N/A | N/A |
| 13 – AA14 | 13 - U7 | ETH_TXD0 | 87 | 88 | ETH_MDC | 13 - T9 | 13 – Y14 |
| 13 – AA15 | 13 - V7 | ETH_TXD1 | 89 | 90 | ETH_MDIO | 13 - U10 | 13 – Y15 |
| 13 – U19 | 13 - V8 | ETH_TXD2 | 91 | 92 | ETH_TX_CLK | 13 - T5 | 13 – V18 |
| 13 – V19 | 13 - W8 | ETH_TXD3 | 93 | 94 | ETH_TX_CTRL | 13 - U5 | 13 – W18 |
| N/A | N/A | **GND** | 95 | 96 | **GND** | N/A | N/A |
| 0 – L12 | 0 - K9 | N/C | 97 | 98 | N/C | 0 - M9 | 0 – N12 |
| 0 – M11 | 0 - L10 | N/C | 99 | 100 | N/C | 0 - M10 | 0 – N11 |

**Table 12 – JX2 Connections**

| PicoZed 7015/7030 Bank-Pin # | PicoZed 7010/7020 Bank-Pin # | PicoZed Net | JX2 Pin # | JX2 Pin # | PicoZed Net | PicoZed 7010/7020 Bank-Pin # | PicoZed 7015/7030 Bank-Pin # |
|---|---|---|---|---|---|---|---|
| 500 - G16 | 500 - E8 | PSPMOD_D0 | 1 | 2 | PSPMOD_D1 | 500 - E9 | 500 – A17 |
| 500 - B17 | 500 - C6 | PSPMOD_D2 | 3 | 4 | PSPMOD_D3 | 500 - D9 | 500 – E17 |
| 500 - C18 | 500 - E6 | PSPMOD_D4 | 5 | 6 | PSPMOD_D5 | 500 - B5 | 500 – B19 |
| 500 - G17 | 500 - C5 | PSPMOD_D6 | 7 | 8 | PSPMOD_D7 | 500 - C8 | 500 – C19 |
| 0 – T8 | 0 - R10 | N/C | 9 | 10 | VCCIO_EN | N/A | N/A |
| 500 – B18 | 500 - C7 | PG_MODULE | 11 | 12 | **VIN_HDR** | N/A | N/A |
| 34 – H8 | 35 - G14 | HDMI_DE | 13 | 14 | FMC_PRSNT | 35 - J15 | 34 – R8 |
| N/A | N/A | **GND** | 15 | 16 | **GND** | N/A | N/A |
| 34 – M4 | 35 - C20 | HDMI_SCLK | 17 | 18 | HDMI_SPDIF | 35 - B19 | 34 – J2 |
| 34 – M3 | 35 - B20 | HDMI_SDATA | 19 | 20 | HDMI_PPICLK | 35 - A20 | 34 – J1 |
| N/A | N/A | **GND** | 21 | 22 | **GND** | N/A | N/A |
| 34 – K7 | 35 - E17 | ADV7511_HPD | 23 | 24 | ADV7511_D28 | 35 - D19 | 34 – J3 |
| 34 – L7 | 35 - D18 | ADV7511_INT_N | 25 | 26 | ADV7511_D29 | 35 - D20 | 34 – K2 |
| N/A | N/A | **GND** | 27 | 28 | **GND** | N/A | N/A |
| 34 – P7 | 35 - E18 | ADV7511_D20 | 29 | 30 | ADV7511_D30 | 35 - F16 | 34 – L2 |
| 34 – R7 | 35 - E19 | ADV7511_D21 | 31 | 32 | ADV7511_D31 | 35 - F17 | 34 – L1 |
| N/A | N/A | **GND** | 33 | 34 | **GND** | N/A | N/A |
| 34 – N4 | 35 - L19 | ADV7511_D22 | 35 | 36 | ADV7511_D32 | 35 - M19 | 34 – P3 |
| 34 – N3 | 35 - L20 | ADV7511_D23 | 37 | 38 | ADV7511_D33 | 35 - M20 | 34 – P2 |
| N/A | N/A | **GND** | 39 | 40 | **GND** | N/A | N/A |
| 34 – M2 | 35 - M17 | ADV7511_D24 | 41 | 42 | ADV7511_D34 | 35 - K19 | 34 – N1 |
| 34 – M1 | 35 - M18 | ADV7511_D25 | 43 | 44 | ADV7511_D35 | 35 - J19 | 34 – P1 |
| N/A | N/A | **GND** | 45 | 46 | **GND** | N/A | N/A |
| 34 – K4 | 35 - L16 | ADV7511_D26 | 47 | 48 | LA17_CC_P | 35 - K17 | 34 – L5 |
| 34 – K3 | 35 - L17 | ADV7511_D27 | 49 | 50 | LA17_CC_N | 35 - K18 | 34 – L4 |
| N/A | N/A | **GND** | 51 | 52 | **GND** | N/A | N/A |
| 34 – T2 | 35 - H16 | CLK0_M2C_P | 53 | 54 | LA18_CC_P | 35 - J18 | 34 – U2 |
| 34 – T1 | 35 - H17 | CLK0_M2C_N | 55 | 56 | LA18_CC_N | 35 - H18 | 34 – U1 |
| N/A | N/A | **VIN_HDR** | 57 | 58 | **VIN_HDR** | N/A | N/A |
| N/A | N/A | **VIN_HDR** | 59 | 60 | **VIN_HDR** | N/A | N/A |
| 34 – R3 | 35 - G17 | LA05_P | 61 | 62 | LA06_P | 35 - F19 | 34 – L6 |
| 34 – R2 | 35 - G18 | LA05_N | 63 | 64 | LA06_N | 35 - F20 | 34 – M6 |
| N/A | N/A | **GND** | 65 | 66 | **GND** | N/A | N/A |
| 34 – J5 | 35 - G19 | LA09_P | 67 | 68 | LA10_P | 35 - J20 | 34 – R5 |
| 34 – K5 | 35 - G20 | LA09_N | 69 | 70 | LA10_N | 35 - H20 | 34 – R4 |
| N/A | N/A | **GND** | 71 | 72 | **GND** | N/A | N/A |
| 34 – J7 | 35 - K14 | LA13_P | 73 | 74 | LA14_P | 35 - H15 | 34 – P6 |
| 34 – J6 | 35 - J14 | LA13_N | 75 | 76 | LA14_N | 35 - G15 | 34 – P5 |
| N/A | N/A | **GND** | 77 | 78 | **VCCO_35** | N/A | N/A |
| N/A | N/A | **VCCO_35** | 79 | 80 | **VCCO_35** | N/A | N/A |
| 34 – J8 | 35 - N15 | LA23_P | 81 | 82 | LA27_P | 35 - L14 | 34 – N6 |
| 34 – K8 | 35 - N16 | LA23_N | 83 | 84 | LA27_N | 35 - L15 | 34 – N5 |
| N/A | N/A | **GND** | 85 | 86 | **GND** | N/A | N/A |
| 34 – M8 | 35 - M14 | LA26_P | 87 | 88 | HDMI_HSYNC | 35 - K16 | 34 – N8 |
| 34 – M7 | 35 - M15 | LA26_N | 89 | 90 | HDMI_VSYNC | 35 - J16 | 34 – P8 |
| N/A | N/A | **GND** | 91 | 92 | **GND** | N/A | N/A |
| 13 – AB21 | 13 - Y12 | ETH_RXD0 | 93 | 94 | ETH_RX_CLK | 13 - V11 | 13 – AB18 |
| 13 – AB22 | 13 - Y13 | ETH_RXD1 | 95 | 96 | ETH_RX_CTRL | 13 - V10 | 13 – AB19 |
| 13 – AA19 | 13 - V6 | ETH_RXD2 | 97 | 98 | **VCCO_13** | N/A | N/A |
| 13 – AA20 | 13 - W6 | ETH_RXD3 | 99 | 100 | PL_PB1 | 13 - V5 | 13 – T16 |

**Table 13 – JX3 Connections**

| PicoZed 7015/7030 Bank-Pin # | PicoZed 7010/7020 Bank-Pin # | PicoZed Net | JX3 Pin # | JX3 Pin # | PicoZed Net | PicoZed 7010/7020 Bank-Pin # | PicoZed 7015/7030 Bank-Pin # |
|---|---|---|---|---|---|---|---|
| 112 – U9 | N/A | PCIE-JREFCLK_P | 1 | 2 | MGTREFCLK_P | N/A | 112 – U5 |
| 112 – V9 | N/A | PCIE-JREFCLK_N | 3 | 4 | MGTREFCLK_N | N/A | 112 – V5 |
| N/A | N/A | **MGTAVCC** | 5 | 6 | **GND** | N/A | N/A |
| N/A | N/A | **MGTAVCC** | 7 | 8 | PCIE-RX0_P | N/A | 112 – AA7 |
| N/A | N/A | **MGTAVCC** | 9 | 10 | PCIE-RX0_N | N/A | 112 – AB7 |
| N/A | N/A | **MGTAVCC** | 11 | 12 | **GND** | N/A | N/A |
| 112 – AA3 | N/A | PCIE-TX0_P | 13 | 14 | MGTRX1_P | N/A | 112 – W8 |
| 112 – AB3 | N/A | PCIE-TX0_N | 15 | 16 | MGTRX1_N | N/A | 112 – Y8 |
| N/A | N/A | **GND** | 17 | 18 | **GND** | N/A | N/A |
| 112 – W4 | N/A | MGTTX1_P | 19 | 20 | MGTRX2_P | N/A | 112 – AA9 |
| 112 – Y4 | N/A | MGTTX1_N | 21 | 22 | MGTRX2_N | N/A | 112 – AB9 |
| N/A | N/A | **GND** | 23 | 24 | **GND** | N/A | N/A |
| 112 – AA5 | N/A | MGTTX2_P | 25 | 26 | FMC_MGT_RX_P | N/A | 112 – W6 |
| 112 – AB5 | N/A | MGTTX2_N | 27 | 28 | FMC_MGT_RX_N | N/A | 112 – Y6 |
| N/A | N/A | **GND** | 29 | 30 | **MGTAVTT** | N/A | N/A |
| 112 – W2 | N/A | FMC_MGT_TX_P | 31 | 32 | **MGTAVTT** | N/A | N/A |
| 112 – Y2 | N/A | FMC_MGT_TX_N | 33 | 34 | SD_CMD | 501 – C17 | 501 – C15 |
| N/A | N/A | **GND** | 35 | 36 | SD_D1 | 501 – A9 | 501 – B12 |
| 501 – D15 | 501 – D14 | SD_D0 | 37 | 38 | SD_D3 | 501 – B15 | 501 – B14 |
| 501 – E10 | 501 – F13 | SD_D2 | 39 | 40 | PS_LED1 | 501 - B14 | 501 - B13 |
| 501 – D11 | 501 – D16 | SD_CD | 41 | 42 | USB_UART_RXD | 501 – B12 | 501 – D12 |
| 501 – E9 | 501 – D14 | SD_CLK | 43 | 44 | USB_UART_TXD | 501 – C12 | 501 – C9 |
| N/A | N/A | **VCCO_13** | 45 | 46 | **VCCO_13** | N/A | N/A |
| N/A | N/A | PETH_PHY_LED0 | 47 | 48 | PETH_PHY_LED1 | N/A | N/A |
| N/A | N/A | **GND** | 49 | 50 | **GND** | N/A | N/A |
| N/A | N/A | PETH_MD1_P | 51 | 52 | PETH_MD2_P | N/A | N/A |
| N/A | N/A | PETH_MD1_N | 53 | 54 | PETH_MD2_N | N/A | N/A |
| N/A | N/A | **GND** | 55 | 56 | **GND** | N/A | N/A |
| N/A | N/A | PETH_MD3_P | 57 | 58 | PETH_MD4_P | N/A | N/A |
| N/A | N/A | PETH_MD3_N | 59 | 60 | PETH_MD4_N | N/A | N/A |
| N/A | N/A | **GND** | 61 | 62 | **GND** | N/A | N/A |
| N/A | N/A | USB_OTG_ID | 63 | 64 | PS_PB1 | 501 – B9 | 501 – C13 |
| N/A | N/A | **GND** | 65 | 66 | PS_ETHRST_N | 501 – B13 | 501 – D10 |
| N/A | N/A | USB_OTG_P | 67 | 68 | **USB_VBUS_OTG** | N/A | N/A |
| N/A | N/A | USB_OTG_N | 69 | 70 | USB_OTG_CPEN | N/A | N/A |
| N/A | N/A | **GND** | 71 | 72 | **GND** | N/A | N/A |
| 13-Y18 | 13-Y7 | PL_LED1 | 73 | 74 | PMOD1_D0_P | 13-Y9 | 13-AA16 |
| 13-Y19 | 13-Y6 | PL_LED2 | 75 | 76 | PMOD1_D0_N | 13-Y8 | 13-AA17 |
| N/A | N/A | **GND** | 77 | 78 | **GND** | N/A | N/A |
| 13-AA11 | 13-W10 | PMOD1_D1_P | 79 | 80 | PMOD1_D2_P | 13-U9 | 13-Y12 |
| 13-AB11 | 13-W9 | PMOD1_D1_N | 81 | 82 | PMOD1_D2_N | 13-U8 | 13-Y13 |
| N/A | N/A | **GND** | 83 | 84 | **GND** | N/A | N/A |
| 13-V11 | 13-W11 | PMOD1_D3_P | 85 | 86 | PCIE_RST_N | N/A | 13-V13 |
| 13-W11 | 13-Y11 | PMOD1_D3_N | 87 | 88 | PL_PB2 | N/A | 13-V14 |
| N/A | N/A | **GND** | 89 | 90 | **GND** | N/A | N/A |
| 13-W12 | N/A | MUX_D1_P | 91 | 92 | MUX_D0_P | N/A | 13-R17 |
| 13-W13 | N/A | MUX_D1_N | 93 | 94 | MUX_D0_N | N/A | 13-T17 |
| N/A | N/A | **GND** | 95 | 96 | **GND** | N/A | N/A |
| 13-V15 | N/A | MUX_D3_P | 97 | 98 | MUX_D2_P | N/A | 13-V16 |
| 13-W15 | N/A | MUX_D3_N | 99 | 100 | MUX_D2_N | N/A | 13-W16 |

**Table Legend colors:**

| | |
|---|---|
| Orange highlight: | SOM control signals |
| Red: | Power pins |
| Blue: | PicoZed 15/30 SOM only |
| **Bold Black:** | Ground pins |
| Black: | All other SOM pins. |

## 2.6 Multi-Gigabit Transceivers (MGTs)

The PicoZed 7015 and 7030 SOMs have four gigabit full-duplex transceiver lanes that reside on Bank 112 of the Zynq device. These high speed transceivers are used to interface to multiple high speed interface protocols such as PCI Express and FMC. In addition to the PCIe and FMC interface, they can interface the remaining available MGT pins to other high speed interfaces such as Ethernet, Serial ATA, etc....

The PicoZed 7015 is fitted with the XC7Z015-1CLG484 and is enabled with GTP transceivers which are capable of a transceiver data rate up to 3.75Gb/s. Speed grade devices of -2 or -3 are capable of data transceiver rates up to 6.25Gb/s.

The PicoZed 7030 is fitted with the XC7Z030-1SBG485 and is enabled with GTX transceivers which are capable of a transceiver data rate up to 6.6Gb/s. Speed grade devices of -2 or -3 are also capable of data transceiver rates up to 6.6Gb/s in the SBG package.

Two differential MGT reference clock inputs are available for use with the GTP/GTX lanes. Either clock input can be used as the clock reference for any one or more of the GT lanes in bank 112. This allows the user to implement various protocols requiring different line rates.

Gigabit transceiver lanes and their associated reference clocks are connected to the carrier board via the JX3 Micro Header. The table below shows the MGT connections between the Zynq device and the JX Micro Header.

**Table 14 – MGT Pin Assignments**

| GTP/GTX | Net Name | Zynq Pin | JX3 Pin |
|---|---|---|---|
| MGT0 | PCIE-TX0_P | AA3 | JX3.13 |
| | PCIE-TX0_N | AB3 | JX3.15 |
| | PCIE-RX0_P | AA7 | JX3.8 |
| | PCIE-RX0_N | AB7 | JX3.10 |
| MGT1 | MGTTX1_P | W4 | JX3.19 |
| | MGTTX1_N | Y4 | JX3.21 |
| | MGTRX1_P | W8 | JX3.14 |
| | MGTRX1_N | Y8 | JX3.16 |
| MGT2 | MGTTX2_P | AA5 | JX3.25 |
| | MGTTX2_N | AB5 | JX3.27 |
| | MGTRX2_P | AA9 | JX3.20 |
| | MGTRX2_N | AB9 | JX3.22 |
| MGT3 | FMC_MGT_TX_P | W2 | JX3.31 |
| | FMC_MGT_TX_N | Y2 | JX3.33 |
| | FMC_MGT_RX_P | W6 | JX3.26 |
| | FMC_MGT_RX_N | Y6 | JX3.28 |
| MGT_REFCLK0 | MGTREFCLK0_P | U9 | JX3.1 |
| | MGTREFCLK0_N | V9 | JX3.3 |
| MGT_REFCLK1 | MGTREFCLK1_P | U5 | JX3.2 |
| | MGTREFCLK1_N | V5 | JX3.4 |

### 2.6.1 MGT Clock Synthesizer

The MGT clock is generated by using U12, a Texas Instruments CDCM61002RHB programmable clock synthesizer IC. Switches SW9 and SW10 set the clock output frequency. The clock output, OUT1_P/N is routed to U14, a clock multiplexer and is passed through to JX3. OUT0_P/N are also available via J15/J16 SMA connectors. The default frequency for the synthesizer is set to 62.5000MHz. Due to the number of output frequency settings available with this IC, the user should consult the Texas Instruments web site to view all possible combinations if a frequency other than 62.5000MHz is desired.
www.ti.com → Search CDCM61002

**Table 15 – Synthesizer switch settings**

| CDCM61002 SW9, SW10 FREQ SELECTION TABLE | | | | | | | |
|---|---|---|---|---|---|---|---|
| FREQ - MHz: | SW9.1 (PR1): | SW9.2 (PR0): | SW10.1 (CE): | SW10.2 (OD2): | SW10.3 (OD1): | SW10.4 (OD0): | Interface USE: |
| 62.5000 | OFF | OFF | OFF | OFF | OFF | OFF | GigE |
| 100.0000 | ON | ON | OFF | OFF | ON | OFF | PCI Exp |
| 125.0000 | OFF | OFF | OFF | ON | OFF | OFF | GigE |
| 156.2500 | OFF | ON | OFF | ON | OFF | OFF | 10 GigE |
| 200.0000 | ON | ON | OFF | ON | OFF | ON | PCI Exp |
| 250.0000 | OFF | OFF | OFF | ON | ON | OFF | GigE |
| NOTE: For all other frequencies please see the TI datasheet | | | | | | | |
| Note: "ON" position labeled on switch; "ON" = a logic low on CDCM pin | | | | | | | |
| Note: "OFF" position = a logic high on CDCM pin | | | | | | | |

### 2.6.2 MGT Clock Multiplexer

The MGT clocks (MGTCLK_SYNTH_P/N) are multiplexed with the FMC_GBTCLK_P/N clocks via U14, a SY89853U low jitter, high speed IC. This configuration allows the user to choose which source the MGT reference clocks (MGTREFCLK1_P/N) are to be driven by. JP6 is used to select whether the source is to be FMC or MGT Synthesizer. The default setting is JP6 off, which selects the FMC clock as the source. JP6 does not require an external pullup resistor as the IC has an internal 25K.

### 2.6.3 SMA Data input

The PZCC-FMC has four MGT Data SMA connectors for differential TX and RX Data connections. These I/O are DC blocked via in line capacitors and terminated at 100 ohms. The data connections are listed in **Table 14 – MGT Pin Assignments**.

## 2.7 USB UART – J6

The PZCC-FMC implements a USB-to-UART bridge connected to a PS UART peripheral. U5 is a Silicon Labs CP2104 USB-to-UART Bridge device and allows connection to a host computer via USB. The CP2104 connects to the USB Micro AB connector, J6, (FCI 10104111-0001LF). Only basic TXD/RXD connection is implemented.

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers which permit the CP210x USB-to-UART bridge to appear as a COM port to host computer communications application software (for example, HyperTerm or Tera Term). Please refer to the *Silicon Labs CP210x USB-to-UART Setup Guide* available at www.picozed.org. Note that each CP2104 ships with a unique ID and appears as a unique device when connected to a PC. Windows will enumerate multiple PicoZed FMC Carrier boards with a unique COM port for each one. This means that multiple PicoZed FMC Carriers can be connected to a single PC without issue.

The uart1 Zynq PS peripheral is accessed through MIO Bank 1/501 (1.8V). The CP2104 features adjustable I/O voltage, so it is connected directly to Zynq.

**Table 16 – CP2104 Connections**

| UART Function | Schematic Net Name | JX3 Pin # | PicoZed 7010/7020 Bank-Pin # | PicoZed 7015/7030 Bank-Pin # |
|---|---|---|---|---|
| TXD | USB_UART_TXD | 44 | 501 – C12 | 501 – C9 |
| RXD | USB_UART_RXD | 42 | 501 – B12 | 501 – D12 |

### 2.7.1 USB circuit protection

USB data lines, D+/-, are ESD protected with Bourns Steering Diodes, CDSOT23-SR208.

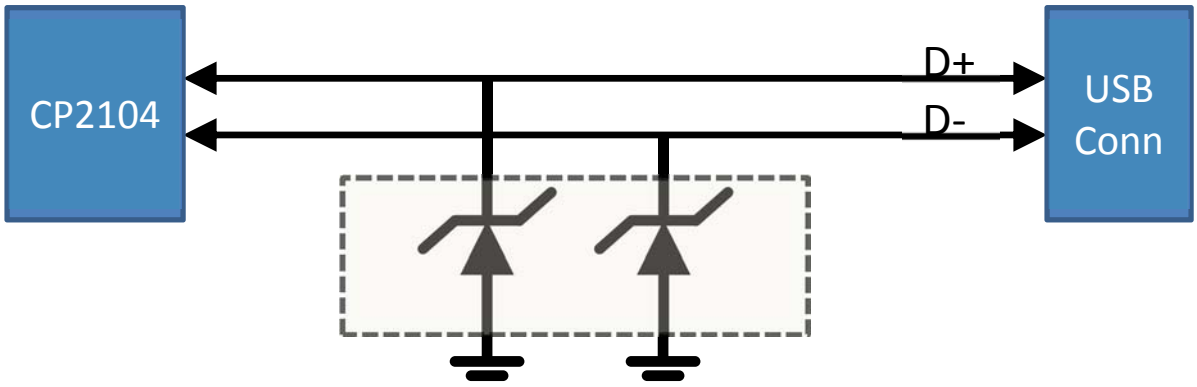



**Figure 6 – ESD Protection**

## 2.8 USB OTG Interface – J5

A USB OTG connector is routed to the SOM via header JX3 pins 63, 67, 69 and 70. In USB OTG Host mode, this interface can source VIN_HDR power onto the USB_VBUS rail via power switch (U15) and active high control signal USB_OTG_CPEN (JX3.70). This signal is level translated from SOM 3.3V to VIN_HDR via Q18 as shown below. The USB_OTG_ID signal is brought out to JX3.63 to allow Host or Device selection. When grounded the interface is in host mode, when floating the interface is in device mode.

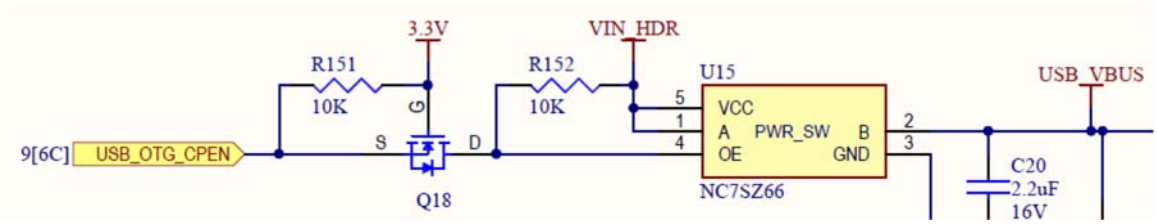



**Figure 7 – USB Interface control**

### 2.8.1 USB Interface protection

The 2.0 OTG interface include D15, a PolyZen PN ZEN056V130A24LS 1.3 Ampere Zener clamp to clamp any excessive voltage on the USB_VBUS and USB5V0 J5 interface rail. This diode will begin conducting when the voltage on the USB_VBUS line exceeds 5.6V and is capable of sinking up to 1.3 amps. The Data Plus and Data Minus (USB_OTG_P/N) lines are also ESD protected using a Bourns Steering Diodes, CDSOT23-SR208 as depicted in the following figure.

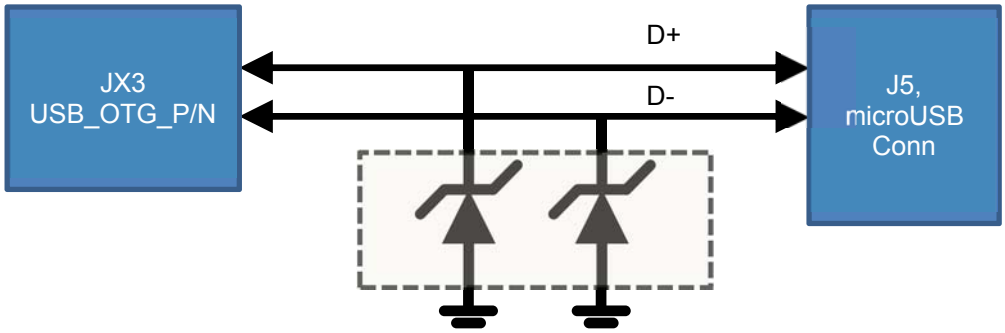
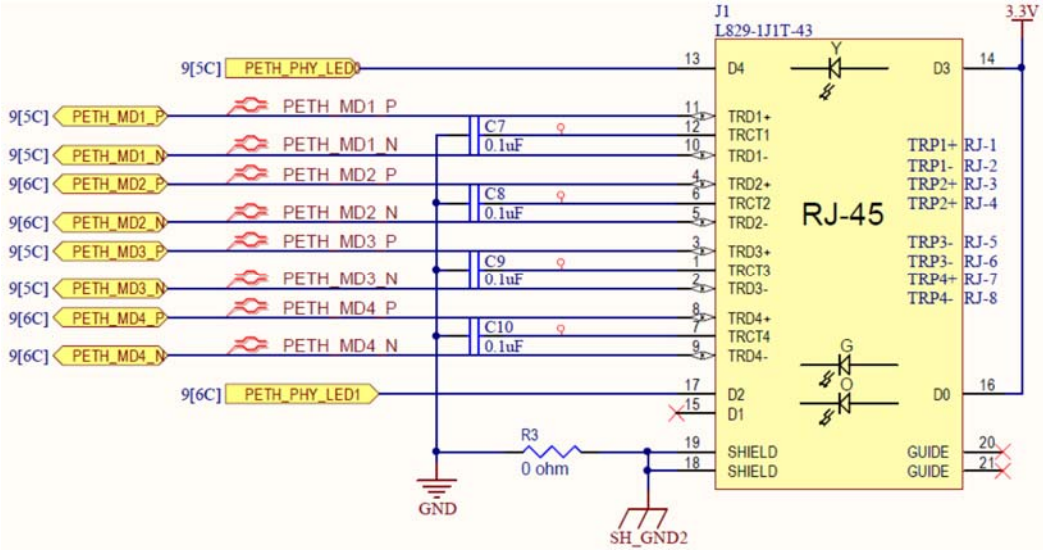



**Figure 8 – ESD Protection**

## 2.9 SOM 10/100/1000 Ethernet RJ45 – J1

J1 is a SOM driven Ethernet port. The connector is a MagJack L829-1J1T-43 and contains integrated magnetics and two LEDs for connection indication. The left side LED[1] is green and indicates link status while the right side LED[0] is amber and indicates link activity.




The SOM's PHY is routed through JX3 directly to J1. For this reason, the PHY is configured via the SOM. The PZCC-FMC net names for this connector interface begin with PETH and are listed in

Table 13 – JX3 Connections.

## 2.10 10/100/1000 Ethernet PHY – J11

Like port J1, the connector on this port uses the MagJack L829-1J1T-43 integrated magnetics and LED part. The LED operation is the same as J1 in paragraph 0. J11 is connected via JX2 and an on-board Marvell 88E1512 PHY. The PHY connects to Bank 13 and interfaces to the Zynq-7000 AP SoC via RGMII. There are two methods in which to interface to J11 from the SOM, PS and PL. The below sections detail the implementation method types.

### 2.10.1 PS interface:

A GEM1 MAC interface is used in the ARM core and is routed as the GMII interface. A RGMII shim is then used to connect the GMII to the PHY's RGMII interface.

### 2.10.2 PL interface:

The PL requires a soft TMAC IP core. This core is connected via the AXI interface to the processor. The TMAC core allows you to select an RGMII interface, thus negating the need for a shim.

### 2.10.3 Base Address

The Marvell 88E1512 PHY Address (PHYAD) is a 5-bit value. PHYAD[4:1] are fixed at 0000. PHYAD[0] is set based on the status of the CONFIG pin after the de-assertion of RESETn. For both the SOM and the PZCC-FMC, the CONFIG pin is tied through a zero-ohm resistor (R80) to VSS/GND. This signals the 88E1512 to configure two things:

- PHYAD[0] = 0
- VDDO_LEVEL = 3.3V

A high-level block diagram the 10/100/1000 Ethernet interface is shown in the following figure.

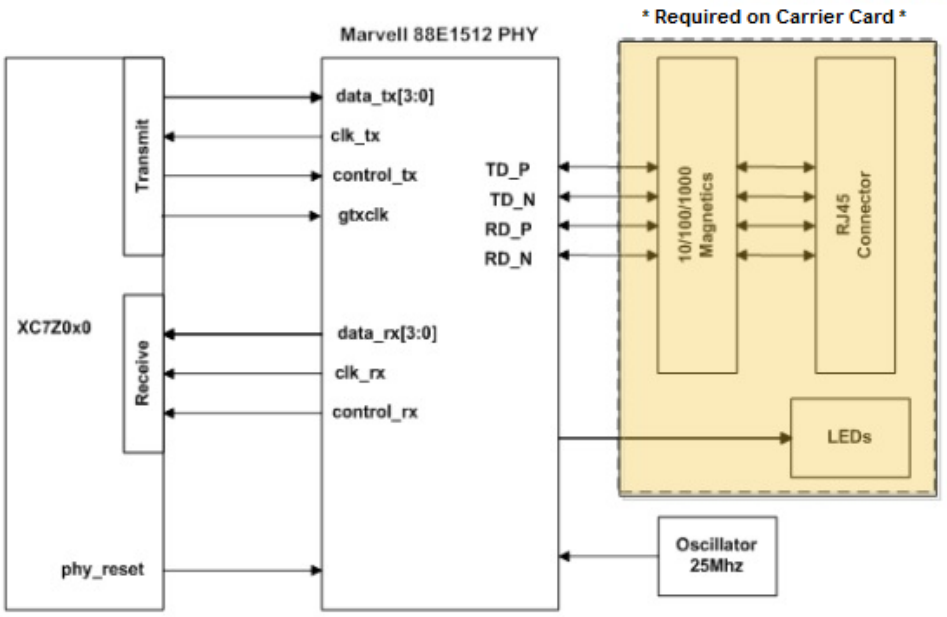



**Figure 9 – 10/100/1000 Ethernet Interface**

Zynq requires a voltage reference for RGMII interfaces. Thus PS_MIO_VREF, E11, is tied to 0.9V, half the bank voltage of MIO Bank 1/501. The 0.9V is generated through a resistor divider.

The PHY's reset is ANDed with the PG_MODULE signal and the PS_ETHRST_N signal. This allows the user to assert a reset or the board to assert a reset when powering up. MOSFETs Q6-Q9 are placed to prevent backfeed from the RJ-45's 3.3V LED source. U10, a 1.8V 25.0000MHz clock is used in the default configuration and R83 is for development purposes only and is not fitted by default.

**Table 17 – J11 Ethernet PHY Pin Assignment and Definitions**

| Signal Name | Description | JX pins | PicoZed 7020 Bank & Pin # | PicoZed 7015/30 Bank & Pin # | 88E1512 pin |
|---|---|---|---|---|---|
| ETH_RX_CLK | Receive Clock | JX2.94 | 13 - V11 | 13 – AB18 | 46 |
| ETH_RX_CTRL | Receive Control | JX2.96 | 13 - V10 | 13 – AB19 | 43 |
| ETH_RXD[3:0] | Receive Data | RXD3: JX2.99<br>RXD2: JX2.97<br>RXD1: JX2.95<br>RXD0: JX2.93 | 13 - W6<br>13 - V6<br>13 - Y13<br>13 - Y12 | 13 – AA20<br>13 – AA19<br>13 – AB22<br>13 – AB21 | 44<br>45<br>47<br>48 |
| ETH_TX_CLK | Transmit Clock | JX1.92 | 13 - T5 | 13 – V18 | 53 |
| ETH_TX_CTRL | Transmit Control | JX1.94 | 13 - U5 | 13 – W18 | 56 |
| ETH_TXD[3:0] | Transmit Data | TXD3: JX1.93<br>TXD2: JX1.91<br>TXD1: JX1.89<br>TXD0: JX1.87 | 13 - W8<br>13 - V8<br>13 - V7<br>13 - U7 | 13 – V19<br>13 – U19<br>13 – AA15<br>13 – AA14 | 50<br>51<br>54<br>55 |
| ETH_MDIO | Management Data | JX1.90 | 13 - U10 | 13 – Y15 | 8 |
| ETH_MDC | Management Clock | JX1.88 | 13 - T9 | 13 – Y14 | 7 |
| PS_ETHRST_N | PHY Reset | JX3.66 | 501 – B13 | 501 – D10 | 16 ** |

** Requires a resistor change to the board to use PHY Reset. By default MIO47 is routed to JX3.

The datasheet for the Marvell 88E1512 is not available publicly. An NDA is required for this information. Please contact your local Avnet or Marvell representative for assistance.

## 2.11 HDMI Interface – J10

The PZCC-FMC has a HDMI V1.4 and DVI V1.0 video output port, J10. This port is based on the Analog Devices ADV7511 225MHz HDMI transmitter IC, capable of transmitting up to 1080p resolution video. The port is a 16 bit interface, using data signals ADV7511_D20:ADV7511_D35 and is routed to microheader JX2. Refer to **Table 12 – JX2 Connections** for the pin assignments.

The IC is configured via the I2C interface at address 0x72, based on the PD pin being pulled low. The user can assert this signal prior to change the address to 0x7A.

LED D9 is used to indicate a Hot Plug Detect signal when a valid HDMI connection is made. D9 will turn on when this occurs. CEC Oscillator U8, Discera PN DSC1001AE2 – 012.0000 is not fitted by default but has the footprint in the event a user wishes to clock from this low noise source.

All power supplies are triple filtered to this device using ferrite beads, inductors and capacitors to ensure low EMI emissions. Additionally, the data signals to J10 are ESD protected using ESD protection diodes. The CEC signal is protected using a varistor per Analog Devices design recommendations.

Please refer to Analog Devices ADV7511 datasheet, Hardware User's Guide and Programming guide at www.analog.com for detailed information. The ADI EngineerZone is also a very useful source of information -- https://ez.analog.com/welcome.

## 2.12 JTAG Configuration – J12 PS and J8 FMC

Two JTAG interface ports are provided on the PZCC-FMC. One is dedicated to the FMC interface, J8, and the other to the SOM, J12. A Xilinx JTAG platform cable (HW-USB-II-G) or a Digilent JTAG HS2 or HS3 programming cable should be used when programming via these ports.

The diodes on the VREF pin 2 of each connector are used to prevent the JTAG cable from back feeding into the PZCC-FMC 3.3V power supply.

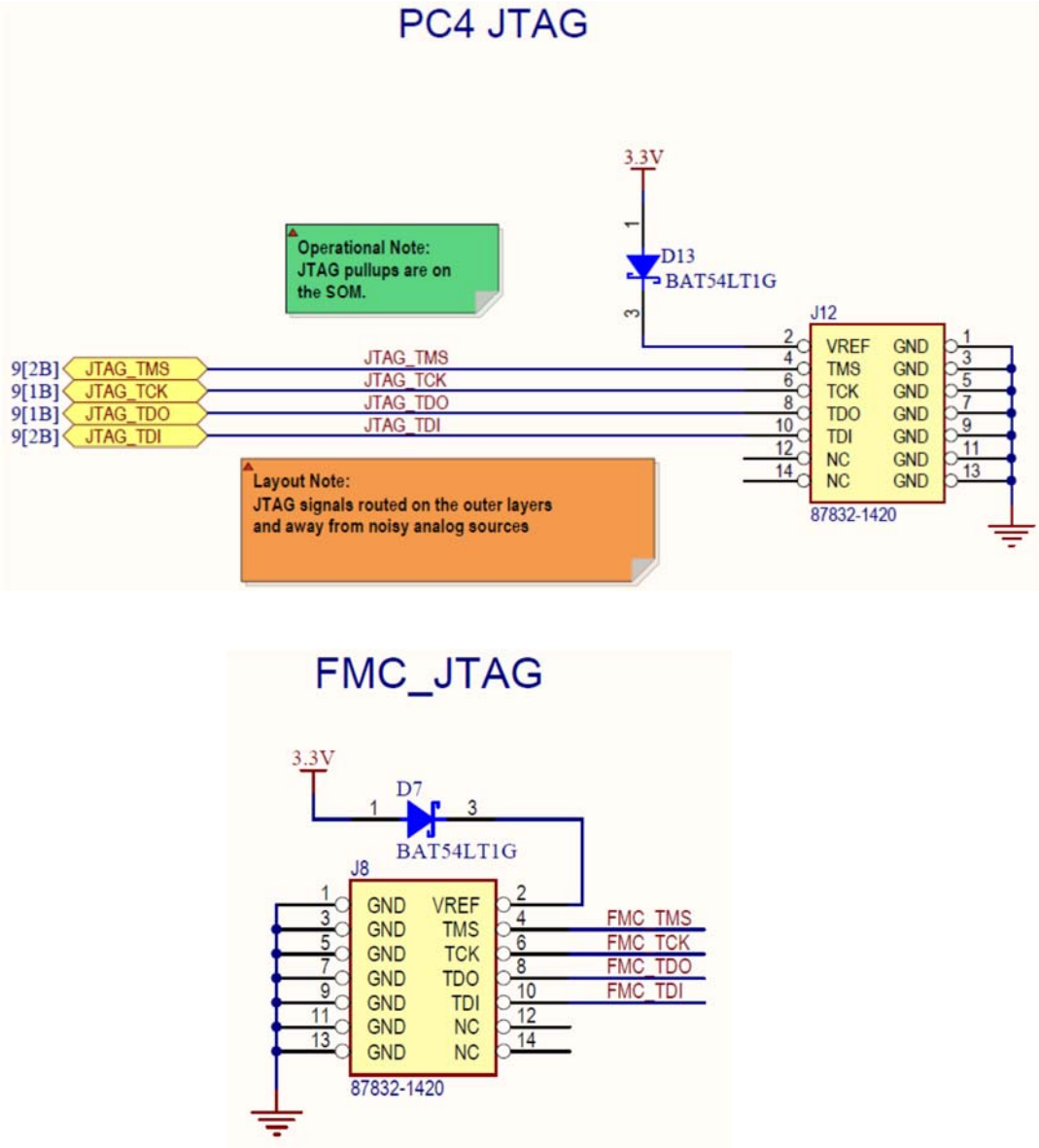
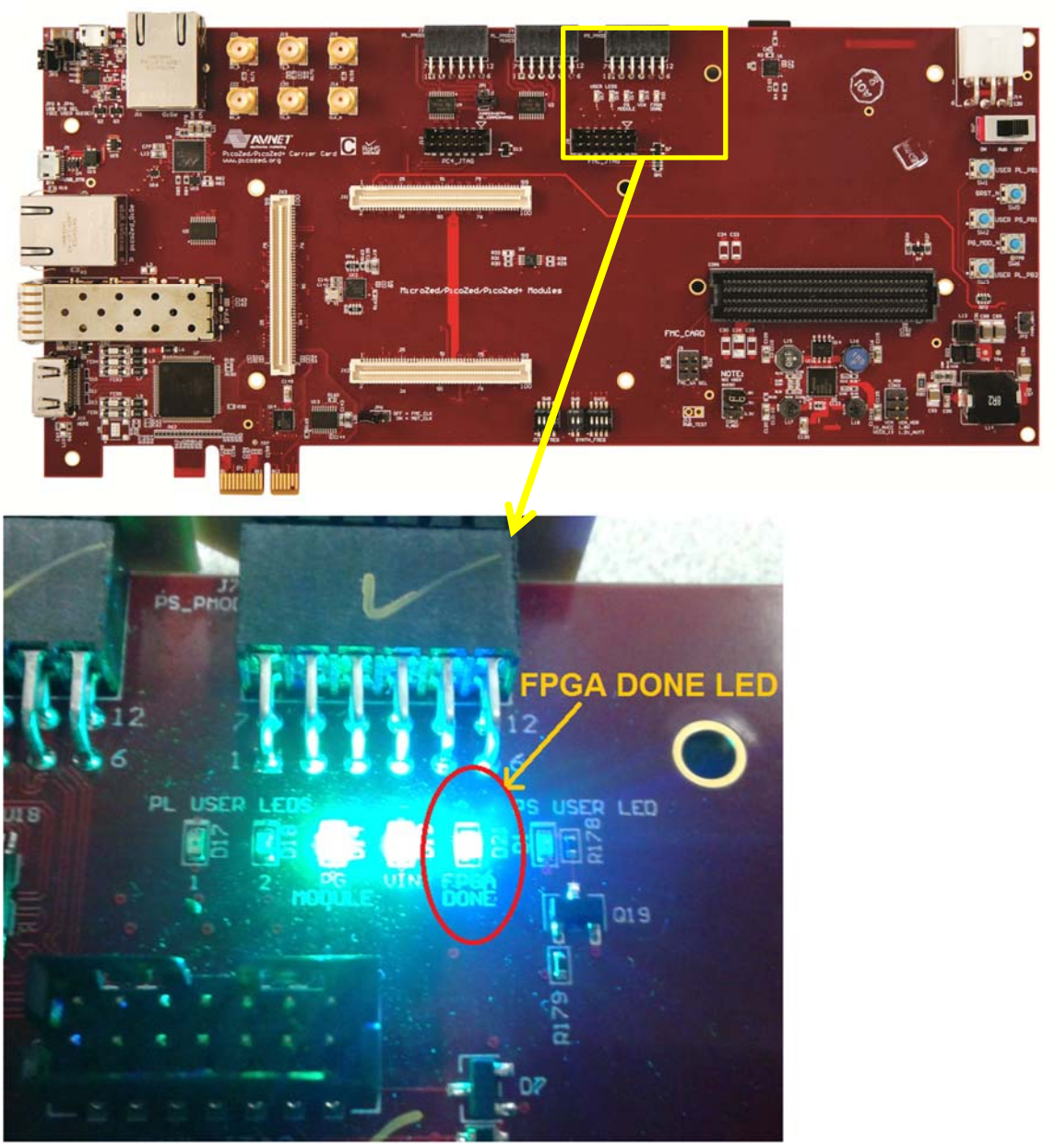



**Figure 10 – PC4 and FMC JTAG Connections**

### 2.12.1 FPGA DONE LED – D21




A blue DONE LED (D21) is connected to the Zynq SOM via JX1.8, net name FPGA_DONE and is located on Bank 0, R11 of the FPGA. When the SOM's PL is properly configured this pin is driven high by the FPGA which turns the DONE LED on.

## 2.13 Power

### 2.13.1 Power Input – J14/SW7

The board is powered through J14 and SW7 power switch. Slide SW7 to the left to turn on the board. Sliding SW7 to the right turns off the board. J14 is a 12V 2x3 6 pin connector which is NOT ATX compatible. While the board can accommodate up to 17VDC in, to maintain FMC compliance the maximum input voltage should not exceed 13.2V, (12V +10%) to minimize component stress thereby increasing the products operational life.

D22 and D23 are used for power steering in the event the user wants to insert the board into a PCIe x1 slot for development purposes.

The maximum input current is limited by filter L13, which has a rating of 5.0 Amps. Any current exceeding this value will damage the filter network. The power supply shipped from Avnet is Avnet part number AES-SLP-12V5A-G. rated at 12V, 5.0 Amps and is recommended for use with the PZCC-FMC board.

- Primary 12V 5A, 2x3 connector.
- NOTE: this connector is NOT ATX compatible.

### 2.13.2 Power Rails

**Table 18** lists the power circuits for the PZCC-FMC carrier card. The table shows the voltage rails, currents, and tolerances.

**Table 18 – Voltage Rails w/ Current Estimates**

| Voltage (V) | Tolerance | IC | Max DC current | Functional area |
|---|---|---|---|---|
| 12V Input | 10% | Wall adapter, NOT ATX compatible | 5.0A | All power |
| 5V | 5% | REG1, MAX15066 | 3.0A | SOM VIN Header |
| VADJ - 1.8V, 2.5V or 3.3V For SOM VCCIO 13, 34, 35 **NOTE: For 7030 SOMs VADJ MUST be set to 1.8V ONLY!** | 1.5% | U11, ADP50502, CH3 | 1.2A | PZCC-FMC & SOM VCCIO banks: 34, 35. |
| 3.3V | 1.5% | U11, ADP50502, CH2 | 3.0A | PZCC-FMC logic, Pmod, Ethernet, Vcco_13, LEDs |
| 1.0V_AVCC | 1.5% | U11, ADP50502, CH1 | 3.2A | SOM MGT Core |
| 1.2V_AVTT | 1.5% | U11, ADP50502, CH4 | 1.2A | SOM MGT |
| 1.8V | 1.5% | U11, ADP50502, CH5 | 200mA | microSD level translator, HDMI |

### 2.13.1 VADJ selection

VADJ rail is configurable via CON2 (see below). VADJ is an independent rail supplying power to the Zynq PL I/O banks and connected Pmods. VADJ drives banks 34 and 35**.** **WARNING: When using a 7030 SOM, VADJ MUST remain at the 1.8V setting otherwise the SOM will be damaged!** **Table 18** shows the voltage rails, currents, and tolerances.

**Table 19 – VADJ Selection Table (CON2)**

| CON2 Jumper Position (pins) | VADJ |
|---|---|
| 1-2 or Open | 1.8V |
| 3-4 | 2.5V |
| 5-6 | 3.3V |

### 2.13.2 Sequencing

- PWR_EN signal, active high, JX1.5, allows the carrier to turn on or off the PicoZed power supplies. R103 and C92 have been placed to adjust the timing of this signal during power off conditions. This signal should not be de-asserted until VCCIO_EN is de-asserted. In the carrier off condition (power plug removed or power switch turned off), this signal is driven low.

- VCCIO_EN signal, active high, JX2.10, originates on the PicoZed and is the output of the 1.8V regulator, PG_1V8. This signal enables the carrier's 3.3V supply, which in turn enables the VADJ regulator. When the carrier is turned off (power switch turned off or power plug removed) or the PicoZed's PG_1V8 signal is de-asserted VCCI_EN is driven low, which turns off the FMC-CC and the PicoZed.

- PG_CARRIER signal, active high, JX2.11, is pulled up by PicoZed's +3.3V PG_MODULE signal. This signal can be pulled low by the carrier board (SW4), the FMC board or the PicoZed when the board's power circuitry is not 'Good' yet.

- The following diagram illustrates the power supply sequencing on power up. Note Vin and PWR_Enable can come up simultaneously, but shown staggered as PWR_Enable can come up later.

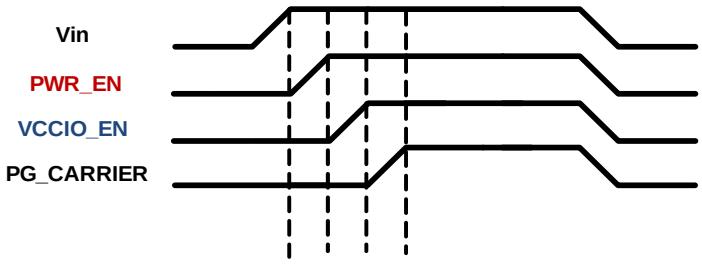



**Figure 11 – Power Sequencing**

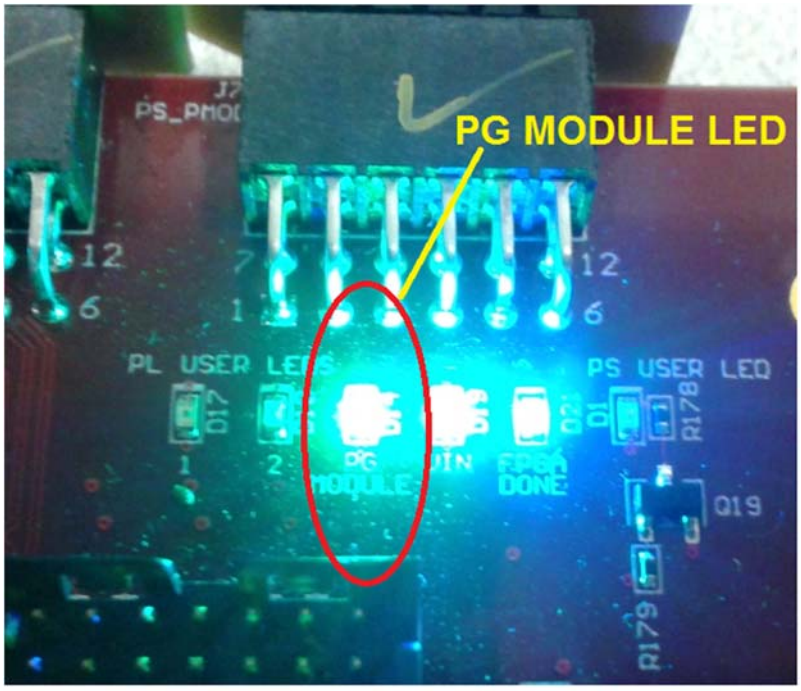
The PG_CARRIER (on PZCC-FMC) and PG_MODULE (on PicoZed) signals are wired OR and tied to the Zynq Power On Reset signal. When the power supplies are valid on both the SOM and carrier, the PG signal de-asserts the Zynq POR signal.

### 2.13.3 Bypassing/Decoupling/Filtering

The PZCC-FMC follows the recommended decoupling and layout techniques per each manufacturer's datasheet.

### 2.13.4 PG Module Power Good LED

A green status LED, D14, illuminates when PG_CARRIER signal is high (good).



# 3 Jumpers, configuration and test points:

The below table is a quick reference to all of the jumpers, configuration settings and test points on the FMC. For detailed information, refer to the appropriate sections in this document.

**Table 20 – Settings**

| Reference Designator | Name | Default | Notes: |
|---|---|---|---|
| JP1 | PMOD or SFP+ SEL | Open (PMOD selected) | Select PMOD or SFP+ interface to be used. |
| JP2 | FPGA_VBAT_TEST | Open | Install a 1.5V battery here to maintain FPGA configuration when board is unpowered. |
| JP3 | USB Mode select | 1-2 shorted = Host Mode | Selects Host or Device mode for the USB OTG circuit. |
| JP4 | USB Mode supplement | shorted = Host Mode | Selects the capacitors for USB OTG circuit. Must be closed for USB OTG compliance. |
| JP6 | CLK MUX select | Open | Open=FMC CLK, Short=MGT CLK |
| J15, J16 | LVDS_CLK P/N1 | Populated | MGT CLK SMA output |
| J19, J20 | MGTX1_P/N | Populated | MGT SMA TX DATA |
| J21, J22 | MGTRX1_P/N | Populated | MGT SMA RX DATA |
| J1 | SOM GiGE CONN | Populated | SOM driven GiGE connector. |
| J2 | Micro SD Card Cage | Populated | MicroSD Card socket |
| J3 | PL PMOD1 | Populated | PL PMOD1 for SOMs 7015/20/30 interface. |
| J4 | PL PMOD2 | Populated | PL PMOD2 for SOMs 7015/30 interface. Muxed with SFP+ connector. |
| J6 | USB UART | Populated | Micro USB UART connection. |
| J7 | PS PMOD | Populated | SOM Processor PMOD interface. |
| J8 | FMC JTAG | Populated | FMC peripheral JTAG interface. |
| J11 | GiGE RJ-45 | Populated | Active Gigabit Ethernet RJ-45. |
| J12 | PC4 JTAG | Populated | SOM JTAG interface. |
| P2 | SFP+ | Populated | SFP+ interface muxed with PL PMOD2. |
| CON1 | FMC | Populated | Low Pin Count FMC Interface. |
| JT1 | UART Power Mode select | Pins 2-3 0 ohm | Selects USB bus power or internally powered . |
| J9 | FMC GA [1:0] | Set to 00 | FMC address select. Use jumper headers for selection. |
| J10 | HDMI | Populated | HDMI header attached to AD7511 HDMI transmitter. |
| J5 | USB OTG | Populated | USB 2.0 OTG microheader. |
| J13 | VCCIO_EN | Open | Short to test the PZCC-FMC power supplies while SOM not installed. Normal operation leave this open. |
| J14 | +12Vin | N/A | +12V input |
| SW1 | PL_PB1 | Populated | PL User pushbutton input. See section 2.2. |
| SW2 | PS_PB1 | Populated | PS User pushbutton input. See section 2.2. |

| | | | |
|---|---|---|---|
| SW3 | PL_PB2 | Populated | PL User pushbutton input. See section 2.2. |
| SW5 | CARRIER SRST N | Populated | Assert a carrier board reset. See section 2. |
| SW6 | PG MODULE N | Populated | Assert a PG MODULE reset. See section 2. |
| SW7 | PWR SWITCH | Off | Use to turn on board. Left = on, right = off. |
| SW8 | PCIe Jitter Freq. select | SW1.1, .2, = off, SW1.3 = on | PCIe jitter attenuator frequency select. |
| SW9 | PCIe prescalar select | Off | Prescalar select |
| SW10 | PCIe Freq. select | Off | Use to select PCIe frequency |
| CON2 | VADJ | Open or 1-2: 1.8V<br>3-4: 2.5V<br>5-6: 3.3V | Used to select 1.8V, 2.5V or 3.3V VADJ level for the SOM VCCIO Banks 34 and 35 as well as the FMC connector. **NOTE: 7030 SOMs MUST be set to 1.8V only!** |
| CON3 | VOLTAGE MONITOR | Not Populated | Use the 0.1" holes to measure the voltage of each rail. |
| P1 | PCIe Edge | Populated | PCIe x1 Edge Connector. |
| TP1-4 | USB UART GPIO TP | Populated | UART GPIO pads |
| TP5-6 | PCIe 12V | Populated | 12V PCIe voltage pads |
| TP7 | PCIe_WAKE_N | Populated | PCIe Wake signal pad. |
| TP8 | PG_MODULE | Populated | PG Module signal pad. |

### 3.1.1 FMC GA [1:0] jumper header

The carrier allows the user to select the FMC board address via J9 and 2 jumper headers. The address range is from 0 to 3 via jumper headers. The jumpers force a high or a low on address bits 1 or 0. Default FMC address is 00 where the jumpers are placed at location 3-5 and 4-6 on J9.

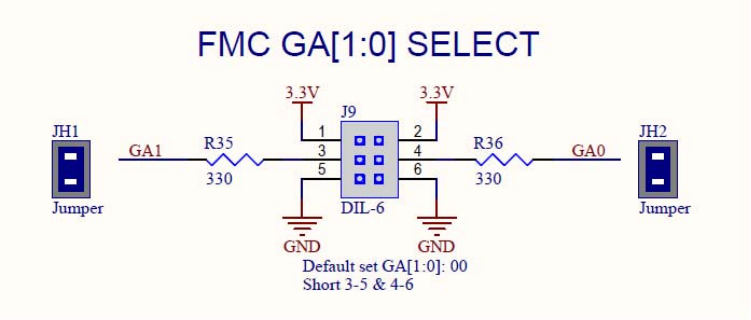



**Table 21 – FMC GA [1:0] address select**

| Carrier Net Name | FMC LPC CON2E connection |
|---|---|
| GA0 | C34 |
| GA1 | D35 |

### 3.1.2 Power Supply monitor header.

The PZCC-FMC has a power supply monitor connection. While this is primarily for testing, it can be accessed by the user to monitor the voltage levels on the PZCC-FMC. Figure 12 shows the available voltage monitor points.

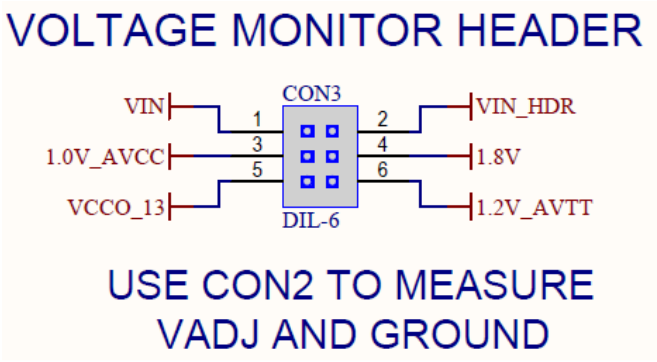



**Figure 12 – Voltage Monitor Connections**

# 4 Mechanical

## 4.1 Diagram and Model

A mechanical diagram and a 3D Model for the PZCC-FMC are available for download at **www.picozed.org** → **Documentation** → **PicoZed FMC Carrier Card** under the ***Mechancial Drawings*** heading.

## 4.2 Weight

The weight of the PZCC-FMC with rubber feet, SD card, and jumpers populated and without the faceplate or SOM attached is 155 grams (5.47 ounces).

# 5 Revision History

| Rev date | Rev # | Reason for change |
|---|---|---|
| 8 APR 2015 | 1.0 | Initial release |
| 9 SEP 2015 | 1.1 | Made corrections to 7015/7030 pinouts in Tables 3, 4, 8, 11, 12, 13, and 17 |
| | | |