

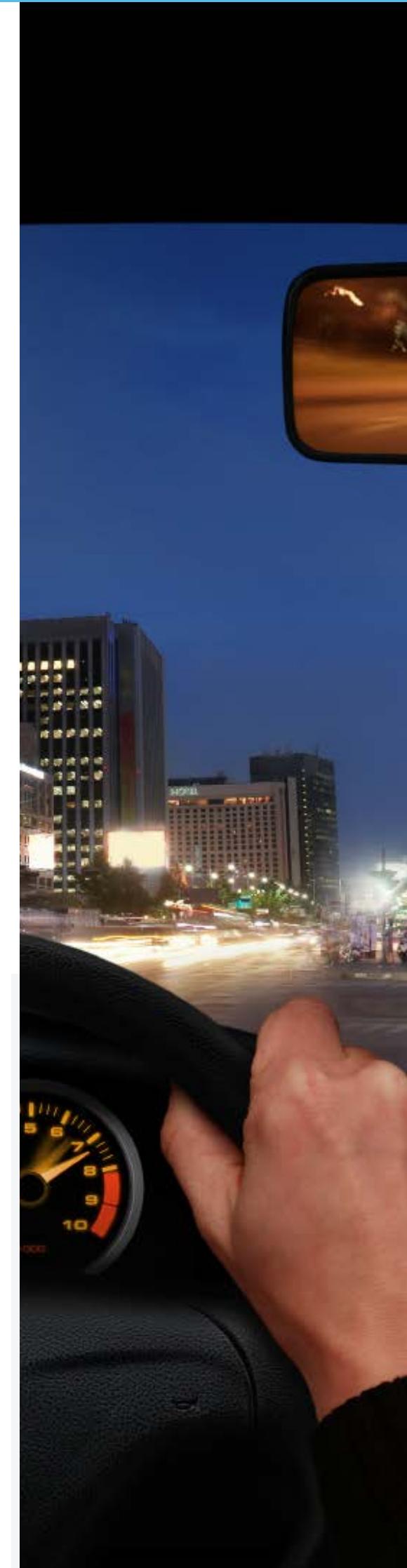
ALL PROGRAMMABLE SOLUTIONS FOR AUTOMOTIVE SYSTEMS





TABLE OF CONTENTS

Silicon	4-5
Software / Tool Chain	6-7
Solutions	
Applications	8-11
Intellectual Property (IP)	12
AUTOSAR	13
Functional Safety	14
Ecosystem	15
XA Product Line	16-19



As Xilinx celebrates more than 30 years, 3,500 patents and 6,500 industry firsts, we also reflect on the remarkable progress of automotive technology over the same period. Nothing has been more transformative to the automobile than the electronics revolution which includes the introduction of the microprocessor into nearly every vehicle system from entertainment to engine controls. Software programmability has also resulted in a geometric progression of vehicle capability which has greatly enhanced the driver and passenger experience.

As millions of lines of software code become commonplace in many automotive systems, the next evolutionary surge of programmable electronic platforms is underway. This next frontier stems from the desire for the connected car that sees, understands, reacts, and communicates intuitively with the outside world and vehicle occupants; keeping them safe, informed, productive, and entertained.

The system flexibility and processing throughput, required for this next big step is exceeding what can practically be achieved in traditional software programmable embedded processors. Fixed hardware processors and application specific devices are giving way to all programmable devices and systems, where dynamic configuration and optimization of system hardware will be achieved with the same ease that system designers now take for granted in the software domain. This may seem far-fetched to some, but so did a million lines of embedded code in the early days of 8-bit controllers programmed in assembly language.

Xilinx is at the forefront of this new challenge; reinventing and producing all programmable devices, SoCs, design tools, and – with our partners – the application solutions needed to realize the next generation of automotive electronic systems including Infotainment, Driver Information, and Advanced Driver Assistance Systems. Welcome to the future of automotive electronics.



Nick DiFiore
Director Automotive Segment
Xilinx Inc.

Xilinx 30 Year History

- 1984 — Founding of Xilinx
- 1985 — Xilinx launched first LCA XC2064
- 1989 — Xilinx went public on NASDAQ and launched first low-cost Spartan FPGA family
Xilinx launches first low-cost FPGA family: Spartan™
- 2002 — Xilinx introduced Virtex-II® Pro FPGAs with integrated high-speed transceivers and PPC405 hard-IP2004
- 2004 — Xilinx launched Automotive (XA) product line
- 2008 — Xilinx introduced Automotive-specific Solutions (hardware + software + IP + boards to address focus application)
- 2010 — Xilinx introduced 7 Series product line (28nm)
- 2011 — Xilinx launched first Zynq™ All Programmable SoC
- 2013 — Xilinx launched first XA 7 Series

XA Zynq-7000 All Programmable SoC

The XA Zynq-7000 All Programmable SoC supports a homogeneous software-centric architecture with optimal hardware and software partitioning for functional acceleration. Capable of both serial processing in the ARM® Cortex®-A9 cores, and parallel processing in the programmable logic, this device boosts overall system performance by more than 130% compared with traditional multi-chip solutions. There are over 3000 high-bandwidth low-latency interconnects between the processing system and programmable logic sides of the XA Zynq-7000 All Programmable SoC, allowing for massive throughput of data that eclipses the bandwidth capabilities of multi-chip systems.

Dedicated Automotive Product Line

Xilinx offers the most comprehensive, fully automotive-qualified FPGA and All Programmable SoC product lines in the market. With a wide variety of densities, packages and extended temperature grades, Xilinx began the XA (Xilinx Automotive) program in 2004, and has become the world's leading supplier of automotive-grade programmable logic devices. The flexibility and scalability of the XA product line enables Xilinx customers to develop customized platforms to meet the demands for greater product differentiation and innovation. With the recent addition of the Zynq-7000 All Programmable SoC to the XA product line, Xilinx has revolutionized the automotive semiconductor industry with the first hardware and software programmable device to address the technical and business challenges for one of the fastest growing automotive applications: Advanced Driver Assistance Systems (ADAS).

These automotive-grade devices deliver increased system performance through a highly integrated architecture utilizing a hardened dual-core ARM processing system, coupled with programmable logic including DSP blocks for hardware acceleration, all on a single monolithic chip. The insatiable need for more bandwidth and performance, along with the programmable imperative, has arrived to the automotive market, and Xilinx's XA product line continues to lead the way.

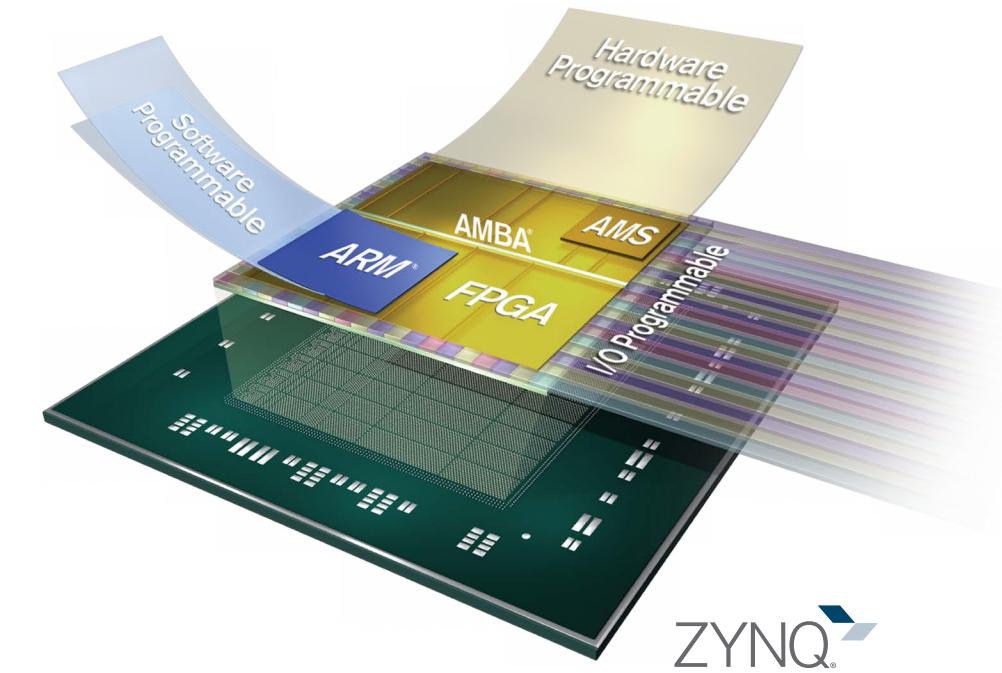
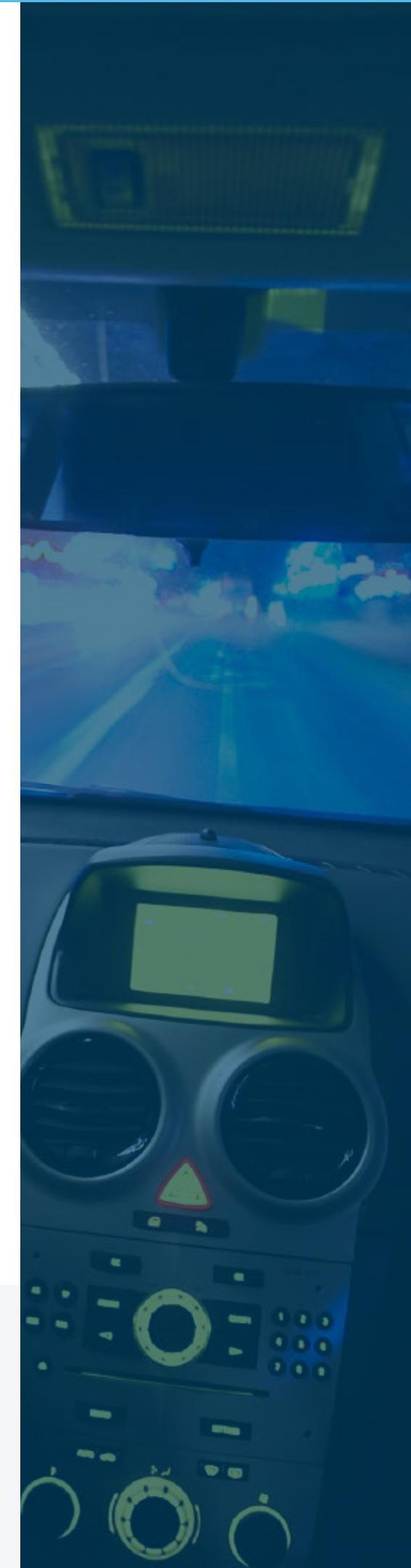
Beyond the AEC-Q100

Xilinx began its Xilinx Automotive (XA) program by testing according to the automotive AEC-Q100 qualification standard. However, it quickly became obvious that this standard is just a baseline, and many automotive suppliers and OEM automakers required further testing. Based on this acquired knowledge, starting with the 90nm XA Spartan-3A family, Xilinx created and began testing to "Beyond AEC-Q100." Combining the automotive industry's toughest test requirements from customers worldwide, Xilinx has created a world-class in-house semiconductor device qualification standard, doubling many of the AEC-Q100 test element requirements, and allowing shipment of high quality and robust XA products into the automotive market.

 [Click here for more information](#)

XA Spartan-6 FPGA Family

The XA Spartan-6 family of products was built to offer an optimal balance of cost, power and performance. The Spartan-6 LX FPGAs are cost-optimized for logic, DSP slices and memory, while the Spartan-6 LXT FPGAs also include embedded 3.125Gbps low-power serial transceivers, along with PCIe interface cores for high-speed serial connectivity. With various densities in the same package, automotive Tier One designers can choose the right-sized FPGA device for their OEM vehicle platform needs.



About the Xilinx Zynq All Programmable SoC

The Xilinx Automotive (XA) Zynq-7000 All Programmable SoC is a highly integrated device with unprecedented design flexibility as it is a single chip that combines a dual core ARM Cortex-A9 processor system for serial application processing and system control, high-speed programmable I/O, and programmable logic including DSP blocks for hardware acceleration of critical design components. The programmability of this architecture enables end product differentiation with complete control of the IP, and can help system designers keep up with constantly changing feature requirements, especially in emerging application areas such as ADAS.

With the immense processing power of this integrated device, driver assistance systems that have typically utilized an FPGA (image capture and pixel-level processing), a DSP (object processing) and a microcontroller (frame-level processing, decision making and communication), can now replace these with one XA Zynq All Programmable SoC device, reducing overall system power, lowering system bill of material (BOM) costs, and system design complexity.

XA Artix-7 FPGA Family

The Artix-7 is a low-power and high-performance FPGA device line-up available in smaller packages. With a range of devices from 35k logic cells to 100k logic cells, the highest BRAM and DSP block ratios available in the XA product line, integration of Analog Mixed Signal and 6.25Gbps transceivers for the latest serial interface standards, such as PCIe Gen 2, the Artix-7 FPGAs can be utilized for key automotive applications requiring high performance. The enhanced productivity of the Vivado® Design Suite, and design optimization techniques such as clock gating through the tool, enables as much as 50% total power reduction over XA Spartan-6.

Partial Reconfiguration
Reconfigurable FPGA technology **FPGA technology provides the flexibility of on-site programming and re-programming without going through re-fabrication with a modified design.** Partial Reconfiguration takes this flexibility one step further, allowing the dynamic change of modules within an active design by loading a partial configuration file. Benefits include the reduction of the required device size to implement a given function, flexibility in the choices of algorithms or protocols available to an application, and enabling new techniques in design security leading to savings in cost and power consumption.

Rapid Algorithm Deployment

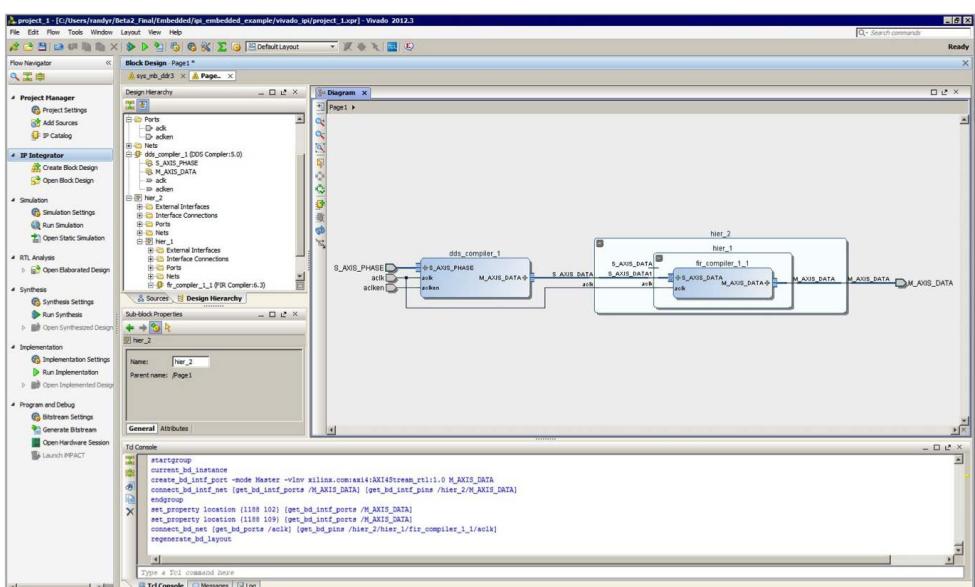
All Programmable Abstractions, through system modelling environment Alliance Members like the MathWorks® and National Instruments®, allow system engineers to evaluate the feasibility and performance of their algorithms on all programmable FPGAs and SoCs early in the development process to optimize system performance through hardware/software partitioning. These abstractions automate the rapid deployment of algorithms onto application specific hardware platforms interfaced to real-world signals, videos or networks.

For model-based design, the MathWorks has released a new guided workflow which enables software developers and hardware design engineers to create and model their algorithms in MATLAB™ and Simulink™, partition their designs between software and hardware, and automatically target, integrate, debug and test those models on Xilinx targeted design platforms for Zynq-7000 All Programmable SoC devices.

The new flow helps users to partition an algorithm into software and hardware modules and then generate C code for the ARM processor-based Zynq All Programmable SoC with the MathWorks Embedded Coder and RTL code for the programmable logic using the MathWorks HDL Coder or Xilinx's System Generator.

Vivado IP Integrator

The Vivado Design Suite is also now delivering intelligent IP integration with the new IP Integrator feature. Vivado IP Integrator (IPI), provides a graphical and Tcl based, correct by-construction, IP- and system-centric design development flow. This integration environment is platform aware which simplifies the integration of hardware board peripherals and device aware to ensure that maximum system bandwidth is achieved.

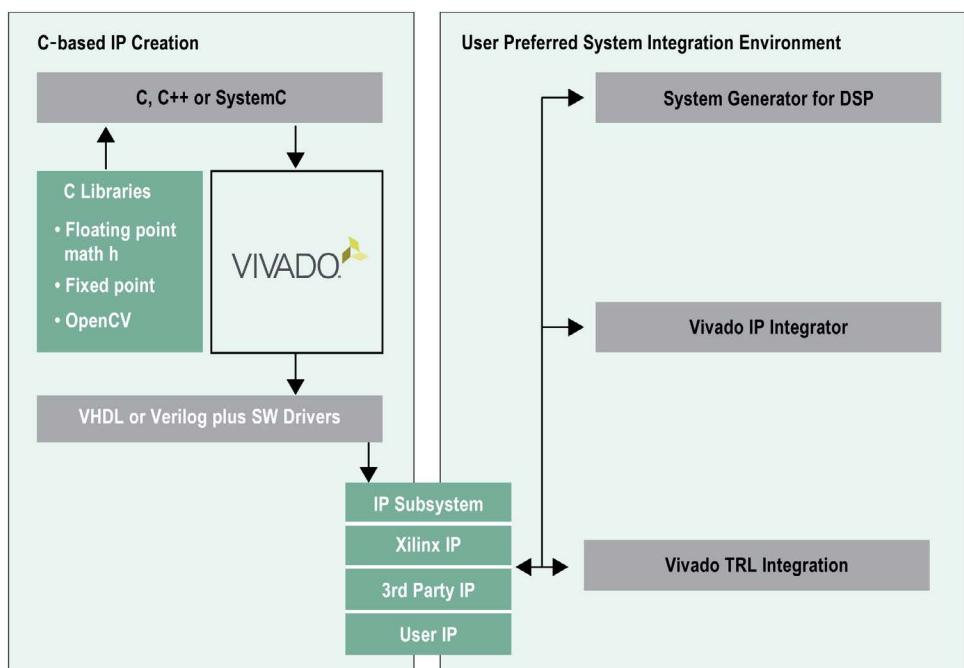


[Click here for more information](#)

C-Based IP Generation with Vivado High-Level Synthesis

Advanced algorithms used today in applications like Advanced Driver Assistance Systems (ADAS) are more sophisticated than ever before. To model these algorithms, many design teams turn to C/C++ or SystemC because of the sheer simulation performance over RTL-based simulations, making the process up to a thousand times faster. The challenge becomes the need to recode these algorithms in RTL for hardware implementation which is time consuming and error prone.

With C-based IP generation with Vivado High-level Synthesis (HLS), this process is greatly accelerated, by enabling the C specification to be directly targeted into Xilinx all programmable devices without the need to manually create RTL. Vivado HLS is part of the Vivado Design Suite, System Edition.



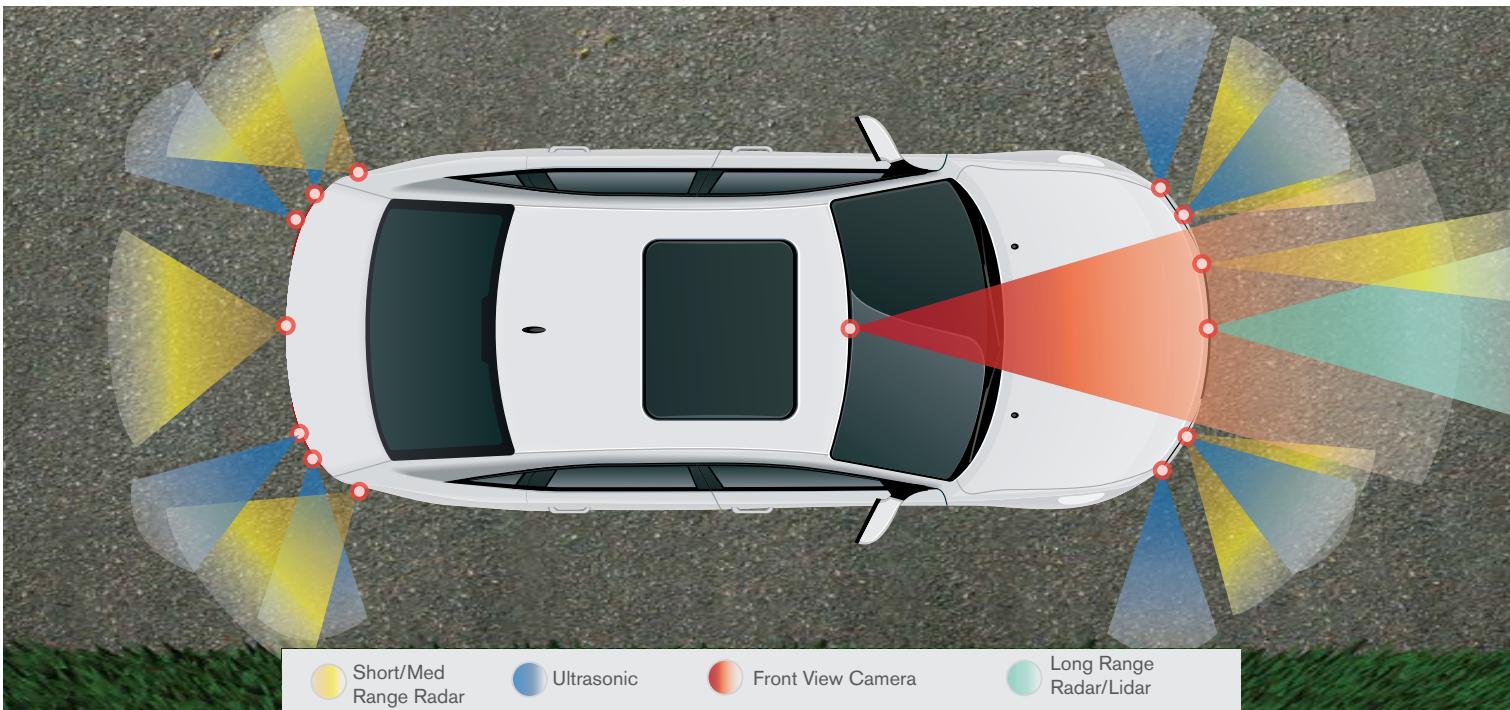
SDAccel™ Development Environment

Part of the SDx™ family of development environments for systems and software engineers, the SDAccel development environment helps customers to achieve up to 25X better performance/watt when designing FPGAs. It's the industry's first architecturally optimizing compiler supporting any combination of OpenCL, C, and C++ kernels, along with libraries, development boards, and the first complete CPU/GPU-like development and run-time experience for FPGAs.

The integrated design environment (IDE) provides coding templates and software libraries, and enables compiling, debugging, and profiling against the full range of development targets including emulation on x86, performance validation using fast simulation, and native execution on FPGA processors.

All Programmable Abstractions

All Programmable Abstractions are a set of design flow abstractions from Xilinx and its ecosystem of alliance members. They accelerate product development and enable developers to use custom hardware accelerators, and assist systems engineers to optimize hardware/software performance. All Programmable Abstractions push beyond traditional RTL design methodologies to automate all aspects of system development and algorithm deployment into all programmable FPGAs and SoCs.



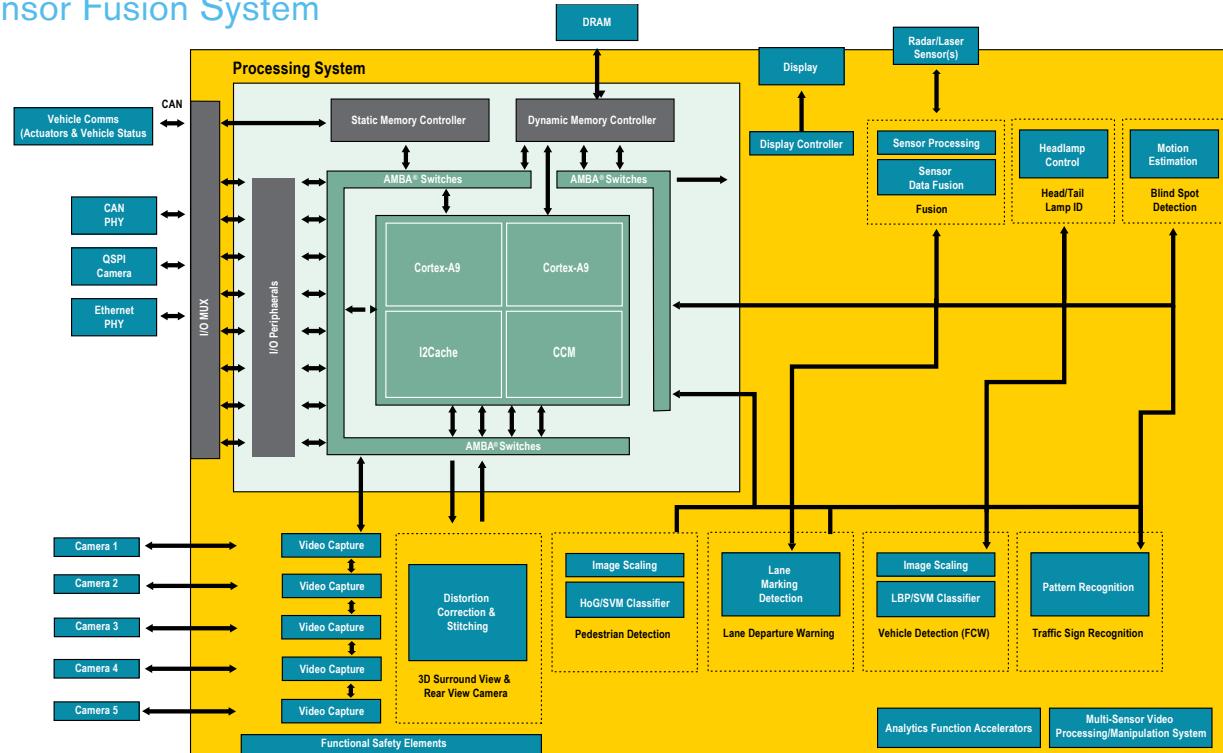
Xilinx in ADAS

The XA product family of FPGAs and All Programmable SoCs enable the creation of highly differentiated Advanced Driver Assistance Systems (ADAS). From distributed smart sensors to centralized multi-sensor fusion systems, developers can scale their device selection to meet specific processing needs and cost targets.

Xilinx's FPGA fabric supports custom hardware acceleration of the most complex and challenging computational functions while hardened ARM or softcore MicroBlaze CPUs allow for software implementation of those functions more appropriate for serial processing. The all programmable nature of the Zynq SoC offers ADAS developers the ultimate in hardware/software partitioning flexibility so an optimal solution can be reached for each platform design.

A variety of networking connectivity options coupled with unique functional safety architecture configurations are also key factors driving adoption of Xilinx devices for current and future ADAS modules.

Multi-Sensor Fusion System

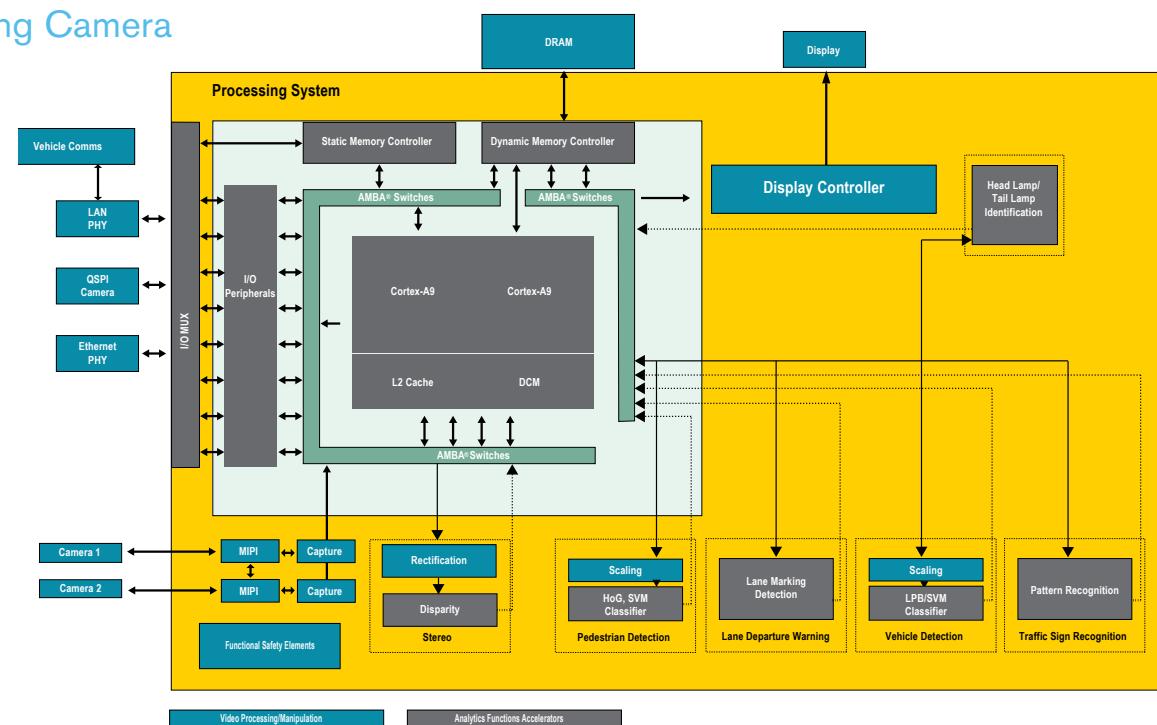


As automobile manufacturers add automated and autonomous driving systems, the centralized multi-sensor fusion module is under consideration. The Zynq All Programmable SoC offers advantages in this ADAS domain. Connectivity flexibility allows developers to leverage the latest in smart sensor interfaces and networks. Ethernet, MIPI, CAN, and a variety of LVDS/SERDES options can be accommodated on the Zynq All Programmable SoC.

To handle the immense bandwidth of information, customized hardware based interfaces and front-end processing is combined with independent AXI ports to provide direct access to

the hardened DDR controller. In addition, a second external memory controller can be added in fabric, providing developers with an extensible fusion platform. The ability to create independent hardware processing channels for various features is a key enabler in allowing developers to create vehicle specific feature bundles. And because each processing chain can be fully customized, customers can now differentiate their ADAS system performance from the competition.

Front Looking Camera



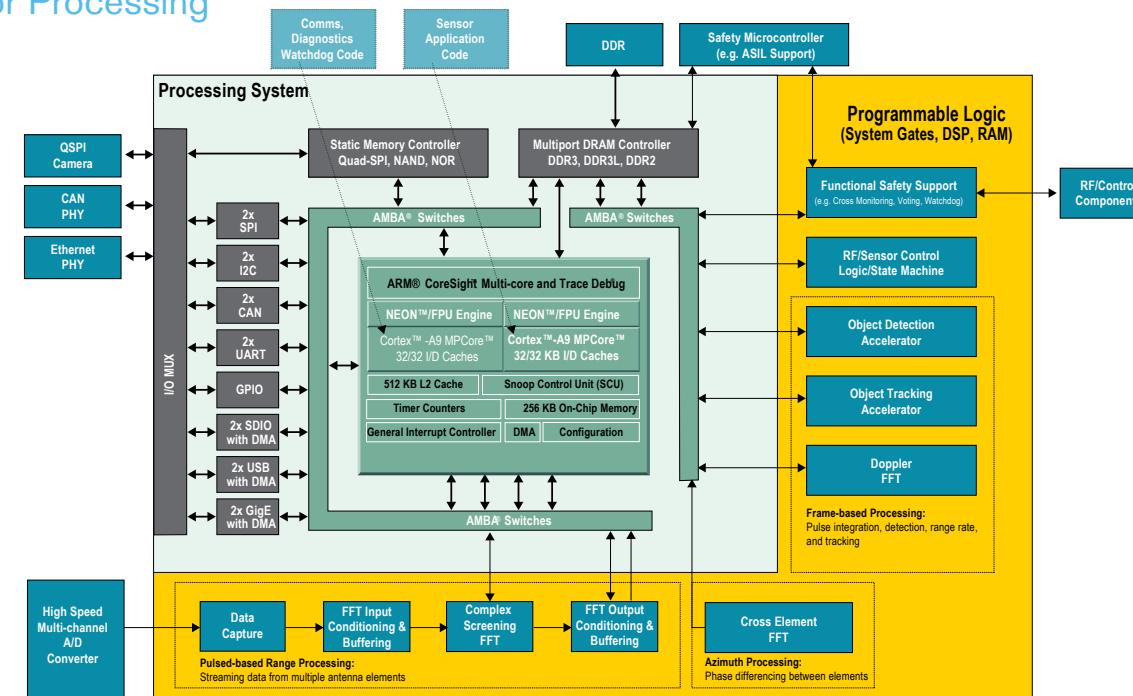
Logic Edition Xilinx Zynq All Programmable SoC devices are well-suited to meet the needs of today's Forward-Looking Camera ADAS systems. In these applications, a wide variety of features are based on complex image analytics from single camera video sequences. Divergent analytics methods are needed to support each feature – from a classification process for Pedestrian Detection, to pattern recognition for Traffic Sign Recognition. A key challenge is to perform the processing for each feature simultaneously and in real-time.

The Zynq All Programmable SoC and its fine-grain programmable logic allow developers to create independent and simultaneous processing paths to carry out the bulk of calculations

with hardware acceleration support. Additionally, high bandwidth interconnect allows the multi-core Cortex A9s to exchange data with the hardware accelerators and run multi-threaded applications which complete the functionality of each feature from a software perspective.

Further processing power is required with the inclusion of a second camera to add stereo processing and corresponding range-based features to the system. Fortunately, again an independent hardware processing path can be created to handle the complex stereo rectification and disparity calculations without effecting the other analytics feature processing.

Radar Sensor Processing



Creating effective ADAS systems requires characterization of the vehicle driving environment with higher fidelity than previously achieved. This technological challenge is accompanied by pressure to reduce system development costs.

One approach is to create more multi-modal radar sensors which provide the required detection sensitivity at long ranges as well as high resolution spatial discrimination at near ranges over a wide field of view. Creating such a sensor means combining complex antenna structures, adaptive front-end RF electronics, and powerful back-end digital processing. For these types of sensor architectures, the Zynq All Programmable SoC is a natural fit.

The Zynq All Programmable SoC offers highly programmable streaming FFT's in real-time, buffer multi-channel data in local memory, and store Stage 1 processed data over high bandwidth memory ports for subsequent frame based multi-dimensional FFT processing. Object detection and object tracking functions can also be hardware accelerated. The entire processing chain can be pipelined with independent hardware processing blocks to minimize system latency and maximize sensor performance.

Additionally, unique RF and antenna control functions can be processed automatically offering adaptive performance of the sensor based on driving conditions.

Connected to the Future

Many new functions of next generation cars like semi-autonomous driver assistance, car-to-x communication or advanced user interfaces are distributed and leverage different ECUs. This trend drives significant changes in the vehicle's network architecture and the required bandwidth. In addition telematics and connectivity with consumer devices like tablets or smartphones drive new external communication standards with increased security requirements.

Xilinx XA FPGAs provide the performance for high-bandwidth and low-latency communication with strong security. These devices offer the flexibility to quickly adopt new communication standards while allowing maximum integration to minimize BOM cost and use of PCB real estate.



Next generation cars will be much more connected and semi-autonomous.

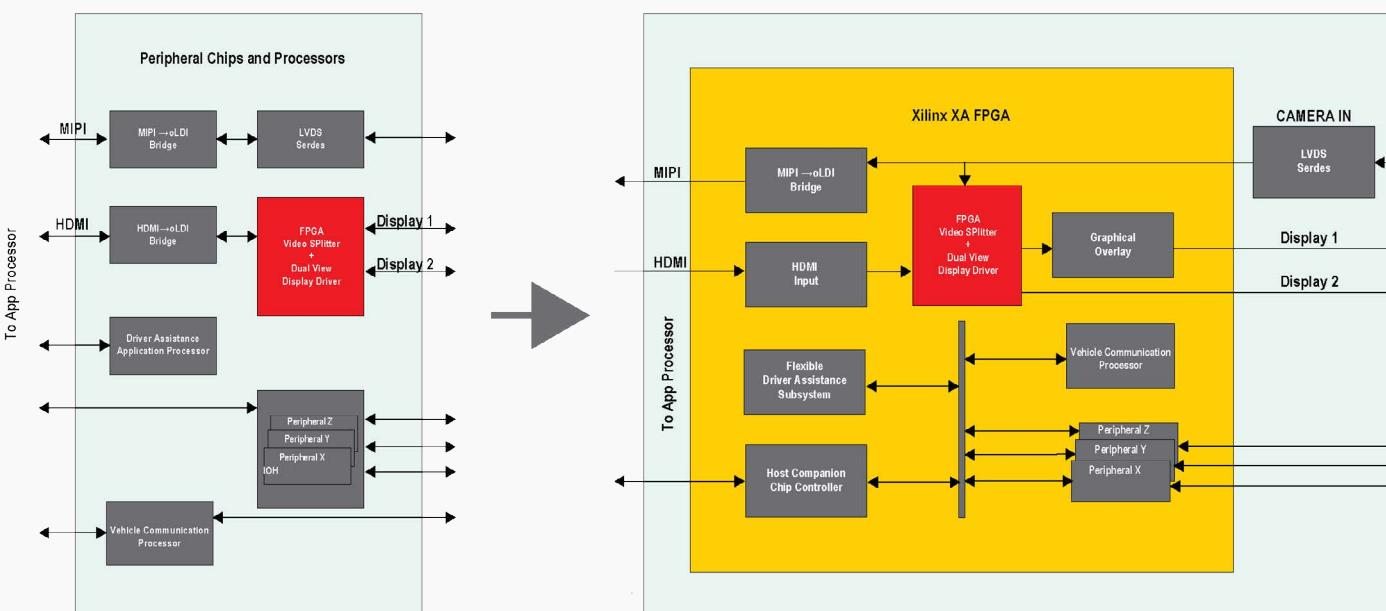


New HMI Experience

With more communication services like in-vehicle Internet access and Advanced Driver Assistance functions now available in cars, driver distraction is a real challenge. One possible solution is a more natural Human Machine Interface (HMI) that includes augmented reality (AR) technologies and driver distraction monitoring. This will give the driver a differentiating and completely new experience of interacting with the car by integrating camera based eye tracking and gesture detection. High-resolution wide-angle head-up displays will provide the driver all the information required while leading to minimum distraction. AR combines information from internal and external cameras with a rendered graphics overlay.

Companion Chip Design Platform

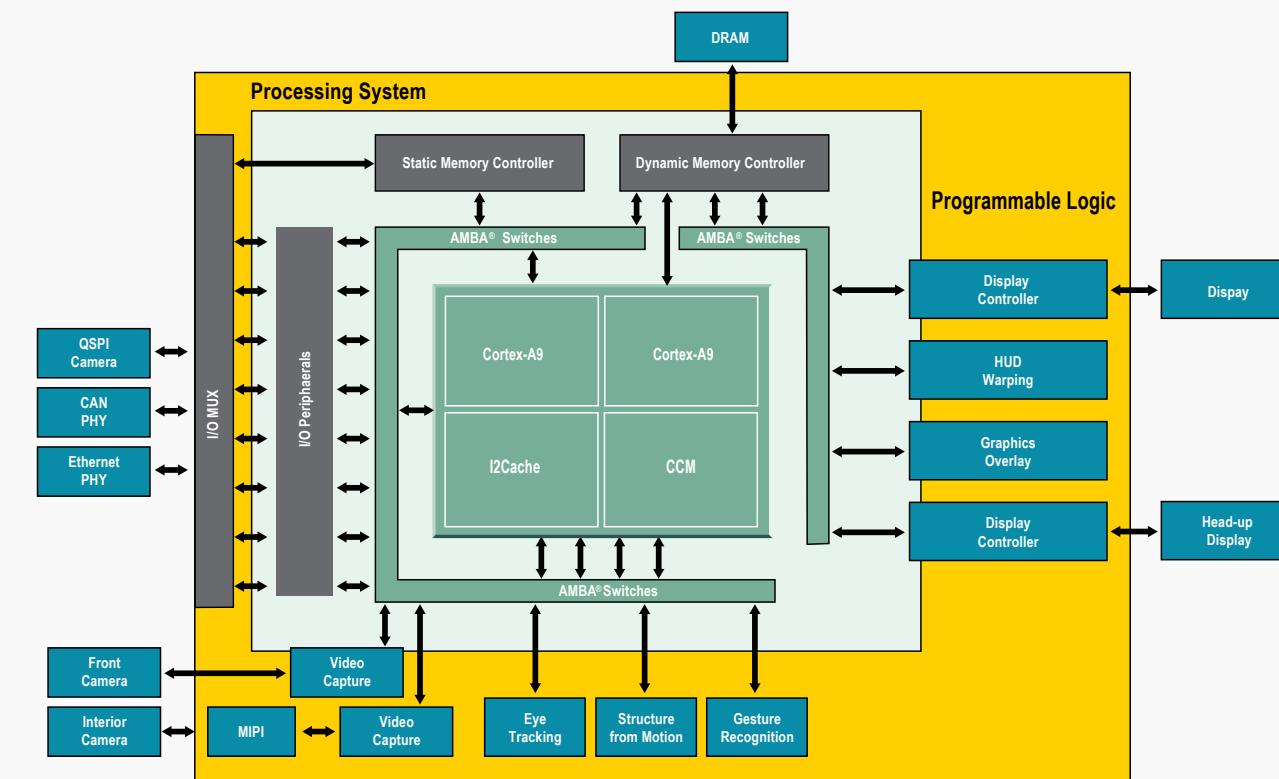
Xilinx XA FPGAs offer high bandwidth combined with programmable I/Os. They deliver performance, flexibility and scalability to implement multiple bridging solutions around a host processor on a single FPGA. With pin compatibility between the same packages through multiple device densities the design can be optimized for multiple ECU variants reducing BOM costs and power. The Xilinx Automotive Companion Chip Platform provides flexible interfacing and is optimized to complement a variety of host processors. A rich portfolio of available IP and software enables rapid extension of system interfaces, peripherals or processing with minimal development effort. Various popular host processor interfaces are supported and can be changed quickly based on host availability and overall bandwidth requirements.



[Click here for more information](#)

Augmented Reality HMI Solution

Augmented reality using eye tracking, gesture recognition, 3D reconstruction based on Structure from Motion and perspective rendering requires massive parallel processing. The scalable Xilinx XA Zynq All Programmable SocCfamily provides the right mix of power efficient parallel processing in the programmable logic and ARM processor performance to implement advanced HMI solutions in a cost efficient way in a single chip. The logiADAK reference platform enables short time to market. The Xilinx XA Zynq solution can be used as a stand-alone center stack solution or augmented reality companion inside the head unit.





Reference Designs

Xilinx Targeted Design Platforms (TDPs) provide pre-verified reference designs, consisting of source code for RTL design and software packages such as OS, device drivers and the software application. The reference designs showcase various features and capabilities of Xilinx devices and enable software developers to start programming immediately.

Why Intellectual Property?

As today's designs integrate increasing amounts of functionality, designers must have access to proven, up-to-date, easy-to-use Intellectual Property (IP) from reliable sources to accelerate their design cycles. The ability to deliver high-performance systems at the lowest total design cost on time and within budget depends upon the ability to rapidly combine and configure dozens or hundreds of design elements. These include on-chip blocks, processor cores, and a wide range of IP cores. Xilinx's growing IP portfolio is the response to the growing customer demand for system-level support.

These IP blocks combined with Xilinx all programmable devices families including FPGAs, SoCs and 3D ICs allows design teams to maximize system performance, lower power consumption, and reduce BOM costs with maximum design flexibility across a wide range of end markets and target applications. To ensure portability and interoperability among IP from Xilinx and its Alliance members, Xilinx has taken a standards-based approach.

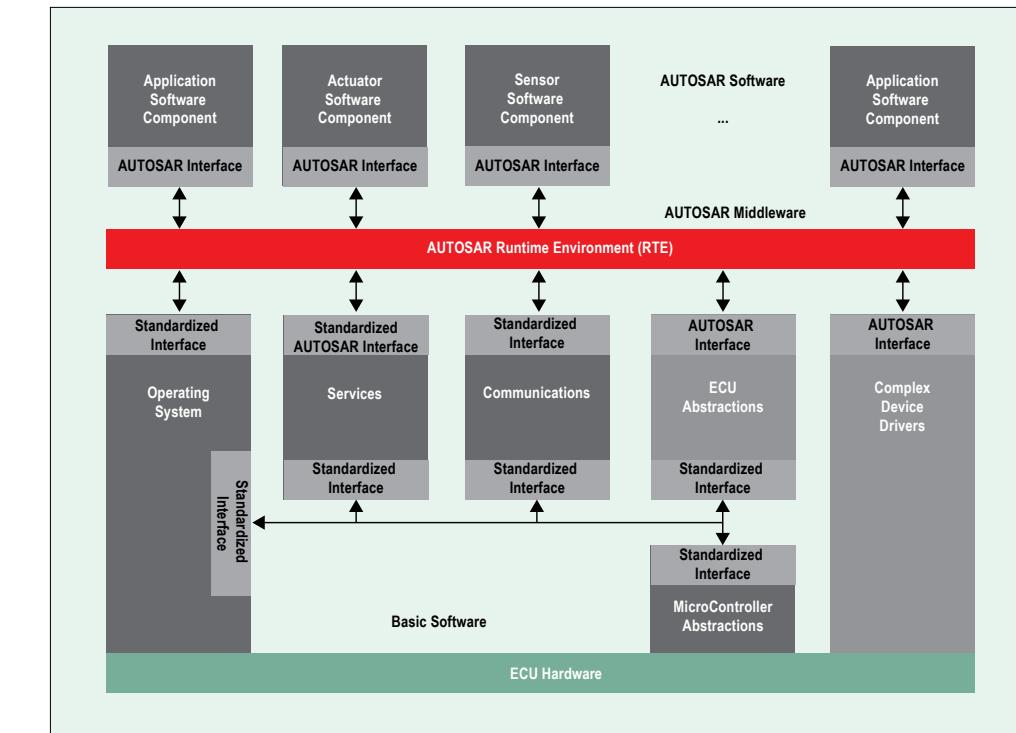
Premier Automotive Partner IP Examples		
IP provider	IP core	Description
Xilinx	CAN FD	CAN 2.0B compatible network controller supporting FD protocol extension
Xilinx	CAN	CAN 2.0B compatible network controller
Xylon	logiVIEW	Perspective Transformation and Lens Correction Image Processor
Xylon/eVS	logiPDET	Pedestrian Detector
Xylon/eVS	logiLMD	Lane Marking Detector
Xylon	logiMLB	Media Local Bus Interface supporting MLB Spec. V4.2
Xylon	logiWIN	Versatile Video Input Controller
Xylon	logiBITBLT	Bit Block Transfer 2D Graphics Accelerator
Xylon	logiCAN	CAN 2.0B compatible network controller
Xylon	logiBAYER	Color Camera Sensor Bayer Decoder
Xylon	logiI2S	Audio I2S Transmitter/Receiver
Xylon	logiBMP	Bitmap 2.5D Graphics Accelerator
Xylon	logiCVC-ML	Compact Multilayer Video Controller
Xylon	logi3D	Scalable 3D Graphics Accelerator
Xylon	logiSDHC	SD Card Host Controller

[Click here for information](#)

AUTOSAR Software Package

Xilinx offers via our AUTOSAR partner ARCCORE a high-quality, efficient, reliable and scalable AUTOSAR-compliant set of Microcontroller Abstraction Layer (MCAL) drivers for the Xilinx XA Zynq family. The drivers are developed in an automotive SPICE level

3 process framework and can be used in ECUs developed according to ISO26262. Supported are the industry standard compilers GCC and ARM Compiler 5. The MCAL drivers are provided with a command-line based code generator to be integrated in any AUTOSAR configuration tool and basic software. In addition, ARCCORE offers a complete AUTOSAR solution for the Zynq All Programmable SoC with their Arctic Core Embedded Software platform and the Arctic Studio Development Tooling.



Zynq AUTOSAR MCAL Driver Package

MCU Drivers	MEM Drivers	Comm Drivers	I/O Drivers
MCU	Flash	SPI	DIO
GPT		LIN	ICU
WDG		CAN	PWM

AUTOSAR

AUTOSAR standardizes the basic automotive ECU software functionality including operating system and basic services like communication and diagnosis. An RTE based on a virtual functional bus abstracts the underlying hardware. AUTOSAR also includes an ECU development methodology which allows scalability for different vehicle and platform variants re-use of software and support of different functional domains.

ISO 26262

The standard ISO 26262 is an adaptation of the functional safety standard IEC 61508 for automotive electric/electronic systems. ISO 26262 defines functional safety for automotive equipment applicable throughout the lifecycle of all automotive electronic and electrical safety-related systems.

It covers functional safety aspects of the entire development process, starting with requirements specification, design, implementation, integration, verification, validation, and configuration.



ISE Design Suite – Xilinx FPGA Programming Tool Chain – has been certified by TÜV SÜD according to IEC 61508-3:2010 and ISO 26262-8:2011

Functional Safety Requirements

Xilinx FPGAs and All Programmable SoCs are used at the heart of products that comply with functional safety requirements. Designers are specifically concerned with how to leverage the benefits of the FPGA while meeting the functional safety requirements imposed by the established standards.

Xilinx provides a certified and comprehensive functional safety design flow solution for FPGAs and All Programmable SoCs which includes:

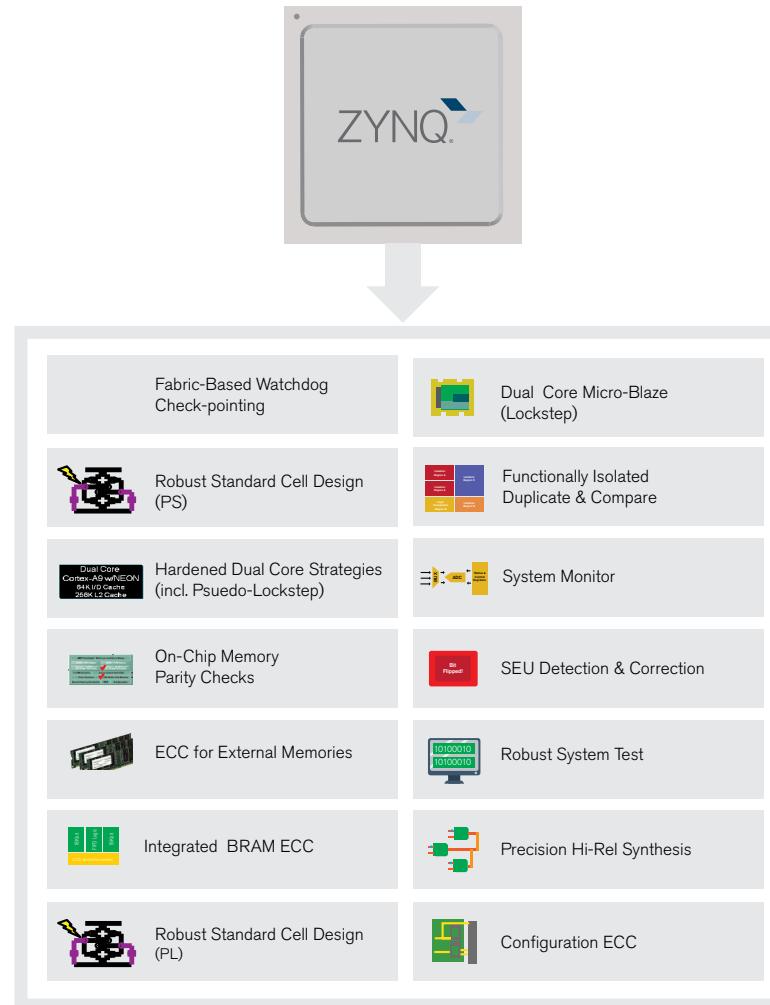
- Certificate and reports
- FPGA design and verification tools and methodologies
- IP and devices

This solution delivers essential project documentation and guidelines along with functional safety system IP, and significantly helps shorten the customer's certification process.

Xilinx's unique and certified functional safety design methodologies allow customers to integrate safety with general applications in the same device. Xilinx's Isolation Design Flow (IDF) and Isolation Verification Tools (IVT) provide a certified methodology to separate areas on the FPGA.

Designs can be placed into these areas and physically isolated. The areas can be changed at any time without impacting other isolated locations, proven by the IVT tools.

Click here for information



Xilinx Alliance Program

The Xilinx Alliance Program is a global ecosystem of qualified companies collaborating with Xilinx to further the development of all programmable technologies. Leveraging open platforms and standards, Xilinx has built this ecosystem to meet customer needs and is committed to its long-term success. Comprised of IP providers, EDA vendors, embedded software providers, design service providers, system integrators, and hardware suppliers, members help accelerate design productivity while minimizing risk.

The logiADAk Automotive Driver Assistance Kit

The logiADAk Automotive Driver Assistance kit is the Xilinx Zynq-7000 All Programmable SoC based development platform for ADAS applications that require intensive real-time video processing, parallel execution of multiple complex algorithms and versatile interfacing with sensors and the vehicle's communication backbones.



Design with Confidence

- Alliance members provide products across all technology and market solutions relevant to customer needs
- Members demonstrate the highest quality, expertise, and customer satisfaction standards
- Access to quality metrics for member IP cores accelerate the evaluation process

Deliver Better Products Faster

- Leverage leading-edge products from members to improve overall system performance while minimizing resource utilization
- Accelerate product development by easily integrating member solutions with your design on Xilinx technologies
- Reduce design integration time through solutions supporting industry key standards such as AMBA AXI4 and FMC

Instant Access to a Comprehensive Ecosystem

- Easily identify required expertise from a wide range of qualified companies
- Quickly find member solutions supporting Xilinx All Programmable devices

In order to help Xilinx customers accelerate design productivity through engineering consulting and design services, Xilinx provides qualification and access to advanced technical training and support to its Xilinx Alliance Members worldwide. Certified Members of the Alliance Program have passed a comprehensive corporate self-audit and maintain FPGA experts who have passed the same rigorous training as Xilinx field engineering worldwide.

The kit comes with a full set of DA demo applications, customizable reference SoC designs, software drivers, libraries, and documentation. The logiADAk hardware platform is appropriate for test vehicle installations and rapid engagements in proof-of-concept or demonstration projects.

Click here for information

Automotive Ecosystem

To realize the next generation of automotive solutions in Infotainment, Driver Information and Advanced Driver Awareness Systems, Xilinx is delivering a portfolio of all programmable devices, SoCs, design tools and automotive application solutions. To deliver these application solutions, Xilinx leverages the best in the industry by maintaining an Ecosystem of trusted companies with proven solutions on Xilinx platforms, stable business and technical processes, and automotive market experience. These automotive alliance partners compliment the Xilinx portfolio by providing high quality IP, solutions and design services that enable our customers to succeed with their toughest design challenges.



XA Zynq®-7000 All Programmable SoC						
	Device Name	Z-7010	Z-7020	Z-7030		
Processing System	Part Number	XA7Z010	XA7Z020	XA7Z030		
	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™				
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor				
	Maximum Frequency	667 MHz				
	L1 Cache	32 KB Instruction, 32 KB Data per processor				
	L2 Cache	512 KB				
	On-Chip Memory	256 KB				
	External Memory Support ⁽¹⁾	DDR3, DDR2, LPDDR2				
	External Static Memory Support ⁽¹⁾	2x Quad-SPI, NAND, NOR				
	DMA Channels	8 (4 dedicated to Programmable Logic)				
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO				
	Peripherals w/ built-in DMA ⁽¹⁾	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO				
	Security ⁽²⁾	AES and SHA 256b Decryption and Authentication for Secure Boot				
Programmable Logic	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts				
	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix®-7 FPGA	Kintex®-7 FPGA		
	Programmable Logic Cells (Approximate ASIC Gates ⁽³⁾)	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)		
	Look-Up Tables (LUTs)	17,600	53,200	78,600		
	Flip-Flops	35,200	106,400	157,200		
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	560 KB (140)	1,060 KB (265)		
	Programmable DSP Slices (18x25 MACCs)	80	220	400		
	Peak DSP Performance (Symmetric FIR)	100 GMACs	276 GMACs	593 GMACs		
	PCI Express® (Root Complex and End Point)	-	-	Gen2 x4		
	Analog Mixed Signal (AMS) / XADC ⁽⁴⁾	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs				
	Security ⁽²⁾	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration				
Speed Grades	Automotive I-Grade (Tj=−40°C to 100°C)	-1				
	Automotive Q-Grade (Tj=−40°C to 125°C)	-1				
Packages	Package Type ⁽⁴⁾	CLG225 ⁽¹⁾	CLG400	CLG400	CLG484	FBG484
	Size (mm)	13x13	17x17	17x17	19x19	23x23
	Pitch (mm)	0.8	0.8	0.8	0.8	1.0
	Processing System User I/Os (excludes DDR dedicated I/Os) ⁽⁵⁾	32	54	54	54	54
	Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	54	100	125	200	100
	Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	-	-	-	-	63
	Serial Transceivers	-	-	-	-	4
	Maximum Transceiver Speed (Speed Grade Dependent)	NA	NA	NA	NA	6.6 Gb/s
	XMP088 (v1.1DRAFT)					

Notes: 1. Z-7010 in CLG225 has restrictions on PS peripherals, Memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.

2. Security block is shared by the Processing System and the Programmable Logic.

3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

4. Devices in the same package are pin-to-pin compatible.

5. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.

Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com
More info: www.xilinx.com/products/silicon-devices/

XA Artix®-7 FPGAs						
Optimized for Lowest Cost and Lowest Power Applications (1.0V)						
	Part Number	XA7A15T	XA7A35T	XA7A50T	XA7A75T	XA7A100T
Logic Resources	Logic Cells	16,640	33,280	52,160	75,520	101,440
	Slices	2,600	5,200	8,150	11,800	15,850
	CLB Flip-Flops	20,800	41,600	65,200	94,400	126,800
Memory Resources	Maximum Distributed RAM (Kb)	200	400	600	892	1,188
	Block RAM/FIFO w/ ECC (36 Kb each)	25	50	75	105	135
	Total Block RAM (Kb)	900	1,800	2,700	3,780	4,860
Clock Resources	CMTs (1 MMCM + 1 PLL)	5	5	5	6	6
	Maximum Single-Ended I/O	210	210	210	285	285
I/O Resources	Maximum Differential I/O Pairs	100	100	100	137	137
	DSP Slices	45	90	120	180	240
Integrated IP Resources	PCIe® Gen2 ⁽¹⁾	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1
	GTP Transceivers (6.25 Gb/s Max Rate) ⁽²⁾	4	4	4	4	4
	Industrial (−40°C to +100°C)	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
Speed Grades	Automotive (−40°C to +125°C)	-1	-1	-1	-1	-1
	Package	Dimensions (mm)	Available User I/O: 3.3V SelectIO™ HR I/O (GTP Transceivers)			
CPG236		10 x 10	106 (2)	106 (2)	106 (2)	
CSG324		15 x 15	210 (0)	210 (0)	210 (0)	210 (0)
CSG325		15 x 15	150 (4)	150 (4)	150 (4)	
FGG484		23 x 23			285 (4)	285 (4)

CPG: 0.5mm Wire-bond chip-scale; **CSG:** 0.8mm Wire-bond chip-scale; **FGG:** 1.0mm Wire-bond fine-pitch

Notes: 1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.

2. GTP transceiver: 6.25 Gb/s available in -2 speed grade only; 3.75 Gb/s in -1 speed grade.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com
More info: www.xilinx.com/products/silicon-devices/

SPARTAN⁶



Spartan®-6 LX FPGAs										Spartan-6 LXT FPGAs										
Optimized for Lowest-Cost Logic, DSP, and Memory (1.2V)										Optimized for Lowest-Cost Logic, DSP, and Memory with Serial Connectivity (1.2V)										
	Part Number	XA6SLX4 ^(10,11)	XA6SLX9	XA6SLX16	XA6SLX25 ⁽¹⁰⁾	XA6SLX45	XA6SLX75	XA6SLX100	XA6SLX25T ⁽¹⁰⁾	XA6SLX45T	XA6SLX75T		Part Number	XA6SLX45	XA6SLX75	XA6SLX100	XA6SLX25T ⁽¹⁰⁾	XA6SLX45T	XA6SLX75T	
Logic Resources	Slices ⁽¹⁾	600	1,430	2,278	3,758	6,822	11,662	15,822	3,758	6,822	11,662		Slices ⁽²⁾	960	2,448	4,656	8,672	14,752		
	Logic Cells ⁽²⁾	3,840	9,152	14,579	24,051	43,661	74,637	101,261	24,051	43,661	74,637		Logic Cells	2,160	5,508	10,476	19,512	33,192		
	CLB Flip-Flops	4,800	11,440	18,224	30,064	54,576	93,296	126,576	30,064	54,576	93,296		CLB Flip-Flops	1,920	4,896	9,312	17,344	29,504		
Memory Resources	Maximum Distributed RAM (Kb)	75	90	136	229	401	692	976	229	401	692		Maximum Distributed RAM (Kb)	15	38	73	136	231		
	Block RAM (18 Kb each)	12	32	32	52	116	172	268	52	116	172		Block RAM Blocks	4	12	20	28	36		
	Total Block RAM (Kb) ⁽³⁾	216	576	576	936	2,088	3,096	4,824	936	2,088	3,096		Total Block RAM (Kb)	72	216	360	504	648		
Clock Resources	Clock Management Tiles (CMT) ⁽⁴⁾	2	2	2	4	6	6	2	4	6		Digital Clock Managers (DCMs)	2	4	4	8	8			
I/O Resources	Maximum Single-Ended Pins	132	200	232	266	316	280	326	250	296	268		Maximum Single-Ended I/Os	108	172	190	304	376		
	Maximum Differential Pairs	66	100	116	133	158	140	163	125	148	134		Maximum Differential I/O Pairs	40	68	77	124	156		
Embedded Hard IP Resources	DSP48A1 Slices ⁽⁵⁾	8	16	32	38	58	132	180	38	58	132		I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL18 Class I, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, SSTL2 Class I, SSTL18 Class I, Bus LVDS, LVDS25, LVPECL25, Mini-LVDS25, and RSDS25						
	Endpoint Block for PCI Express®	—	—	—	—	—	—	—	1	1	1		Dedicated Multipliers	4	12	20	28	36		
	Memory Controller Blocks	0	2	2	2	2	2	2	2	2	2		Device DNA Security	—	—	—	—	—		
Miscellaneous	GTP Low-Power Transceivers	—	—	—	—	—	—	—	2	4	4		Temperature Grades ⁽⁴⁾	I, Q	I, Q	I, Q	I, Q	I, Q		
	Speed Grade	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3		Speed Grade	-4	-4	-4	-4	-4		
Miscellaneous	Temperature Grade ⁽⁶⁾	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q		X A Released	Yes	Yes	Yes	Yes	Yes		
	X A Released	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes		Configuration	Configuration Memory (Mb)	0.6	1.4	2.3	3.8	6	
Configuration	Configuration Memory (Mb)	2.7	2.7	3.7	6.4	11.9	19.6	26.5	6.4	11.9	19.6		Package	Footprint Area	Maximum User I/Os					
Package										VQFP Packages (VQG): Pb-free, very thin QFP (0.5 mm lead spacing)										
CSG225 ⁽⁸⁾										VQG100										
CSG324										16 x 16 mm										
BGA Packages (FTG): Pb-free wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)										66										
FTG256										190 (2)										
BGA Packages (FGG): Pb-free wire-bond, fine-pitch, BGA (1.0 mm ball spacing)										190 (4)										
FGG484 ⁽⁹⁾										266										
XMP079 (v2.0)										280										
326										250 (2)										
296 (4)										268 (4)										
Notes:										XMP079 (v2.0)										
1. Each slice contains four LUTs and eight flip-flops.										Notes:										
2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT structure.										1. System gates include 20%–30% of CLBs used as RAMs.										
3. Block RAM is fundamentally 18 Kb in size. Each block can also be used as two independent 9 Kb blocks.										2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.										
4. Each CMT contains two DCMs and one PLL.										3. Temperature Range Automotive I ($T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$); Automotive Q ($T_j = -40^\circ\text{C}$ to $+125^\circ\text{C}$).										
5. Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.										Important: Verify all data in this document with the device data sheets found at www.xilinx.com										
6. Temperature Range Automotive I ($T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$); Automotive Q ($T_j = -40^\circ\text{C}$ to $+125^\circ\text{C}$).										More info: <a href="http://www.xilinx.com										

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe

Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan

Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

India

Meenakshi Tech Park
Block A, B, C, 8th & 13th floors,
Meenakshi Tech Park, Survey No. 39
Gachibowli(V), Seri Lingampally (M),
Hyderabad -500 084
Tel: +91-40-6721-4000
www.xilinx.com

TAKE THE NEXT STEP
VISIT US ONLINE AT WWW.XILINX.COM



facebook.com/XilinxInc



twitter.com/XilinxInc



youtube.com/XilinxInc



©Copyright 2015 Xilinx, Inc. XILINX, the Xilinx logo, Virtex, Spartan, ISE and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners. PN WW2015