

**FACULTY OF ENGINEERING****B.E. 3/4 (ECE) II – Semester (Main) Examination, May / June 2015****Subject : Computer Organisation and Architecture****Time : 3 hours****Max. Marks : 75****Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.****PART – A (25 Marks)**

- |      |  |   |
|------|--|---|
| 1    | Describe the characteristics of various generations of computer.   | 2 |
| 2    | Represent the number $(+37.8)_{10}$ as a floating point binary number with normalized fraction mantissa 16 bits and exponent 8 bits.   | 3 |
| 3    | Explain the use of following registers :   | 3 |
| i)   | PC   |   |
| ii)  | MAR  |   |
| iii) | IR   |   |
| 4    | Define i) Microprogram ii) Microinstruction  | 2 |
| 5    | A stack is organized in such that SP always points at the next empty location on the stack. List the micro operations for the push and pop operations. Assume stack grows downwards. | 3 |
| 6    | Determine the number of clock cycles that it takes to process 200 tasks in a six segment pipeline.   | 2 |
| 7    | Write functions of an I/O interface.   | 2 |
| 8    | Why does DMA have priority over the CPU when both request a memory transfer?   | 3 |
| 9    | What is the difference between RAM and ROM?  | 2 |
| 10   | What do you mean by a page fault? Which hardware is responsible for detecting the page fault?  | 3 |

**PART – B (50 Marks)**

- |       |   |   |
|-------|---|---|
| 11 a) | Explain, (with the help of suitable examples) IEEE standard for floating-point numbers.                     | 4 |
| b)    | Using booth's multiplication algorithm, multiply the $3 \times -4$ , showing all the steps.                 | 6 |
| 12 a) | With neat diagram of a common bus system, show how to execute the micro-operation $AC \leftarrow AC + DR$ . | 6 |
| b)    | Compare and contrast between horizontal and vertical approach of microinstruction.                          | 4 |
| 13 a) | What is stack frame? Explain using a suitable example how is it used for nested subroutines.                | 6 |
| b)    | Explain any four addressing modes giving suitable example.  | 4 |

- 2 -

- |   |    |
|---|----|
| 14 a) What are the three basic techniques to perform Input/Output operations?   | 6  |
| b) What is the disadvantages of transferring data through strobe control method?<br>How handshaking overcomes this disadvantage? Explain. | 4  |
| 15 a) Why page-table is required in a virtual memory system? Explain different ways of organizing a page table.                           | 5  |
| b) What do you mean by memory hierarchy? Describe in detail.  | 5  |
| 16 a) Describe in detail how data is transferred in using DMA. Draw necessary diagrams to support your explanation.                       | 6  |
| b) Draw and explain the organization of 4 MB semiconductor memory constructed using 256 K x 1 chips.                                      | 4  |
| 17 Write a brief note about any two of the following :  | 10 |
| i) Pipelining   |    |
| ii) Comparison between CISC and RISC  |    |
| iii) Array processors   |    |

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**FACULTY OF ENGINEERING**  
**B.E. 3/4 (ECE) II - Semester (Suppl.) Examination, January 2015**

**Subject : Computer Organization and Architecture**

**Time : 3 Hours**

**Max. Marks: 75**

**Note: Answer all questions of Part - A and answer any five questions from Part-B.**

**PART – A (25 Marks)**

- |    |   |     |
|----|---|-----|
| 1  | Perform the subtraction of following using 2's complement.                            | (3) |
|    | (i) $(25)_{10} - (10)_{10}$ (ii) $(17)_{10} - (33)_{10}$                              |     |
| 2  | Represent a condition evaluation of a typical expression using RTL with two examples. | (3) |
| 3  | Compare Hardwired and Micro programmed control unit.                                  | (3) |
| 4  | Discuss various types of CPU organizations.   | (2) |
| 5  | Draw the flow chart of interrupt cycle.   | (2) |
| 6  | Explain briefly the micro instruction format.   | (3) |
| 7  | What are the limitations of a pipelining process?                                     | (2) |
| 8  | Explain the need for an I/O interface.  | (2) |
| 9  | Draw the timing diagram of a Strobe control method of I/O interface.                  | (2) |
| 10 | Write the need for virtual memory concept.  | (3) |

**PART – B (50 Marks)**

- |    |  |      |
|----|--|------|
| 11 | (a) Explain the process of floating point number multiplication with a flow chart.<br>(b) Explain the operation of a BCD adder with block diagram.   | (5)  |
| 12 | (a) Explain the operation of a micro programmed control unit with block diagram.<br>(b) Discuss about common bus system with an example.   | (6)  |
| 13 | (a) Compare CISC and RISC Architectures.<br>(b) Classify the instructions based on the fields of a instruction format.   | (4)  |
| 14 | (a) Explain the DMA Transfer with block diagram.<br>(b) Draw the block diagram of an Asynchronous communication interface and explain its operation in detail.   | (6)  |
| 15 | Explain various elements of cache design and various mapping techniques used with cache.   | (10) |
| 16 | (a) How many 128x8 memory chips are needed to provide a memory capacity of 4096 x 16? Give the circuit diagram of the memory using the memory chips?<br>(b) Explain how programmed I/O and Interrupt initiated I/O operations are carried out. | (5)  |
| 17 | Write short notes on any two of the following:<br>(a) Handshaking control of asynchronous data Transfer<br>(b) Instruction cycle<br>(c) Array processors   | (10) |

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**FACULTY OF ENGINEERING**  
**B.E. 3/4 (ECE) II – Semester (Main) Examination, June 2014**

**Subject: Computer Organization and Architecture**

**Time: 3 Hours**

**Max.Marks: 75**

**Note: Answer all questions from Part A. Answer any five questions from Part B.**  
**PART – A (25 Marks)**

- 1 Define computer organization and computer architecture. (2)
- 2 Represent the number  $(+46.5)_{10}$  as a floating point binary number with normalized fraction mantissa 16 bits and exponent 8 bits. (3)
- 3 Define micro operation and micro instruction. (2)
- 4 Draw the timing diagram for the following control operation.  $C_7T_3 : SC \leftarrow 0$ . (3)
- 5 What are the basic differences between a branch instruction, a call subroutine instruction, and program interrupt. (3)
- 6 Determine the number of clock cycles to process 200 tasks in a six-segment pipeline. (2)
- 7 What is the difference between isolated I/O and memory-mapped I/O. (2)
- 8 Explain the need for an I/O interface. (3)
- 9 What is the advantage of direct mapping over associative mapping in Cache memory organization? (3)
- 10 Draw the block diagram of a memory table for mapping a virtual address. (2)

**PART – B (50 Marks)**

- 11 (a) Draw the flow chart for a sign magnitude addition and subtraction algorithm. (4)  
 (b) Explain the Booth's multiplication with an example. (6)
- 12 (a) Explain the all addressing modes of a basic computer. (6)  
 (b) Explain the operation of a address sequencer in a micro programmed control unit. (4)
- 13 (a) Explain various phases of an instruction cycle in detail. (6)  
 (b) A non-pipeline system takes a 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? (4)
- 14 (a) Explain the operation of Daisy chaining method of priority interrupt. (6)  
 (b) Write the sequence of steps to be followed for DMA transfer. (4)
- 15 (a) Explain the virtual memory concept with block diagram. (6)  
 (b) Draw the diagram showing the memory connections to CPU. (4)
- 16 Explain the various elements of Cache design and various mapping techniques used with Cache. (10)
- 17 Write a brief note about any two of the following:  
 a) Non-restoring division    b) Array processors    c) Asynchronous data transfer. (10)

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Time : 3 Hours

Max. Marks: 75

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1. Draw the flow chart for add and subtract operations.
2. Differentiate between restoring and non-restoring division algorithm.
3. What is stored program organization?
4. What is Instruction set completeness?
5. Write the need for different addressing modes.
6. Write features of RISC.
7. Mention the ways that computer buses can be used to communicate with memory and I/O.
8. Draw the flow chart for source initiate transfer using handshaking.
9. How CAM is different from read / write memory?
10. Define address space and memory space.

PART – B (50 Marks)

11. Explain Booth's multiplication algorithm for signed 2's complement numbers in details, with a suitable example and give the hard ware requirement.
- 12.(a) Explain the common bus system of a computers with a neat sketch.  
(b) Explain input-output configuration of a computer and list any five I/O instructions with their control functions and micro operations.
- 13.(a) Explain instruction formats for various types of computer organizations as single accumulator, general register and stack.  
(b) Explain various types of interrupts in brief.
14. Explain the following nodes of transfer in brief  
(i) Interrupt - initiated I/O  
(ii) DMA  
(iii) Explain the methods employed for establishing priority for simultaneous interrupts.
- 15.(a) Draw the block diagram of an association memory and explain its operation in terms of match logic, read and write operations.  
(b) Mention various page replacement algorithms.
- 16.(a) Explain pipeline conflicts and discuss the remedies for those conflicts.  
(b) Explain any four data manipulation instruction.
17. Write short notes on the following.  
(a) CPU-IOP communication  
(b) Microprogram sequencer  
(c) Floating point arithmetic (addition and multiplication)

**FACULTY OF ENGINEERING****B.E. 3/4 (ECE) II-Semester (New)(Supplementary) Examination, December 2013****Subject : Computer Organization and architecture****Time : 3 hours****Max. Marks : 75****Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.****PART – A (25 Marks)**

1. Draw the hardware requirement for performing signed magnitude addition and subtraction.
2. Draw the flow chart showing multiplication of floating point numbers.
3. Define the terms instruction code and operation code.
4. Differentiate between hard wired control and microprogrammed control.
5. What is the purpose of a stack?
6. What is an instruction format?
7. Write the need for an I/O interface.
8. Write the sequence of events for destination initiated transfer using hand shaking.
9. Write about memory hierarchy in a computer system.
10. Define a page fault.

**PART – B (50 Marks)**

11. Explain restoring and non-restoring division algorithms in detail.
- 12.a) What is an interrupt? Draw the flow chart for interrupt cycle and explain the series of steps that follow the occurrence of interrupt.  
b) List any 5 memory reference instructions along with their symbolic description.
- 13.a) Explain about the following addressing modes in detail.  
i) Relative addressing modes      ii) Indexed addressing mode  
iii) Base addressing mode  
b) Explain the concept of pipeline in general and arithmetic pipeline in detail.
- 14.a) Draw the block diagram of a typical asynchronous communication interface and explain its operation in detail.  
b) Explain the procedure to initiate DMA by the CPU.
- 15.a) Explain in detail about memory management hardware.  
b) Explain various methods of writing into cache and brief about cache initialization.
- 16.a) Explain set associative mapping in detail.  
b) Explain memory organization in vector processors.
17. Write short notes on :  
a) Computers generations  
b) Array processors  
c) Computer registers

UNDER VALUATION

Code No.2096/O

FACULTY OF ENGINEERING

BE 3/4 (ECE) I-Sem (Old) Examinations, November / December 2012

MJCE1 8/2/13

Subject: Computer Organization and Architecture

Max. Marks: 75

150  
23  
4

Time: 3 Hours

Note: Answer all questions from Part-A any five questions From Part-B

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7/2/13

Part-A (25 Marks)

- |  |   |
|--|---|
| 1. Draw Flow Chart for a multiplication operation  | 2 |
| 2. Represent a condition evaluation of a typical expression using RTL with two examples?     | 2 |
| 3. Differentiate between Hard wired and micro programmed control                             | 2 |
| 4. Write the functions of micro programmed sequences   | 2 |
| 5. Discuss various types of CPU organizations  | 3 |
| 6. Write the features of a RISC processor  | 3 |
| 7. Explain the need for an I/o Interface   | 2 |
| 8. Draw a chart showing CPU-IOP communication  | 3 |
| 9. Define association <sup>ve</sup> memory & draw a block diagram showing its implementation | 3 |
| 10. Write the need for virtual memory concept  | 2 |

Part-B (50 Marks)

- |   |                   |
|---|-------------------|
| 11. a) Explain the process of floating point number multiplication with a flow chart.   | 5                 |
| b) Show the Hardware for a 2 bit-by-2bit array a multiplier & explain its working.  | 5                 |
| 12. a) Explain various phases of an instruction cycles in detail.   | 5                 |
| b) Draw the flow chart that explains the complete operations of how an instructions in fetched, decoded & executed in a computer.   | 5                 |
| 13. a) Write the need for addressing modes. Explain various addressing modes supported by a general purpose CPU.  | 6                 |
| b) Differentiate between various interrupts?  | 4                 |
| 14. a) Draw the Block diagram of an Asynchronous communication interface and explain its operation in detail.   | 5                 |
| b) Explain daisy-chaining process of prioritizing interrupts.   | 5                 |
| 15. Explain various elements of cache design and various mapping techniques used with cache.  | 6                 |
| 16. a) Differentiate between Restoring & non-Restoring division.  | 3                 |
| b) Explain one-address, 2-address & 3-address instructions related to CPU organizations.  | 7                 |
| 17. Write a brief note about any two of the following<br>(i) Isolated VS memory mapped I/o.<br>(ii) Memory hierarchy.<br>(iii) Data transfer and manipulation instructions. | $5 \times 2 = 10$ |

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V.K.N.F

**FACULTY OF ENGINEERING**  
**B.E. 3/4 (ECE) First Semester (Suppl.) Examination, June/July 2011**  
**COMPUTER ORGANIZATION AND ARCHITECTURE**

**Time : Three Hours]**

**[Maximum Marks : 75]**

**Note :— Answer ALL questions from Part A. Answer any FIVE questions from Part B.**

**PART—A (Marks : 25)**

1. Why do we use dividend alignment while performing division operation of binary numbers ? 2
2. Mention the advantages of RISC over CISC. 3
3. Distinguish between a single processor and multi-processor system. 2
4. Explain about stored program organization. 3
5. Brief about pipeline processing. 3
6. What is meant by 'locality of reference' and how does it help in faster execution of the programs ? 3
7. Explain any 5 logical operations of a basic computer. 2
8. Differentiate between Synchronous and Asynchronous data transfer. 2
9. Classify the printers. 2
10. Draw a one bit RAM cell (Block diagram) and explain the function of each pin. 3

**PART—B (Marks : 50)**

11. Explain Booth's multiplication algorithm with the help of a block diagram. Use a numerical example. 10
12. (a) What is the purpose of microprogram sequencer ? Explain with a block diagram, how the sequencer present addresses to control memory. 7  
(b) Differentiate between restoring and non-restoring division algorithms. 3

13. (a) Explain data manipulation operations of a basic computer. 7  
(b) What is normalization ? 3
14. (a) Draw the block diagram and explain vector processing. 6  
(b) How vector processing is different from Array processing and give their application areas. 4
15. (a) Explain ~~Stroke~~<sup>Strobe</sup> method of Asynchronous data transfet. 3  
(b) Draw the Block diagram and explain how data is transferred with the help of DMA. 7
16. Explain instruction pipeline scheme. List the 3 major difficulties that cause the instruction pipeline to deviate from its normal operation and give their remedies. 10
17. Write short notes on :—  
(a) Virtual memory concept  
(b) Stack organized Instruction formats. 10

**FACULTY OF ENGINEERING**  
**B.E. 3/4 (ECE) I Semester (Main) Examination, Dec. 2011**  
**COMPUTER ORGANIZATION AND ARCHITECTURE**

Time: 3 Hours]

[Max. Marks: 75]

**Note :** Answer all questions of Part A.  
 Answer five questions from Part B.

**PART – A****(25 Marks)**

1. Draw the Block diagram of 4-bit combinational circuit shifter and write its function table. 3
2. Show the hardware for implementing Booth's algorithm. 3
3. How many clock <sup>pulses</sup> are required to execute the following micro-operations ? 3
  - a)  $IR \leftarrow M[Pc]$
  - b)  $AC \leftarrow AC + TR$
  - c)  $DR \leftarrow DR + AC$
4. Differentiate between a memory-mapped I/O and an isolated mapped I/O. 2
5. Explain Flynn's classification of processor. 2
6. Explain Hand-shaking method of Asynchronous data transfer. 3
7. Mention different phases in an instruction cycle. 2
8. What is bootstrap loader ? 2
9. Differentiate between complier Assembler and language translator. 3
10. Write briefly about multiprocessor. 2

**PART – B****(50 Marks)**

11. a) Derive an algorithm in flow chart form for the non-restoring method of fixed point binary division. 6  
 b) Draw the logic diagram of a 4-bit adder-subtractor and explain with the help of a truth table. 4
12. Draw the flow chart for interrupt cycle and explain in detail all the phases. 10
13. a) Discuss SIMD processor organization. 4  
 b) Explain instruction pipeline conflicts and their remedies. 6



14. a) Explain Daisy-chain interrupt priority and draw the logic circuit for one stage of diary chain priority arrangement. 6  
b) Explain CPU-IOP communication. 4
15. a) Explain read and write operations with respect to Association Memory. 7  
b) A magnetic disc system has the following 3
- $P_s$  — Average time to position the magnetic head over the track.  
 $R$  — Rotation speed in revolutions/sec.  
 $N_t$  — No. of bits/track  
 $N_s$  — No. of bits/sector
- Calculate the average time  $T_a$  that will take to read one sector.
16. a) Explain DMA transfer in detail with all relevant Block diagrams. 6  
b) Draw the circuit diagram of a  $4 \times 4$  FIFO buffer and explain its operation. 4
17. Write short notes on : 3
- a) Functional aspects of operating systems 3  
b) RISC/CISC – Differentiate 4  
c) Stored program organization. 3

13/12/16

Code No. : 3036

**FACULTY OF ENGINEERING**

**B.E. 3/4 (ECE) I Semester (Main) Examination, December 2010**  
**COMPUTER ORGANIZATION AND ARCHITECTURE**

Time : 3 Hours]

[Max. Marks : 75

**Note : Answer all questions from Part – A. Answer any five questions from Part – B.**

**PART – A**

**(25 Marks)**

1. What is the IEEE standard for Binary floating point numbers ? 2
2. The following transfer statement specify a memory. Explain the memory operation in each case.  
a)  $R_2 \leftarrow M[AR]$       b)  $M[AR] \leftarrow R_3$       c)  $R5 \leftarrow M[R5]$  3
3. Differentiate between hardwired and microprogrammed control. 3
4. Write the Basic computer instruction formats the memory, register and I/O reference instructions. 3
5. Write the differences between 2 and 3 address instructions. 2
6. Mention the different types of instruction formats. 3
7. Why does DMA have priority over the CPU when both request a memory transfer ? 3
8. List few advantages of the memory - mapped I/O techniques. 2
9. How many  $128 \times 8$  RAM chips are needed to provide a memory capacity of  $2048 \times 16$  words ? 2
10. What is mapping and what are the types ? 2

(This paper contains 3 pages)

1

**P.T.O.**



## PART - B

(50 Marks)

11. a) Explain Booths multiplication algorithm with the help of an example. 6
- b) Design a 4 bit combinational cbt for incrementers/decrementers cbt 4  
using adders.
12. a) Explain the phases of an instruction cycle with necessary control functions 7  
and micro - operations.
- b) Explain about Von-Neumann machine. 3
13. a) What is an Addressing mode and list the different types ? 5
- b) An instruction is stored at location 300 with its adder field at 301.  
The adder field has the value 400. A process register R1 contains the number  
200. Evaluate the effective address if addressing mode of the instruction is  
 i) Direct  
 ii) Immediate  
 iii) Relative  
 iv) Register Indirect  
 v) Index with R1 as the Index Reg. 5
14. a) Explain segmented page mapping technique with the help of a numerical 5  
example.
- b) Explain associative memory with a neat block diagram and derive the match  
logic for one word of association memory. 5



15. A digital computer has a memory unit of  $64 \times 16$  and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

a) How many bits are there in the tag, index, block and word fields of the address format ?

4

b) How many bits are there in each word of cache and how are they divided into functions ? Include a valid bit.

4

c) How many blocks can the cache accommodate ?

2

16. a) Design a 4 - bit arithmetic cbt which implements addition subtraction, increment and decrement operations.

5

b) Draw the block diagram of a micro program sequences and explain.

5

17. Write short notes on :

a) Interrupts

3

b) Asynchronous communication interface.

4

c) Virtual memory.

3

**FACULTY OF ENGINEERING**

**B.E. III/IV Year (ECE) I Semester (Main) Examination, November/December 2008**

**(New)**

**COMPUTER ORGANIZATION AND ARCHITECTURE**

**Time : 3 Hours]**

**[Max. Marks : 75]**

*Answer all questions from Part A.*

*Answer any five questions from Part B.*

**Part A — (Marks : 25)**

1. Explain the memory operation of the following transfer statements.
  - (a)  $R2 \leftarrow M[AR]$
  - (b)  $M[AR] \leftarrow R3$
  - (c)  $R5 \leftarrow M[R5]$
2. Specify the sequence of micro operations that will perform the following operations in a basic computer  
 $IR \leftarrow M[AC]$   
 $AC \leftarrow AC + TR$   
 $DF \leftarrow DF + AC$
3. Give the instruction format of a basic computer the memory, register and I/O reference instructions.
4. Draw the Block diagram of a 4-bit binary incrementer.
5. Differentiate between internal and external interrupts.
6. Give the no. of memory references, when  $w$  fetches and executes an indirect addressing mode instruction if instruction is
  - (a) Computational type requiring an operand from memory
  - (b) a branch type
7. Explain the need for an I/O interface.
8. Differentiate between an isolated I/O and memory mapped I/O.
9. Explain the concept of virtual memory.
10. Explain the terms Tag, Index and Block in relation to cache memory.

[P.T.O.]

**Part B — (Marks : 50)**

**FACULTY OF ENGINEERING**

B. E. III Year (ECE) I-Semester(Old) Examination, November / December 2008

**Subject : Computer Organization and Micro Processors****Time : 3 Hours}****{Max. Marks: 75}****Note: Answer all questions of Part - A and answer any five questions from Part-B.****PART – A (25 Marks)**

1. Explain what do you understand by stored program concept.  
To implement this concept, which functional component plays an important role. (2)
2. Represent the number  $(+46.5)_{10}$  as a floating point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits. (3)
3. What is a stack and what is its role in the operation or execution of computer instructions ? (3)
4. What is the difference in direct mapping and set-associative mapping techniques in cache memories ? (2)
5. Distinguish between memory mapped I/O, and I/O mapped I/O, how many I/O devices can be addressed in each case? (3)
6. Explain the functions of ALE and I/O/M signals of the 8085 microprocessor. (2)
7. Write a ALP (Program) in 8085 to subtract two 8-bit decimal numbers. (3)
8. What are different operating modes of 8255 ? (3)
9. What is the difference between an assembler and a compiler ? (2)
10. Draw a schematic of an array Processor. (2)

**PART – B (5x10=50 Marks)**

11. Draw the flow chart for computer cycle control and explain what happens during fetch, execute and indirect cycles? (10)
- 12.(a) Convert the following numerical arithmetic expression into RPN and show the stack operations for evaluating the numerical result.  
 $(3 + 4) [ 10 (2+6) + 8]$  (5)  
(b) Explain briefly various addressing modes. (5)
- 13.(a) Write an ALP for 8085 to add two multiple precision BCD numbers. (5)  
(b) Explain 'STA adds' instruction with timing diagram . (5)
14. Using a 8254 programmable interval timer as an interfacing device to a 8085 microprocessor, explain how a square wave of 20ms time period is generated. Assume clock frequency of 8085 to be 2MHZ. (10)
15. Explain what do you understand by virtual memory. Explain the address translation mechanism of any typical processor used in contemporary computer systems. (10)
- 16.(a) What is Flynn's classification of computers ? Explain. (3)  
(b) Draw the block schematic of a five-stage pipelined processor. Explain. (7)
17. Explain the various issues concerning the interrupt processing in micro processor systems. How multiple interrupts are handled and how does processor respond to interrupt request ? (10)

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**FACULTY OF ENGINEERING****B.E. III/IV Year (ECE) I Semester (Main) Examination, November 2007****COMPUTER ORGANIZATION AND MICROPROCESSORS**

Time : 3 Hours]

[Max. Marks : 75]

*Answer all questions of Part A.**Answer five questions from Part B.***Part A – (Marks : 25)**

1. How does a Microprocessor differentiate between data and Instruction? 2
2. What are the basic elements of floating point addition and subtraction. 3
3. How are data read from and written onto a magnetic disk. 3
4. Distinguish between memory mapped I/O, and I/O mapped I/O, how many I/O devices can be addressed in each case. 3
5. Define Instruction cycle, machine cycle and T-state. 3
6. What is the function of ALE signal of 8085 microprocessor. 3
7. What is the result of the following program segment  
MVIA, OCH  
SIM 2
8. Find the error and correct the following instruction  
ADD DS #0030H  
ROR BX, CX 2
9. Mention the functions of an Assembler. 2
10. List the features of RISC Machines. 2

**Part B – (Marks :  $5 \times 10 = 50$ )**

11. (a) Explain the stock organisation of a computer with an example. 6  
(b) Explain about the basic components of computer. 4
12. (a) What are the differences among direct mapping, associative mapping and set-associative mapping? 6  
(b) What are the various functions of I/O module? 4

[P.T.O.]

13. (a) Write an ALP for 8085 to add two multiple - precision BCD numbers. 6  
(b) Explain "CALL Addr" Instruction with timing diagram. 4
14. (a) Explain the function of the following pins of 8085 6  
(i) ALE (ii) IO /  $\bar{M}$  (iii)  $S_0, S_1$  (iv) SID and SOD.  
(b) Draw the machine cycle diagram and explain the instruction. 4  
MOV A, M.
15. (a) Explain with a neat diagram how a matrix key board is interfaced to 8085 write a program to read a key pressed. 5  
(b) Interface an 8-bit DAC to 8085 through PA8255 write an ALP to generate a square waveform with 100  $\mu$ second time period. 5
16. (a) Show the block schematic diagram of 8253 PIT chip and explain any three modes of its operation. 7  
(b) Design and draw a memory interface circuit to an 8085 CPU bus to meet the following specifications using  $4K \times 8$  bits SRAM chips  
(i) 8k bytes of ROM area starting OOOOH  
(ii) 8k bytes of SRAM area starting 8000H. 3
17. (a) Compare RISC and CISC Processors. 5  
(b) Write about array processors. 5



**FACULTY OF ENGINEERING**

**B.E. III/IV Year (ECE) I Semester Main Examination,  
November 2005**

**COMPUTER ORGANISATION AND MICROPROCESSORS**

**Time : 3 Hours]**

**[Max. Marks : 75**

*Answer all questions from Part A in the same order  
as appeared in the question paper  
and Answer any five questions from Part B.*

**Part A – (Marks : 25)**

1. Distinguish between a logical shift and arithmetic shift of a signed binary number. 2
2. What is a stack machine? 2
3. Write a program to evaluate  $Y = A - B$ , with Zero-address instructions. 3
4. Differentiate between external and internal interrupts. 2
5. How many T-states are required for the following 8085 instructions:
  - (a) MOV C B (b) CALL 3500 H 2
6. Write a program sequence that generates a square waveform on the SOD pin of 8085. 3
7. Draw the block diagram of 8253 timer. 3
8. Explain how an EPROM is erased. 2
9. What are typical services provided by an operating system? 3
10. Explain briefly about pipeline processing. 3

**Part B – (Marks :  $5 \times 10 = 50$ )**

11. (a) What do you understand by stack organisation? Draw the block diagram of a memory stack and explain the basic PUSH and POP operations. 6  
(b) Explain briefly various addressing modes. 4

**[P.T.O**

12. (a) Explain DMA with an example. 6  
(b) Distinguish between memory mapped I/O and I/O mapped I/O. 4
13. (a) Explain about the following pins of 8085: 5  
(i) HLDA    (ii) RESET    (iii) SID    (iv) READY    (v) ALE  
(b) With the help of algorithm and flow chart write an 8085 ALP to sort an integer array into ascending order. 5
14. (a) How do you interface a 8-bit ADC to the 8085 bus using 8255? Develop the driver subroutine for the ADC. 6  
(b) How do you interface  $4 \times 4$  matrix keyboard to 8085 using 8255? 4
15. (a) Differentiate between RISC Vs CISC machine and explain about RISC architecture. 6  
(b) Distinguish between compiler and assembler. 4
16. Give a scheme and circuit diagram to measure the width of a square wave. Write the ALP with a neat flow chart and algorithm for the same. 10
17. Write short notes on the following: 10  
(a) Features of Motorola and Zilog CPU's  
(b) Language translators  
(c) Array processors.
-

## FACULTY OF ENGINEERING

## B.E. 3/4 (ECE) I - Semester Supplementary Examination

April/May 2004

## COMPUTER ORGANISATION AND ARCHITECTURE

Time : 3 Hours]

[Max. Marks : 75

**Note :** Answer all questions from Part A and any five questions from Part B.

## PART - A

25

1. What is the difference between a direct and an indirect address instruction ? How many references to memory are needed for each type of instruction to bring an operand into a processor register ? 2
2. Define the terms a) Micro instruction and b) Microprogram. 2
3. Convert the following arithmetic expressions from infix to reverse polish notation.
  - a)  $A * B + C * D + E * F$
  - b)  $AB + A(BD + CE)$
2
4. How many memory chips of  $256 \times 8$  are needed to provide a memory capacity of 4K bytes ? And how many address lines are required to access 4K bytes of memory ? 2
5. What do you understand by indexed addressing mode ? 2
6. Give at least six status conditions for the setting of individual bits in the status register of an asynchronous communication interface. 3
7. What is DMA ? Explain its advantages. 3
8. Draw the block diagram of an associative memory and explain. 3
9. What is the difference between parallel processing and pipeline processing ? Explain. 3
10. Write sequence of micro-operations for the fetch cycle of basic computer. 3

(This paper is of 2 pages)

(Turn over)

## PART - B

 $5 \times 10 = 50$ 

- 11.** a) What is the difference between the BSA instruction and the interrupt cycle. Explain the BSA instruction can not fulfill the function of the interrupt cycle. 6
- b) Three micro-operations that change the contents of PC are given by :
- $x_1 : PC \leftarrow PC + 1$
  - $x_2 : PC \leftarrow MBR(AD)$
  - $x_3 : PC \leftarrow O$
- Determine the control functions  $x_1, x_2, x_3$ . 4
- 12.** Explain the floating point addition/subtraction algorithm with flow chart. 10
- 13.** Write a program to evaluate the arithmetic statement  
 $X = (A + B) * (C + D)$ 
  - a) Using an accumulator type computer with one address instruction. 3
  - b) Using two and three address instructions and 4
  - c) Using stack-organised computer with zero address instructions. 3
- 14.** a) Explain the function of a memory management unit in a typical computer. 4
- b) The logical address space in a computer system consists of 128 segments, each having upto 32 pages of 4K words each. Physical memory consists of 4K blocks of 4K words each. Formulate the logical and physical address formats. 6
- 15.** What is priority interrupt technique ? Explain parallel priority interrupt technique with the help of block diagram. 3 + 7
- 16.** Draw the block diagram of microprogram sequencer for a control memory and explain. 10
- 17.** Write short notes on :
  - a) Compilers and Interpreters. 5
  - b) Vector Processing. 5
-

**FACULTY OF ENGINEERING**

**B.E. III/IV Year (ECE) I Semester Main Examination, November 2004.**

**(New)**

**COMPUTER ORGANISATION AND MICROPROCESSORS**

**Time : 3 Hours]**

**[Max. Marks : 75]**

**Answer all questions of Part A and answer any five questions from Part B.**

**Part A – (Marks : 25)**

1. Explain what do you understand by stored program concept to implement this concept, which functional component plays an important role. 3
2. Explain the format of IEEE 754 floating point number format. 2
3. What is a stack and what is its role in the operation or execution of computer instructions? 3
4. In Cache memory organizations, a write policy like WRITE ONCE, WRITE THROUGH is considered. Why only a WRITE Policy and not a READ policy is considered in CACHE memories? 4
5. What is the difference between DMA I/O and interrupt I/O? 2
6. Give examples of different instruction formats of 8085. 3
7. What is the difference between an assembler and a compiler? 2
8. In microprocessor interfacing explain what do you understand by device address pulse and device select pulse. 2
9. Draw a schematic of an array processor. 2
10. What do you understand by the term BIOS? Explain one simple function of BIOS. 2

**Part B – (Marks :  $5 \times 10 = 50$ )**

11. Explain the various elements of bus design.
12. Explain what you understand by virtual memory. Explain the address translation mechanism of any typical processor used in contemporary computer systems.

**[P.T.O.]**

13. Explain the various issues concerning the interrupt processing in microprocessor systems like how multiple interrupts are handled, how long should interrupt be active, how does processor respond to interrupt request etc..
  14. Using a 8254 programmable interval timer as an interfacing device to a 8085 microprocessor, explain how a square wave of 20 ms time period.  
Assume clock frequency of 8085 to be 2 MHZ.
  15. Explain with a neat schematic the internal architecture of any RISC processor.
  16. Explain with examples the various addressing modes used in 8085 microprocessor.
  17. With the help of a single bus organization of CPU, explain how an arithmetic operation is performed on it.
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FACULTY OF ENGINEERING  
 B.E.3/4 (ECE) I-Semester Main Examination, November, 2004  
 (For Backlog Students)

**Subject: COMPUTER ORGANISATION & ARCHITECTURE**

**Time: 3 Hours**

**Max. Marks: 75**

N.B: Answer all questions of Part-A and any Five questions from Part-B.

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**PART - A (25 Marks)**

1. A 36-bit floating point binary number has 8 bits plus a sign for the exponent. The Mantissa is assumed to be a normalized fraction. Negative numbers in the Mantissa and exponent are in signed-magnitude representation. What are the largest and smallest positive quantities that can be represented excluding zero?
2. Design a 4-bit arithmetic circuit with one select variable 'S' and two 4-bit data inputs 'A' and 'B'. When S=0. The circuit performs the addition A+B, when S=1, the circuit performs A-B by 2's complement of 'B'.
3. Under what conditions would it be more feasible to use a hard wired control than a microprogrammed control unit?
4. List the advantages and disadvantages of memory mapped compared to isolated I/o.
5. A DMA module is transferring characters to memory using cycle-stealing, from a device transmitting at 9600 bps. The cpu is fetching instructions at the rate of 1 million instructions per second. By how much will the processor be slowed down due to the DMA module.
6. Draw a flow chart for Booths multiplication algorithm.
7. Explain the importance of Associative memory and its operation.
8. Describe how the multiple interrupts are being serviced?
9. Brief the services typically provided by an operating system.
10. Compare RISC and CISC machines.

**PART - B (5x10=50 Marks)**

11. Draw the logic diagram of a 4-bit register with clocked JK flip flops having control inputs for the increment, complement, and parallel transfer micro-operations. Show how the 2'-s complement can be implemented in this register?
12. It is possible to reduce the time it takes the control to process a register reference instruction in the basic computer. Show that if the register-reference instructions are executed with timing variable  $t_3$ -during the fetch cycle, the control will process them in half the time it now takes. Show the register transfer relations for the fetch cycle that will take care of this proposed change.
13. Explain various types of Instruction formats and addressing methods employed in a general purpose computer with examples.

....2.

14. Show how a 9-bit micro operation field in a micro instruction can be divided into subfields to specify 46 micro operations. How many micro-operations can be specified in one micro-instruction? Mention the applications of Micro-programming.
15. What is meant by locality of reference in memory systems? Explain mapping, store through, load through and replacement algorithms with reference to Cache-memory.
16. What are the scheduling strategies followed in an O.S. in a multiprocessor environment?
17. Write short notes on:
  - a) Stack organisation
  - b) Assemblers.

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