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**CSE301** Enrol. No. .. .....

[ET]

END SEMESTER EXAMINATION : NOV.–DEC., 2018

# COMPUTER ORGANIZATION AND ARCHITECTURE

*Time : 3 Hrs.* *Maximum Marks : 70*

**Note:** ***Attempt questions from all sections as directed.***

## SECTION – A (30 Marks)

*Attempt any* **five** *questions out of* **six.**

*Each question carries* **06** *marks.*

1. (a) Draw a diagram of a bus system with the use of three state buffers and a decoder. (3)

   (b) Design a 4-bit combination circuit decrementer using four full adder circuits. (3)

2. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

P.T.O.

(a) How many bits are there in the operation code, the register code part, and the address part? (2)

(b) Draw the instruction word format and indicate the number of bits in each part. (2)

(c) How many bits are there in the data and address inputs of the memory? (2)

3. A bus-organized CPU has 16 registers with 32 bits in each, an ALU and a destination decoder.

(a) How many multiplexers are there in the A bus, and what is the size of each multiplexer and how many selection inputs are needed for MUX A and MUX B? (2)

(b) How many inputs and outputs are there in the decoder? How many inputs and outputs are there in the ALU for data, including input and output carries? (2)

(c) Formulate a control word for the system assuming that the ALU has 35 operations. (2)

4. Briefly describe the hardware organization of associative memory. Also discuss the read and write operation for the associative memory.

5. (a) Discuss the difference between tightly coupled multiprocessors and loosely coupled multiprocessors from the view point of hardware organization and programming techniques. (3)

(b) How many switch points are there in a crossbar switch network that connects p processors to m memory modules? (3)

6. (a) What is the difference between serial and parallel transfer? Using a shift register with parallel load, explain how to convert serial input data to parallel output and parallel input data to serial output. (4)

(b) How many 128 × 8 memory chips are needed to provide a memory capacity of 4096 × 16? (2)

## SECTION – B (20 Marks)

*Attempt any* **two** *questions out of* **three.**
*Each question carries* **10** *marks.*

7. (a) Show that adding B after the operation A + B + 1 restores the original value of A. What should be done with the end carry?

Why should the sign of the remainder after a division be the same as the sign of the dividend? (6)

P.T.O.

(b) Explain the difference between hardwired control and microprogrammed control. Is it possible to have a hardwired control associated with a control memory? (4)

8. (a) A computer employs RAM chips of 256 × 8 and ROM chips of 1024 × 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped 1/0 configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

(i) How many RAM and ROM chips are needed?

(ii) Draw a memory-address map for the system.

(iii) Give the address range in hexadecimal for RAM, ROM, and interface. (6)

(b) An output program resides in memory starting from address 2300. It is executed after the computer recognizes an interrupt when FGO becomes a 1 (while IEN = 1).

(i) What instruction must be placed at address 1?

(ii) What must be the last two instructions of the output program? (4)

9. (a) What is cache coherence and why is it important in shared-memory multiprocessors system? How can the problem be resolved with a snoopy cache controller? (6)

(b) The 8-bit registers AR, BR, CR, and DR initially have the following values :

AR = 11110010
BR = 11111111
CR = 101 11001
DR = 11101010

Determine the 8-bit values in each register after the execution of the following sequence of micro operations.

AR <- AR + BR
CR <- CR /\ DR, BR <- BR + 1
AR <- AR – CR (4)

## SECTION – C (20 Marks)

*(Compulsory)*

10. (a) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry $C_{in}$. Draw the logic diagram for the first two stages.

P.T.O.

| S | $C_{in}=0$ | $C_{in}=1$ |
|---|---|---|
| 0 | A+B | A+1 |
| 1 | A–1 | A+B+1 |

(6)

(b) List different types of addressing modes. Explain any two with suitable diagrams and examples. (3)

(c) The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two-word call subroutine instruction is located in memory at address 1 120 followed by the address field of 6720 at location 1121. What are the content of PC, SP, and the top of the stack :

(i) Before the call instruction is fetched from memory?

(ii) After the call instruction is executed?

(iii) After the return from subroutine? (5)

(d) A DMA controller transfers 16-bit words to memory using cycle stealing-The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of the DMA transfer?

Give at least six status conditions for the setting of individual bits in the status register of an asynchronous interface. (6)