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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2017

Course Code: EE203

Course Name: ANALOG ELECTRONICS CIRCUITS (EE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks. Marks

1		With a neat circuit diagram explain the working of a negative voltage clamping circuit. Also sketch the output waveform for ±5V square wave input.	(5)
2		Explain the construction and operation of Enhancement type metal oxide semiconductor FET with neat diagrams.	(5)
3		In an amplifier open loop gain changes by ±50% using a series voltage negative feedback. The amplifier is to be modified toget a gain of 100 with ±0.1% variation. Find the required open loop gain of the amplifier and the amount of negative feedback.	(5)
4		Explain Barkhausen criteria of sustained oscillation	(5)
5		Derive the expression for voltage gain of a non-inverting amplifier.	(5)
6		Design a three input summing amplifier using op-amp having gains of 2,3and 5 respectively for each input.	(5)
7		Define slew rate and explain its effect on waveform generation.	(5)
8		Design a phase shift oscillator to have 1.5kHz output frequency using a 741 op-amp with Vcc = ±12 V.	(5)

PART B

Answer any two full questions, each carries 10 marks.

9		Design a voltage divider bias circuit to operate from a 18V supply in which bias conditions are to be $V_{CE} = V_E = 6$ V and $I_C = 1.5$ mA. $\beta = 90$. Also calculate the stability factor S.	(10)
10	a)	Draw a common source FET amplifier. Using small signal equivalent circuit derive the expression of the voltage gain.	(6)
	b)	Explain the reasons for reduction of gain at high frequencies of a CE amplifier.	(4)
11	a)	Explain the operation of a Zener voltage regulator with a neat circuit diagram.	(5)
	b)	Define Miller's theorem.	(2)
	c)	In a CE amplifier circuit, h_{fe} =50, h_{ie} =1.3kΩ, C_{bc}= 5pF, R_C =3kΩ, $R_{L=}$ 2.2 kΩ Calculate the Miller capacitance.	(3)

PART C

Answer any two full questions, each carries 10 marks.

12	a)	Draw the circuit diagrams of two stage RC coupled and Transformer coupled amplifiers. Discuss the important features and applications of both.	(6)

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	b)	A transformer coupled classA power amplifier draws a current of 250mA from a collector supply of 13 V. When no signal is applied to it determine i) Maximum output power ii) Power rating of the transistor iii) Maximum collector efficiency.	(4)
13	a)	With a neat diagram explain the working of a Hartley oscillator.	(8)
	b)	A Wien bridge oscillator has the following components $R_1 = R_2 = R_4 = 5.6\ k\Omega$, $R_3 = 12\ k\Omega$ and $C_1 = C_2 = 2000pF$. Calculate the oscillating frequency.	(2)
14	a)	Derive the expression for voltage gain of a dual input balanced output differential amplifier.	(7)
	b)	Why open loop op amp configurations are not used for linear applications?	(3)

PART D

Answer any two full questions, each carries 10 marks.

15	a)	Draw and explain the operation of a square waveform generator using opamp.	(5)
	b)	Explain inverting Schmitt trigger circuit with relevant waveforms.	(5)
16	a)	Draw and explain the circuit of IC 555 in Monostable mode with relevant waveforms.	(7)
	b)	What are the advantages of crystal oscillators.	(3)
17	a)	Explain the working of Instrumentation amplifier with a neat diagram.	(6)
	b)	In an astable multivibrator using 555, $R_B = 750\ \Omega$. Determine the values of R_A and C to generate a 1.0 MHz clock that has a duty cycle of 25%.	(4)

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