COMPUTER ORGANIZATION AND ARCHITECTURE

PC 404 EC

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

1. Implement the fixed-point and floating-point addition, subtraction, multiplication & Division.
2. Describe the basic structure and operation of a digital computer and Discuss the different ways of communicating with I/O devices and standard I/O interfaces
3. Analyze the hierarchical memory system including cache memories and virtual memory. Understand issues affecting modern processors.

Outcomes: On successful completion of the course, the students would be able to

1. Perform mathematical operations on fixed and floating point digital data.
2. Illustrate the operation of a digital computer.
3. Understand I/O interfacing of a computer.
4. Interface microprocessor with memory devices.
5 Understand latest trends in microprocessors.

UNIT – I
***Data representation and Computer arithmetic*:** Introduction to Computer Systems, Organization and architecture, evolution and computer generations; Fixed point representation of numbers, digital arithmetic algorithms for Addition, Subtraction, Multiplication using Booth's algorithm and Division using restoring and non-restoring algorithms. Floating point representation with IEEE standards and its arithmetic operations.
UNIT – II
***Basic Computer organization and Design*:** Instruction codes, stored program organization, computer registers and common bus system, computer instructions, timing and control, instruction cycle: Fetch and Decode, Register reference instructions; Memory reference instructions. Input, output and Interrupt: configuration, instructions, Program interrupt, Interrupt cycle, Micro programmed Control organization, address sequencing, micro instruction format and micro program sequencer.
UNIT – III
***Central Processing Unit*:** General register organization, stack organization, instruction formats, addressing modes, Data transfer and manipulation, Program control. CISC and RISC: features and comparison. Pipeline and vector Processing, Parallel Processing, Pipelining, Instruction Pipeline, Basics of vector processing and Array Processors.
UNIT – IV
***Input-output Organization*:** I/O interface. I/O Bus and interface modules, I/O versus Memory Bus. Asynchronous data transfer: Strobe control, Handshaking, Asynchronous serial transfer. Modes of Transfer: Programmed I/O, Interrupt driven I/O, Priority interrupt; Daisy chaining, Parallel Priority interrupt. Direct memory Access, DMA controller and transfer. Input output

Processor, CPU-IOP communication, I/O channel.
UNIT – V
Memory Organization: Memory hierarchy, Primary memory, Auxiliary memory, Associative memory, Cache memory: mapping functions, Virtual memory: address mapping using pages, Memory management.

Suggested Readings:

1	Morris Mano, M., "*Computer System Architecture"*, 3/e, Pearson Education, 2005.
2	William Stallings, "*Computer Organization and Architecture: Designing for performance*", 7/e, Pearson Education, 2006.
3	John P. Hayes, "*Computer Architecture and Organization"*, 3/e, TMH, 1998.
4	Govindarajalu, "*Computer Architecture and Organization"*, TMH.
5	Hebbar, "*Computer Architecture"*, Macmillan, 2008.