CSE-301 Roll No. .....

[ETD]

END SEMESTER EXAMINATION: NOV.- DEC., 2014

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : 3 Hrs. *Maximum Marks : 70*

Note: ***Attempt questions from all sections as directed.***

SECTION – A (30 Marks)

Attempt any **5** *questions out of six.*
Each question carries **6** *marks.*

1. Design an arithmetic circuit with one selection variable 'S' and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages.

S	$C_{in} = 0$	$C_{in} = 1$
0	D = A+B (Add)	D=A+1(Increment)
1	D= A – 1(Decrement)	D= A+B+1 (Subtract)

P.T.O.

2. The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 832E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 5A8E. Calculate the following:-

   (a) What is the instruction that will be fetched and executed next?

   (b) Show the binary operation that will be performed in the AC when the instruction is executed?

   (c) Give the contents of registers PC, AR, DR, AC and IR in hexadecimal and the values of E, I and the sequence counter SC in binary at the end of the instruction cycle? (2,2,2)

3. Explain address sequencing process of micro programmed control unit with suitable block diagram?

4. Drive an algorithm for evaluation the square root of a binary fixed point number?

5. Calculate the following:-

   (a) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

(c) How many lines must be decoded for chip select? Specify the size of decoders? (2,2,2)

6. Draw a space-time diagram for a six segment pipeline showing the time it takes to process eight tasks?

SECTION – B (20 Marks)

Attempt any **two** *questions out of three.*
Each question carries **10** *marks.*

7. Discuss mapping process in contrast with memory management? Also explain each type of mapping process with suitable diagram?

8. (a) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?

(b) Explain working of four segment instruction pipeline with suitable flow chart? (4,6)

P.T.O.

9. Show the step-by-step multiplication process using Booth algorithm, when the following binary numbers are multiplied. Assume 5-bit registers that hold signed numbers.

(+11) × (-17)

SECTION – C (20 Marks)

(Compulsory)

10. (a) Differentiate between following:-

(1) RISC and CISC

(2) Tightly coupled and loosely coupled multiprocessor. (3,3)

(b) Define addressing modes? Explain various type of addressing modes in details? (10)

(c) Show complete logic of interrupt flip-flop 'R' in basic computer system? Use JK-flip flop and minimize the number of gates? (4)