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CSE301 Enrol. No. .....

[ET]

END SEMESTER EXAMINATION : NOV. —DEC., 2017

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : 3 Hrs. Maximum Marks : 70

Note: ***Attempt questions from all sections as directed.***

SECTION — A **(30Marks)**

Attempt any **five** questions out of **six**.

Each question carries **06** marks.

1. If a magnetic disc has 100 cylinders, each containing 10 tracks of 10 sectors, and each sector can contain 128 bytes, what is the maximum capacity of the disk in bytes?

2. Which interrupt is used for which hardware automatically transfers the program to a specific memory location? Explain how it works?

3. What are the advantages of assembly language? How is it different from high-level language?

P.T.O

4. Write short notes on the following :

(i) Flip-Flops
(ii) (ii) Multiplexer

5. Explain with neat flow chart for addition and subtraction of floating point Numbers.

6. Design a combinational circuit using a ROM.The circuit accepts a 3-bit number and generates an output in binary number equal to the square of the input number.

SECTION — B (20 Marks)

Attempt any two questions out of three.

Each question carries 10 marks.

7. Give the hardware organization of associative memory. Why associative memory is faster than other memories. Deduce the logic equation used to find the match in the associative memory. Explain how four-bit argument register is realized.

8. Write shot. notes an any two of the followings :

(i) DMA data transfer

(ii) Handshaking method of data transfer

(iii) Isolated Vs memory mapped I/O

(iv) RISC architecture

9. With the help of a neat sketch, explain the working of a 4-bit universal shift register.

SECTION — C **(20 Marks)**

(*Compulsory*)

10. A bus is a set of wires connecting computer components. A computer may have several buses, e.g. a system bus, an internal bus, and special purpose local buses. All communication between the various components takes place over one of these buses. For example, data transfer between the CPU and memory normally occurs on the system bus, while movement of data between registers and the ALU takes place on a bus internal to the microprocessor chip. The speed at which data can be transferred is dependent on the number of data lines in the bus and, in the case of synchronous buses, the clock speed of the bus. The transfer rate or bandwidth of a particular system bus can be calculated from the number of cycles required for transfer, the length of the cycle and the number of data lines. For example, if a bus has S data lines, requires 4 cycles to transfer data,

and each cycle is 250 nsecs then the bandwidth of the bus is 1 byte per 1000 nsecs. This is equivalent to 1 byte per microsecond or 1 Megabyte/second.

Answer the following questions :

(a) In order to execute a program instructions must be transferred from memory along a bus to the CPU. If the bus has 8 data lines, at most one 8 bit byte can be transferred at a time. How many memory access would be needed in this cast to. transfer a 32 bit instruction from memory torithc;, CPU? Explain.

(b) (b) Suppose that a bus has 16 data lines and reares 4 cycles of 250 nsecs each to transfer data. 11C bandwidth of this bus would be 2 Megabytesecri If the cycle time of the bus was reduced to 12Q"-nsecs and the number of cycles required WI transfer stayed the same, what would the bandwidth of the bus?

(c) (c) Nam: the buses that computer must at least consist of during circuit designing.